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Visvesvaraya Technological University

Belagavi

A Mini Project Report

on

Cost Effective QCA XOR-XNOR Topology for Nanotechnology Applications

Submitted by

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Autonomous College Permanently Affiliated to VTU, Approved by AICTE & UGC
Accredited by NAAC with 'A' Grade, Accredited by NBA

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CHAPTER 1

INTRODUCTION

Gordon Moore predicted in 1965 that the number of transistors that could be integrated into a single die would increase exponentially over time. According to existing studies, the laws of nature will begin to control microprocessor design and manufacture during the next two decades. Many integrated circuits are being produced using 0.25-0.33nm technologies. Physical restrictions of traditional electronics, including as power consumption, connectivity, and lithography, will become increasingly difficult to overcome when device sizes shrink to the order of 0.05 microns.

The tremendous increase in the number of transistors in a single chip, as well as the decrease in transistor size, has become an important obstacle for integrated circuit design and VLSI technology. The issue is that with this CMOS technology, transistor size reduction is limited and almost impossible beyond 10 nm because of the possibility of causing abnormal quantum behaviours at the nano metric scale. Researchers have suggested a quantum cellular automata (QCA) approach to computing with quantum dots as an alternative to CMOS-VLSI.

Quantum-dot cellular automata (QCA) is an innovative nano level computer that shows less dimension, less power consumption, and greater speed, and was created as a supplement to the scaling difficulty with CMOS technology. In contrast with conventional computers, digital information in QCA is represented as combinations of pairs of electrons linked together to form quantum dot arrays. In QCA designer, these quantum dot arrays are used to build Boolean logic functions.

CHAPTER 2

LITERATURE REVIEW

	RESULTS	CONCLUSION
[1]	The purpose of this review paper is to look at the projected trends and compare it with various circuits. Different logic circuits are compared using criteria such cell count, area, and delay. For the XOR gate with 1 clock delay, at least 10 QCA cells are used. A complete adder with 1.25 clock delay requires at least 44 QCA cells.	Based on the comparison, designers may select the best-fitting circuit for their logic implementation. The extensive study of QCA technology enables researchers to master this topic quickly and attempt to create designs with fewer cell counts and delay.
[2]	They employed 32 QCA cells in the proposed circuit design approach, thus the circuit size is lowered and it is comparably dense enough, and there is also 180o of delay.	The presented designs are evidently efficient in terms of cell count, majority gate, delay, crossover, and area to mimic circuits. The proposed design pattern may be simply used to create sophisticated XOR circuits.
[3]	In this paper, they created a standard equation based on the SR flip flop and used it to create other flip flops such as the D, T and JK flip-flops. This is a novel way to designing flip-flops with minimal hardware complexity in nanotechnology.	The flip-flops designed in this study may be used to create any memory storage device. The layout has been created, and the results have been validated using the QCA Designer tool. The 3-D graphs of kink energy of the two possible output cell combinations established the circuit's stability.
[4]	At 1.0Ek, the proposed XOR gate requires 57% fewer cells and wastes 71% less power. The proposed half subtractors increased cell count by 58% while taking up 48% less space. Full subtractors, on the other hand, are 73% area efficient.	An XOR gate is proposed in this work. This gate is simple and made of standard cells. Finally, results confirmed the designs' domination over cutting-edge designs in terms of power consumption, consumed cell count, area occupied, and circuit latency.
[5]	Using the coplanar crossover technique, this approach can	From 2-input XOR gate, several topologies of 4-input and 8-input

	produce and build 4-input and 8-input logical "XOR" gates. According to the calculations, the suggested QCA multiplexer configuration improves circuit complexity (10 cells), area (0.008 m2), and latency (1 clock).	XOR gates are created. In the receiver and transmitter units, these gates may perform parity checking, detection, and correction operations. They optimized the amount of QCA cellules and minimize wire crossing.
[6]	Based on the simulation findings, it has been determined that the output high (or low) voltage in the PTL-based XOR and XNOR design deviates from the VDD (or ground) by a multiple of the threshold voltage.	The design methods are evaluated in terms of delay, power consumption, PDP, and EDP. These design strategies are appropriate for arithmetic circuits and other VLSI applications that require very low power consumption and good performance.
[7]	The implemented designs and simulation results are the solution for the idea of QCA-based digital circuits with fewer QCA cells and a smaller size criteria.	This study showed how to use QCA designer to enhance the design and implementation of various logic gates and showed considerable improvements.
[8]	The simulation results show that the suggested circuits outperform alternative designs in terms of speed, power consumption, and power-delay product (PDP). The suggested designs exhibit low dynamic and short-circuit power consumptions, as well as minimal leakage power, resulting in a low average power usage.	This article proposes novel direct designs for 3-input exclusive-OR (XOR) functions at the transistor level. These designs are suitable for both low-power and high-speed applications.

CHAPTER 3

EXISTING SYSTEM

This section contains an overview of a digital circuit known as a "XOR" gate. It is a significant digital circuit that is utilised in a variety of computational applications. Arithmetic logic circuits, Multiplexers, Full adders, Comparators, and Error detection circuits are examples of such circuits. An Exclusive "OR" gate, sometimes known as a "XOR" gate, is a digital logic gate with several inputs but only one output.

Fig 1. Block diagram of XOR gate

A "XOR" gate produces true output only if one of its inputs is true. When both of a "XOR" gate's inputs are false, or when both of the inputs it accepts are true, the output of a "XOR" gate is true. The "XOR" gate returns false. Different architectures are offered to construct a two-input XOR gate, however most researchers base their designs on three stages: the "AND" stage, the "NAND" stage, and the "OR" stage.

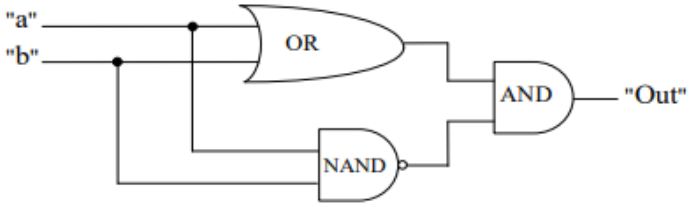


Fig 2. Schematic of the XOR Gate

An XNOR Gate is a type of digital logic gate that takes two inputs and one output. Both of "a" and "b" are the inputs, while "Out" is the output signal. The inputs are treated with the exact same logic, with equivalent responses to similar inputs. The gate's output, also known as "Equivalence Gate," requires its two inputs to be the similar in order to create a high output.

The gate works by receiving two inputs, each designated with either a 1 or a 0. If both inputs are 0, the gate will produce a 1. If both inputs are 1, the gate will also produce a 1. However, if either input differs from the other, the gate will output a 0.

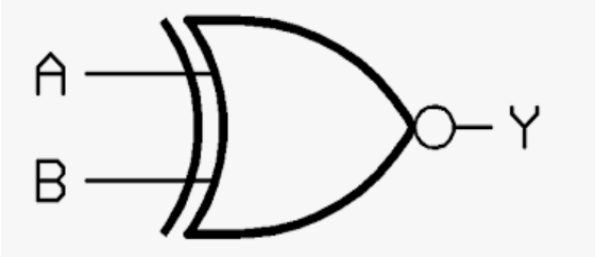


Fig 3. Block diagram of XNOR Gate

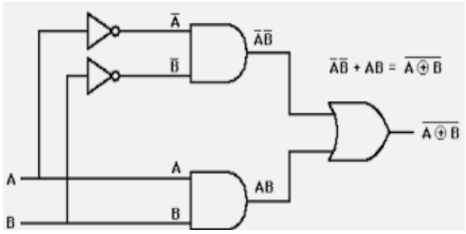


Fig 4. Schematic of XNOR Gate

[9] M.T. Niemier constructed a QCA "XOR" gate with 60 cells, 0.09 μm2 area, 5 gate count, and 1.5 clock zone latency, as illustrated in Fig. 5. This architecture contains a vast number of cells and covers a large area. To address these issues, S. Hashemi et al. [11] developed a novel 2-input QCA "XOR" gate, illustrated in Fig 7, with just 54 cells, 5 gate count, 0.08 μm2 area, and 2 clock zone delay. Chabi and al [13] propose another construction to reduce the number of cells, which has 29 cells, 4 gate count, 0.03 μm2 area, and 0.75 clock zone delay, as illustrated in Fig. 9. G. Singh et al. [10] offered another design to lower the area of the QCA "XOR" gate, utilising two inverters, three inputs, and five inputs majority gate, with 28 cells, an area of 0.02 μm2, 28 gate count, and 0.75 clock zone delay in Fig. 6. Figures 8 and 10 show A.N. Bahar et al. [12] with A.Chabi et al. [14] lowered the number of cells to 12 and 14 cells, respectively, using 0.0116 μm2 and 0.01μm2 areas with the same clock zone latency of 0.5.

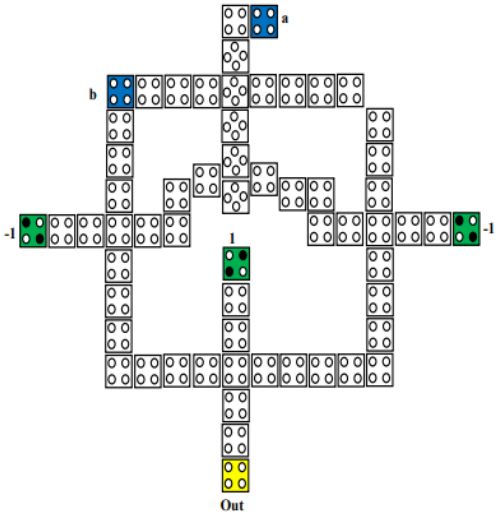


Fig 5. QCA layout for [9]

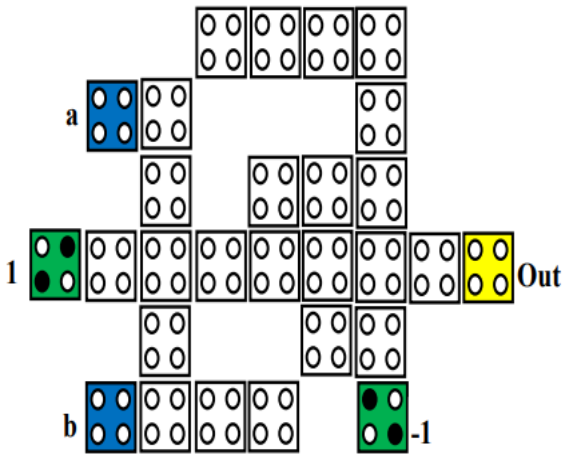


Fig 6. QCA layout for [10]

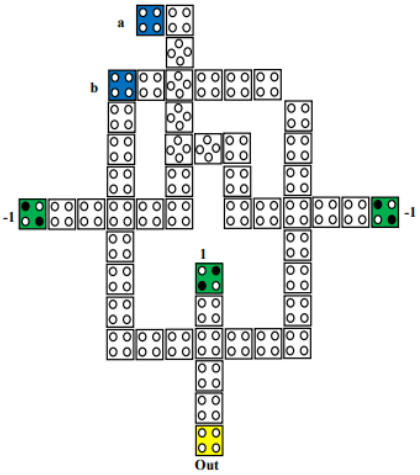


Fig 7. QCA layout for [11]

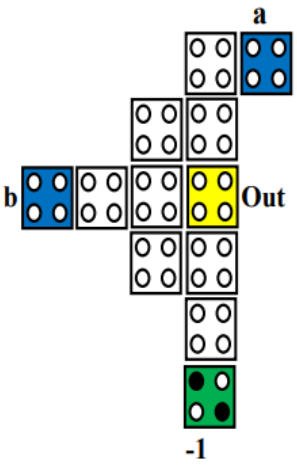


Fig 8. QCA layout for [12]

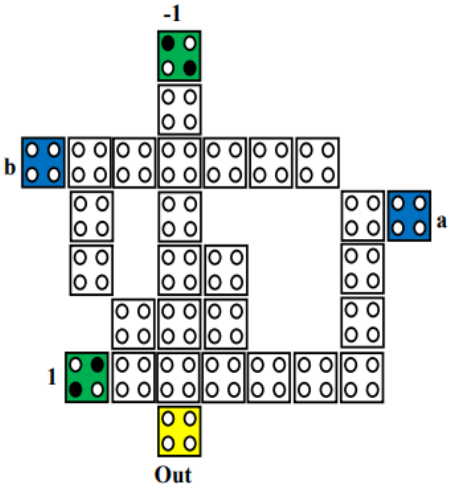


Fig 9. QCA layout for [13]

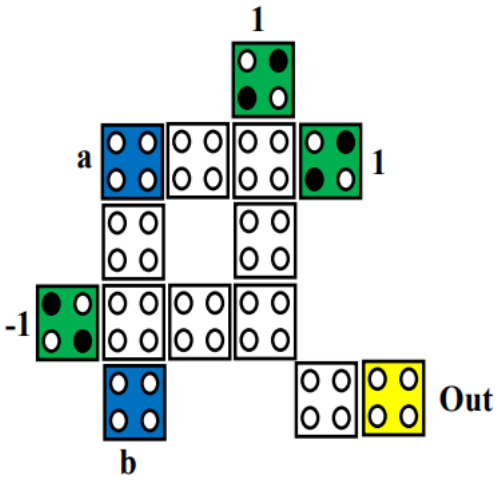


Fig 10. QCA layout for [14]

CHAPTER 4

PROBLEM STATEMENT AND OBJECTIVE

4.1 Problem Statement

Because of increased scaling of metal oxide semiconductor (MOS) devices, Moore's law has reached its practical limits. A more agile and effective technical strategy is required. Quantum-dot cellular automata (QCA) is a new technique that overcomes the physical constraints of the MOS chip.

4.2 Objectives

Extensive research and testing resulted in nanotechnology and a viable alternative to complementary metal-oxide semiconductor (CMOS) technology. The study gives a thorough investigation into the principles of QCA technology as well as the way of designing logic circuits. Various existing QCA-based circuits are described and compared for various criteria.

CHAPTER 5

PROPOSED SYSTEM

To create a digital logic circuit, basic gates such as AND, OR, and NOT, as well as universal gates such as NAND and NOR, are required. Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates are also utilized to create digital circuits in addition to these gates. XOR and XNOR gates are very helpful in arithmetic tasks as well as error detection and correction circuits.

Based on fundamental logic gate configurations, we present the QCA design and layout of an XOR gate. This configuration requires just two clock cycles and has 10 QCA cells (including input and output cells) and an area of about 0.0096 μm2. There is also no cross over in the circuit.

Based on fundamental logic gate configurations, we present the QCA design and layout of an XNOR gate. This configuration requires just two clock cycles and has 11 QCA cells (including input and output cells) and an area of about 0.01152 μm2. There is also no cross over in the circuit.

We employed a standard technique, employing three majority gates, two of which are used for AND operations and one for OR operations.

The following default values are utilized for bitable approximation: cell size=18nm, clock high=9.800000e-022J, clock low=3.800000e-023J, and dot diameter=5nm.

CHAPTER 6

SOFTWARE SPECIFICATIONS

QCA Designer 2.0.3

6.1 About QCA

A quantum cellular automaton (QCA) is an abstract model of quantum computation developed in the same way that conventional cellular automata models are. The same term can also apply to quantum dot cellular automata, a proposed physical implementation of "classical" cellular automata that makes use of quantum mechanical processes. QCA have received a lot of interest because to its incredibly tiny feature size (at the molecular or even atomic scale) and ultra-low power consumption, making them a possible replacement for CMOS technology.

6.2 QCA Elements

- **Quantum Dot Cells**

The spacing between quantum dots in QCA cells is around 20 nm, while the gap between cells is roughly 60 nm. Quantum dot Cellular Automata, like any other CA, are built on basic interaction rules between cells placed on a grid. A QCA cell is made up of four quantum dots that are placed in a square shape. By tunnelling to these quantum dots, electrons can inhabit them. Due to mutual electrostatic repulsion, if the cell is charged with two electrons, each of which is free to tunnel to any site in the cell, these electrons will strive to occupy the farthest possible site with regard to each other. As a result, two distinct cell states occur.

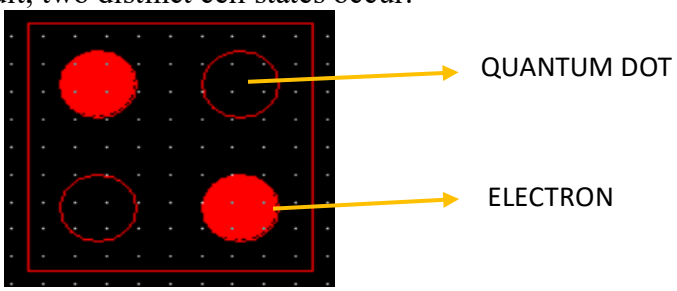


Fig 11. QCA Dot Cell

Polarisation, indicated as P, is the condition of a cell. Despite the fact that it was chosen arbitrarily, utilising cell polarisation P = -1 to represent logic "0" and P = +1 to represent logic "1" has become normal practise.

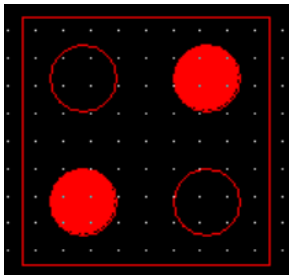


Fig 12. QCA Cell with P=+1, STATE 1

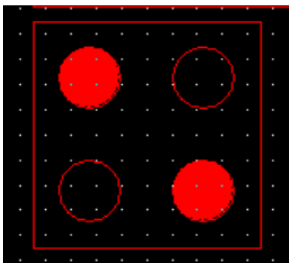


Fig 13. QCA Cell with P=-1, STATE 0

- **QCA wire**

  Placing quantum-dot cells in series, side by side, yields the simplest practicable cell layout. If any of the cells in the arrangement's polarisation were to change, the remainder of the cells would rapidly synchronise to the new polarisation due to Coulombic interactions. In this manner, a "wire" of quantum-dot cells that communicates polarisation state may be created. Such wire configurations can be used to create a complete set of logic gates for computing.

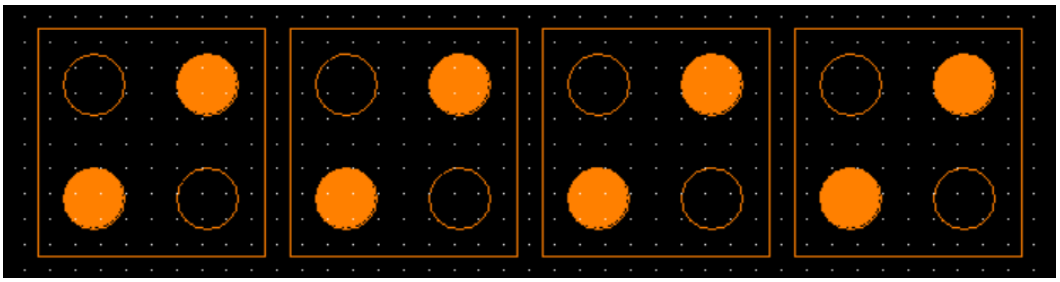


Fig 14. QCA wire

- **Basic Logic gates**

  The fundamental architecture of AND, OR, and NOT gates can be used to create large digital circuits utilising quantum-dot cellular automata (QCA) cells. When any of the three inputs is set to one, the OR operation is performed; when any of the three inputs is set to "0," the AND operation is performed. AND gate is obtained by polarising one input as logic "0".

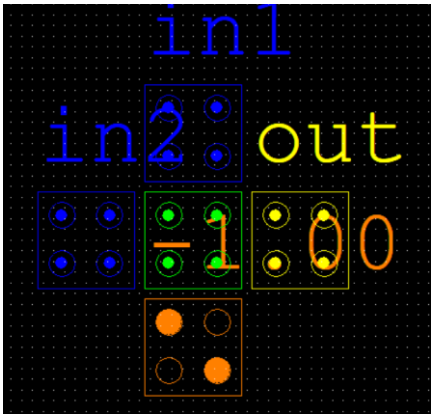


Fig 15. QCA AND Gate

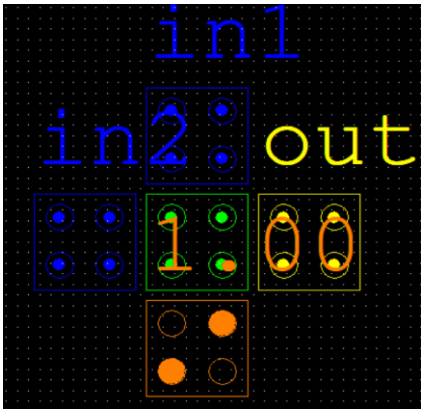


Fig 16. QCA OR Gate

CHAPTER 7

METHODOLOGY

7.1 Block Diagram

- **XOR Gate**

  When there are an odd number of 1s in the input, the Exclusive OR gate produces an output 1.

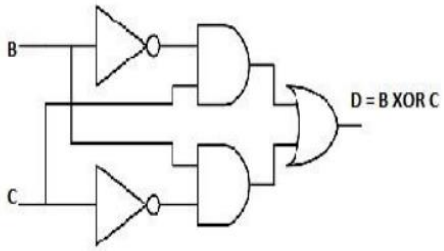


Fig 17. Basic XOR Gate using AND and OR

B	C	XOR
0	0	0
0	1	1
1	0	1
1	1	0

Table 1. XOR Gate

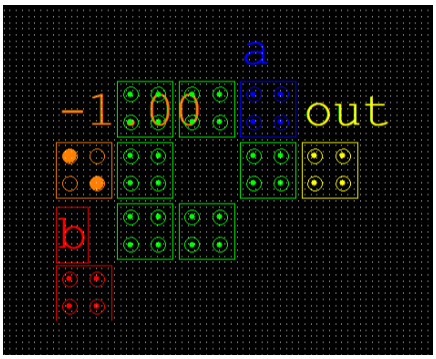


Fig 18. Proposed QCA XOR Diagram

- **XNOR Gate**

  When there are an odd number of 1s in the input, the Exclusive NOR gate produces an output 0. It can also be said as a complementary of exclusive OR Gate.

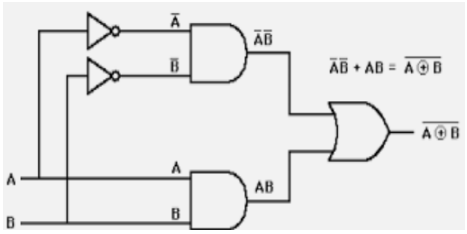


Fig 19. Basic XNOR Gate using AND and OR

A	B	XNOR
0	0	1
0	1	0
1	0	0
1	1	1

Table 2. XNOR Gate

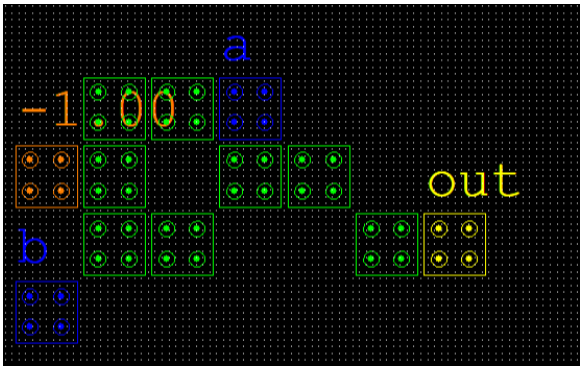


Fig 20. Proposed QCA XNOR Diagram

CHAPTER 8

ADVANTAGES AND APPLICATIONS

8.1 Advantages

- They outperform cmos technology in terms of efficiency.
- They take up less space than cmos technology.
- They use less electricity than cmos technology.

8.2 Applications

- These topologies serve specific purposes in communication-based circuit applications.
- They are particularly helpful in digital phase detectors.
- They are employed in mathematical operations.
- They are employed in error-detection circuits.
- They are employed in circuit correction.

CHAPTER 9
RESULTS AND DISCUSSION

A QCAD Designer is a well-known simulation programme for creating and testing QCA circuits. This software includes two simulation engines: a bistable engine and a coherence vector engine. By running simulation, the bistable gives better outcomes than the coherence vector engine does. The proposed logic gate is implemented and simulated in this study utilising QCA Designer software. This proposed structure can clearly perform XOR and XNOR logic functions by manipulating the values that permit inputs. The simulation results for the XOR and XNOR logic functions are displayed.

XOR Gate:

When the input a and b is equal to 0 the output is equal to 0, when a=0 and b=1 the output is equal to 1, when a=1 and b=0 the output is equal to 1 and when both the inputs are 1 the output is 0.

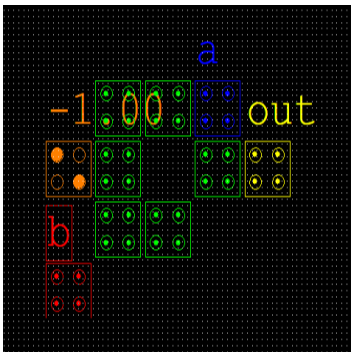


Fig 18. Proposed QCA XOR

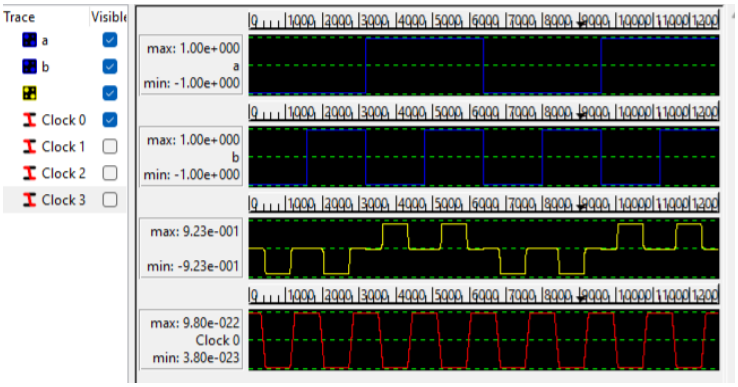


Fig 21 QCA XOR Simulation Output

XNOR Gate:

When the input a and b is equal to 0 the output is equal to 1, when a=0 and b=1 the output is equal to 0, when a=1 and b=0 the output is equal to 0 and when both the inputs are 1 the output is 1.

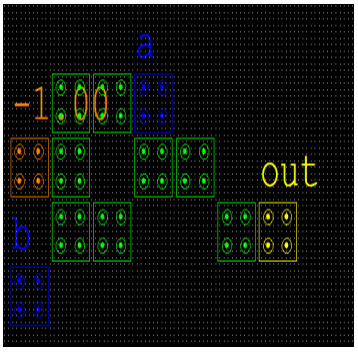


Fig 20. Proposed QCA XNOR

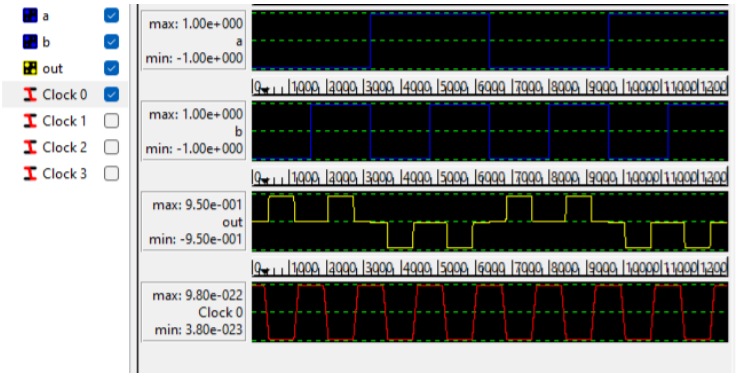


Fig 22 QCA XNOR Simulation Output

Analysis and Evaluation:

Table 3 shows a comparison of the proposed 2-input digital "XOR" gate to the other layouts. The intricacy of this table is determined by the amount of required cells. Latency is determined by the number of needed clock zones, area by μm2, cell size by (nm). Based on the suggested 2-input digital "XOR" gate depicted in Fig. 18, simulation findings in Fig. 21, the current "XOR" gate outperforms existing architectures in terms of complexity and area.

Table 3. QCA comparison with Existing

Structure	Cell Size (nm * nm)	Latency (clock)	Complexity	Area (μm2)
[9]	18 × 18	1.5	60	0.09
[11]	18 × 18	2.0	54	0.08
[13]	18 × 18	0.75	29	0.03
[10]	18 × 18	0.75	28	0.02
[12]	18 × 18	0.5	12	0.0116
[14]	18 × 18	0.5	14	0.01
Proposed QCA	**18 × 18**	**1.0**	**10**	**0.0096**

There are several benefits to employing QCA technology, such as the fact that it is "edge driven," which means that an input is delivered to one edge of a QCA block, evaluated, and output at another edge. This also eliminates the requirement for internal power wires. Because there is no current owing, QCA systems should be very low power. Only a small amount of energy is required to elevate the electrons from their ground states. Finally, because QCA cells are so small in size, the needed space for a circuit is relatively little. Clocking is controlled by a reference signal in VLSI design, while in QCA, timing is handled by clocking in four separate and periodic states, as shown in fig4.

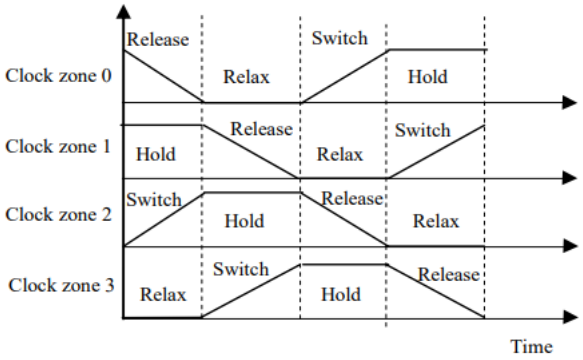


Fig 23. Different phases of QCA clock zones

A QCA circuit is separated into one-dimensional zones, each of which is kept in phase. The use of the quasiadiabatic switching technique for QCA circuits necessitates the use of a 4-phased clocking signal, which is often supplied via CMOS wires buried beneath the QCA circuitry for modifying the electric field. Relax, Switch, Hold, and Release are the names given to these four phases. The actual computing occurs during the first phase, so the inter-dot barrier gradually rises and a cell attains a final polarity under the influence of its neighbours. Barriers are substantial during the second phase, and a cell maintains its polarity. During the third phase, barriers decrease and a cell loses its polarity, and lastly, there's no inter-dot barrier and a cell stays un-polarized in the final phase. The following regular processing of these four clock phases is used to arrange the timing zones of a QCA circuit.

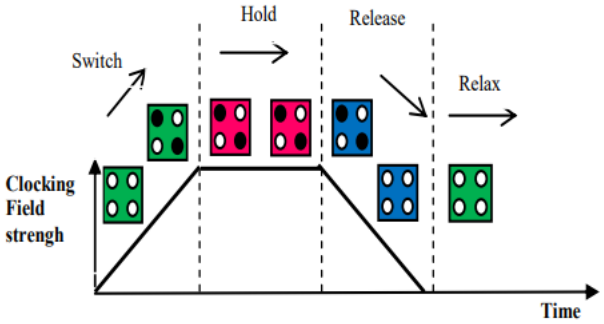


Fig 24. Schematic of interdot barriers in a clocking zone

A latch between two clocking zones is required. When one clocking zone enters Hold mode, a signal is latched and acts as input to the next zone. The clocking method incorporates pipelining and enables multi-bit information transfer for QCA via signal latching.

As a result of a zone in the Hold phase being followed by a zone in the Switch phase. Designs are partitioned in one dimension, resulting in clocking zone columns.

Table 4. Operation of QCA clock phases

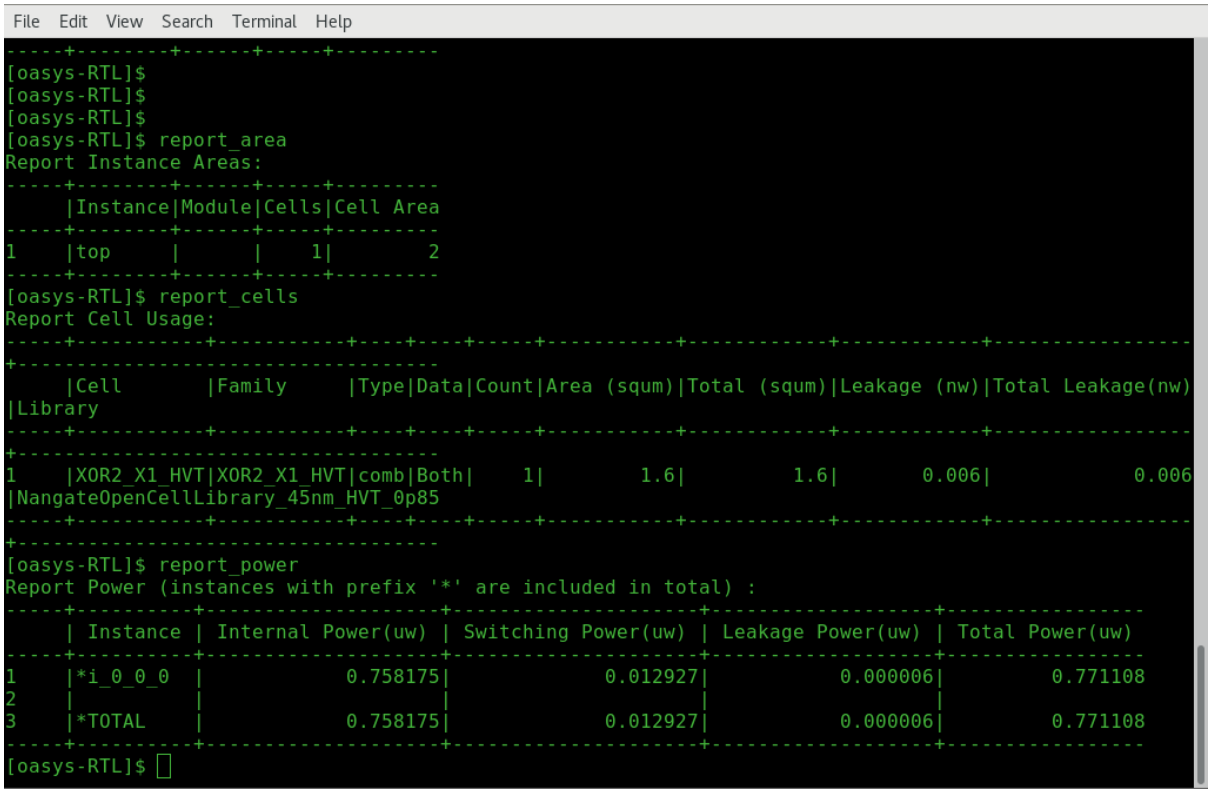
Clock Phase	Potential Barrier	Polarization state of the Cells
Hold	Held High	Polarized
Switch	Low to High	Polarized
Relax	Low	Unpolarized
Release	Lowered	Unpolarized

Performance Analysis :

The performance analysis parameters of the realised logic gates XOR and XNOR in QCA and CMOS are tabulated in Table 5. According to Table 5, logic gates constructed with QCA technology give highly efficient integrated design in comparison to CMOS technology. Table 5 shows the total number of QCA cells required in the design of XOR and XNOR gates, as well as the total area used to realise each gate in both QCA and CMOS technologies.
The tabulated QCA results indicate the improvements over the CMOS results. To design and acquire the covered area of all realised gates, CMOS software tools Oasysis utilised. In conclusion, the number of cells used to build XOR and XNOR gates in QCA is substantially lower than in CMOS.

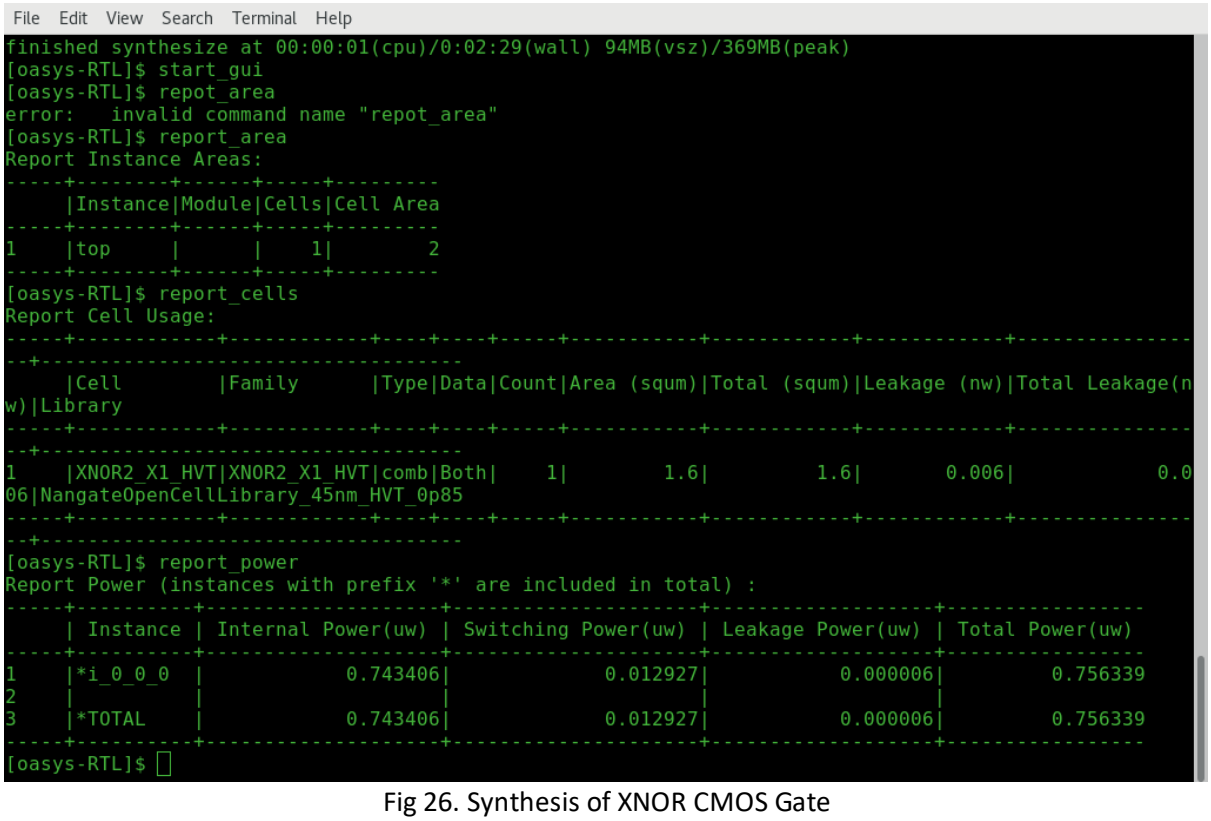
Table 5. Performance analysis of realized xor and xnor gates

Parameters	XOR gate	XNOR gate
Number of Cells in QCA	10	11
Number of Cells in CMOS	1	1
Cell Area in QCA	324 nm2	324 nm2
Cell Area in CMOS	2 μm2	2 μm2
Total Area in QCA	0.0096 μm2	0.01152 μm2
Total Area in CMOS	1.6 μm2	1.6 μm2



```
File  Edit  View  Search  Terminal  Help
-----+--------+------+-----+---------
[oasys-RTL]$
[oasys-RTL]$
[oasys-RTL]$
[oasys-RTL]$ report_area
Report Instance Areas:
-----+--------+------+-----+---------
     |Instance|Module|Cells|Cell Area
-----+--------+------+-----+---------
1    |top     |      |    1|        2
-----+--------+------+-----+---------
[oasys-RTL]$ report_cells
Report Cell Usage:
-----+-----------+-----------+----+----+-----+-----------+-----------+-----------+----------------
+-----------------------------------
     |Cell       |Family     |Type|Data|Count|Area (squm)|Total (squm)|Leakage (nw)|Total Leakage(nw)
|Library
-----+-----------+-----------+----+----+-----+-----------+-----------+-----------+----------------
+-----------------------------------
1    |XOR2_X1_HVT|XOR2_X1_HVT|comb|Both|    1|        1.6|        1.6|      0.006|           0.006
|NangateOpenCellLibrary_45nm_HVT_0p85
-----+-----------+-----------+----+----+-----+-----------+-----------+-----------+----------------
+-----------------------------------
[oasys-RTL]$ report_power
Report Power (instances with prefix '*' are included in total) :
-----+----------+--------------------+--------------------+------------------+----------------
     | Instance | Internal Power(uw) | Switching Power(uw) | Leakage Power(uw) | Total Power(uw)
-----+----------+--------------------+--------------------+------------------+----------------
1    |*i_0_0_0  |            0.758175|            0.012927|          0.000006|         0.771108
2    |          |                    |                    |                  |
3    |*TOTAL    |            0.758175|            0.012927|          0.000006|         0.771108
-----+----------+--------------------+--------------------+------------------+----------------
[oasys-RTL]$
```

Fig 25. Synthesis of XOR CMOS Gate



```
File  Edit  View  Search  Terminal  Help
finished synthesize at 00:00:01(cpu)/0:02:29(wall) 94MB(vsz)/369MB(peak)
[oasys-RTL]$ start_gui
[oasys-RTL]$ repot_area
error:   invalid command name "repot_area"
[oasys-RTL]$ report_area
Report Instance Areas:
-----+--------+------+-----+---------
     |Instance|Module|Cells|Cell Area
-----+--------+------+-----+---------
1    |top     |      |    1|        2
-----+--------+------+-----+---------
[oasys-RTL]$ report_cells
Report Cell Usage:
-----+------------+------------+----+----+-----+-----------+-----------+-----------+---------------
--+-----------------------------------
     |Cell        |Family      |Type|Data|Count|Area (squm)|Total (squm)|Leakage (nw)|Total Leakage(n
w)|Library
-----+------------+------------+----+----+-----+-----------+-----------+-----------+---------------
--+-----------------------------------
1    |XNOR2_X1_HVT|XNOR2_X1_HVT|comb|Both|    1|        1.6|        1.6|      0.006|            0.0
06|NangateOpenCellLibrary_45nm_HVT_0p85
-----+------------+------------+----+----+-----+-----------+-----------+-----------+---------------
--+-----------------------------------
[oasys-RTL]$ report_power
Report Power (instances with prefix '*' are included in total) :
-----+----------+--------------------+--------------------+------------------+----------------
     | Instance | Internal Power(uw) | Switching Power(uw) | Leakage Power(uw) | Total Power(uw)
-----+----------+--------------------+--------------------+------------------+----------------
1    |*i_0_0_0  |            0.743406|            0.012927|          0.000006|         0.756339
2    |          |                    |                    |                  |
3    |*TOTAL    |            0.743406|            0.012927|          0.000006|         0.756339
-----+----------+--------------------+--------------------+------------------+----------------
[oasys-RTL]$
```

Fig 26. Synthesis of XNOR CMOS Gate

CHAPTER 10

FUTURE SCOPE AND CONCLUSION

Quantum-dot cellular automata (QCA) is a novel Nano scale circuit design approach that can be used to create highly scalable logic circuits. Because logic gates are fundamental in most digital circuits, having fast speed, less complex, and smaller designs is critical. The implemented designs and simulation results are the solution for the idea of QCA-based digital circuits with fewer QCA cells and a smaller size criteria.

This study revealed how to use QCA designer to improve the design and implementation of various logic gates, which outperformed all previous designs and showed considerable improvements. The main goal of this study is to construct simple QCA-based logic gates with considerable adaptability and compatibility utilising a majority gate. Furthermore, the resulting results are validated against the associated truth table.

The various digital "XOR" gates can be used in receiver and sender units for parity checking, detection, and correction. Furthermore, the "XOR" gate architecture is significant in the arithmetic and logical unit (ALU) of a CPU. We have optimised the number of QCA cellules and decreased wire-crossings in the current planned work. This research could be expanded to create more reversible QCA gates.

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