User's Manual

1chip

User's Manual

Multimedia Processor for Mobile Applications
EMMA Mobile TM EV2

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Technology Corp. website (http://www.renesas.com).

Renesas Electronics
www.renesas.com

Rev.8.00 May 2011

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the EMMA Mobile EV2. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	EMMA Mobile EV2 Datasheet	R19DS0010EJxxxx
User's manual (1chip)	Hardware whole specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	EMMA Mobile EV2 User's manual 1chip	R19UH0036EJxxxx
User's manual (module)	Hardware each macro specifications and operation description.	EMMA Mobile EV2 User's manual each module	See below

Document Name	Document No.	Document Name	Document No.
1chip	R19UH0036EJxxxx	DMA Controller	R19UH0043EJxxxx
System Management Unit	R19UH0037EJxxxx	LP-DDR/DDR2 Controller	R19UH0039EJxxxx
Timer	R19UH0054EJxxxx	SD Memory Card Interface	R19UH0061EJxxxx
System Timer	R19UH0055EJxxxx	SDIO Interface	R19UH0042EJxxxx
HD Video Decoder	R19UH0056EJxxxx	CF Card Interface	R19UH0062EJxxxx
Rotator	R19UH0057EJxxxx	Unified Serial Interface	R19UH0047EJxxxx
Resizer	R19UH0058EJxxxx	UART interface	R19UH0040EJxxxx
Image Composer	R19UH0038EJxxxx	USB 2.0 Host Controller	R19UH0045EJxxxx
LCD Interface	R19UH0044EJxxxx	USB 2.0 Function Contoller	R19UH0034EJxxxx
ITU-R BT.656 Interface	R19UH0059EJxxxx	IIC Interface	R19UH0052EJxxxx
Digital Terrestrial TV Interface	R19UH0048EJxxxx	General Purpose I/O Interface	R19UH0041EJxxxx
Camera Interface	R19UH0060EJxxxx	Pulse Width Modulation Interface	R19UH0063EJxxxx

4 digits of end shows the version.

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b or 11
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX register

This register (XXXXXXX: xxxx_xxxxh) …..

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.

*1 *3 *2

*1

R/W: Read and Write.

R: Read only.

W: Write only.

-: Nothing is assigned.

*2

Reserved bit.

Reserved bit. Set to specified value.

*3

・ Nothing is assigned.

Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.

・ Do not set to a value.

Operation is not guaranteed when a value is set.

・ Function varies according to the operating mode.

The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

All trademarks and registered trademarks are the property of their respective owners.

EMMA Mobile is registered trademark of Renesas Electronics Corporation in Japan, USA and other countries.
ARM is the registered trademark of ARM Limited in the EU and other countries.
Coretex-A9 is the trademarks of ARM Limited in the EU and other countries.

Table of Contents

1. Overview 1
1.1 Features 1
1.2 Product List 2
1.3 Block Diagram 3
1.4 Pin Layout 4

2. Pin Functions 8
2.1 Pin Configuration 8
2.2 Pin Functions 9
2.2.1 System control signals 9
2.2.2 OSC signals 9
2.2.3 JTAG interface signals 10
2.2.4 External memory interface signals 11
2.2.5 DDR SDRAM interface signals 12
2.2.6 Unified serial interface port 0 signals 14
2.2.7 Unified serial interface port 1 signals 14
2.2.8 Unified serial interface port 2 signals 14
2.2.9 Unified serial interface port 3 signals 14
2.2.10 Unified serial interface port 4 signals 15
2.2.11 Unified serial interface port 5 signals 15
2.2.12 Digital terrestrial TV interface signals 15
2.2.13 UART interface port 0 signals 16
2.2.14 UART interface port 1 signals 16
2.2.15 UART interface port 2 signals 16
2.2.16 UART interface port 3 signals 16
2.2.17 USB interface port 1 signals 16
2.2.18 USB interface port 2 signals 16
2.2.19 I2C interface port 0 signals 17
2.2.20 I2C interface port 1 signals 17
2.2.21 LCD interface signals 18
2.2.22 YUV interface signals 19
2.2.23 SD card interface signals 19
2.2.24 SDIO interface port 0 signals 20
2.2.25 SDIO interface port 1 signals 20
2.2.26 SDIO interface port 2 signals 20
2.2.27 CF card interface signals 21
2.2.28 GPIO interface signals 22
2.2.29 PWM interface signals 26
2.2.30 Camera interface signals 26
2.2.31 ITU-R BT.656 interface signals 26
2.2.32 Trace port interface signals 27
2.2.33 Power supply pins 28
2.3 Pin Multiplex Function 29

3. Core Functions 37
3.1 CPU 37
3.2 System Management Unit 38
3.2.1 Clock distribution 38
3.2.2 Reset distribution 38
3.2.3 Power domains 39

3.3 System Buses 40
3.4 Embedded Memory 41
3.4.1 SRAM 41
3.4.2 ROM 41
3.5 Testing and Debugging 42
3.5.1 Debugging features 42
3.5.2 Debug interface 42
3.5.3 Trace interface 42
3.6 DMA Controller 43
3.7 Timers 44
3.8 Interrupt Controller 45
3.9 AVE 46
3.9.1 Video decoder 46
3.9.2 Audio decoder 47
3.10 Rotator 48
3.10.1 Raster order mode 48
3.10.2 Random mode 48
3.10.3 Input (source)/output (destination) pixel boundary 48
3.11 Resizer 49
3.11.1 Resize channel 49
3.11.2 Rotate channel 49
3.11.3 Output (destination) pixel boundary 49
3.11.4 Input (source) pixel boundary 49
3.12 Image Composer 51
3.12.1 Image size 51
3.12.2 Color format 52
3.12.3 Layers 52
3.12.4 Block diagram 53
3.12.5 Gamma correction 53
3.12.6 Write back 53
3.12.7 Color format transfer 53
3.12.8 Interlace and de-interlace 53
3.12.9 Image wraparound 53
3.12.10 Direct path from resizer 53
3.12.11 Output interface 54
3.12.12 Endian 54
3.13 3D Graphics Accelerator 55
3.13.1 Performance 55
3.13.2 API 55
3.13.3 Output color format 55
3.14 SDRAM Interface 56
3.15 External Memory Interface 57
3.15.1 Features 57
3.15.2 NOR flash memory support 57
3.15.3 Asynchronous memory support 57
3.16 SD Card Interface 58
3.17 SDIO Interface 59
3.18 CF Interface 60
3.19 LCD Interface 61
3.19.1 LCD interface image data 62
3.19.2 YUV output interface image data 62
3.20 Camera Interface 64
3.21 USB Interface 65
3.22 UART Interface 66

3.23 I²C Interface ... 67
3.24 Unified Serial Interface ... 68
3.24.1 SPI features ... 68
3.24.2 Audio (PCM) features ... 68
3.25 General-Purpose I/O Interface (GPIO) ... 70

4. System Control ... 71
4.1 Memory Map ... 71
4.2 PLLs ... 73

5. Power Control ... 75
5.1 Power Separation Diagram ... 75
5.2 Power Mode Transition ... 76

6. Bus Structure ... 78
6.1 Bus configuration ... 78
6.2 BUS1 Registers ... 80

7. Interrupt Control ... 82
7.1 Overview ... 82
7.1.1 Interrupt source ... 83
7.1.2 Registers ... 87

8. Alternate Pin Function Switching (CHG) ... 88
8.1 Register List ... 88
8.2 Register details ... 91
8.2.1 Boot mode register ... 91
8.2.2 P[0:2] OFF data hold control register ... 92
8.2.3 SDIO[2:0]/SDC interrupt mask register ... 93
8.2.4 AB0 (ASYNC) boot switch register ... 95
8.2.5 1.8 V/3.3 V LCD enable register ... 96
8.2.6 GPIO[31:0] pin function selection register ... 97
8.2.7 GPIO[63:48] pin function selection register ... 98
8.2.8 GPIO[95:64] pin function selection register ... 99
8.2.9 GPIO[127:96] pin function selection register ... 100
8.2.10 GPIO[158:128] pin function selection register ... 101
8.2.11 3.3 V LCD pin function selection register ... 102
8.2.12 UART pin function selection register ... 103
8.2.13 IIC pin function selection register ... 104
8.2.14 AB pin function selection register ... 105
8.2.15 USI pin function selection register ... 106
8.2.16 HSI pin function selection register ... 107
8.2.17 Pull-up/pull-down/input enable/Schmitt trigger control register 0 ... 108
8.2.18 Pull-up/pull-down/input enable/Schmitt trigger control register 1 ... 109
8.2.19 Pull-up/pull-down/input enable/Schmitt trigger control register 2 ... 110
8.2.20 Pull-up/pull-down/input enable/Schmitt trigger control register 3 ... 111
8.2.21 Pull-up/pull-down/input enable/Schmitt trigger control register 4 ... 112
8.2.22 Pull-up/pull-down/input enable/Schmitt trigger control register 5 ... 113
8.2.23 Pull-up/pull-down/input enable/Schmitt trigger control register 6 ... 114
8.2.24 Pull-up/pull-down/input enable/Schmitt trigger control register 7 ... 115
8.2.25 Pull-up/pull-down/input enable/Schmitt trigger control register 8 ... 116
8.2.26 Pull-up/pull-down/input enable/Schmitt trigger control register 9 ... 117
8.2.27 Pull-up/pull-down/input enable/Schmitt trigger control register 10 ... 118
8.2.28 Pull-up/pull-down/input enable/Schmitt trigger control register 11 ... 119

8.2.29 Pull-up/pull-down/input enable/Schmitt trigger control register 12 ... 120
8.2.30 Pull-up/pull-down/input enable/Schmitt trigger control register 13 ... 121
8.2.31 Pull-up/pull-down/input enable/Schmitt trigger control register 14 ... 122
8.2.32 Pull-up/pull-down/input enable/Schmitt trigger control register 15 ... 123
8.2.33 Pull-up/pull-down/input enable/Schmitt trigger control register 16 ... 124
8.2.34 Pull-up/pull-down/input enable/Schmitt trigger control register 17 ... 125
8.2.35 Pull-up/pull-down/input enable/Schmitt trigger control register 18 ... 126
8.2.36 Pull-up/pull-down/input enable/Schmitt trigger control register 19 ... 127
8.2.37 Pull-up/pull-down/input enable/Schmitt trigger control register 20 ... 128
8.2.38 Pull-up/pull-down/input enable/Schmitt trigger control register 21 ... 129
8.2.39 Pull-up/pull-down/input enable/Schmitt trigger control register 22 ... 130
8.2.40 Pull-up/pull-down/input enable/Schmitt trigger control register 25 ... 131
8.2.41 Driving capability selection register 0 ... 132
8.2.42 Driving capability selection register 1 ... 133
8.2.43 Driving capability selection register 2 ... 134
8.2.44 Driving capability selection register 3 ... 135
8.2.45 Driving capability selection register 4 ... 136
8.2.46 Driving capability selection register 5 ... 137
8.2.47 Bus hold function on/off switching register ... 138
8.2.48 AB_CLK output selection register ... 139
8.2.49 3.3 V LCD delay/phase setting register ... 140
8.2.50 AB_CLK delay/phase setting register ... 141
8.2.51 3.3 V ICE delay/phase setting register ... 142
8.2.52 1.8 V ICE delay/phase setting register ... 144
8.2.53 CHGREG reset control register (for testing) ... 145

APPENDIX A. Register List ... 146
A.1 Timers (TI0, TI1, TI2, TI3, TW0, TW1, TW2, TW3, TW4, TG0, TG1, TG2, TG3, TG4, TG5) ... 146
A.2 Unified Serial Interface (SIO0 to SIO5) ... 147
A.3 Interrupt Interface (INTA) ... 149
A.4 LCD Interface ... 151
A.5 General-Purpose I/O Interface (GIO) ... 154
A.6 I^2C Interface (IIC0, IIC1) ... 156
A.7 LP-DDR/ DDR2 Controller (MEMC) ... 157
A.8 PDMA ... 158
A.9 Power Management Unit (PMU) ... 159
A.10 System Management Unit (SMU) ... 160
A.11 Alternate Function Switching (CHG) ... 172
A.12 System Timer (STI) ... 175
A.13 UART Interface (UART) ... 176
A.14 DMA Controller (DMAC) ... 177
A.15 Camera Interface (CAM) ... 190
A.16 Pulse Width Modulation Interface ... 192
A.17 Digital Terrestrial TV Interface (DTV) ... 194
A.18 Resizer (SIZ) ... 195
A.19 HD Video Decoder (AVE) ... 197
A.20 ITU-R BT.656 Interface (NTS) ... 199
A.21 Rotator (ROT) ... 200
A.22 Image Composer (IMC/IMCW) ... 201
A.23 SD Card Interface ... 211
A.24 CF Card Interface ... 213
A.25 SDIO Interface ... 214

APPENDIX B. Clock Tree ... 216

APPENDIX C. Boot Loader 217
C.1 Overview 217
C.1.1 Restrictions 217
C.1.2 Cautions 217
C.2 Operational Overview 218
C.2.1 SD boot 219
C.2.2 eMMC boot 220
C.3 Processing Flow 221
C.3.1 ROM-internal boot loader common processing 221
C.3.2 eMMC boot processing 226
C.3.3 SD boot processing 230
C.4 Memory Allocation 235
C.4.1 SRAM 235
C.4.2 ROM 236

APPENDIX D. Signal Pins 237

APPENDIX E. External Bus Interface 240
E.1 Registers 240
E.1.1 System control registers 240
E.1.2 Parameter registers 241
E.1.3 Parameter retention registers 242
E.2 Register Details 243
E.2.1 Flash command start register 243
E.2.2 Flash read data latch register 244
E.2.3 Flash command (ADD0) setting register 244
E.2.4 Flash command (DATA0) setting register 245
E.2.5 Flash command (ADD1) setting register 246
E.2.6 Flash command (DATA1) setting register 247
E.2.7 Flash clock control register 248
E.2.8 Wait pin status register 249
E.2.9 CSn base address register 250
E.2.10 CSn bit compare register 251
E.2.11 CSn wait control register 253
E.2.12 CSn write wait control register 256
E.2.13 CSn read mode register 259
E.2.14 CSn wait mask register 261
E.2.15 CSn control register 262
E.2.16 CSn read configuration register 263

APPENDIX F. Internal SRAM (SRC) 264
F.1 Overview 264
F.1.1 Function overview 264
F.2 Registers 265
F.3 Register Details 265
F.3.1 CPU L2 cache mode enable register 265
F.3.2 Interrupt status register 266
F.3.3 Interrupt raw status register 266
F.3.4 Interrupt enable/monitor register 267
F.3.5 Interrupt enable clear register 267
F.3.6 Interrupt source clear register 268
F.4 Function overview 268
F.4.1 Clocks and reset 268

APPENDIX G. PMU 269
G.1 Overview 269
G.1.1 Function overview 269
G.1.2 WDT control and reset request 271
G.1.3 Transition to power-on sequence by interrupt signal 271
G.2 Registers 272
G.2.1 Register details 273
G.3 Function Details 291
G.3.1 PMU commands 291
G.4 PMU Commands 292
G.4.1 Register access commands 292
G.4.2 Logical operation commands 293
G.4.3 Branch and jump commands 293
G.4.4 Wait commands 294
G.4.5 Interrupt mask commands 295
G.4.6 Other commands 296
G.4.7 Other commands 297

APPENDIX H. Power supply required specification 298
H.1 About each power supply system state 298
H.1.1 Normal 299
H.1.2 DeepSleep 299
H.1.3 PowerOff 299
H.1.4 Without power supply 299
H.2 EM/EV power supply connection diagram (reference) 300
H.3 Power supply sequence 301
H.3.1 Without power supply -> Normal 301
H.3.2 DeepSleep <-> Normal 302
H.3.3 PowerOff <-> Normal 305

1. Overview

EMMA Mobile™ EV (EM/EV) is an application processor for mobile multimedia handset devices. EM/EV utilizes two ARM® Coretex-A9 cores with two Neon extensions, an integrated audio video engine (AV engine), and a 3D graphics block to enable high-class processing in a range of applications. The processor contains a wide variety of interfaces for cameras, displays, mass storage devices, memory devices, and many other peripherals.
EM/EV achieves high-performance multimedia processing of up to HD-level decoding by means of hardware acceleration, while consuming minimal power.

1.1 Features

- CPU: ARM Cortex-A9 (Frequency: 533 MHz, I-cache: 32 KB, D-cache: 32 KB, L2 cache : 256KB)
- AV engine: High-performance multimedia processor
  - Video:
    - Decoder: Multi decoder (H.264, VC-1, MPEG 1/2, H.263, MPEG-4: up to 1920×1080p 30fps), other decoders/encoders may be implemented by software using CPU resources
  - Audio:
    - Decoder: MPEG-4 HE-AAC decoder, enhanced aacPlus decoder
- 3D Graphics accelerator (A3D)
  - 3D: 14.7 Mpix/sec
    Supporting OpenGL-ES2.0, OpenGL-ES1.x
- Image processor: Resizing, rotating, image composing with alpha blending and key color masking
- Image composer: Image composing with alpha blending and key color masking, gamma correction
  - Direct connection to LCD interface
- Security functions: Secure boot function, secure timer, secure watchdog timer, secure DMA
- Internal memories: SRAM: 128 KB, ROM: 64 KB
- DMA controller: 8 channels
- Timers: Interval timers and watchdog timers: 15 channels
- DRAM interface:
  LPDDR-SDRAM interface: Max 200 MHz DDR (DDR400), 32 bits, up to 1.6 GB/s
  DDR2-SDRAM interface: Max 266 MHz DDR (DDR533), 32 bits, up to 2.1 GB/s
- NOR-Flash interface: 16-bit data bus
- Peripheral interfaces:
  - Memory card interface: SD card (with CPRM [Note])× 1, SDIO × 3, CF card interface (Note Option)
  - Image interfaces:
    - LCD interface → Parallel interface
    - ITU-R BT.656 interface
    - Camera interface → Parallel interface
  - Other serial interfaces:
    - USB 2.0 host × 1 and peripheral × 1 (with PHY)
    - UART × 4
    - I2C × 2
    - Unified serial interface × 6 (SPI, I2S)

- General-purpose I/O port interface × 159

- Testing and debugging: ARM CoreSight, JTAG

- Power supply voltage
  - Core Logic: 1.1V to 1.2 V
  - PLL: 1.1 V to 1.2V
  - IO power supply: 1.8 V, 3.3 V
- Power management

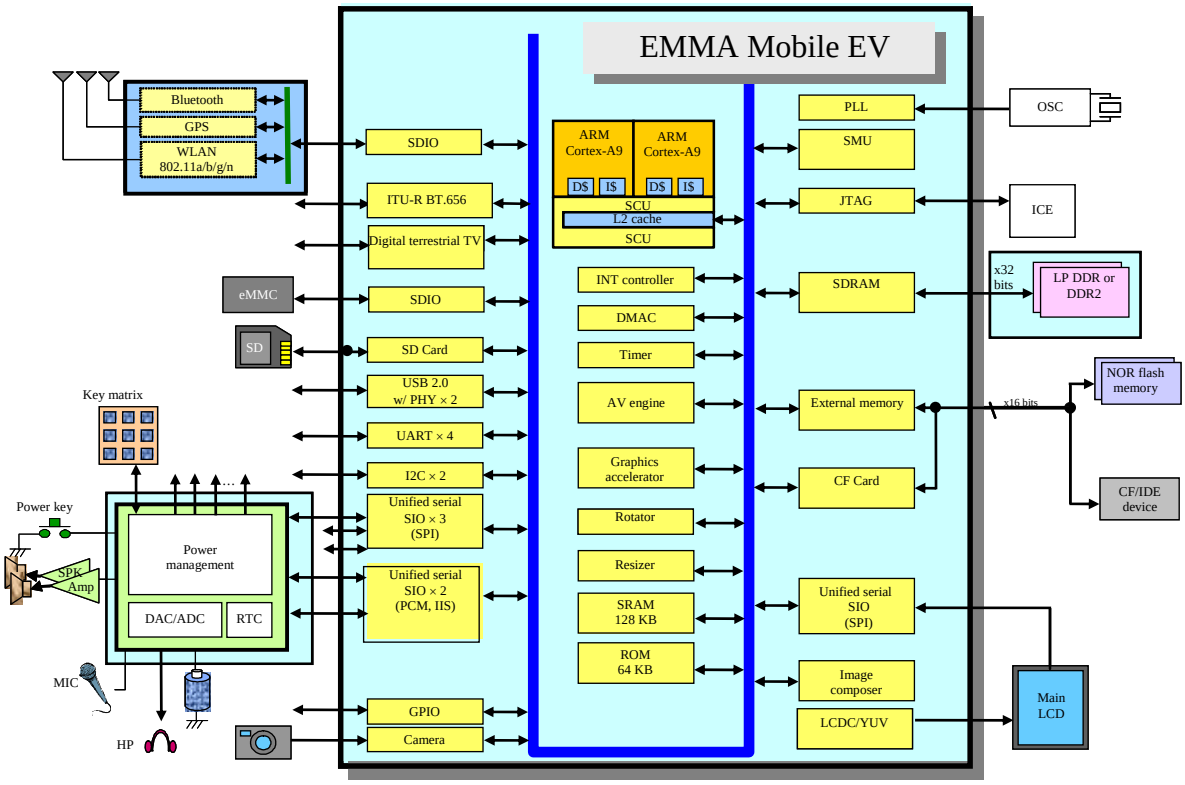
  Several power saving operation modes are supported.

1.2 Product List

Part No.	Package Type
μPD77642BF1-GA9-A	393pin FPBGA (16mm×16mm, 0.65mm pitch)

1.3 Block Diagram

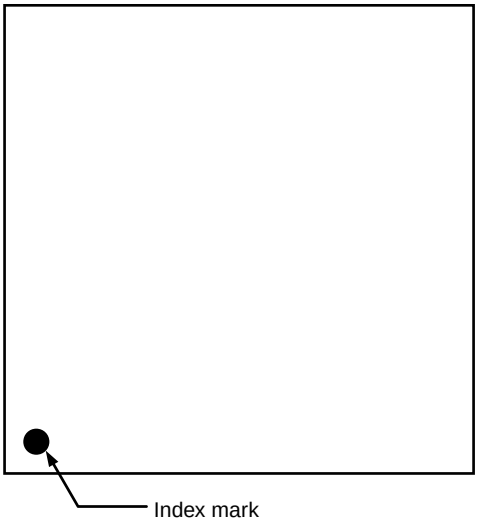
Figure 1-1 EM/EV Block Diagram



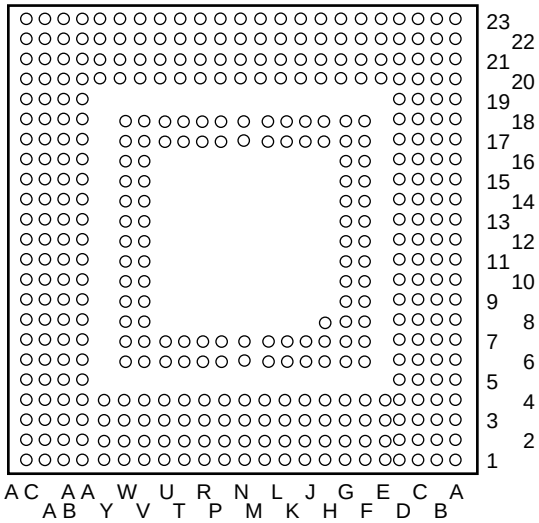
1.4 Pin Layout

393-pin FPBGA (16 × 16 mm, 0.65-min pitch)

Top View



Bottom View



(1/4)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	GND	A22	GND	B20	LCD3_R1
A2	GND	A23	GND	B21	LCD3_HS
A3	VDD33D	B1	GND	B22	LCD3_PXCLK
A4	AVDD	B2	GND	B23	GND
A5	C32K	B3	AFS_ARSTB	C1	DDR_DQ7
A6	GND	B4	AVDD	C2	DDR_DQ0
A7	GND	B5	GND	C3	DDR_DQ2
A8	OSC0_XT2	B6	USI0_CLK	C4	AGND
A9	OSC0_XT1	B7	USI0_CS0	C5	NECTESTIO
A10	GND	B8	USI0_CS1	C6	UTEST (When being unused, "L" is fixed.)
A11	JT_TCK	B9	USI0_CS2	C7	GND
A12	LOWPWR	B10	USI0_DI	C8	GND
A13	PONDET	B11	USI0_DO	C9	USI1_CLK
A14	GND	B12	SRESETB	C10	USI1_DI
A15	LCD3_B1	B13	VDD18	C11	JT_TRSTB
A16	LCD3_B0	B14	LCD3_B5	C12	NC (leave open)
A17	LCD3_G1	B15	LCD3_B2	C13	JT_TDI
A18	LCD3_G0	B16	LCD3_G5	C14	LCD3_B6
A19	LCD3_R2	B17	LCD3_G2	C15	LCD3_B3
A20	LCD3_R0	B18	LCD3_R5	C16	LCD3_G6
A21	LCD3_CLK_I	B19	LCD3_R3	C17	LCD3_G3

(2/4)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
C18	LCD3_R6	F7	VDD33	H7	GND
C19	LCD3_R4	F8	TRSTB	H8	GND
C20	LCD3_VS	F9	VDD11	H17	VDD33
C21	GPIO_019	F10	VDD11	H18	GPIO_030
C22	AB_AD1	F11	BOOTSEL2	H20	AB_WRB
C23	AB_AD0	F12	BOOTSEL0	H21	AB_AD14
D1	DDR_DM0	F13	JT_TDOEN	H22	AB_AD13
D2	DDR_DQ4	F14	JT_TMS	H23	AB_AD12
D3	DDR_DQ6	F15	VDD18	J1	DDR_A0
D4	DDR_DQ1	F16	GPIO_026	J2	DDR_A2
D5	AGND	F17	GPIO_027	J3	DDR_GND
D6	TE1	F18	GPIO_028	J4	DDR_DQ14
D7	TE2	F20	AB_CSB2	J6	DDR_CS1B
D8	GND	F21	AB_AD8	J7	VDD11
D9	GND	F22	AB_AD7	J17	VDD11
D10	USI1_DO	F23	AB_AD6	J18	GPIO_031
D11	USI1_CS0	G1	DDR_DQ11	J20	AB_RDB
D12	JT_DBG_EN	G2	DDR_DQ8	J21	AB_A17
D13	JT_TDO	G3	DDR_DM1	J22	AB_AD15
D14	LCD3_B7	G4	DDR_DQ9	J23	AB_CLK
D15	LCD3_B4	G6	VDD11	K1	DDR_BA2
D16	LCD3_G7	G7	GND	K2	DDR_BA0
D17	LCD3_G4	G8	VDD18	K3	DDR_A3
D18	LCD3_R7	G9	GND	K4	DDR_A10
D19	LCD3_DE	G10	GND	K6	DDR_CASB
D20	GPIO_024	G11	BOOTSEL1	K7	DDR_VDDIO
D21	AB_CSB0	G12	VDD33M	K17	VDD33
D22	AB_AD3	G13	VDD11	K18	VDD11
D23	AB_AD2	G14	GND	K20	AB_ADV
E1	DDR_DQS0	G15	VDD33	K21	AB_A18
E2	DDR_DQS0B	G16	VDD11	K22	HSI_CAWAKE Note1
E3	DDR_DQ3	G17	GND	K23	HSI_CADATA Note1
E4	DDR_DQ5	G18	GPIO_029	L1	DDR_CKE0
E20	GPIO_025	G20	AB_CSB3	L2	DDR_A14
E21	AB_CSB1	G21	AB_AD11	L3	DDR_A1
E22	AB_AD5	G22	AB_AD10	L4	DDR_BA1
E23	AB_AD4	G23	AB_AD9	L6	DDR_RASB
F1	DDR_DQS1	H1	DDR_DQ12	L7	DDR_CS0B
F2	DDR_DQS1B	H2	DDR_DQ15	L17	AB_A27
F3	DDR_GND	H3	DDR_DQ13	L18	AB_A24
F4	DDR_VREFL	H4	DDR_DQ10	L20	AB_WAIT
F6	DDR_VDDIO	H6	DDR_VDDIO	L21	AB_A19

Note1 : The HSI function is not available.

(3/4)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
L22	HSI_ACREADY Note1	R4	DDR_DQ20	U23	CAM_YUV5
L23	HSI_CAFLAG Note1	R6	DDR_VDDIO	V1	DDR_DQS2
M1	DDR_CK	R7	GND	V2	DDR_DQS2B
M2	DDR_CKB	R17	VDD33	V3	DDR_GND
M3	DDR_GND	R18	NTSC_DATA3	V4	DDR_VREFH
M4	DDR_WEB	R20	NTSC_DATA2	V6	VDD18
M6	DDR_ODT Note2	R21	GND	V7	VDD33M
M7	GND	R22	IC	V8	GPIO_004
M17	AB_A28	R23	IC	V9	GPIO_002
M18	AB_A25	T1	DDR_DQ16	V10	GPIO_000
M20	AB_A22	T2	DDR_DQ17	V11	VDD18
M21	AB_A20	T3	DDR_DQ22	V12	UART0_TX
M22	HSI_CAREADY Note1	T4	DDR_DQ19	V13	UART0_RX
M23	HSI_ACFLAG Note1	T6	DDR_VDDIO	V14	VDD11
N1	DDR_CKE1	T7	GND	V15	GPIO_009
N2	DDR_GND	T17	VDD11	V16	GPIO_008
N3	DDR_A11	T18	NTSC_DATA5	V17	GPIO_007
N4	DDR_A13	T20	NTSC_DATA4	V18	GPIO_006
N6	DDR_CKERSTB	T21	CAM_YUV0	V20	NTSC_CLK
N7	DDR_VDDIO	T22	CAM_YUV1	V21	CAM_HS
N17	VDD18	T23	CAM_YUV2	V22	CAM_YUV6
N18	AB_A26	U1	DDR_DQ21	V23	CAM_YUV7
N20	AB_A23	U2	DDR_DQ18	W1	DDR_DQS3
N21	AB_A21	U3	DDR_DQ23	W2	DDR_DQS3B
N22	HSI_ACWAKE Note1	U4	DDR_DM2	W3	DDR_DQ31
N23	HSI_ACDATA Note1	U6	VDD11	W4	DDR_DQ30
P1	DDR_A12	U7	GND	W20	GPIO_017
P2	DDR_A7	U8	GPIO_005	W21	GPIO_016
P3	DDR_A8	U9	GPIO_003	W22	CAM_VS
P4	DDR_A6	U10	GPIO_001	W23	CAM_CLKO
P6	VDD11	U11	GND	Y1	DDR_DM3
P7	GND	U12	GND	Y2	DDR_DQ27
P17	VDD11	U13	VDD11	Y3	DDR_DQ25
P18	NTSC_DATA1	U14	VDD33	Y4	DDR_DQ29
P20	NTSC_DATA0	U15	VDD33	Y5	PWM1
P21	GND	U16	GND	Y6	USI2_CS2
P22	IC	U17	VDD18	Y7	USI2_CS0
P23	IC	U18	NTSC_DATA7	Y8	IIC1_SDA
R1	DDR_A9	U20	NTSC_DATA6	Y9	IIC1_SCL
R2	DDR_A5	U21	CAM_YUV3	Y10	UART1_TX
R3	DDR_A4	U22	CAM_YUV4	Y11	UART1_RX

Note1 : The HSI function is not available.

Note2 : The on die termination function for DDR-ODT is not available.

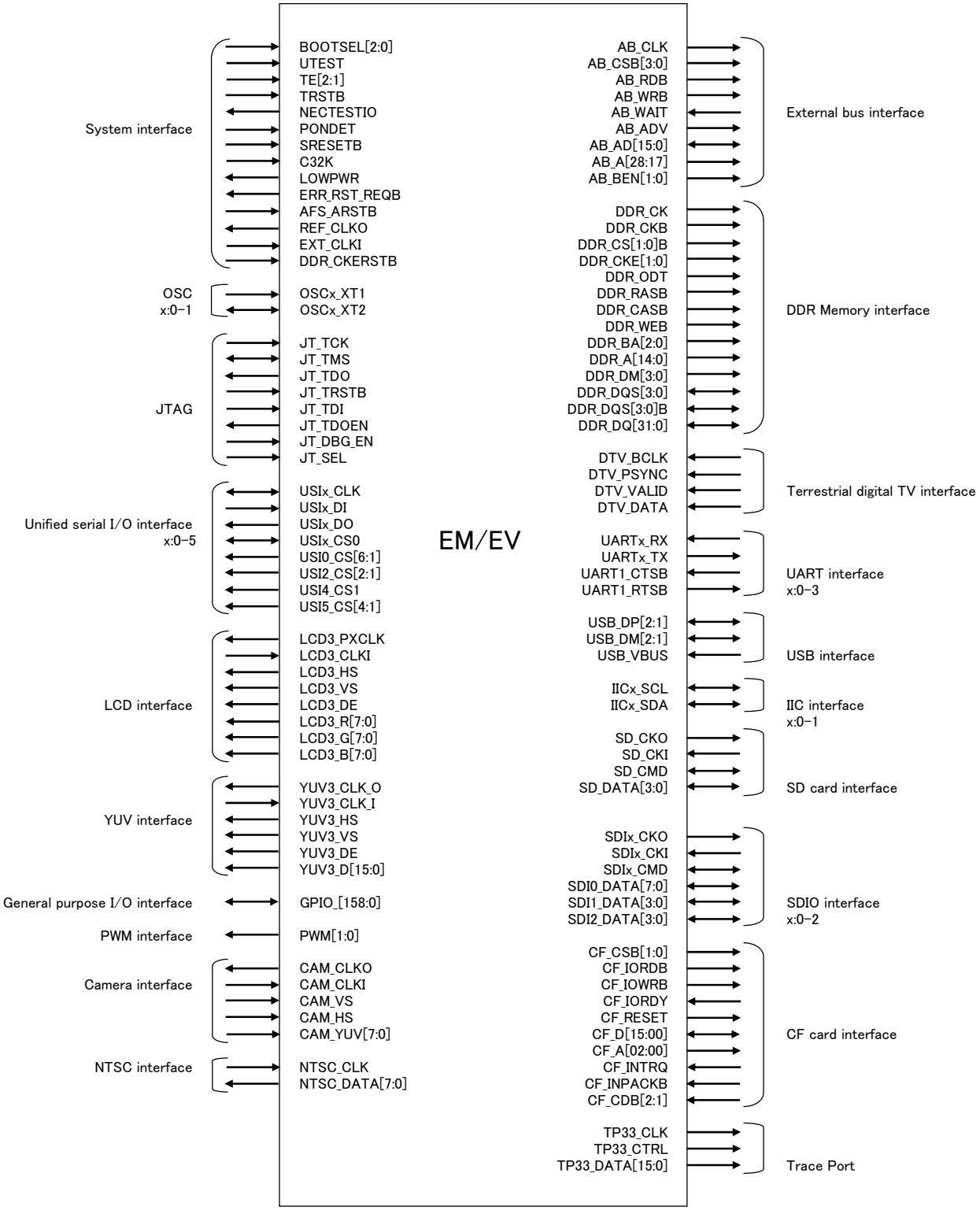
(4/4)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
Y12	SDI0_CMD	AA18	SD_DATA1	AC1	GND
Y13	SDI0_DATA1	AA19	SDI1_DATA3	AC2	GND
Y14	SDI0_DATA3	AA20	GPIO_012	AC3	USI3_DO
Y15	SDI0_DATA5	AA21	GPIO_011	AC4	USI3_DI
Y16	SDI0_DATA7	AA22	GPIO_010	AC5	USI3_CLK
Y17	SD_DATA2	AA23	SDI1_CKI	AC6	USB_AVDD2
Y18	SD_DATA0	AB1	GND	AC7	USB_RREF2
Y19	GPIO_015	AB2	GND	AC8	USB_GND12
Y20	GPIO_014	AB3	GPIO_119	AC9	USB_DM2
Y21	GPIO_013	AB4	USI3_CS0	AC10	USB_GND22
Y22	GND	AB5	USI2_CLK	AC11	USB_RREF1
Y23	CAM_CLKI	AB6	USB_AVSS2	AC12	USB_PVSS1
AA1	DDR_DQ24	AB7	USB_PVSS2	AC13	USB_DM1
AA2	DDR_DQ28	AB8	USB_VD3312	AC14	USB_GND21
AA3	DDR_DQ26	AB9	USB_DP2	AC15	OSC1_XT1
AA4	PWM0	AB10	UART1_RTSB	AC16	OSC1_XT2
AA5	USI2_DO	AB11	USB_AVDD1	AC17	GND
AA6	USI2_DI	AB12	USB_AVSS1	AC18	SDI0_CKI
AA7	USI2_CS1	AB13	USB_DP1	AC19	SD_CKI
AA8	IIC0_SDA	AB14	USB_VD3311	AC20	SD_CKO
AA9	IIC0_SCL	AB15	GND	AC21	SDI1_CMD
AA10	UART1_CTSB	AB16	GPIO_049	AC22	GND
AA11	USB_GND11	AB17	SD_CMD	AC23	GND
AA12	USB_VBUS	AB18	SDI0_CKO		
AA13	SDI0_DATA0	AB19	SDI1_DATA2		
AA14	SDI0_DATA2	AB20	SDI1_DATA1		
AA15	SDI0_DATA4	AB21	SDI1_DATA0		
AA16	SDI0_DATA6	AB22	SDI1_CKO		
AA17	SD_DATA3	AB23	GND		

2. Pin Functions

2.1 Pin Configuration

Figure 2-1 EM/EV Pin Configuration



2.2 Pin Functions

2.2.1 System control signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
BOOTSEL2	F11	Input	Boot mode selection 2	VDD18	BOOTSEL2
BOOTSEL1	G11	Input	Boot mode selection 1	VDD18	BOOTSEL1
BOOTSEL0	F12	Input	Boot mode selection 0	VDD18	BOOTSEL0
UTEST Note	C6	Input	Test	VDD18	UTEST
TE1	D6	Input	Test	VDD18	TE1
TE2	D7	Input	Test	VDD18	TE2
TRSTB	F8	Input	Test	VDD18	TRSTB
NECTESTIO	C5	Output	Test	VDD33	NECTESTIO
PONDET	A13	Input	Power-on reset	VDD18	PONDET
SRESETB	B12	Input	System reset	VDD18	SRESETB
C32K	A5	Input	32.768 kHz clock	VDD18	C32K
ERR_RST_REQB	U9	Output	Error reset request	VDD18/VDD33	GPIO_003
LOWPWR	A12	Output	Low power control signal	VDD18	LOWPWR
AFS_ARSTB	B3	Input	Antifuse asynchronous reset	VDD18	AFS_ARSTB
REF_CLKO	V8	Output	Reference clock output	VDD18/VDD33	GPIO_004
EXT_CLKI	U8	Input	Reference clock input	VDD18/VDD33	GPIO_001
DDR_CKERSTB	N6	Input	Clock reset input	VDD18	DDR_CKERSTB

Note : When being unused, "L" is fixed.

2.2.2 OSC signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
OSC0_XT1	A9	Input	OSC input	VDD18	OSC0_XT1
OSC0_XT2	A8	I/O	OSC output	VDD18	OSC0_XT2
OSC1_XT1	AC15	Input	OSC input	VDD18	OSC1_XT1
OSC1_XT2	AC16	I/O	OSC output	VDD18	OSC1_XT2

2.2.3 JTAG interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
JT_TCK	A11	Input	JTAG clock input	VDD18	JT_TCK
JT_TRSTB	C11	Input	JTAG reset input	VDD18	JT_TRSTB
JT_TMS	F14	I/O	JTAG test mode	VDD18	JT_TMS
JT_TDI	C13	Input	JTAG data input	VDD18	JT_TDI
JT_TDO	D13	Output	JTAG data output	VDD18	JT_TDO
JT_TDOEN	F13	Output	JTAG data output enable	VDD18	JT_TDOEN
JT_DBG_EN	D12	Input	JTAG debug enable	VDD18	JT_DBG_EN
JT_SEL	V9	Input	JTAG select	VDD18/VDD33	JT_SEL

2.2.4 External memory interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
AB_AD15	J22	I/O	Address/data bus bit 15	VDD33	GPIO_092
AB_AD14	H21	I/O	Address/data bus bit 14	VDD33	GPIO_091
AB_AD13	H22	I/O	Address/data bus bit 13	VDD33	GPIO_090
AB_AD12	H23	I/O	Address/data bus bit 12	VDD33	GPIO_089
AB_AD11	G21	I/O	Address/data bus bit 11	VDD33	GPIO_088
AB_AD10	G22	I/O	Address/data bus bit 10	VDD33	GPIO_087
AB_AD9	G23	I/O	Address/data bus bit 9	VDD33	GPIO_086
AB_AD8	F21	I/O	Address/data bus bit 8	VDD33	GPIO_085
AB_AD7	F22	I/O	Address/data bus bit 7	VDD33	GPIO_084
AB_AD6	F23	I/O	Address/data bus bit 6	VDD33	GPIO_083
AB_AD5	E22	I/O	Address/data bus bit 5	VDD33	GPIO_082
AB_AD4	E23	I/O	Address/data bus bit 4	VDD33	GPIO_081
AB_AD3	D22	I/O	Address/data bus bit 3	VDD33	GPIO_080
AB_AD2	D23	I/O	Address/data bus bit 2	VDD33	GPIO_079
AB_AD1	C22	I/O	Address/data bus bit 1	VDD33	GPIO_078
AB_AD0	C23	I/O	Address/data bus bit 0	VDD33	GPIO_077
AB_A28	M17	Output	Address bus bit 26	VDD33	GPIO_104
AB_A27	L17	Output	Address bus bit 26	VDD33	GPIO_103
AB_A26	N18	Output	Address bus bit 26	VDD33	GPIO_102
AB_A25	M18	Output	Address bus bit 25	VDD33	GPIO_101
AB_A24	L18	Output	Address bus bit 24	VDD33	GPIO_100
AB_A23	N20	Output	Address bus bit 23	VDD33	GPIO_099
AB_A22	M20	Output	Address bus bit 22	VDD33	GPIO_098
AB_A21	N21	Output	Address bus bit 21	VDD33	GPIO_097
AB_A20	M21	Output	Address bus bit 20	VDD33	GPIO_096
AB_A19	L21	Output	Address bus bit 19	VDD33	GPIO_095
AB_A18	K21	Output	Address bus bit 18	VDD33	GPIO_094
AB_A17	J21	Output	Address bus bit 17	VDD33	GPIO_093
AB_RDB	J20	Output	Read strobe	VDD33	GPIO_073
AB_WRB	H20	Output	Write strobe	VDD33	GPIO_074
AB_ADV	K20	Output	Address valid	VDD33	GPIO_076
AB_WAIT	L20	Input	Wait	VDD33	GPIO_075
AB_CSB3	G20	Output	Chip select 3	VDD33	GPIO_072
AB_CSB2	F20	Output	Chip select 2	VDD33	GPIO_071
AB_CSB1	E21	Output	Chip select 1	VDD33	GPIO_070
AB_CSB0	D21	Output	Chip select 0	VDD33	GPIO_069
AB_CLK	J23	Output	Bus clock output	VDD33	GPIO_068

2.2.5 DDR SDRAM interface signals

(1/2)

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
DDR_A14	L2	Output	Command/address bit 14	VDD18	DDR_A14
DDR_A13	N4	Output	Command/address bit 13	VDD18	DDR_A13
DDR_A12	P1	Output	Command/address bit 12	VDD18	DDR_A12
DDR_A11	N3	Output	Command/address bit 11	VDD18	DDR_A11
DDR_A10	K4	Output	Command/address bit 10	VDD18	DDR_A10
DDR_A9	R1	Output	Command/address bit 9	VDD18	DDR_A9
DDR_A8	P3	Output	Command/address bit 8	VDD18	DDR_A8
DDR_A7	P2	Output	Command/address bit 7	VDD18	DDR_A7
DDR_A6	P4	Output	Command/address bit 6	VDD18	DDR_A6
DDR_A5	R2	Output	Command/address bit 5	VDD18	DDR_A5
DDR_A4	R3	Output	Command/address bit 4	VDD18	DDR_A4
DDR_A3	K3	Output	Command/address bit 3	VDD18	DDR_A3
DDR_A2	J2	Output	Command/address bit 2	VDD18	DDR_A2
DDR_A1	L3	Output	Command/address bit 1	VDD18	DDR_A1
DDR_A0	J1	Output	Command/address bit 0	VDD18	DDR_A0
DDR_CS0B	L7	Output	Chip select 0	VDD18	DDR_CSB0
DDR_CS1B	J6	Output	Chip select 1	VDD18	DDR_CSB1
DDR_CK	M1	Output	Clock +	VDD18	DDR_CK
DDR_CKB	M2	Output	Clock –	VDD18	DDR_CKB
DDR_CKE0	L1	Output	Clock enable 0	VDD18	DDR_CKE0
DDR_CKE1	N1	Output	Clock enable 1	VDD18	DDR_CKE1
DDR_DM3	Y1	I/O	Data mask bit 3	VDD18	DDR_DM3
DDR_DM2	U4	I/O	Data mask bit 2	VDD18	DDR_DM2
DDR_DM1	G3	I/O	Data mask bit 1	VDD18	DDR_DM1
DDR_DM0	D1	I/O	Data mask bit 0	VDD18	DDR_DM0
DDR_DQ31	W3	I/O	Data bit 31	VDD18	DDR_DQ31
DDR_DQ30	W4	I/O	Data bit 30	VDD18	DDR_DQ30
DDR_DQ29	Y4	I/O	Data bit 29	VDD18	DDR_DQ29
DDR_DQ28	AA2	I/O	Data bit 28	VDD18	DDR_DQ28
DDR_DQ27	Y2	I/O	Data bit 27	VDD18	DDR_DQ27
DDR_DQ26	AA3	I/O	Data bit 26	VDD18	DDR_DQ26
DDR_DQ25	Y3	I/O	Data bit 25	VDD18	DDR_DQ25
DDR_DQ24	AA1	I/O	Data bit 24	VDD18	DDR_DQ24
DDR_DQ23	U3	I/O	Data bit 23	VDD18	DDR_DQ23
DDR_DQ22	T3	I/O	Data bit 22	VDD18	DDR_DQ22
DDR_DQ21	U1	I/O	Data bit 21	VDD18	DDR_DQ21
DDR_DQ20	R4	I/O	Data bit 20	VDD18	DDR_DQ20
DDR_DQ19	T4	I/O	Data bit 19	VDD18	DDR_DQ19
DDR_DQ18	U2	I/O	Data bit 18	VDD18	DDR_DQ18
DDR_DQ17	T2	I/O	Data bit 17	VDD18	DDR_DQ17

(2/2)

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
DDR_DQ16	T1	I/O	Data bit 16	VDD18	DDR_DQ16
DDR_DQ15	H2	I/O	Data bit 15	VDD18	DDR_DQ15
DDR_DQ14	J4	I/O	Data bit 14	VDD18	DDR_DQ14
DDR_DQ13	H3	I/O	Data bit 13	VDD18	DDR_DQ13
DDR_DQ12	H1	I/O	Data bit 12	VDD18	DDR_DQ12
DDR_DQ11	G1	I/O	Data bit 11	VDD18	DDR_DQ11
DDR_DQ10	H4	I/O	Data bit 10	VDD18	DDR_DQ10
DDR_DQ9	G4	I/O	Data bit 9	VDD18	DDR_DQ9
DDR_DQ8	G2	I/O	Data bit 8	VDD18	DDR_DQ8
DDR_DQ7	C1	I/O	Data bit 7	VDD18	DDR_DQ7
DDR_DQ6	D3	I/O	Data bit 6	VDD18	DDR_DQ6
DDR_DQ5	E4	I/O	Data bit 5	VDD18	DDR_DQ5
DDR_DQ4	D2	I/O	Data bit 4	VDD18	DDR_DQ4
DDR_DQ3	E3	I/O	Data bit 3	VDD18	DDR_DQ3
DDR_DQ2	C3	I/O	Data bit 2	VDD18	DDR_DQ2
DDR_DQ1	D4	I/O	Data bit 1	VDD18	DDR_DQ1
DDR_DQ0	C2	I/O	Data bit 0	VDD18	DDR_DQ0
DDR_DQS3	W1	I/O	Data strobe bit 3 +	VDD18	DDR_DQS3
DDR_DQS3B	W2	I/O	Data strobe bit 3 –	VDD18	DDR_DQS3B
DDR_DQS2	V1	I/O	Data strobe bit 2 +	VDD18	DDR_DQS2
DDR_DQS2B	V2	I/O	Data strobe bit 2 –	VDD18	DDR_DQS2B
DDR_DQS1	F1	I/O	Data strobe bit 1 +	VDD18	DDR_DQS1
DDR_DQS1B	F2	I/O	Data strobe bit 1 –	VDD18	DDR_DQS1B
DDR_DQS0	E1	I/O	Data strobe bit 0 +	VDD18	DDR_DQS0
DDR_DQS0B	E2	I/O	Data strobe bit 0 –	VDD18	DDR_DQS0B
DDR_RASB	L6	Output	RAS	VDD18	DDR_RASB
DDR_CASB	K6	Output	CAS	VDD18	DDR_CASB
DDR_WEB	M4	Output	Write enable	VDD18	DDR_WEB
DDR_BA2	K1	Output	Bank address bit 2	VDD18	DDR_BA2
DDR_BA1	L4	Output	Bank address bit 1	VDD18	DDR_BA1
DDR_BA0	K2	Output	Bank address bit 0	VDD18	DDR_BA0
DDR_ODT	M6	Output	On-die termination –	VDD18	DDR_ODT

Note : The on die termination function for DDR-ODT is not available.

2.2.6 Unified serial interface port 0 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
USI0_DI	B10	Input	Port 0 data input	VDD18/VDD33	USI0_DI
USI0_DO	B11	Output	Port 0 data output	VDD18/VDD33	USI0_DO
USI0_CLK	B6	I/O	Port 0 clock input/output	VDD18/VDD33	USI0_CLK
USI0_CS6	AB4	Output	Port 0 CS6	VDD18/VDD33	GPIO_118
USI0_CS5	AC3	Output	Port 0 CS5	VDD18/VDD33	GPIO_117
USI0_CS4	AC4	Output	Port 0 CS4	VDD18/VDD33	GPIO_116
USI0_CS3	AC5	Output	Port 0 CS3	VDD18/VDD33	GPIO_115
USI0_CS2	B9	Output	Port 0 CS2	VDD18/VDD33	GPIO_106
USI0_CS1	B8	Output	Port 0 CS1	VDD18/VDD33	GPIO_105
USI0_CS0	B7	I/O	Port 0 CS0	VDD18/VDD33	USI0_CS0

2.2.7 Unified serial interface port 1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
USI1_DI	C10	Input	Port 1 data input	VDD18/VDD33	USI1_DI
USI1_DO	D10	Output	Port 1 data output	VDD18/VDD33	USI1_DO
USI1_CLK	C9	I/O	Port 1 clock input/output	VDD18/VDD33	USI1_CLK
USI1_CS0	D11	I/O	Port 1 CS0	VDD18/VDD33	USI1_CS0

2.2.8 Unified serial interface port 2 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
USI2_DI	AA6	Input	Port 2 data input	VDD18/VDD33	USI2_DI
USI2_DO	AA5	Output	Port 2 data output	VDD18/VDD33	USI2_DO
USI2_CLK	AB5	I/O	Port 2 clock input/output	VDD18/VDD33	USI2_CLK
USI2_CS2	Y6	Output	Port 2 CS2	VDD18/VDD33	GPIO_114
USI2_CS1	AA7	Output	Port 2 CS1	VDD18/VDD33	GPIO_113
USI2_CS0	Y7	I/O	Port 2 CS0	VDD18/VDD33	USI2_CS0

2.2.9 Unified serial interface port 3 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
USI3_DI	AC4	Input	Port 3 data input	VDD18/VDD33	GPIO_116
USI3_DO	AC3	Output	Port 3 data output	VDD18/VDD33	GPIO_117
USI3_CLK	AC5	I/O	Port 3 clock input/output	VDD18/VDD33	GPIO_115
USI3_CS0	AB4	I/O	Port 3 CS0	VDD18/VDD33	GPIO_118

2.2.10 Unified serial interface port 4 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
USI4_DI	AA4	Input	Port 4 data input	VDD18/VDD33	GPIO_120
USI4_DO	Y5	Output	Port 4 data output	VDD18/VDD33	GPIO_121
USI4_CLK	AB3	I/O	Port 4 clock input/output	VDD18/VDD33	GPIO_119
USI4_CS1	Y6	Output	Port 4 CS1	VDD18/VDD33	GPIO_114
USI4_CS0	AA7	I/O	Port 4 CS0	VDD18/VDD33	GPIO_113

2.2.11 Unified serial interface port 5 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
USI5_DI	G23	Input	Port 5 data input	VDD33	GPIO_086
	M22			VDD18	GPIO_150
USI5_DO	G22	Output	Port 5 data output	VDD33	GPIO_087
	K23			VDD18	GPIO_144
USI5_CLK	F21	I/O	Port 5 clock input/output	VDD33	GPIO_085
	K22			VDD18	GPIO_143
USI5_CS4	M23	Output	Port 5 CS4	VDD18	GPIO_149
USI5_CS3	N23	Output	Port 5 CS3	VDD18	GPIO_148
USI5_CS2	H22	Output	Port 5 CS2	VDD33	GPIO_090
	N22			VDD18	GPIO_147
USI5_CS1	H23	Output	Port 5 CS1	VDD33	GPIO_089
	L22			VDD18	GPIO_146
USI5_CS0	G21	I/O	Port 5 CS0	VDD33	GPIO_088
	L23			VDD18	GPIO_145

2.2.12 Digital terrestrial TV interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
DTV_BCLK	F21	Input	DTV clock input	VDD33	GPIO_085
	AB5	Input	DTV clock input	VDD18/VDD33	USI2_CLK
DTV_PSYNC	G23	Input	DTV sync.	VDD33	GPIO_086
	AA6	Input	DTV sync.	VDD18/VDD33	USI2_DI
DTV_VALID	G22	Input	DTV valid	VDD33	GPIO_087
	AA5	Input	DTV valid	VDD18/VDD33	USI2_DO
DTV_DATA	G21	Input	DTV data input	VDD33	GPIO_088
	Y7	Input	DTV data input	VDD18/VDD33	USI2_CS0

2.2.13 UART interface port 0 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
UART0_RX	V13	Input	Port 0 SIN	VDD18/VDD33	UART0_RX
UART0_TX	V12	Output	Port 0 SOUT	VDD18/VDD33	UART0_TX

2.2.14 UART interface port 1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
UART1_RX	Y11	Input	Port 1 SIN	VDD18/VDD33	GPIO_155
UART1_TX	Y10	Output	Port 1 SOUT	VDD18/VDD33	GPIO_156
UART1_RTSB	AB10	Output	Port 1 RTS	VDD18/VDD33	GPIO_158
UART1_CTSB	AA10	Input	Port 1 CTS	VDD18/VDD33	GPIO_157

2.2.15 UART interface port 2 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
UART2_RX	AA10	Input	Port 2 SIN	VDD18/VDD33	GPIO_157
UART2_TX	AB10	Output	Port 2 SOUT	VDD18/VDD33	GPIO_158

2.2.16 UART interface port 3 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
UART3_RX	Y9	Input	Port 3 SIN	VDD18/VDD33	IIC1_SCL
UART3_TX	Y8	Output	Port 3 SOUT	VDD18/VDD33	IIC1_SDA

2.2.17 USB interface port 1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
USB_DP1	AB13	I/O	USB port 1 data input/output	VDD33	USB_DP1
USB_DM1	AC13	I/O	USB port 1 data input/output	VDD33	USB_DM1

2.2.18 USB interface port 2 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
USB_DP2	AB9	I/O	USB port 2 data input/output	VDD33	USB_DP2
USB_DM2	AC9	I/O	USB port 2 data input/output	VDD33	USB_DM2
USB_VBUS	AA12	Input	USB VBUS	VDD33	USB_VBUS

2.2.19 I2C interface port 0 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
IIC0_SCL	AA9	OT	IIC0 clock	VDD18/VDD33	IIC0_SCL
IIC0_SDA	AA8	OT	IIC0 data	VDD18/VDD33	IIC0_SDA

Remark OT: 3-state output

2.2.20 I2C interface port 1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
IIC1_SCL	Y9	OT	IIC1 clock	VDD18/VDD33	IIC1_SCL
IIC1_SDA	Y8	OT	IIC1 data	VDD18/VDD33	IIC1_SDA

Remark OT: 3-state output

2.2.21 LCD interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
LCD3_PXCLK	B22	Output	Pixel clock	VDD33	GPIO_018
LCD3_CLK_I	A21	Input	Clock input	VDD33	GPIO_020
LCD3_HS	B21	Output	H sync	VDD33	GPIO_021
LCD3_VS	C20	Output	V sync	VDD33	GPIO_022
LCD3_DE	D19	Output	Enable	VDD33	GPIO_023
LCD3_R7	D18	Output	Red 7	VDD33	GPIO_039
LCD3_R6	C18	Output	Red 6	VDD33	GPIO_038
LCD3_R5	B18	Output	Red 5	VDD33	GPIO_037
LCD3_R4	C19	Output	Red 4	VDD33	GPIO_036
LCD3_R3	B19	Output	Red 3	VDD33	GPIO_035
LCD3_R2	A19	Output	Red 2	VDD33	GPIO_034
LCD3_R1	B20	Output	Red 1	VDD33	GPIO_033
LCD3_R0	A20	Output	Red 0	VDD33	GPIO_032
LCD3_G7	D16	Output	Green 7	VDD33	LCD3_G7
LCD3_G6	C16	Output	Green 6	VDD33	LCD3_G6
LCD3_G5	B16	Output	Green 5	VDD33	LCD3_G5
LCD3_G4	D17	Output	Green 4	VDD33	LCD3_G4
LCD3_G3	C17	Output	Green 3	VDD33	LCD3_G3
LCD3_G2	B17	Output	Green 2	VDD33	LCD3_G2
LCD3_G1	A17	Output	Green 1	VDD33	GPIO_041
LCD3_G0	A18	Output	Green 0	VDD33	GPIO_040
LCD3_B7	D14	Output	Blue 7	VDD33	LCD3_B7
LCD3_B6	C14	Output	Blue 6	VDD33	LCD3_B6
LCD3_B5	B14	Output	Blue 5	VDD33	LCD3_B5
LCD3_B4	D15	Output	Blue 4	VDD33	LCD3_B4
LCD3_B3	C15	Output	Blue 3	VDD33	LCD3_B3
LCD3_B2	B15	Output	Blue 2	VDD33	LCD3_B2
LCD3_B1	A15	Output	Blue 1	VDD33	GPIO_043
LCD3_B0	A16	Output	Blue 0	VDD33	GPIO_042

2.2.22 YUV interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
YUV3_D15	D14	Output	Data bit 15	VDD33	LCD3_B7
YUV3_D14	C14	Output	Data bit 14	VDD33	LCD3_B6
YUV3_D13	B14	Output	Data bit 13	VDD33	LCD3_B5
YUV3_D12	D15	Output	Data bit 12	VDD33	LCD3_B4
YUV3_D11	C15	Output	Data bit 11	VDD33	LCD3_B3
YUV3_D10	B15	Output	Data bit 10	VDD33	LCD3_B2
YUV3_D9	A15	Output	Data bit 9	VDD33	GPIO_043
YUV3_D8	A16	Output	Data bit 8	VDD33	GPIO_042
YUV3_D7	D16	Output	Data bit 7	VDD33	LCD3_G7
YUV3_D6	C16	Output	Data bit 6	VDD33	LCD3_G6
YUV3_D5	B16	Output	Data bit 5	VDD33	LCD3_G5
YUV3_D4	D17	Output	Data bit 4	VDD33	LCD3_G4
YUV3_D3	C17	Output	Data bit 3	VDD33	LCD3_G3
YUV3_D2	B17	Output	Data bit 2	VDD33	LCD3_G2
YUV3_D1	A17	Output	Data bit 1	VDD33	GPIO_041
YUV3_D0	A18	Output	Data bit 0	VDD33	GPIO_040
YUV3_CLK_O	B22	Output	Clock	VDD33	GPIO_018
YUV3_CLK_I	A21	Input	Clock	VDD33	GPIO_020
YUV3_HS	B21	Output	Hsync	VDD33	GPIO_021
YUV3_VS	C20	Output	Vsync	VDD33	GPIO_022
YUV3_DE	D19	Output	Enable	VDD33	GPIO_023

2.2.23 SD card interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
SD_CKO	AC20	Output	SD card clock output	VDD33	SD_CKO
SD_CKI	AC19	Input	SD card clock input	VDD33	SD_CKI
SD_CMD	AB17	I/O	SD card command	VDD33	SD_CMD
SD_DATA3	AA17	I/O	SD card data bit 3	VDD33	SD_DATA3
SD_DATA2	Y17	I/O	SD card data bit 2	VDD33	SD_DATA2
SD_DATA1	AA18	I/O	SD card data bit 1	VDD33	SD_DATA1
SD_DATA0	Y18	I/O	SD card data bit 0	VDD33	SD_DATA0

2.2.24 SDIO interface port 0 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
SDI0_CMD	Y12	I/O	SDIO0 command	VDD33	SDI0_CMD
SDI0_DATA7	Y16	I/O	SDIO0 data bit 7	VDD33	GPIO_060
SDI0_DATA6	AA16	I/O	SDIO0 data bit 6	VDD33	GPIO_059
SDI0_DATA5	Y15	I/O	SDIO0 data bit 5	VDD33	GPIO_058
SDI0_DATA4	AA15	I/O	SDIO0 data bit 4	VDD33	GPIO_057
SDI0_DATA3	Y14	I/O	SDIO0 data bit 3	VDD33	SDI0_DATA3
SDI0_DATA2	AA14	I/O	SDIO0 data bit 2	VDD33	SDI0_DATA2
SDI0_DATA1	Y13	I/O	SDIO0 data bit 1	VDD33	SDI0_DATA1
SDI0_DATA0	AA13	I/O	SDIO0 data bit 0	VDD33	SDI0_DATA0
SDI0_CKO	AB18	Output	SDIO0 clock output	VDD33	GPIO_050
SDI0_CKI	AC18	Input	SDIO0 clock input	VDD33	SDI0_CKI

2.2.25 SDIO interface port 1 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
SDI1_CMD	AC21	I/O	SDIO1 command	VDD33	SDI1_CMD
SDI1_DATA3	AA19	I/O	SDIO1 data bit 3	VDD33	SDI1_DATA3
SDI1_DATA2	AB19	I/O	SDIO1 data bit 2	VDD33	SDI1_DATA2
SDI1_DATA1	AB20	I/O	SDIO1 data bit 1	VDD33	SDI1_DATA1
SDI1_DATA0	AB21	I/O	SDIO1 data bit 0	VDD33	SDI1_DATA0
SDI1_CKO	AB22	Output	SDIO1 clock output	VDD33	GPIO_083
SDI1_CKI	AA23	Input	SDIO1 clock input	VDD33	SDI1_CKI

2.2.26 SDIO interface port 2 signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
SDI2_CMD	N20	I/O	SDIO2 command	VDD33	GPIO_099
SDI2_DATA3	J22	I/O	SDIO2 data bit 3	VDD33	GPIO_092
SDI2_DATA2	H21	I/O	SDIO2 data bit 2	VDD33	GPIO_091
SDI2_DATA1	H22	I/O	SDIO2 data bit 1	VDD33	GPIO_090
SDI2_DATA0	H23	I/O	SDIO2 data bit 0	VDD33	GPIO_089
SDI2_CKO	N21	Output	SDIO2 clock output	VDD33	GPIO_097
SDI2_CKI	M20	Input	SDIO2 clock input	VDD33	GPIO_098

2.2.27 CF card interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
CF_D15	J22	I/O	CF data bit 15	VDD33	GPIO_092
CF_D14	H21	I/O	CF data bit 14	VDD33	GPIO_091
CF_D13	H22	I/O	CF data bit 13	VDD33	GPIO_090
CF_D12	H23	I/O	CF data bit 12	VDD33	GPIO_089
CF_D11	G21	I/O	CF data bit 11	VDD33	GPIO_088
CF_D10	G22	I/O	CF data bit 10	VDD33	GPIO_087
CF_D09	G23	I/O	CF data bit 9	VDD33	GPIO_086
CF_D08	F21	I/O	CF data bit 8	VDD33	GPIO_085
CF_D07	F22	I/O	CF data bit 7	VDD33	GPIO_084
CF_D06	F23	I/O	CF data bit 6	VDD33	GPIO_083
CF_D05	E22	I/O	CF data bit 5	VDD33	GPIO_082
CF_D04	E23	I/O	CF data bit 4	VDD33	GPIO_081
CF_D03	D22	I/O	CF data bit 3	VDD33	GPIO_080
CF_D02	D23	I/O	CF data bit 2	VDD33	GPIO_079
CF_D01	C22	I/O	CF data bit 1	VDD33	GPIO_078
CF_D00	C23	I/O	CF data bit 0	VDD33	GPIO_077
CF_CSB1	G20	Output	CF chip select 1	VDD33	GPIO_072
CF_CSB0	F20	Output	CF chip select 0	VDD33	GPIO_071
CF_RESET	K20	Output	CF reset output	VDD33	GPIO_076
CF_A02	L21	Output	CF address bit 2	VDD33	GPIO_095
CF_A01	K21	Output	CF address bit 1	VDD33	GPIO_094
CF_A00	J21	Output	CF address bit 0	VDD33	GPIO_093
CF_IOWRB	H20	Output	CF write strobe	VDD33	GPIO_074
CF_IORDB	J20	Output	CF read strobe	VDD33	GPIO_073
CF_IORDY	L20	Input	CF I/O ready	VDD33	GPIO_075
CF_INTRQ	N21	Input	CF INT request	VDD33	GPIO_097
CF_INPACKB	L18	Input	IO read reply input (asynchronous)	VDD33	GPIO_100
CF_CDB1	M18	Input	CF card detection 1	VDD33	GPIO_101
CF_CDB2	N18	Input	CF card detection 2	VDD33	GPIO_102

2.2.28 GPIO interface signals

(1/4)

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
GPIO_158	AB10	I/O	General-purpose I/O	VDD18/VDD33	GPIO_158
GPIO_157	AA10	I/O	General-purpose I/O	VDD18/VDD33	GPIO_157
GPIO_156	Y10	I/O	General-purpose I/O	VDD18/VDD33	GPIO_156
GPIO_155	Y11	I/O	General-purpose I/O	VDD18/VDD33	GPIO_155
GPIO_154	A12	I/O	General-purpose I/O	VDD18	LOWPWR
GPIO_153	AA12	I/O	General-purpose I/O	VDD33	USB_VBUS
GPIO_152	F13	I/O	General-purpose I/O	VDD18	JT_TDOEN
GPIO_151	D13	I/O	General-purpose I/O	VDD18	JT_TDO
GPIO_150	M22	I/O	General-purpose I/O	VDD18	GPIO_150
GPIO_149	M23	I/O	General-purpose I/O	VDD18	GPIO_149
GPIO_148	N23	I/O	General-purpose I/O	VDD18	GPIO_148
GPIO_147	N22	I/O	General-purpose I/O	VDD18	GPIO_147
GPIO_146	L22	I/O	General-purpose I/O	VDD18	GPIO_146
GPIO_145	L23	I/O	General-purpose I/O	VDD18	GPIO_145
GPIO_144	K23	I/O	General-purpose I/O	VDD18	GPIO_144
GPIO_143	K22	I/O	General-purpose I/O	VDD18	GPIO_143
GPIO_142	V23	I/O	General-purpose I/O	VDD33	GPIO_142
GPIO_141	V22	I/O	General-purpose I/O	VDD33	GPIO_141
GPIO_140	U23	I/O	General-purpose I/O	VDD33	GPIO_140
GPIO_139	U22	I/O	General-purpose I/O	VDD33	GPIO_139
GPIO_138	U21	I/O	General-purpose I/O	VDD33	GPIO_138
GPIO_137	T23	I/O	General-purpose I/O	VDD33	GPIO_137
GPIO_136	T22	I/O	General-purpose I/O	VDD33	GPIO_136
GPIO_135	T21	I/O	General-purpose I/O	VDD33	GPIO_135
GPIO_134	V21	I/O	General-purpose I/O	VDD33	GPIO_134
GPIO_133	W22	I/O	General-purpose I/O	VDD33	GPIO_133
GPIO_132	Y23	I/O	General-purpose I/O	VDD33	GPIO_132
GPIO_131	W23	I/O	General-purpose I/O	VDD33	GPIO_131
GPIO_130	U18	I/O	General-purpose I/O	VDD33	GPIO_130
GPIO_129	U20	I/O	General-purpose I/O	VDD33	GPIO_129
GPIO_128	T18	I/O	General-purpose I/O	VDD33	GPIO_128
GPIO_127	T20	I/O	General-purpose I/O	VDD33	GPIO_127
GPIO_126	R18	I/O	General-purpose I/O	VDD33	GPIO_126
GPIO_125	R20	I/O	General-purpose I/O	VDD33	GPIO_125
GPIO_124	P18	I/O	General-purpose I/O	VDD33	GPIO_124
GPIO_123	P20	I/O	General-purpose I/O	VDD33	GPIO_123
GPIO_122	V20	I/O	General-purpose I/O	VDD33	GPIO_122
GPIO_121	Y5	I/O	General-purpose I/O	VDD18/VDD33	GPIO_121

Remark See 2.3 Pin Multiplex Function for details about GPIO multi-function pins and default pins.

(2/4)

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
GPIO_120	AA4	I/O	General-purpose I/O	VDD18/VDD33	GPIO_120
GPIO_119	AB3	I/O	General-purpose I/O	VDD18/VDD33	GPIO_119
GPIO_118	AB4	I/O	General-purpose I/O	VDD18/VDD33	GPIO_118
GPIO_117	AC3	I/O	General-purpose I/O	VDD18/VDD33	GPIO_117
GPIO_116	AC4	I/O	General-purpose I/O	VDD18/VDD33	GPIO_116
GPIO_115	AC5	I/O	General-purpose I/O	VDD18/VDD33	GPIO_115
GPIO_114	Y6	I/O	General-purpose I/O	VDD18/VDD33	GPIO_114
GPIO_113	AA7	I/O	General-purpose I/O	VDD18/VDD33	GPIO_113
GPIO_112	Y7	I/O	General-purpose I/O	VDD18/VDD33	USI2_CS0
GPIO_111	AA5	I/O	General-purpose I/O	VDD18/VDD33	USI2_DO
GPIO_110	AA6	I/O	General-purpose I/O	VDD18/VDD33	USI2_DI
GPIO_109	AB5	I/O	General-purpose I/O	VDD18/VDD33	USI2_CLK
GPIO_108	D10	I/O	General-purpose I/O	VDD18/VDD33	USI1_DO
GPIO_107	C10	I/O	General-purpose I/O	VDD18/VDD33	USI1_DI
GPIO_106	B9	I/O	General-purpose I/O	VDD18/VDD33	GPIO_106
GPIO_105	B8	I/O	General-purpose I/O	VDD18/VDD33	GPIO_105
GPIO_104	M17	I/O	General-purpose I/O	VDD33	GPIO_104
GPIO_103	L17	I/O	General-purpose I/O	VDD33	GPIO_103
GPIO_102	N18	I/O	General-purpose I/O	VDD33	GPIO_102
GPIO_101	M18	I/O	General-purpose I/O	VDD33	GPIO_101
GPIO_100	L18	I/O	General-purpose I/O	VDD33	GPIO_100
GPIO_099	N20	I/O	General-purpose I/O	VDD33	GPIO_099
GPIO_098	M20	I/O	General-purpose I/O	VDD33	GPIO_098
GPIO_097	N21	I/O	General-purpose I/O	VDD33	GPIO_097
GPIO_096	M21	I/O	General-purpose I/O	VDD33	GPIO_096
GPIO_095	L21	I/O	General-purpose I/O	VDD33	GPIO_095
GPIO_094	K21	I/O	General-purpose I/O	VDD33	GPIO_094
GPIO_093	J21	I/O	General-purpose I/O	VDD33	GPIO_093
GPIO_092	J22	I/O	General-purpose I/O	VDD33	GPIO_092
GPIO_091	H21	I/O	General-purpose I/O	VDD33	GPIO_091
GPIO_090	H22	I/O	General-purpose I/O	VDD33	GPIO_090
GPIO_089	H23	I/O	General-purpose I/O	VDD33	GPIO_089
GPIO_088	G21	I/O	General-purpose I/O	VDD33	GPIO_088
GPIO_087	G22	I/O	General-purpose I/O	VDD33	GPIO_087
GPIO_086	G23	I/O	General-purpose I/O	VDD33	GPIO_086
GPIO_085	F21	I/O	General-purpose I/O	VDD33	GPIO_085
GPIO_084	F22	I/O	General-purpose I/O	VDD33	GPIO_084
GPIO_083	F23	I/O	General-purpose I/O	VDD33	GPIO_083
GPIO_082	E22	I/O	General-purpose I/O	VDD33	GPIO_082
GPIO_081	E23	I/O	General-purpose I/O	VDD33	GPIO_081
GPIO_080	D22	I/O	General-purpose I/O	VDD33	GPIO_080

Remark See 2.3 Pin Multiplex Function for details about GPIO multi-function pins and default pins.

(3/4)

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
GPIO_079	D23	I/O	General-purpose I/O	VDD33	GPIO_079
GPIO_078	C22	I/O	General-purpose I/O	VDD33	GPIO_078
GPIO_077	C23	I/O	General-purpose I/O	VDD33	GPIO_077
GPIO_076	K20	I/O	General-purpose I/O	VDD33	GPIO_076
GPIO_075	L20	I/O	General-purpose I/O	VDD33	GPIO_075
GPIO_074	H20	I/O	General-purpose I/O	VDD33	GPIO_074
GPIO_073	J20	I/O	General-purpose I/O	VDD33	GPIO_073
GPIO_072	G20	I/O	General-purpose I/O	VDD33	GPIO_072
GPIO_071	F20	I/O	General-purpose I/O	VDD33	GPIO_071
GPIO_070	E21	I/O	General-purpose I/O	VDD33	GPIO_070
GPIO_069	D21	I/O	General-purpose I/O	VDD33	GPIO_069
GPIO_068	J23	I/O	General-purpose I/O	VDD33	GPIO_068
GPIO_067	AA19	I/O	General-purpose I/O	VDD33	SDI1_DATA3
GPIO_066	AB19	I/O	General-purpose I/O	VDD33	SDI1_DATA2
GPIO_065	AB20	I/O	General-purpose I/O	VDD33	SDI1_DATA1
GPIO_064	AB21	I/O	General-purpose I/O	VDD33	SDI1_DATA0
GPIO_063	AC21	I/O	General-purpose I/O	VDD33	SDI1_CMD
GPIO_062	AA23	I/O	General-purpose I/O	VDD33	SDI1_CKI
GPIO_061	AB22	I/O	General-purpose I/O	VDD33	GPIO_061
GPIO_060	Y16	I/O	General-purpose I/O	VDD33	GPIO_060
GPIO_059	AA16	I/O	General-purpose I/O	VDD33	GPIO_059
GPIO_058	Y15	I/O	General-purpose I/O	VDD33	GPIO_058
GPIO_057	AA15	I/O	General-purpose I/O	VDD33	GPIO_057
GPIO_056	Y14	I/O	General-purpose I/O	VDD33	SDI0_DATA3
GPIO_055	AA14	I/O	General-purpose I/O	VDD33	SDI0_DATA2
GPIO_054	Y13	I/O	General-purpose I/O	VDD33	SDI0_DATA1
GPIO_053	AA13	I/O	General-purpose I/O	VDD33	SDI0_DATA0
GPIO_052	Y12	I/O	General-purpose I/O	VDD33	SDI0_CMD
GPIO_051	AC18	I/O	General-purpose I/O	VDD33	SDI0_CKI
GPIO_050	AB18	I/O	General-purpose I/O	VDD33	GPIO_050
GPIO_049	AB16	I/O	General-purpose I/O	VDD33	GPIO_049
GPIO_048	AC19	I/O	General-purpose I/O	VDD33	SD_CKI
GPIO_047	Y8	I/O	General-purpose I/O	VDD18/VDD33	IIC1_SDA
GPIO_046	Y9	I/O	General-purpose I/O	VDD18/VDD33	IIC1_SCL
GPIO_045	AA8	I/O	General-purpose I/O	VDD18/VDD33	IIC0_SDA
GPIO_044	AA9	I/O	General-purpose I/O	VDD18/VDD33	IIC0_SCL
GPIO_043	A15	I/O	General-purpose I/O	VDD33	GPIO_043
GPIO_042	A16	I/O	General-purpose I/O	VDD33	GPIO_042
GPIO_041	A17	I/O	General-purpose I/O	VDD33	GPIO_041
GPIO_040	A18	I/O	General-purpose I/O	VDD33	GPIO_040
GPIO_039	D18	I/O	General-purpose I/O	VDD33	GPIO_039

Remark See 2.3 Pin Multiplex Function for details about GPIO multi-function pins and default pins.

(4/4)

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
GPIO_038	C18	I/O	General-purpose I/O	VDD33	GPIO_038
GPIO_037	B18	I/O	General-purpose I/O	VDD33	GPIO_037
GPIO_036	C19	I/O	General-purpose I/O	VDD33	GPIO_036
GPIO_035	B19	I/O	General-purpose I/O	VDD33	GPIO_035
GPIO_034	A19	I/O	General-purpose I/O	VDD33	GPIO_034
GPIO_033	B20	I/O	General-purpose I/O	VDD33	GPIO_033
GPIO_032	A20	I/O	General-purpose I/O	VDD33	GPIO_032
GPIO_031	J18	I/O	General-purpose I/O	VDD33	GPIO_031
GPIO_030	H18	I/O	General-purpose I/O	VDD33	GPIO_030
GPIO_029	G18	I/O	General-purpose I/O	VDD33	GPIO_029
GPIO_028	F18	I/O	General-purpose I/O	VDD33	GPIO_028
GPIO_027	F17	I/O	General-purpose I/O	VDD33	GPIO_027
GPIO_026	F16	I/O	General-purpose I/O	VDD33	GPIO_026
GPIO_025	E20	I/O	General-purpose I/O	VDD33	GPIO_025
GPIO_024	D20	I/O	General-purpose I/O	VDD33	GPIO_024
GPIO_023	D19	I/O	General-purpose I/O	VDD33	GPIO_023
GPIO_022	C20	I/O	General-purpose I/O	VDD33	GPIO_022
GPIO_021	B21	I/O	General-purpose I/O	VDD33	GPIO_021
GPIO_020	A21	I/O	General-purpose I/O	VDD33	GPIO_020
GPIO_019	C21	I/O	General-purpose I/O	VDD33	GPIO_019
GPIO_018	B22	I/O	General-purpose I/O	VDD33	GPIO_018
GPIO_017	W20	I/O	General-purpose I/O	VDD33	GPIO_017
GPIO_016	W21	I/O	General-purpose I/O	VDD33	GPIO_016
GPIO_015	Y19	I/O	General-purpose I/O	VDD33	GPIO_015
GPIO_014	Y20	I/O	General-purpose I/O	VDD33	GPIO_014
GPIO_013	Y21	I/O	General-purpose I/O	VDD33	GPIO_013
GPIO_012	AA20	I/O	General-purpose I/O	VDD33	GPIO_012
GPIO_011	AA21	I/O	General-purpose I/O	VDD33	GPIO_011
GPIO_010	AA22	I/O	General-purpose I/O	VDD33	GPIO_010
GPIO_009	V15	I/O	General-purpose I/O	VDD33	GPIO_009
GPIO_008	V16	I/O	General-purpose I/O	VDD33	GPIO_008
GPIO_007	V17	I/O	General-purpose I/O	VDD33	GPIO_007
GPIO_006	V18	I/O	General-purpose I/O	VDD33	GPIO_006
GPIO_005	U8	I/O	General-purpose I/O	VDD18/VDD33	GPIO_005
GPIO_004	V8	I/O	General-purpose I/O	VDD18/VDD33	GPIO_004
GPIO_003	U9	I/O	General-purpose I/O	VDD18/VDD33	GPIO_003
GPIO_002	V9	I/O	General-purpose I/O	VDD18/VDD33	JT_SEL
GPIO_001	U10	I/O	General-purpose I/O	VDD18/VDD33	GPIO_001
GPIO_000	V10	I/O	General-purpose I/O	VDD18/VDD33	GPIO_000

Remark See 2.3 Pin Multiplex Function for details about GPIO multi-function pins and default pins.

2.2.29 PWM interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
PWM0	AA4	Output	PWM output channel 0	VDD18/VDD33	GPIO_120
PWM1	Y5	Output	PWM output channel 1	VDD18/VDD33	GPIO_121

2.2.30 Camera interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
CAM_YUV7	V23	Input	Data bit 7	VDD33	GPIO_142
CAM_YUV6	V22	Input	Data bit 6	VDD33	GPIO_141
CAM_YUV5	U23	Input	Data bit 5	VDD33	GPIO_140
CAM_YUV4	U22	Input	Data bit 4	VDD33	GPIO_139
CAM_YUV3	U21	Input	Data bit 3	VDD33	GPIO_138
CAM_YUV2	T23	Input	Data bit 2	VDD33	GPIO_137
CAM_YUV1	T22	Input	Data bit 1	VDD33	GPIO_136
CAM_YUV0	T21	Input	Data bit 0	VDD33	GPIO_135
CAM_VS	W22	Input	Vertical sync.	VDD33	GPIO_133
CAM_HS	V21	Input	Horizontal sync.	VDD33	GPIO_134
CAM_CLKI	Y23	Input	Clock input	VDD33	GPIO_132
CAM_CLKO	W23	Output	Clock output	VDD33	GPIO_131

2.2.31 ITU-R BT.656 interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
NTSC_DATA7	U18	Output	Data bit 7	VDD33	GPIO_130
NTSC_DATA6	U20	Output	Data bit 6	VDD33	GPIO_129
NTSC_DATA5	T18	Output	Data bit 5	VDD33	GPIO_128
NTSC_DATA4	T20	Output	Data bit 4	VDD33	GPIO_127
NTSC_DATA3	R18	Output	Data bit 3	VDD33	GPIO_126
NTSC_DATA2	R20	Output	Data bit 2	VDD33	GPIO_125
NTSC_DATA1	P18	Output	Data bit 1	VDD33	GPIO_124
NTSC_DATA0	P20	Output	Data bit 0	VDD33	GPIO_123
NTSC_CLK	V20	Input	NTSC clock input	VDD33	GPIO_122

2.2.32 Trace port interface signals

Pin Name	Pin No.	IO Type	Function	IO Voltage	Default Pin
TP33_DATA15	D14	Output	Trace data bit 15	VDD33	LCD3_B7
TP33_DATA14	C14	Output	Trace data bit 14	VDD33	LCD3_B6
TP33_DATA13	B14	Output	Trace data bit 13	VDD33	LCD3_B5
TP33_DATA12	D15	Output	Trace data bit 12	VDD33	LCD3_B4
TP33_DATA11	C15	Output	Trace data bit 11	VDD33	LCD3_B3
TP33_DATA10	B15	Output	Trace data bit 10	VDD33	LCD3_B2
TP33_DATA9	A15	Output	Trace data bit 9	VDD33	GPIO_043
TP33_DATA8	A16	Output	Trace data bit 8	VDD33	GPIO_042
TP33_DATA7	D16	Output	Trace data bit 7	VDD33	LCD3_G7
TP33_DATA6	C16	Output	Trace data bit 6	VDD33	LCD3_G6
TP33_DATA5	B16	Output	Trace data bit 5	VDD33	LCD3_G5
TP33_DATA4	D17	Output	Trace data bit 4	VDD33	LCD3_G4
TP33_DATA3	C17	Output	Trace data bit 3	VDD33	LCD3_G3
TP33_DATA2	B17	Output	Trace data bit 2	VDD33	LCD3_G2
TP33_DATA1	A17	Output	Trace data bit 1	VDD33	GPIO_041
TP33_DATA0	A18	Output	Trace data bit 0	VDD33	GPIO_040
TP33_CLK	C18	Output	Trace clock output	VDD33	GPIO_038
TP33_CTRL	D18	Output	Trace control	VDD33	GPIO_039

2.2.33 Power supply pins

Pin Name	Pin No.	IO Type	Function
AVDD	A4, B4	–	PLL power supply
AGND	C4, D5	–	PLL GND
DDR_VDDIO	F6, H6, K7, N7, R6, T6	–	DDR IO power supply
DDR_GND	F3, J3, M3, N2, V3	–	DDR GND
DDR_VREFH	V4	–	DDR standard reference current generation
DDR_VREFL	F4	–	DDR standard reference current generation
USB_AVDD1	AB11	–	Power supply for regulators inside USB PHY 1
USB_AVDD2	AC6	–	Power supply for regulators inside USB PHY 2
USB_VD3311	AB14	–	Power supply for USB PHY 1 DP/DM terminals
USB_VD3312	AB8	–	Power supply for USB PHY 2 DP/DM terminals
USB_GND11	AA11	–	USB PHY 1 IO GND
USB_GND12	AC8	–	USB PHY 2 IO GND
USB_GND21	AC14	–	USB PHY 1 IO GND
USB_GND22	AC10	–	USB PHY 2 IO GND
USB_AVSS1	AB12	–	USB PHY 1 regulators GND
USB_AVSS2	AB6	–	USB PHY 2 regulators GND
USB_PVSS1	AC12	–	USB PHY 1 PLL GND
USB_PVSS2	AB7	–	USB PHY 2 PLL GND
USB_RREF1	AC11	–	USB PHY 1 standard reference current generation
USB_RREF2	AC7	–	USB PHY 2 standard reference current generation
VDD33D	A3	–	Anti-fuse power supply (3.3 V)
VDD33	F7, G15, H17, K17, R17, U14, U15	–	3.3 V IO power supply
VDD33M	G12, V7	–	1.8V/3.3 V IO power supply
VDD18	B13, F15, G8, N17, U17, V6, V11	–	1.8 V power supply
VDD11	F9, F10, G6, G13, G16, J7, J17, K18, P6, P17, T17, U6, U13, V14	–	Core power supply
GND	A1, A2, A6, A7, A10, A14, A22, A23, B1, B2, B5, B23, C7, C8, D8, D9, G7, G9, G10, G14, G17, H7, H8, M7, P7, P21, R7, R21, T7, U7, U11, U12, U16, V3, Y22, AB1, AB2, AB15, AB23, AC1, AC2, AC17, AC22, AC23	–	GND

Note One of 1.8V and 3.3V can be chosen and used. It's chosen by setting the voltage supplied to VDD33M to 1.8V or 3.3V.

2.3 Pin Multiplex Function

(1/8)

Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
A05	C32K	C32K				
A08	OSC0_XT2	OSC0_XT2				
A09	OSC0_XT1	OSC0_XT1				
A11	JT_TCK	JT_TCK				
A12	LOWPWR	LOWPWR				GPIO_154
A13	PONDET	PONDET				
A15	LCD3_B1	LCD3_B1	YUV3_D9	TP33_DATA9		GPIO_043
A16	LCD3_B0	LCD3_B0	YUV3_D8	TP33_DATA8		GPIO_042
A17	LCD3_G1	LCD3_G1	YUV3_D1	TP33_DATA1		GPIO_041
A18	LCD3_G0	LCD3_G0	YUV3_D0	TP33_DATA0		GPIO_040
A19	LCD3_R2	LCD3_R2				GPIO_034
A20	LCD3_R0	LCD3_R0				GPIO_032
A21	LCD3_CLK_I	LCD3_CLK_I	YUV3_CLK_I			GPIO_020
B03	AFS_ARSTB	AFS_ARSTB				
B06	USI0_CLK	USI0_CLK				
B07	USI0_CS0	USI0_CS0				
B08	USI0_CS1	USI0_CS1				GPIO_105
B09	USI0_CS2	USI0_CS2				GPIO_106
B10	USI0_DI	USI0_DI				
B11	USI0_DO	USI0_DO				
B12	SRESETB	SRESETB				
B14	LCD3_B5	LCD3_B5	YUV3_D13	TP33_DATA13		
B15	LCD3_B2	LCD3_B2	YUV3_D10	TP33_DATA10		
B16	LCD3_G5	LCD3_G5	YUV3_D5	TP33_DATA5		
B17	LCD3_G2	LCD3_G2	YUV3_D2	TP33_DATA2		
B18	LCD3_R5	LCD3_R5				GPIO_037
B19	LCD3_R3	LCD3_R3				GPIO_035
B20	LCD3_R1	LCD3_R1				GPIO_033
B21	LCD3_HS	LCD3_HS	YUV3_HS			GPIO_021
B22	LCD3_PXCLK	LCD3_PXCLK	YUV3_CLK_O			GPIO_018
C01	DDR_DQ7	DDR_DQ7				
C02	DDR_DQ0	DDR_DQ0				
C03	DDR_DQ2	DDR_DQ2				
C05	NECTESTIO	NECTESTIO				
C06	UTEST	UTEST				
C09	USI1_CLK	USI1_CLK				
C10	USI1_DI	USI1_DI				GPIO_107
C11	JT_TRSTB	JT_TRSTB				
C13	JT_TDI	JT_TDI				

(2/8)

Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
C14	LCD3_B6	LCD3_B6	YUV3_D14	TP33_DATA14		
C15	LCD3_B3	LCD3_B3	YUV3_D11	TP33_DATA11		
C16	LCD3_G6	LCD3_G6	YUV3_D6	TP33_DATA6		
C17	LCD3_G3	LCD3_G3	YUV3_D3	TP33_DATA3		
C18	LCD3_R6	LCD3_R6		TP33_CLK		GPIO_038
C19	LCD3_R4	LCD3_R4				GPIO_036
C20	LCD3_VS	LCD3_VS	YUV3_VS			GPIO_022
C21	GPIO_019					GPIO_019
C22	AB_AD1	AB_AD1		CF_D01		GPIO_078
C23	AB_AD0	AB_AD0		CF_D00		GPIO_077
D01	DDR_DM0	DDR_DM0				
D02	DDR_DQ4	DDR_DQ4				
D03	DDR_DQ6	DDR_DQ6				
D04	DDR_DQ1	DDR_DQ1				
D06	TE1	TE1				
D07	TE2	TE2				
D10	USI1_DO	USI1_DO				GPIO_108
D11	USI1_CS0	USI1_CS0				
D12	JT_DBG_EN	JT_DBG_EN				
D13	JT_TDO	JT_TDO				GPIO_151
D14	LCD3_B7	LCD3_B7	YUV3_D15	TP33_DATA15		
D15	LCD3_B4	LCD3_B4	YUV3_D12	TP33_DATA12		
D16	LCD3_G7	LCD3_G7	YUV3_D7	TP33_DATA7		
D17	LCD3_G4	LCD3_G4	YUV3_D4	TP33_DATA4		
D18	LCD3_R7	LCD3_R7		TP33_CTRL		GPIO_039
D19	LCD3_DE	LCD3_DE	YUV3_DE			GPIO_023
D20	GPIO_024					GPIO_024
D21	AB_CSB0	AB_CSB0				GPIO_069
D22	AB_AD3	AB_AD3		CF_D03		GPIO_080
D23	AB_AD2	AB_AD2		CF_D02		GPIO_079
E01	DDR_DQS0	DDR_DQS0				
E02	DDR_DQS0B	DDR_DQS0B				
E03	DDR_DQ3	DDR_DQ3				
E04	DDR_DQ5	DDR_DQ5				
E20	GPIO_025					GPIO_025
E21	AB_CSB1	AB_CSB1				GPIO_070
E22	AB_AD5	AB_AD5		CF_D05		GPIO_082
E23	AB_AD4	AB_AD4		CF_D04		GPIO_081
F01	DDR_DQS1E	DDR_DQS1E				
F02	DDR_DQS1EB	DDR_DQS1EB				
F04	DDR_VREFL	DDR_VREFL				

(3/8)

Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
F08	TRSTB	TRSTB				
F11	BOOTSEL2	BOOTSEL2				
F12	BOOTSEL0	BOOTSEL0				
F13	JT_TDOEN	JT_TDOEN				GPIO_152
F14	JT_TMS	JT_TMS				
F16	GPIO_026					GPIO_026
F17	GPIO_027					GPIO_027
F18	GPIO_028					GPIO_028
F20	AB_CSB2	AB_CSB2		CF_CSB0		GPIO_071
F21	AB_AD8	AB_AD8	DTV_BCLK	CF_D08	USI5_CLK	GPIO_085
F22	AB_AD7	AB_AD7		CF_D07		GPIO_084
F23	AB_AD6	AB_AD6		CF_D06		GPIO_083
G02	DDR_DQ8	DDR_DQ8				
G03	DDR_DM1E	DDR_DM1E				
G04	DDR_DQ9	DDR_DQ9				
G11	BOOTSEL1	BOOTSEL1				
G11	DDR_DQ11	DDR_DQ11				
G18	GPIO_029					GPIO_029
G20	AB_CSB3	AB_CSB3		CF_CSB1		GPIO_072
G21	AB_AD11	AB_AD11	DTV_DATA	CF_D11	USI5_CS0	GPIO_088
G22	AB_AD10	AB_AD10	DTV_VALID	CF_D10	USI5_DO	GPIO_087
G23	AB_AD9	AB_AD9	DTV_PSYNC	CF_D09	USI5_DI	GPIO_086
H01	DDR_DQ12	DDR_DQ12				
H02	DDR_DQ15	DDR_DQ15				
H03	DDR_DQ13	DDR_DQ13				
H04	DDR_DQ10	DDR_DQ10				
H18	GPIO_030					GPIO_030
H20	AB_WRB	AB_WRB		CF_IOWRB		GPIO_074
H21	AB_AD14	AB_AD14	SDI2_DATA2	CF_D14		GPIO_091
H22	AB_AD13	AB_AD13	SDI2_DATA1	CF_D13	USI5_CS2	GPIO_090
H23	AB_AD12	AB_AD12	SDI2_DATA0	CF_D12	USI5_CS1	GPIO_089
J01	DDR_A0	DDR_A0				
J02	DDR_A2	DDR_A2				
J04	DDR_DQ14	DDR_DQ14				
J06	DDR_CS1B	DDR_CS1B				
J18	GPIO_031					GPIO_031
J20	AB_RDB	AB_RDB		CF_IORDB		GPIO_073
J21	AB_A17	AB_A17		CF_A00		GPIO_093
J22	AB_AD15	AB_AD15	SDI2_DATA3	CF_D15		GPIO_092
J23	AB_CLK	AB_CLK				GPIO_068
K01	DDR_BA2	DDR_BA2				

(4/8)

Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
K02	DDR_BA0	DDR_BA0				
K03	DDR_A3	DDR_A3				
K04	DDR_A10	DDR_A10				
K06	DDR_CASB	DDR_CASB				
K20	AB_ADV	AB_ADV		CF_RESET		GPIO_076
K21	AB_A18	AB_A18		CF_A01		GPIO_094
K22	HSI_CAWAKE Note1	HSI_CAWAKE Note1	USI5_CLK			GPIO_143
K23	HSI_CADATA Note1	HSI_CADATA Note1	USI5_DO			GPIO_144
L01	DDR_CKE0	DDR_CKE0				
L02	DDR_A14	DDR_A14				
L03	DDR_A1	DDR_A1				
L04	DDR_BA1	DDR_BA1				
L06	DDR_RASB	DDR_RASB				
L07	DDR_CS0B	DDR_CS0B				
L17	AB_A27	AB_A27		AB_BEN0		GPIO_103
L18	AB_A24	AB_A24		CF_INPACKB		GPIO_100
L20	AB_WAIT	AB_WAIT		CF_IORDY		GPIO_075
L21	AB_A19	AB_A19		CF_A02		GPIO_095
L22	HSI_ACREADY Note1	HSI_ACREADY Note1	USI5_CS1			GPIO_146
L23	HSI_CAFLAG Note1	HSI_CAFLAG Note1	USI5_CS0			GPIO_145
M01	DDR_CK	DDR_CK				
M02	DDR_CKB	DDR_CKB				
M04	DDR_WEB	DDR_WEB				
M06	DDR_ODT Note2	DDR_ODT Note2				
M17	AB_A28	AB_A28		AB_BEN1		GPIO_104
M18	AB_A25	AB_A25		CF_CDB1		GPIO_101
M20	AB_A22	AB_A22	SDI2_CKI			GPIO_098
M21	AB_A20	AB_A20				GPIO_096
M22	HSI_CAREADY Note1	HSI_CAREADY Note1	USI5_DI			GPIO_150
M23	HSI_ACFLAG Note1	HSI_ACFLAG Note1	USI5_CS4			GPIO_149
N01	DDR_CKE1	DDR_CKE1				
N03	DDR_A11	DDR_A11				
N04	DDR_A13	DDR_A13				
N06	DDR_CKERSTB	DDR_CKERSTB				
N18	AB_A26	AB_A26		CF_CDB2		GPIO_102
N20	AB_A23	AB_A23	SDI2_CMD			GPIO_099

Note1 : The HSI function is not available.

Note2 : The on die termination function for DDR-ODT is not available.

(5/8)

Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
N21	AB_A21	AB_A21	SDI2_CKO	CF_INTRQ		GPIO_097
N22	HSI_ACWAKE Note1	HSI_ACWAKE Note1	USI5_CS2			GPIO_147
N23	HSI_ACDATA Note1	HSI_ACDATA Note1	USI5_CS3			GPIO_148
P01	DDR_A12	DDR_A12				
P02	DDR_A7	DDR_A7				
P03	DDR_A8	DDR_A8				
P04	DDR_A6	DDR_A6				
P18	NTSC_DATA1	NTSC_DATA1				GPIO_124
P20	NTSC_DATA0	NTSC_DATA0				GPIO_123
R01	DDR_A9	DDR_A9				
R02	DDR_A5	DDR_A5				
R03	DDR_A4	DDR_A4				
R04	DDR_DQ20	DDR_DQ20				
R18	NTSC_DATA3	NTSC_DATA3				GPIO_126
R20	NTSC_DATA2	NTSC_DATA2				GPIO_125
T01	DDR_DQ16	DDR_DQ16				
T02	DDR_DQ17	DDR_DQ17				
T03	DDR_DQ22	DDR_DQ22				
T04	DDR_DQ19	DDR_DQ19				
T18	NTSC_DATA5	NTSC_DATA5				GPIO_128
T20	NTSC_DATA4	NTSC_DATA4				GPIO_127
T21	CAM_YUV0	CAM_YUV0				GPIO_135
T22	CAM_YUV1	CAM_YUV1				GPIO_136
T23	CAM_YUV2	CAM_YUV2				GPIO_137
U01	DDR_DQ21	DDR_DQ21				
U02	DDR_DQ18	DDR_DQ18				
U03	DDR_DQ23	DDR_DQ23				
U04	DDR_DM2E	DDR_DM2E				
U08	GPIO_005	EXT_CLKI				GPIO_005
U09	GPIO_003	ERR_RST_REQB				GPIO_003
U10	GPIO_001					GPIO_001
U18	NTSC_DATA7	NTSC_DATA7				GPIO_130
U20	NTSC_DATA6	NTSC_DATA6				GPIO_129
U21	CAM_YUV3	CAM_YUV3				GPIO_138
U22	CAM_YUV4	CAM_YUV4				GPIO_139
U23	CAM_YUV5	CAM_YUV5				GPIO_140
V01	DDR_DQS2E	DDR_DQS2E				
V02	DDR_DQS2EB	DDR_DQS2EB				
V04	DDR_VREFH	DDR_VREFH				
V08	GPIO_004	REF_CLKO				GPIO_004

Note1 : The HSI function is un-installation.

(6/8)

Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
V09	GPIO_002	JT_SEL				GPIO_002
V10	GPIO_000					GPIO_000
V12	UART0_TX	UART0_TX				
V13	UART0_RX	UART0_RX				
V15	GPIO_009					GPIO_009
V16	GPIO_008					GPIO_008
V17	GPIO_007					GPIO_007
V18	GPIO_006					GPIO_006
V20	NTSC_CLK	NTSC_CLK				GPIO_122
V21	CAM_HS	CAM_HS				GPIO_134
V22	CAM_YUV6	CAM_YUV6				GPIO_141
V23	CAM_YUV7	CAM_YUV7				GPIO_142
W01	DDR_DQS3	DDR_DQS3				
W02	DDR_DQS3B	DDR_DQS3B				
W03	DDR_DQ31	DDR_DQ31				
W04	DDR_DQ30	DDR_DQ30				
W20	GPIO_017					GPIO_017
W21	GPIO_016					GPIO_016
W22	CAM_VS	CAM_VS				GPIO_133
W23	CAM_CLKO	CAM_CLKO				GPIO_131
Y01	DDR_DM3	DDR_DM3				
Y02	DDR_DQ27	DDR_DQ27				
Y03	DDR_DQ25	DDR_DQ25				
Y04	DDR_DQ29	DDR_DQ29				
Y05	PWM1	PWM1	USI4_DO			GPIO_121
Y06	USI2_CS2	USI2_CS2	USI4_CS1			GPIO_114
Y07	USI2_CS0	USI2_CS0	DTV_DATA			GPIO_112
Y08	IIC1_SDA	IIC1_SDA	UART3_TX			GPIO_047
Y09	IIC1_SCL	IIC1_SCL	UART3_RX			GPIO_046
Y10	UART1_TX	UART1_TX				GPIO_156
Y11	UART1_RX	UART1_RX				GPIO_155
Y12	SDI0_CMD	SDI0_CMD				GPIO_052
Y13	SDI0_DATA1	SDI0_DATA1				GPIO_054
Y14	SDI0_DATA3	SDI0_DATA3				GPIO_056
Y15	SDI0_DATA5	SDI0_DATA5				GPIO_058
Y16	SDI0_DATA7	SDI0_DATA7				GPIO_060
Y17	SD_DATA2	SD_DATA2				
Y18	SD_DATA0	SD_DATA0				
Y19	GPIO_015					GPIO_015
Y20	GPIO_014					GPIO_014
Y21	GPIO_013					GPIO_013

(7/8)

Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
Y23	CAM_CLKI	CAM_CLKI				GPIO_132
AA01	DDR_DQ24	DDR_DQ24				
AA02	DDR_DQ28	DDR_DQ28				
AA03	DDR_DQ26	DDR_DQ26				
AA04	PWM0	PWM0	USI4_DI			GPIO_120
AA05	USI2_DO	USI2_DO	DTV_VALID			GPIO_111
AA06	USI2_DI	USI2_DI	DTV_PSYNC			GPIO_110
AA07	USI2_CS1	USI2_CS1	USI4_CS0			GPIO_113
AA08	IIC0_SDA	IIC0_SDA				GPIO_045
AA09	IIC0_SCL	IIC0_SCL				GPIO_044
AA10	UART1_CTSB	UART1_CTSB	UART2_RX			GPIO_157
AA12	USB_VBUS	USB_VBUS				GPIO_153
AA13	SDI0_DATA0	SDI0_DATA0				GPIO_053
AA14	SDI0_DATA2	SDI0_DATA2				GPIO_055
AA15	SDI0_DATA4	SDI0_DATA4				GPIO_057
AA16	SDI0_DATA6	SDI0_DATA6				GPIO_059
AA17	SD_DATA3	SD_DATA3				
AA18	SD_DATA1	SD_DATA1				
AA19	SDI1_DATA3	SDI1_DATA3				GPIO_067
AA20	GPIO_012					GPIO_012
AA21	GPIO_011					GPIO_011
AA22	GPIO_010					GPIO_010
AA23	SDI1_CKI	SDI1_CKI				GPIO_062
AB03	GPIO_119		USI4_CLK			GPIO_119
AB04	USI3_CS0	USI3_CS0	USI0_CS6			GPIO_118
AB05	USI2_CLK	USI2_CLK	DTV_BCLK			GPIO_109
AB09	USB_DP2	USB_DP2				
AB10	UART1_RTSB	UART1_RTSB	UART2_TX			GPIO_158
AB13	USB_DP1	USB_DP1				
AB16	GPIO_049					GPIO_049
AB17	SD_CMD	SD_CMD				
AB18	SDI0_CKO	SDI0_CKO				GPIO_050
AB19	SDI1_DATA2	SDI1_DATA2				GPIO_066
AB20	SDI1_DATA1	SDI1_DATA1				GPIO_065
AB21	SDI1_DATA0	SDI1_DATA0				GPIO_064
AB22	SDI1_CKO	SDI1_CKO				GPIO_061
AC03	USI3_DO	USI3_DO	USI0_CS5			GPIO_117
AC04	USI3_DI	USI3_DI	USI0_CS4			GPIO_116
AC05	USI3_CLK	USI3_CLK	USI0_CS3			GPIO_115
AC09	USB_DM2	USB_DM2				
AC13	USB_DM1	USB_DM1				

(8/8)

Pin No.	Default	Mode0	Mode1	Mode2	Mode3	GPIO
AC15	OSC1_XT1	OSC1_XT1				
AC16	OSC1_XT2	OSC1_XT2				
AC18	SDI0_CKI	SDI0_CKI				GPIO_051
AC19	SD_CKI	SD_CKI				GPIO_048
AC20	SD_CKO	SD_CKO				
AC21	SDI1_CMD	SDI1_CMD				GPIO_063

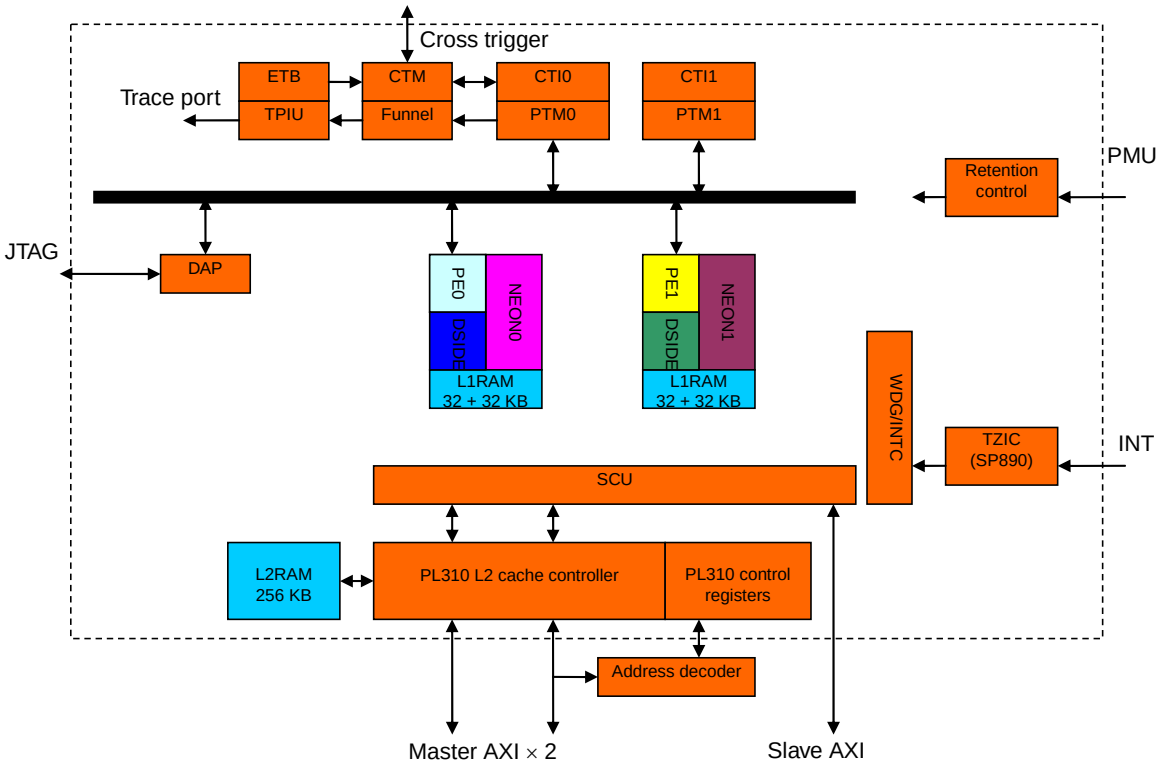
3. Core Functions

3.1 CPU

The CPU has the following features:

- 2 × ARM Cortex A9 processors
  Operates at up to 533 MHz
  L1 cache (I-Cache: 32 KB, D-Cache: 32 KB)
  2 × Neon, 2 × VFP
- 256KB L2 cache
  ARM PL310
- ARM security expansion

Figure 3-1. Block Diagram of ARM Cortex-A9 CPU



Power domain	PD_TOP	PD_HM	PD_DS0	PD_PE0	PD_NE0	PD_DS1	PD_PE1	PD_NE1
Modules	L1RAM L2RAM Retention F/F	SCU/PL310 CoreSight IP	DSIDE0	PE0	NEON0	DSIDE1	PE1	NEON1

3.2 System Management Unit

3.2.1 Clock distribution

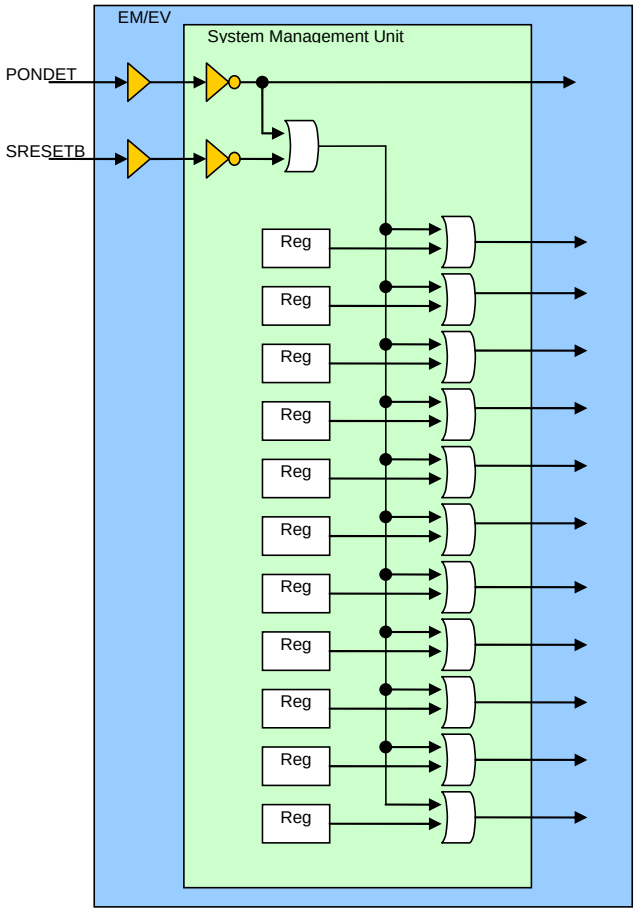
The SMU clock distribution unit includes the following features:

- OSC × 2
- PLL × 4 and clock divider
- Clock gating at clock tree root point
- Automatic clock frequency control

3.2.2 Reset distribution

The SMU in EM/EV includes a reset distribution unit.

Figure 3-2. Reset Distribution



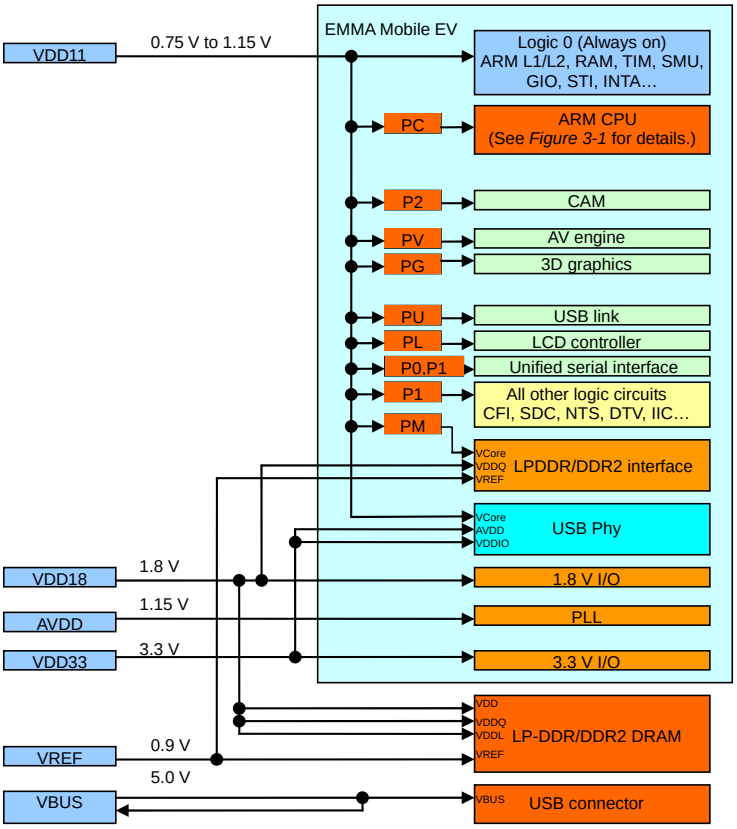
3.2.3 Power domains

EM/EV has 12 power domains for the core logic.

- The contents of all CPU registers are kept in the power-off state.
- The contents of the L1 cache memory are always retained.

EM/EV includes on-chip power switches.
All on-chip power switches able to be turned on and off by the CPU and the PMU.

Figure 3-3. EM/EV Power Domains



3.3 System Buses

The EM/EV bus system includes the following buses:

- Main system bus (AMBA AXI)
- Legacy master bus (AMBA AHB)
- CPU command bus (AMBA APB)
- Display bus (AMBA AXI)

Bus bridges

- AXI bridge for AHB legacy master bus
- AXI to AXI bridge for display bus

Main system bus

- 64-bit 6-layer AMBA AXI bus
- SDRAM × 1 layer
- External memory × 1 layer
- Internal SRAM × 1 layer
- APB bridge × 1 layer

Legacy master bus

- 32-bit AMBA AHB bus

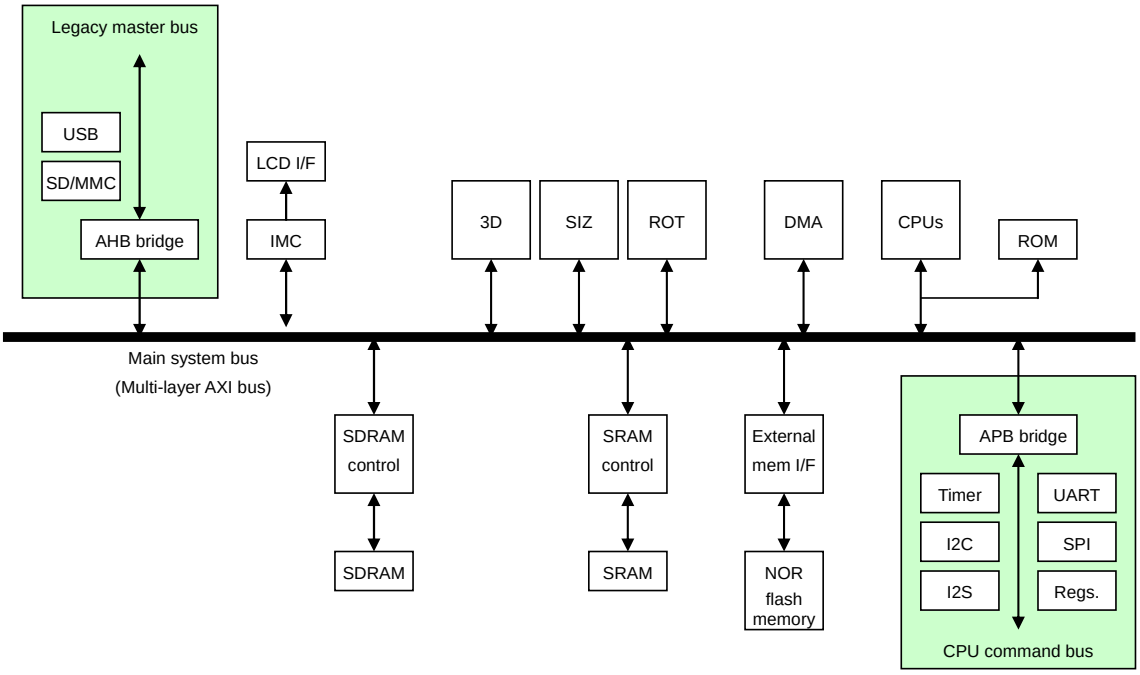
CPU command bus

- 32-bit AMBA APB bus
- Includes security expansion

Display bus

- 64-bit AMBA AXI bus

Figure 3-4. EM/EV Bus Overview



3.4 Embedded Memory

3.4.1 SRAM

EM/EV includes 128 KB of embedded SRAM.

3.4.2 ROM

EM/EV includes 64 KB of embedded ROM.

3.5 Testing and Debugging

3.5.1 Debugging features

- ARM CoreSight debugging system
- Debugging in low power systems

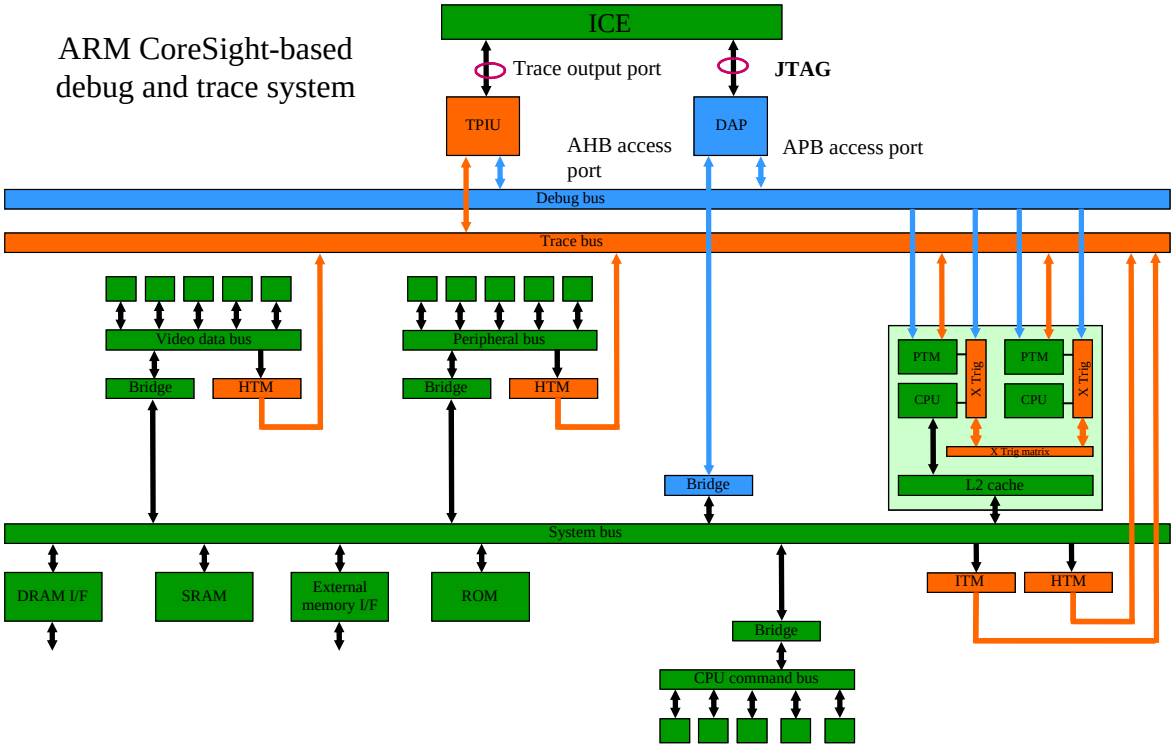
3.5.2 Debug interface

- JTAG interface

3.5.3 Trace interface

- ARM CoreSight trace output port

Figure 3-5. Block Diagram of Testing and Debugging System

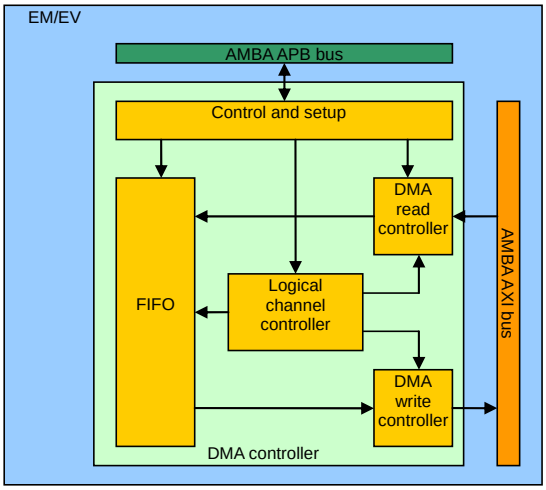


3.6 DMA Controller

The DMA controller has the following features:

- 8 channels, which operate in parallel.
- One AXI read port and one AXI write port for memory access.
- Supports incremental transfer and decremental transfer.
- Includes an AXI bus controller with a byte-aligning function.

Figure 3-6. DMA Controller Block Diagram



3.7 Timers

The timers have the following features:

Configuration: 15 × 32 bit counters

Operating frequency: 32.768 kHz or divided PLL output

Every timer has individual clock selector.

Every timer has a PLL division ratio selector.

Timers operate as interval timers or watchdog timers.

When the mode register is set to timer mode, all timers operate as interval timers.

Every timer counts up to TIMOUT_COUNT.

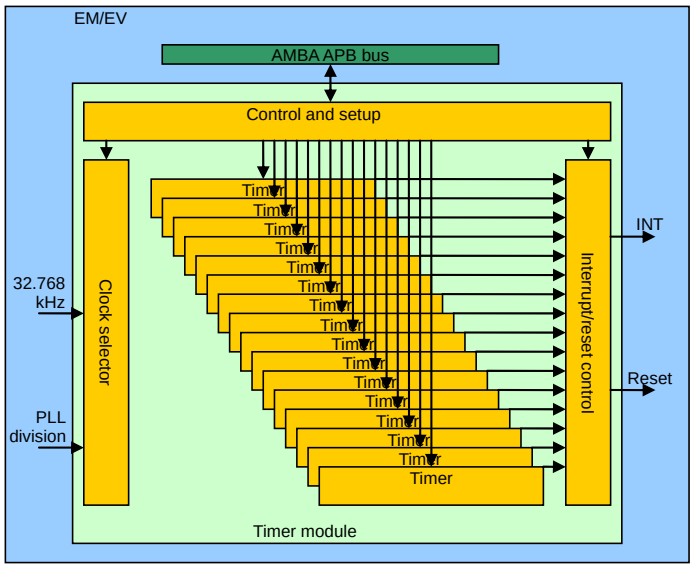
When the timer count reaches TIMOUT_COUNT, the timer issues an interrupt signal, resets the count, and restarts counting up.

When the mode register is set to watchdog timer mode for TW0 and TW1, these work as watchdog timers.

Every timer counts up to TIMOUT_COUNT.

When the timer count reaches TIMOUT_COUNT, the timer issues the RESET signal to the selected CPU, resets the count, and stops counting.

Figure 3-7. Timer Block Diagram

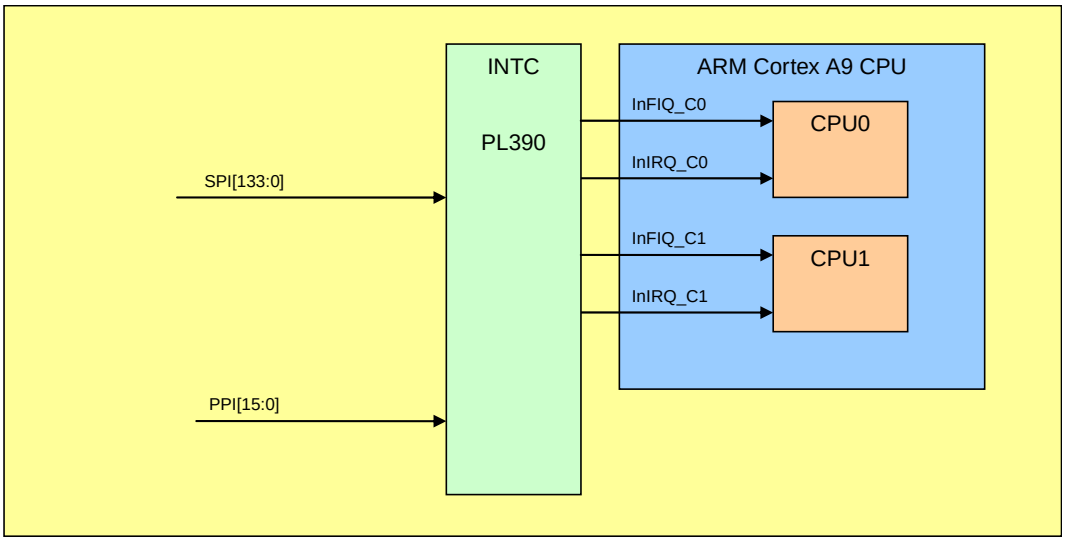


3.8 Interrupt Controller

The interrupt controller is an ARM INTC (PL390) with the following features:

- Supports 134-bit shared peripheral interrupts (SPI).
- Supports 16-bit software-generated (SGI) interrupts.
- Supports 16-bit private peripheral interrupts (PPI).

Figure 3-8. Interrupt Controller



3.9 AVE

3.9.1 Video decoder

The video decoder is a high performance multi-standard video decoder that can perform H.264, VC-1, MPEG-4, MPEG-1/2, and H.264 decoding. The video decoder supports up to HD 1920 × 1080 in case of DDR2-533 with 32bit bus width and can decode multiple video clips that use multiple standards simultaneously.

- Video format
  The supported standards and the maximum resolutions are shown in Table 3-1.

Table 3-1. Supported Standards (With Profiles and Levels) and Maximum Resolution

Standard	Profile	Level	Resolution
H.264	BP/MP/HP	4.1	1920 × 1080
H.263	Profile 3		1920 × 1080
VC-1	SP/MP/AP	3	1920 × 1080
MPEG-4	ASP		1920 × 1080 Note
MPEG-2	Main	High	1920 × 1080

Note The IP in EM/EV can decode 1920 × 1080. However, the maximum resolution is limited to 720 × 576 by the MPEG-4 Visual SP/ASP profile.

- H.264
  Fully compatible with the ITU-T Recommendation H.264 specification in BP/MP and HP.
  Supports CABAC/CAVLC.
  Variable block size (16 × 16, 16 × 8, 8 × 16, 8 × 8, 8 × 4, 4 × 8 and 4 × 4)
  Error detection, concealment and error resilience tools
- VC-1
  Supports all VC-1 profile features as described in the SMPTE document Proposed SMPTE Standard for Television: VC-1 Compressed Video Bit Stream Format and Decoding Process.
  Supports Simple, Main, and Advanced profiles.
  Multi-resolution (dynamic resolution) data is not processed inside the video decoder.
- MPEG-4, H.263
  Supports Simple and Advanced Simple profiles, except GMC.
  Supports H.263 Baseline profile.
- MPEG-2
  Fully compatible with ISO/IEC 13182-2 MPEG2 specification in Main profile.
  Supports I, P and B frames.
  Supports field coded pictures (interlaced) and frame coded pictures.

- Color format of decoded images
  YUV420 (planar, semi-planar)

- Performance
  Supports up to full HD (1920 × 1080) @ 30 fps.

3.9.2 Audio decoder

The audio decoder can decode data in the following formats: MPEG-4 HE-AAC, and enhanced aacPlus.

3.10 Rotator

The rotator (ROT) is a macro that is used to rotate an image. The ROT macro includes an AXI slave interface and can be written directly from a CAM, CPU, or AVE, enabling the following features:

- There is no need for an intermediate buffer (reducing the amount of DRAM required).
- DRAM R/W is reduced, improving the speed and lowering the power consumption.
- The required DRAM bandwidth is reduced (giving a larger bandwidth margin to other masters).

Note, however, that when executing 0 or 180° rotation, the efficiency is almost the same as when using a normal DRAM write, and when executing 90 or 270° rotation, the number of byte-writes will increase, lowering the DRAM bandwidth efficiency. Also, compared with the RGB565 or YUV422 interleave format, executing 90 or 270° rotation in the YUV42* semi planar or planar format will result in double the number of byte-writes. We therefore recommend using the SIZ macro when executing 90 or 270° rotation in the YUV42* semi planar or planar format.

ROT has two modes: raster order mode and random mode. Raster order mode is specified by setting DSTADDRV[3:0] to FH.
In raster order mode, there are no input address restrictions, but the pixels must be input in raster order.
In random mode, the pixels can be input in any order, but the input line addresses must be aligned with 2^n.

3.10.1 Raster order mode

- Rotation: 0°, 90°, 180°, 270°
- Format: ARGB8888, RGB888/YUV444, RGB565
- Byte lane swapping on output side

3.10.2 Random mode

- Rotation: 0°, 90°, 180°, 270°
- X/Y-mirror
- Format: RGB565, YUV422 (interleave/semi-planar/planar), YUV420 (semi-planar/planar)
- Byte lane swapping on output side

3.10.3 Input (source)/output (destination) pixel boundary

RGB565	2 × 1 pixels
YUV422IL	2 × 2 pixels
YUV42*SP	4 × 2 pixels
YUV42*PL	8 × 2 pixels

3.11 Resizer

The resizer (SIZ) is a macro used to resize or rotate an image. The SIZ macro includes an AXI slave interface and can be written directly from a CAM, CPU, or AVE, enabling the following features:

- There is no need for an intermediate buffer (reducing the amount of DRAM required).
- DRAM R/W is reduced, improving the speed and lowering the power consumption.
- The required DRAM bandwidth is reduced (giving a larger bandwidth margin to other masters).

Note, however, that when using the SIZ macro, it is assumed that the pixels are input in raster order.
The SIZ macro has a resize output channel and a rotate output channel, enabling resize and rotate results to be output simultaneously for each pixel input. Moreover, because SIZ enables 4-line buffering, the memory can be accessed more efficiently than when using other macros such as ROT. Note, however, that when using the rotate channel, the data must be input in YUV422IL format with a 4 × 4-pixel boundary and aligned with address 8B, and output in YUV422IL, 422SP, or 420SP format, aligned with address 8B.

3.11.1 Resize channel

- Resizing (×256 to 1/64) with 2 × 2 or 4 × 4 filtering
- Configurable filter
- Format: RGB888/565, YUV422IL/SP/PL, YUV420SP/PL
- Format Conversion: RGB* to RGB* or YUV* to YUV*
- Cropping: By setting Dst[HV]size to a value that is smaller than the resized image, the right and lower edges can be cropped, and by setting Dst[HV]crop to a value other than 0, the left and top edges can be cropped.
- Line skip: By setting DstHskip to a value other than 0, the output area can be specified as an arbitrary rectangle and can be made to overlay an existing image.
- Color conversion: Half of the SRAM (12 KB) in the SIZ macro can be used as a table, and the output data and table values can be switched.

3.11.2 Rotate channel

- Rotation and/or X/Y-mirror
- Format (input): YUV422IL
- Format (output): YUV422IL/422SP/420SP

3.11.3 Output (destination) pixel boundary

RGB*	1 × 1 pixel
YUV*	2 × 1 pixels

3.11.4 Input (source) pixel boundary

RGB888	4 × 1 pixels
RGB565	2 × 1 pixels
YUV422IL	2 × 1 pixels
YUV42*SP	4 × 1 pixels

YUV42*PL 8 × 1 pixels

(Smaller boundaries that those shown above are possible if dummy pixels are used to ensure that 4 bytes are written.)

3.12 Image Composer

The image composer (IMC) generates a synthesized image from source images composed of several layers. It can also overlap a transparent image onto the image in another layer by using alpha-blending or key color masking. The IMC outputs the synthesized image to an LCD interface or memory.

3.12.1 Image size

- Input

  Progressive
  - Minimum size: 0 × 0 pixels
  - Maximum size: 4,094 × 4,094 pixels
  - Minimum block size: 1 × 1 pixel

  Interlaced
  - Minimum size: 0 × 0 pixels
  - Maximum size: 4,094 × 4,094 pixels
  - Minimum block size: 2 × 1 pixels

Remark The image size for interlaced scanning shows the frame size. The field size is half the frame size in the vertical direction.

- Output

  Progressive
  - Minimum size: 1 × 1 pixel
  - Maximum size: 4,094 × 4,094 pixels
  - Minimum block size:
    - RGB888, RGB565: 1 × 1 pixel
    - RGB666: 1 × 4 pixels

  Interlaced
  - Minimum size: 2 × 1 pixels
  - Maximum size: 4,094 × 4,094 pixels
  - Minimum block size:
    - RGB888, RGB565: 2 × 1 pixels
    - RGB666: 2 × 4 pixels

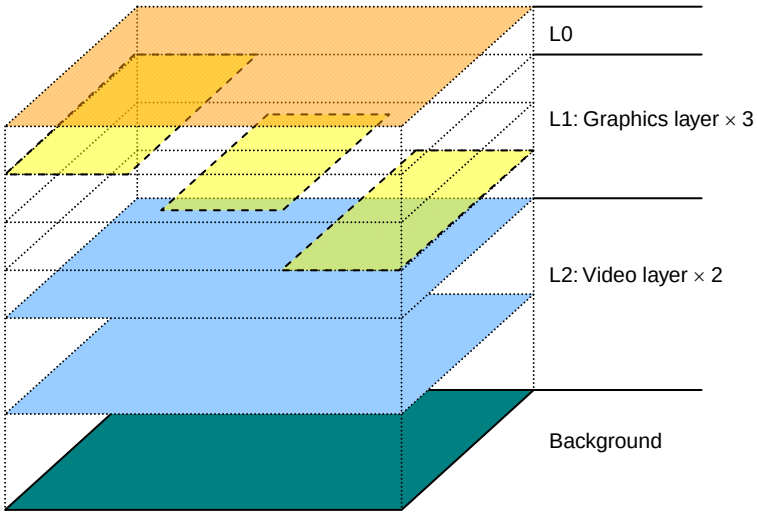
3.12.2 Color format

- Input:
  L0, L1: RGB888, RGB666, RGB565, ARGB8888, ARGB4444, ARGB1555
  L2: RGB888, RGB666, RGB565, ARGB8888, ARGB4444, ARGB1555, YUV422 (interleave, semi-planer, planer), YUV420 (semi-planer, planer), YUV444
  Background: RGB888, RGB666, RGB565
- Output:
  LCD direct: RGB565, RGB666, RGB888
  Write-back: RGB565, RGB666, RGB888

3.12.3 Layers

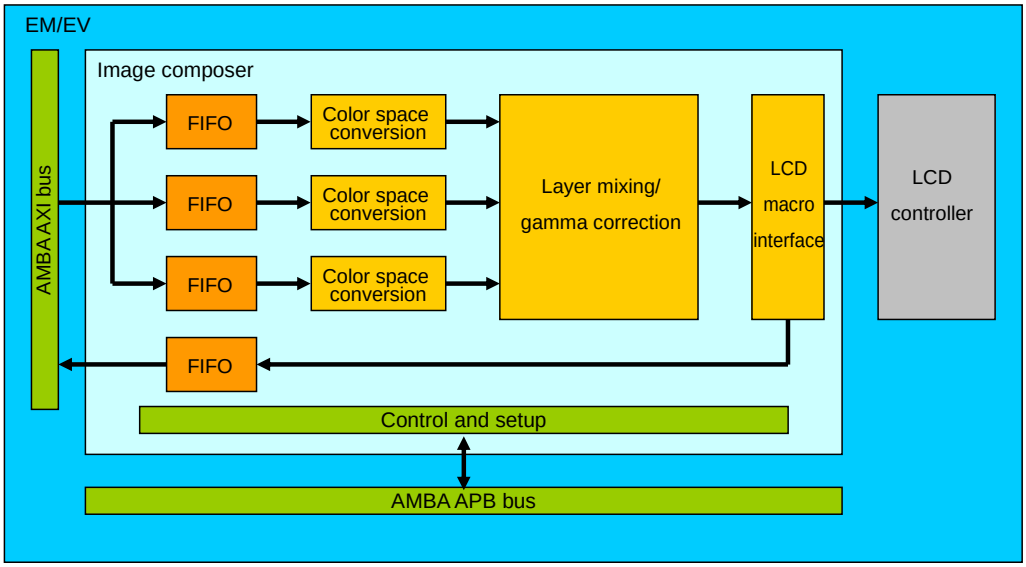
1. L0:
   L0 can be transparently overlapped onto the graphics layer, video layer and background by using alpha-blending or key color masking.
2. L1: Graphics (× 3)
   The graphics layer can be transparently overlapped onto the video layer and background by using alpha-blending or key color masking.
3. The graphics layer has 3 image fields.
4. L2: Video (× 2)
   The video layer can be overlapped onto the background.
5. The video layer has 2 image fields.
6. Background.

Figure 3-10. Image Composer Layers



3.12.4 Block diagram

Figure 3-11. Block Diagram of Image Composer



3.12.5 Gamma correction

- Table lookup (256 words × 8 bits × 3 channels (R, G, B))

3.12.6 Write back

- Supports writing back a composed image into the frame cache area in the system memory.

3.12.7 Color format transfer

- YUV to RGB

3.12.8 Interlace and de-interlace

- Supports interlacing and de-interlacing.

3.12.9 Image wraparound

- Part of an image that is outside the boundary of the visible frame appears from another boundary that is symmetrical with a point based on the center of the visible frame.

3.12.10 Direct path from resizer

- The image composer has a direct path from the resizer (layer).
  (Uses the AXI slave interface.)

3.12.11 Output interface

- LCD interface

3.12.12 Endian

- RGB format: Little endian only
- YUV format:
  - Y (big endian): Default

[31:24]	[23:16]	[15:8]	[7:0]
Y2	Y3	Y0	Y1
Y6	Y7	Y4	Y5

  - UV (big endian): Default

[31:24]	[23:16]	[15:8]	[7:0]
U1	V1	U0	V0
U3	V3	U2	V2

  - Y (little endian)

[31:24]	[23:16]	[15:8]	[7:0]
Y3	Y2	Y1	Y0
Y7	Y6	Y5	Y4

  - UV (little endian)

[31:24]	[23:16]	[15:8]	[7:0]
V1	U1	V0	U0
V3	U3	V2	U2

3.13 3D Graphics Accelerator

3.13.1 Performance

- 14.7 M polys per second (3D performance)
- 500 M pixels per second (2D performance)
- 1.6 GFLOPS (shader performance)

3.13.2 API

- OpenGL-ES 1.x
- OpenGL-ES 2.0

3.13.3 Output color format

- RGB565, ARGB1555, ARGB4444, ARGB8888

3.14 SDRAM Interface

- Supports LPDDR SDRAM and DDR2 SDRAM
- Maximum bandwidth is:
  LPDDR: 1600 MBps (DDR400 × 32 bits)
  DDR2: 2132 MBps (DDR533 × 32 bits)
- Maximum memory size is 4 Gb × 4 = 2048 MB

3.15 External Memory Interface

3.15.1 Features

- 16-bit asynchronous memory interface
- Supports A/D mux mode.
- NOR flash memory control
- 4 chip select signals (shared with GPIO)

3.15.2 NOR flash memory support

Supports A/D mux.

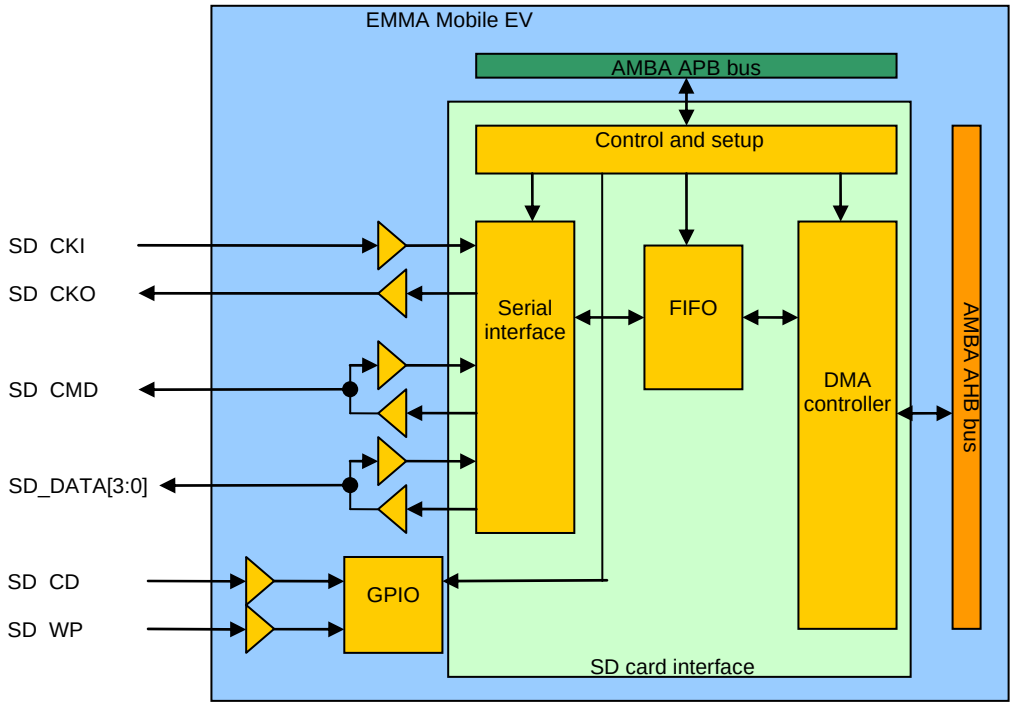
3.15.3 Asynchronous memory support

Supports asynchronous SRAM read and write modes.
The work speed is based on the internal bus clock.
The access cycle can be controlled by setting the configuration register.

3.16 SD Card Interface

The SD card interface supports SD Memory Card Specification Part 1 Physical Layer Specification version 2.00, SD Host Controller Standard Specification version 2.00 including SDHC support.

Figure 3-12. SD Card Interface Block Diagram

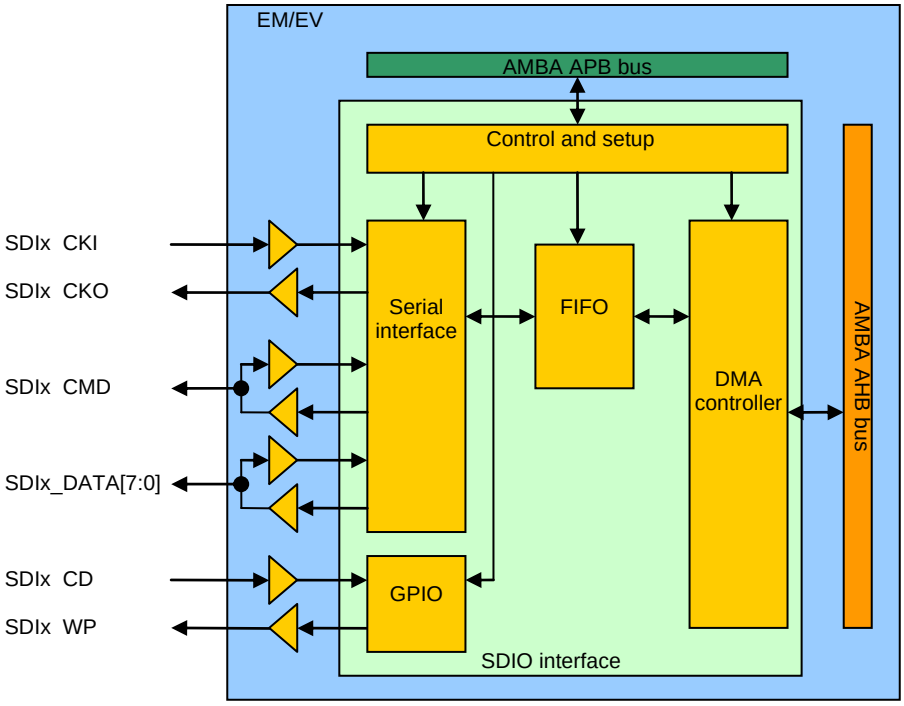


3.17 SDIO Interface

The SDIO interface has the following features:

- 3 ports
- Supports SD memory, SDIO card, SDIO multi-function card, and combo card.
- Supports 1-bit SD and 4 bit SD modes.
- Supports DMA.
- Supports MMC 1-bit, 4-bit, and 8-bit (SDIO0 only) modes.
- Supports MMC high-speed and high-capacity modes.
- Supports CE-ATA Digital Protocol revision 1.1.
- Supports eMMC spec 4.2.
- Supports eSD spec 2.10.

Figure 3-13. SDIO Interface Block Diagram

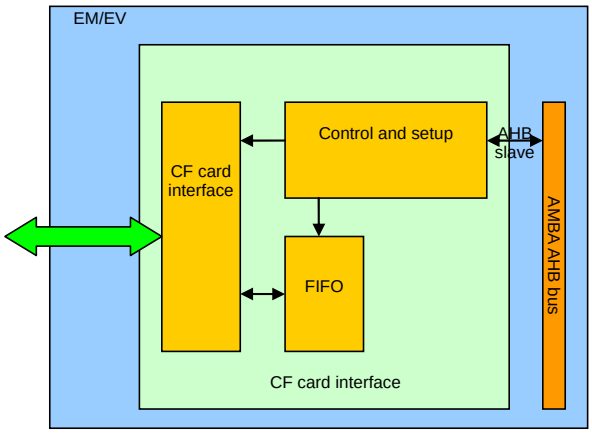


3.18 CF Interface

The CF interface has the following features:

- Supports CF + and CF Card Specification Revision 3.0.
- Supports True IDE PIO mode.
  True IDE PIO mode supports mode 0 to mode 6.
- The access timing to CF can be varied by specifying a register setting.

Figure 3-14. CF Card Interface Block Diagram



3.19 LCD Interface

The LCD macro is used to output sync signals and video signals to an LCD panel externally connected to EM/EV. The LCD macro is also capable of outputting YUV data for an HDMI driver interface.

The major features of the LCD macro are described below.

- Output size
  - Horizontal: 4,090 pixels, max. (with a sync cycle of up to 8,190 CLK)
  - Vertical: 4,094 lines, max. (with a sync cycle of up to 8,190 HSYNC)
- Output format
  - RGB: RGB565, RGB666, RGB888 (up to 16,770,000 colors)
- LCD interface
  - Pixel clock output (PXCLK)
  - Horizontal sync signal (HSYNC)
  - Vertical sync signal (VSYNC)
  - Data bus enable (DATAENABLE)
  - Data bus (RDATA[7:0], GDATA[7:0], BDATA[7:0])
- YUV interface
  - YUV data clock output (YUV_CLK)
  - Horizontal sync signal (YUV_HS)
  - Vertical sync signal (YUV_VS)
  - Data bus enable (YUV_DE)
  - Data bus (YUV_DATA[15:0])
- Data format
  - LCD output can be selected from RGB565, RGB666, and RGB888.
  - RGB565, RGB666, and RGB888 can be selected even when inputting data from the memory. (However, only RGB888 input can be used when RGB888 or YUV is selected as the output format.) By operating the LCD macro in coordination with the separate IMC macro, the YUV422 and YUV420 formats (YUV interleave, Y/UV 2 planar, Y/U/V 3 planar) can also be used.
- Hardware cursor
  - Features 64 × 64 pixels and 256 colors (RGB565 pallet, including translucent colors)
- Data buffer
  - The macro has an built-in 32-bit × 1024-word data buffer (used as an FIFO buffer).
- The LCD macro can be connected by a direct path to the MEMC macro, enabling the low-power standby mode to be used.
- The LCD panel interface signal can be programmed by specifying a register setting.
- Can display black backgrounds and enables fixed-color display in which the colors can be set freely by specifying a register setting.
- Enables simplified QoS linked with the internal FIFO status.
- Simple double-resize feature (can only be used when using a direct path)
- Can handle unscheduled system clock stoppages (long stoppages trigger an underrun).

Clock Signal Name	Frequency Limitation
LCD_CLK (for main operation) LCD_CCLK (for bus access)	Max 266 MHz
LCD_PCLK (for APB registers)	Max 133 MHz (A clock that is the same as LCD_CLK or a synchronous clock divided by 2)
LCD_LCLK (display clock)	Max 100 MHz

Caution The LCD macro can handle resolutions of up to 4096 × 4096 pixels. However, when displaying an image at the maximum resolution, the amount of data transferred from the frame buffer will increase significantly, raising the system bus occupancy rate. Be sure to take into consideration the bus transfer bandwidth that can be used by macros other the LCD macro when determining the size of the LCD panel to use.

3.19.1 LCD interface image data

The LCD macro supports LCD panels that display images in 16 bpp mode (65,536 colors), 18 bpp mode (260,000 colors), and 24 bpp mode (16,770,000 colors). The display format can be switched between RGB666, RGB565, and RGB888 by specifying the output format (OFORMAT).

3.19.2 YUV output interface image data

The LCD macro supports the YUV422 (interleave) format.
RGB888-format data is converted into YUV data in 2-pixel units and then output.
(Data cannot be input in RGB565 or RGB666 format).
Data is output in units of 16 bits per clock cycle. The order in which the Y0, Y1, U, and V data is output can be changed by specifying a register setting.

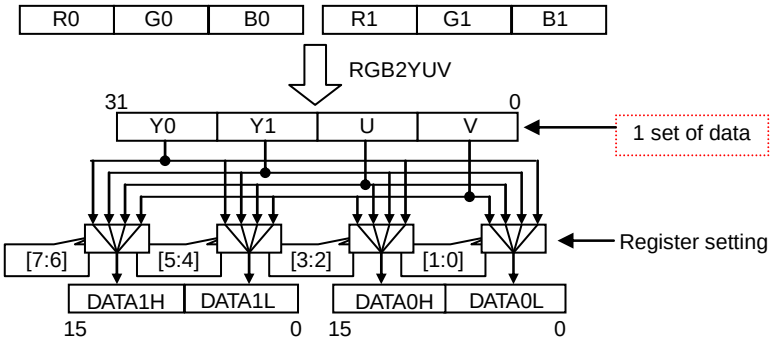
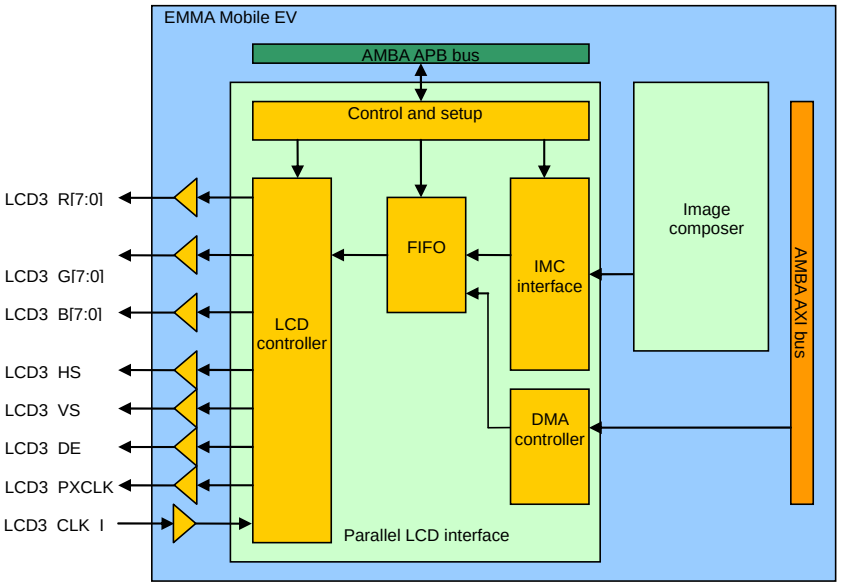


Figure 3-15. Parallel LCD Interface Block Diagram

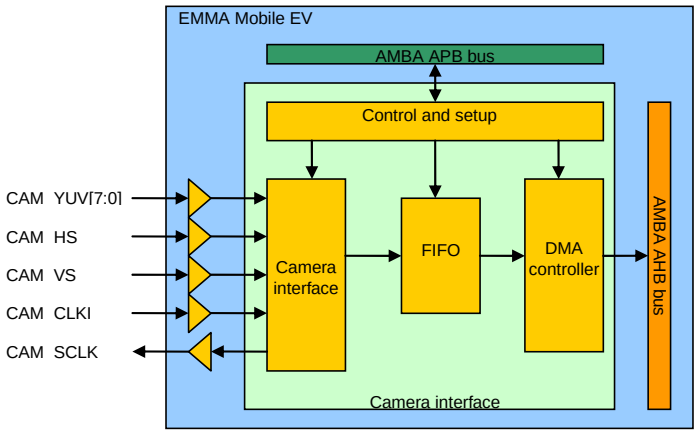


3.20 Camera Interface

The camera interface has the following features:

- Maximum input image: X = 4,088, Y = 4,092 (includes blanking area)
- Supported image formats:
  - Camera input: YUV422
  - Memory output: YUV420, YUV422

Figure 3-16. Camera Interface Block Diagram

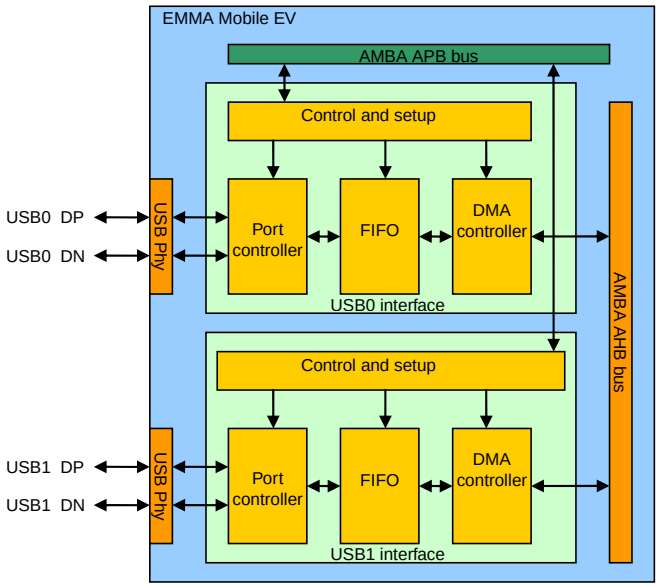


3.21 USB Interface

The USB interface has the following features:

- Supports 1-port USB 2.0 host and 1-port peripheral interfaces.
- Supports USB 2.0 high-speed, full-speed, and low-speed modes.
- Includes a DMA controller.

Figure 3-17. USB Interface Block Diagram



3.22 UART Interface

The UART interface has the following features:

Includes 4 × UART blocks: UART0, UART1, UART2 and UART3.

Incorporates two 64-byte FIFO buffers: one for transmission and one for reception.

The following operating modes are available:

- Non-FIFO mode (16450 mode)
- 16-byte FIFO mode (16550 mode)
- 64-byte FIFO mode

Supports programmable auto-RTS and auto-CTS (only for UART1).

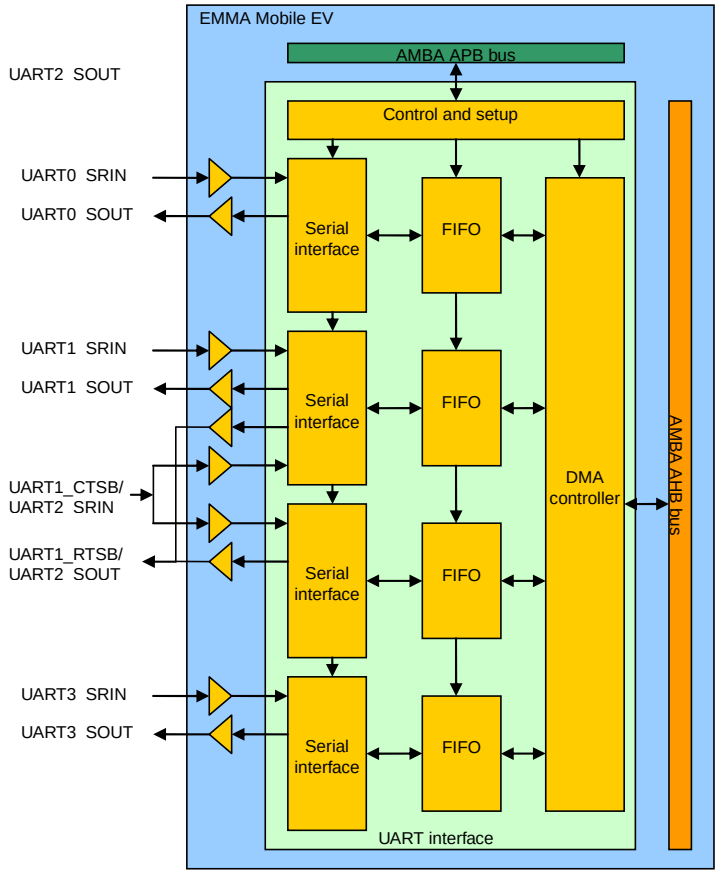
Standard asynchronous communication control bits (start, stop and parity bits) can be added to or deleted from serial data to be transmitted and received.

The following items can be controlled by software:

- Character length: 5, 6, 7 or 8 bits
- Parity bit: Even parity, odd parity, or no parity bit
- Stop bit: 1 or 2 bits
- Baud rate: Reference clock frequency division ratio selectable from 1 to $(2^{16} - 1)$

Supports the modem control interface (CTS, RTS). (Only UART1 supports flow control.)

Figure 3-18. UART Interface Block Diagram



3.23 I²C Interface

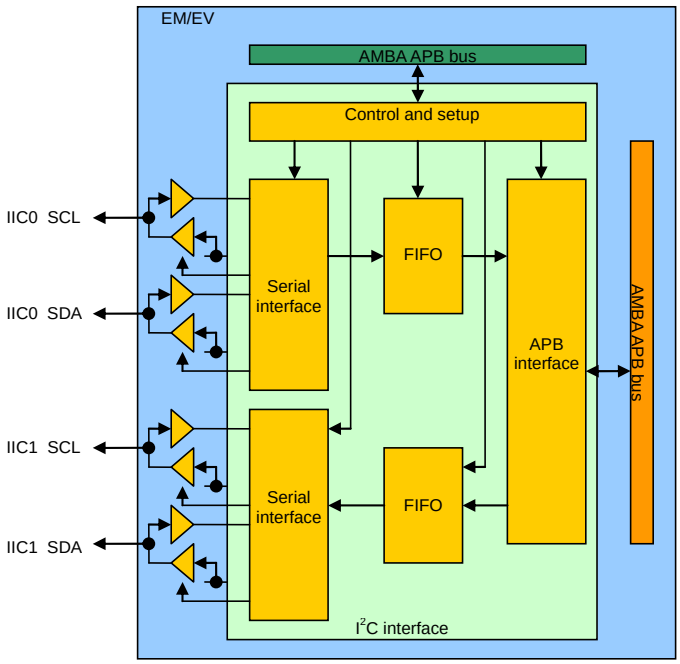
The I²C interface has the following features:

2 ports

Supports standard mode (up to 97 kbps) and high speed mode (up to 383 kbps).

Supports multiple masters.

Figure 3-19. I²C Interface Block Diagram



3.24 Unified Serial Interface

This macro is a general-purpose serial interface with a range of audio serial interface and, SPI interface features.
The main features of the SIO macro are shown below.
The SIO macro supports a 4-wire SPI serial interface as well as serial interfaces for audio and voice codecs.
Also, in SPI mode, the SIO macro can operate as both a master and a slave.

3.24.1 SPI features

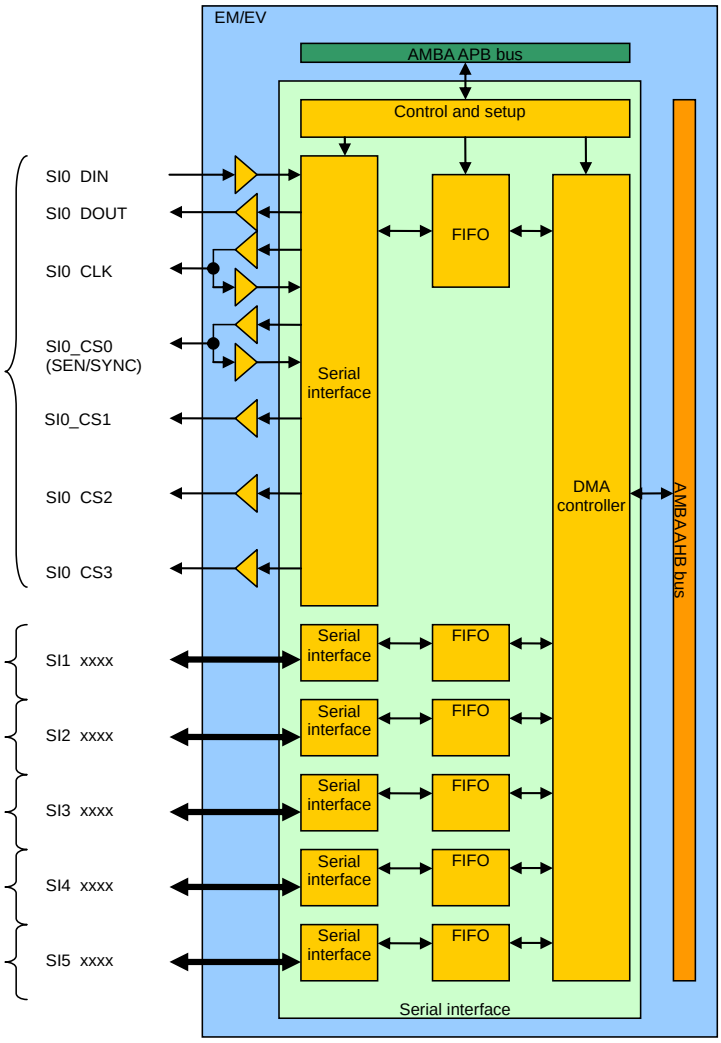
- Transfer modes
  The SPI macro can be set to CPU control mode or DMA control mode when operating as the master and when operating as a slave.
  - CPU control mode: In this mode, transfer ends after one frame of data has been transmitted or received, or transmitted-and-received.
  - DMA control mode: In this mode, data can be transmitted and received continuously using two 32-bit × 32-word FIFO buffers (one for transmission and one for reception).
    Transfer stops when the CPU issues a STOP command or according to the status of the FIFO buffers.
- The SCLK polarity (positive or inverted) and delay (half an SCLK clock cycle) can be specified for each CS signal.
- There are eight CS signals.
- The number of bits to transfer can be set (between 8 and 32 bits).
- Interrupts can be generated.
- Clock request signals (SIO_DMA_CLKREQ, SIO_PCLKREQ, and SIO_CTLCLKREQ) can be generated.
- Transfer can be stopped automatically (in DMA mode).
  - SPI transmission is stopped if the transmit buffer becomes empty while the DMA master is transmitting data.
  - SPI reception is stopped if the amount of data received matches the DMA transfer data length specified by SIOx_DMA_LENG while the DMA master is receiving data. If SIOx_DMA_LENG is set to 0, however, transfer continues until the CPU issues a STOP command.
- CS signals can be fixed by specifying a register setting.
- The I/O phases of SI/SO can be switched.

3.24.2 Audio (PCM) features

The PCM macro now supports AC'97 (by setting the Mode5+AC97 mode bit), specification of LJF or RJF formats.

- Seven operating modes can be specified (modes 0 to 6).
- Data is transferred using DMA. The PCM macro includes two 32-bit × 32-word FIFO buffers (one for transmission and one for reception).
- The control bus clock (SIO_PCLK), serial clock (SIO_SCLK), and AHB bus clock can be automatically controlled.
- The PCM macro can handle periods when the bus clock is not supplied, such as when the bus clock frequency is switched.
- Can be used to interface with an AC'97 controller.
- It is now selectable whether to adjust frames to the right or left when specifying the data transfer format.
- SIO_CS0 is used for sync signal I/O, and SIO_CS1 is used for AC'97 reset signal output.
- SIO_CS2 to SIO_CS6 are fixed to 0 (not used).

Figure 3-20. Block Diagram of Unified Serial I/O Interface



3.25 General-Purpose I/O Interface (GPIO)

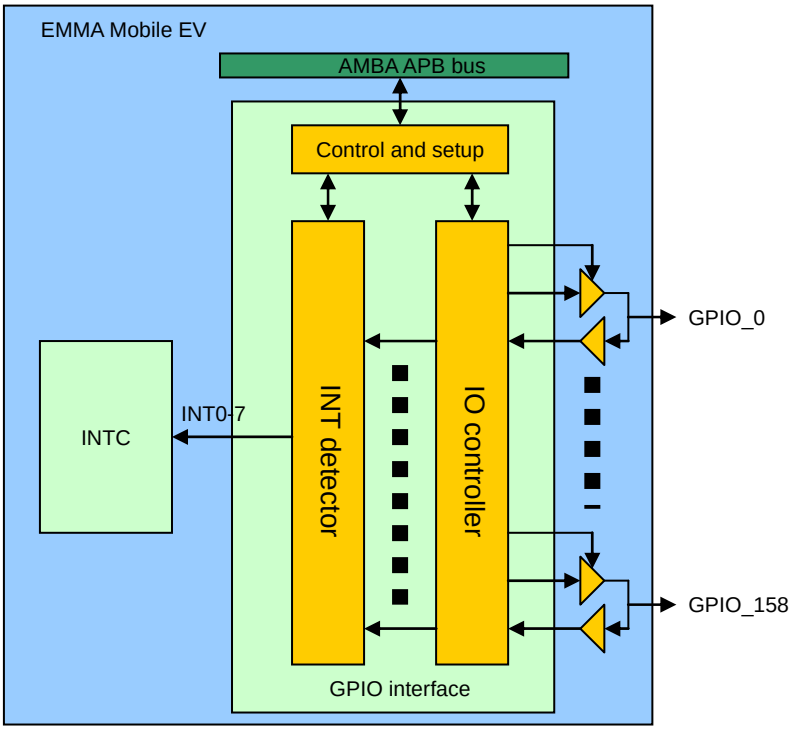
EM/EV has 159 general-purpose I/O ports.

Each port asserts its own interrupt when a signal transition is detected.

The following signal transitions occur:

- Synchronous rising edge detection
- Synchronous falling edge detection
- Synchronous high level detection
- Synchronous low level detection
- Synchronous rising or falling edge detection
- Asynchronous rising edge detection
- Asynchronous falling edge detection
- Asynchronous high level detection
- Asynchronous low level detection
- Asynchronous rising or falling edge detection

Figure 3-21. GPIO Interface Block Diagram



4. System Control

4.1 Memory Map

Figure 4-1. Memory Map 1

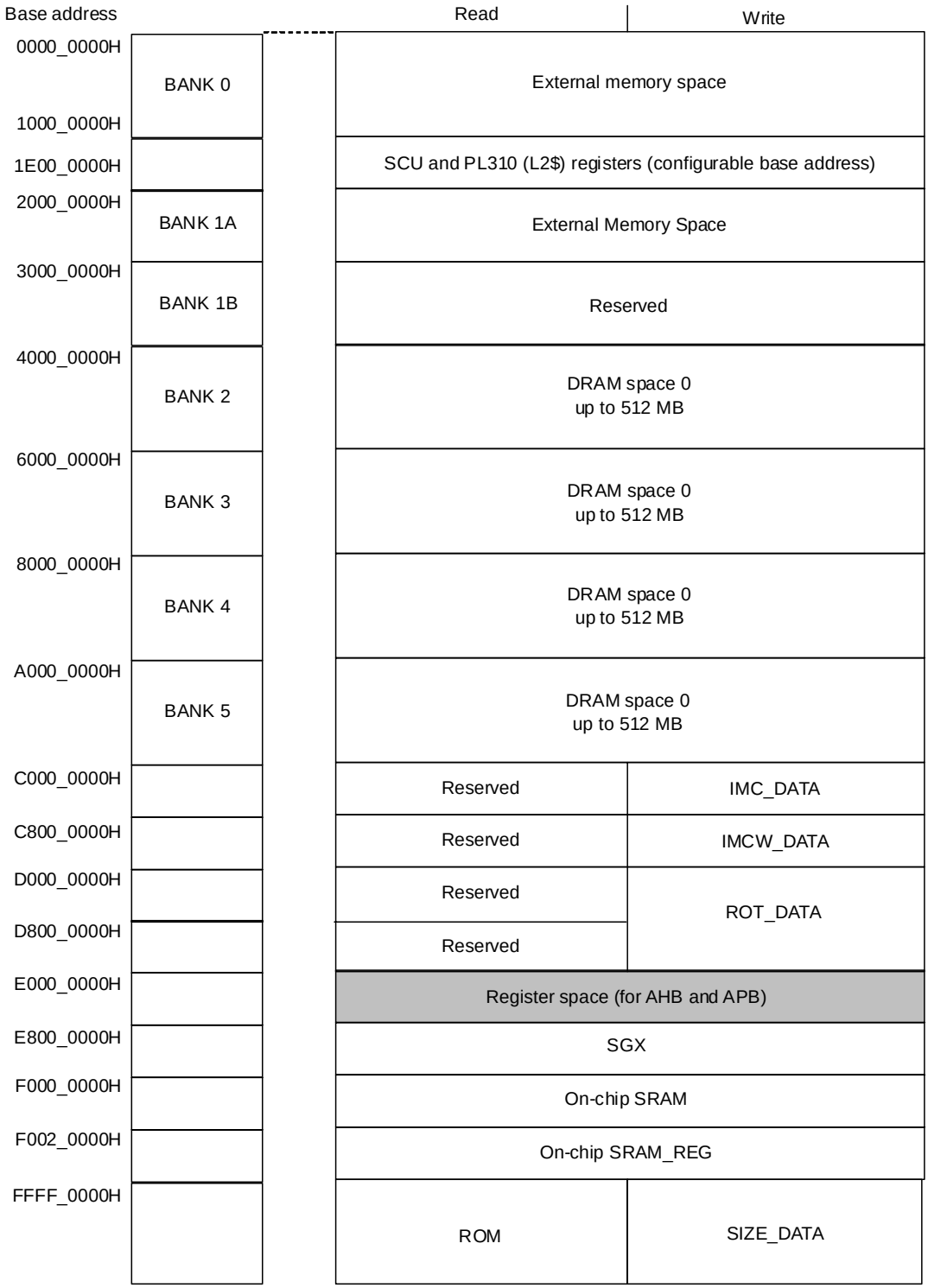


Figure 4-2. Memory Map 2

E000_0000H	TIM
E001_0000H	SIO1
E002_0000H	INTA
E003_0000H	INTA(INTT)
E004_0000H	LCD
E005_0000H	GIO
E006_0000H	Reserved
E007_0000H	IIC0
E008_0000H	Reserved
E009_0000H	PBL0
E00A_0000H	MEMC
E00B_0000H	Reserved
E00C_0000H	AFS
E00D_0000H	Reserved
E00E_0000H	Reserved
E00F_0000H	BUS0 (PDMA)
E010_0000H	PMU
E011_0000H	SMU
E012_0000H	SIO0
E013_0000H	Reserved
E014_0000H	CHG
E015_0000H	Reserved
E016_0000H	Reserved
E017_0000H	Reserved
E018_0000H	STI
E019_0000H	Reserved
E020_0000H	SMU_SEC
E021_0000H	AFS_SEC
E022_0000H	Reserved
E0FF_0000H	Reserved

E100_0000H	CHG1
E101_0000H	Reserved
E102_0000H	UART0
E103_0000H	UART1
E104_0000H	UART2
E105_0000H	UART3
E106_0000H	Reserved
E107_0000H	M2P
E108_0000H	P2M
E109_0000H	M2M
E10A_0000H	IIC1
E10B_0000H	CAM
E10C_0000H	SIO2
E10D_0000H	SIO3
E10E_0000H	SIO4
E10F_0000H	SIO5
E110_0000H	Reserved
E111_0000H	PBL1
E112_0000H	BUS1
E113_0000H	PWM
E114_0000H	Reserved
E115_0000H	DTV
E116_0000H	Reserved
E117_0000H	Reserved
E118_0000H	SIZ
E119_0000H	AVE
E11A_0000H	Reserved
E11B_0000H	Reserved
E11C_0000H	Reserved
E11D_0000H	Reserved
E11E_0000H	Reserved
E11F_0000H	Reserved

E120_0000H	Reserved
E121_0000H	NTS
E122_0000H	ROT
E123_0000H	Reserved
E124_0000H	Reserved
E125_0000H	Reserved
E126_0000H	IMC
E127_0000H	IMCW
E128_0000H	ICE
E129_0000H	Reserved
E12A_0000H	Reserved
E12B_0000H	Reserved
E200_0000H	Reserved
E210_0000H	SDC
E220_0000H	CFI
E230_0000H	Reserved
E240_0000H	Reserved
E250_0000H	Reserved
E260_0000H	Reserved
E270_0000H	USBS0
E280_0000H	USBS1
E290_0000H	SDIO0
E2A0_0000H	SDIO1
E2B0_0000H	SDIO2

4.2 PLLs

PLL1:

Clock frequency: 400 to 533 MHz

Used as the internal system clock.

The multiplication ratio is selectable.

(Before changing the multiplication ratio, change the clock source for other PLLs.)

PLL2:

Clock frequency: 320 to 500 MHz

Used as the main clock in LPDDR mode.

The multiplication ratio is selectable.

(Before changing the multiplication ratio, change the clock source for other PLLs.)

PLL3:

Clock frequency: 229.376 MHz (fixed)

Used as the system clock for peripherals and runs all the time.

PLL4:

Clock frequency: 320 to 533MHz.

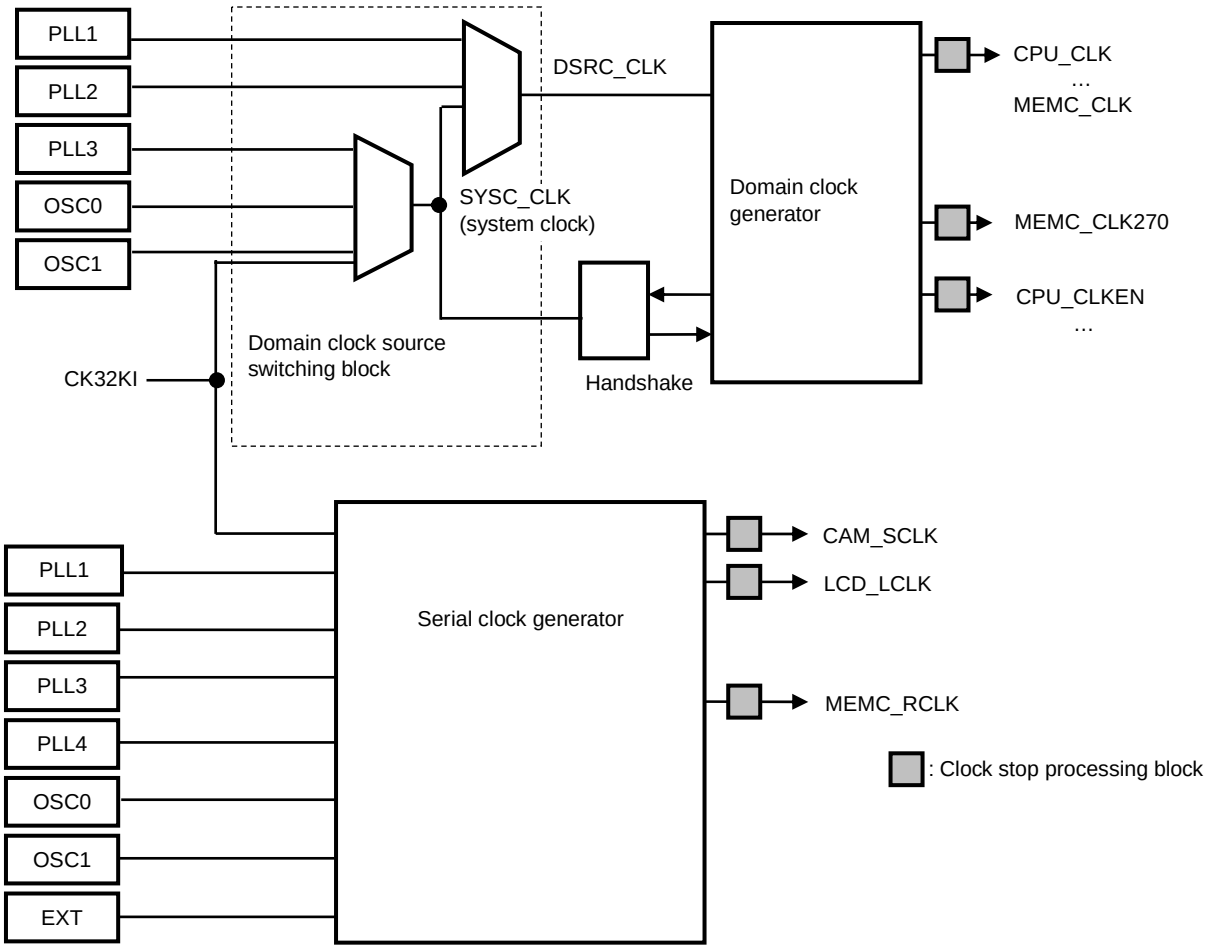
Used as the CPU clock (Serial LCD display clock)

OSC0 and OSC1:

Clock frequency: 10 to 27 MHz

Used as the PLL1 reference clock, source clock in Sleep mode, or reference clock for the USB macro.

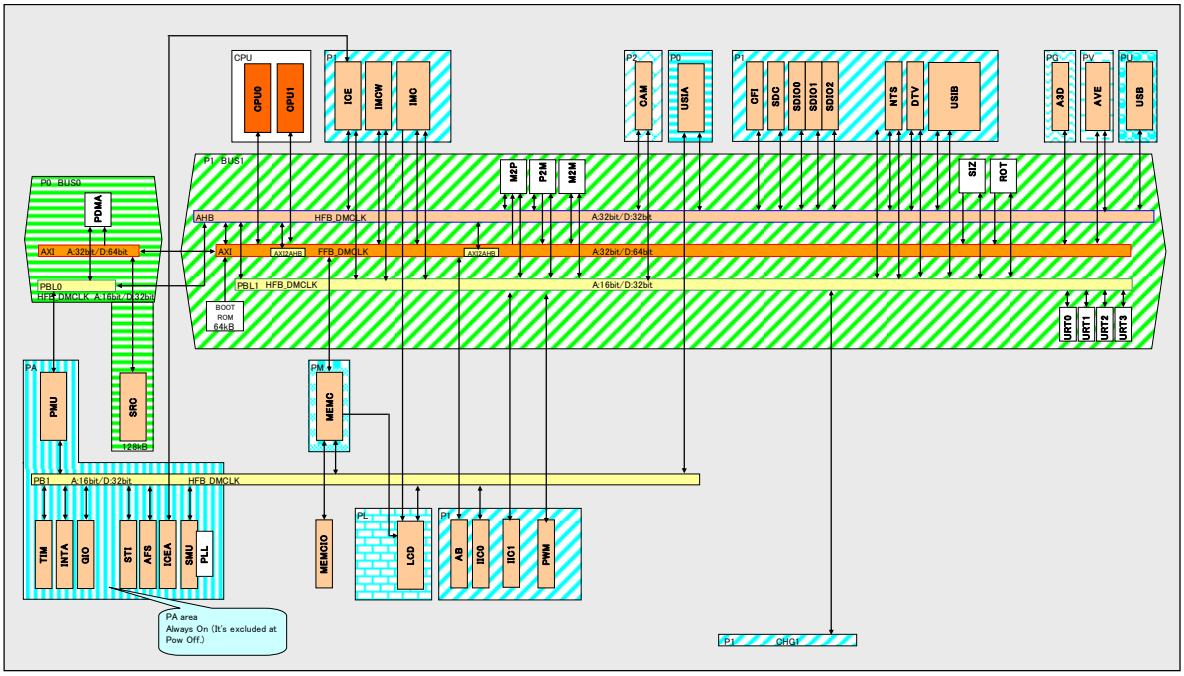
Figure 4-3. Clock System Overview



5. Power Control

5.1 Power Separation Diagram

Figure 5-1. EM/EV Power Domain Configuration



5.2 Power Mode Transition

Figure 5-2. EM/EV Power Mode Transition

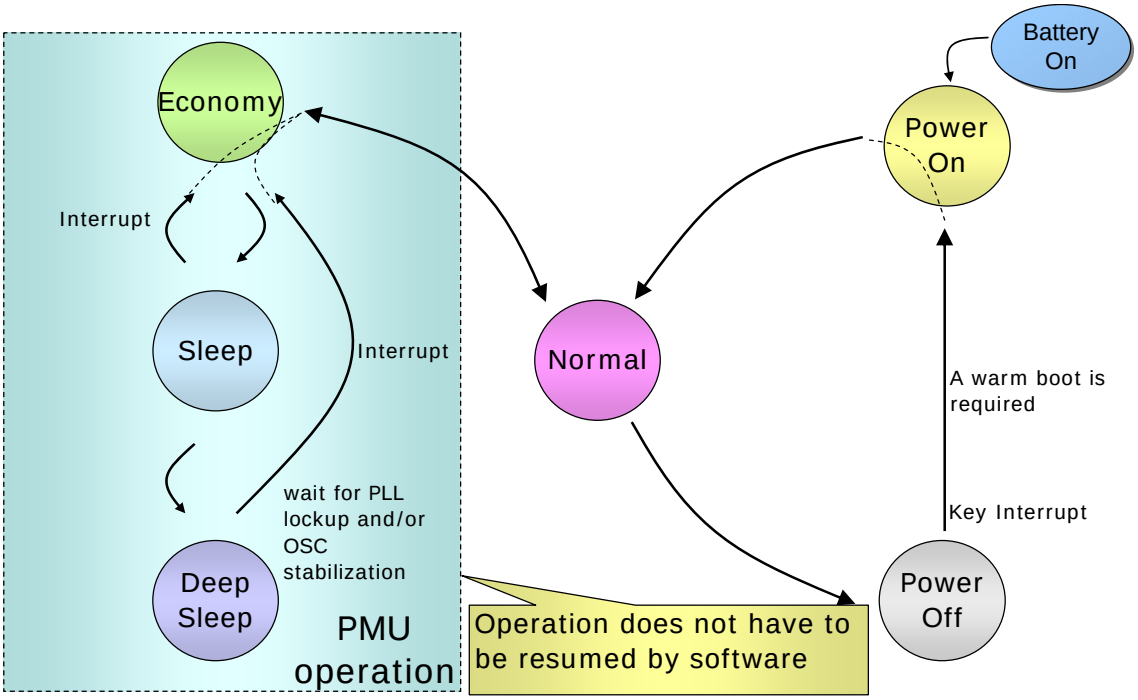


Table 5-1 DDR2 Mode : Clock and V_{DD} Conditions

	Power Mode	Power OFF	Deep Sleep	Sleep	Economy	Normal	Power ON
Divide Rate & condition	CPU (Up to 533MHz)	– (WFI(QR) Power OFF)				1-16	16
	Full-Freq-Bus (Up to 266MHz)	– Power OFF	1	1-16	1-16	1-16	16
	Low-Freq-Bus (Up to 266MHz)	–	–	–	–	1-16	16
	DDR (Up to 266MHz)	Self Refresh (Power OFF)			1-16	1-16	16
Power Supply	VDDD1	0V	0.75V	1.15V			
	On-chip SW	0V				1.15V	
	IO	1.8V/3.3V (Always ON)					
Clock source		32.768KHz		OSC	PLL3	PLL1	PLL3
	PLL1	VDD=0V		Standby		Run	Standby
	PLL3	VDD=0V		Standby	Run		
	OSC 10-30MHz	Stop		Run			Stop
LCD mode		Off			LCD direct	Normal/LCD direct	
Audio mode		Off		PCM direct		Normal/PCM direct	

Table 5-2 LPDDR Mode : Clock and V_{DD} Conditions

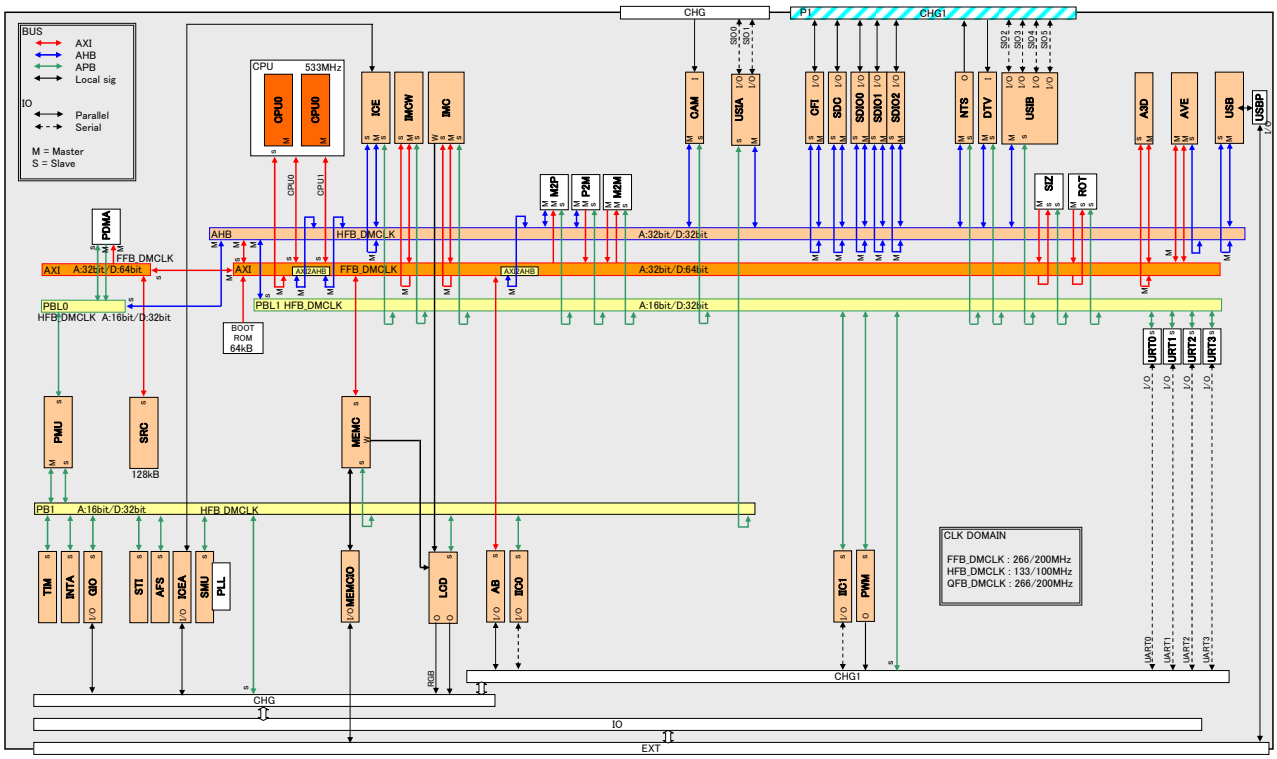
<table>
<tr><th></th><th>Power Mode</th><th>Power OFF</th><th>Deep Sleep</th><th>Sleep</th><th>Economy</th><th>Normal</th><th>Power ON</th></tr>
<tr><td rowspan="4">Divide Rate & condition</td><td>CPU
(Up to 533MHz)</td><td colspan="4">– (WFI(QR) Power OFF)</td><td>1-16</td><td>16</td></tr>
<tr><td>Full-Freq-Bus
(Up to 200MHz)</td><td>–
Power OFF</td><td>1</td><td>1-16</td><td>1-16</td><td>1-16</td><td>16</td></tr>
<tr><td>Low-Freq-Bus
(Up to 200MHz)</td><td>–</td><td>–</td><td>–</td><td>–</td><td>1-16</td><td>16</td></tr>
<tr><td>DDR
(Up to 200MHz)</td><td colspan="3">Self Refresh
(Power OFF)</td><td>1-16</td><td>1-16</td><td>16</td></tr>
<tr><td rowspan="3">Power Supply</td><td>VDDD1</td><td>0V</td><td>0.75V</td><td colspan="4">1.15V</td></tr>
<tr><td>On-chip SW</td><td colspan="5">0V</td><td colspan="2">1.15V</td></tr>
<tr><td>IO</td><td colspan="7">1.8V/3.3V (Always ON)</td></tr>
<tr><td rowspan="4">Clock source</td><td></td><td colspan="2">32.768KHz</td><td>OSC</td><td>PLL3</td><td>PLL2</td><td>PLL3</td></tr>
<tr><td>PLL2</td><td colspan="2">VDD=0V</td><td colspan="3">Standby</td><td>Run</td><td>Standby</td></tr>
<tr><td>PLL3</td><td colspan="2">VDD=0V</td><td>Standby</td><td colspan="3">Run</td></tr>
<tr><td>OSC 10-30MHz</td><td colspan="2">Stop</td><td>Run</td><td colspan="2">Run/Stop</td><td>Stop</td></tr>
<tr><td colspan="2">LCD mode</td><td colspan="4">Off</td><td>LCD direct</td><td colspan="2">Normal/LCD direct</td></tr>
<tr><td colspan="2">Audio mode</td><td colspan="3">Off</td><td colspan="2">PCM direct</td><td colspan="2">Normal/PCM direct</td></tr>
</table>

6. Bus Structure

6.1 Bus configuration

Figure 6-1 shows the EM/EV bus architecture.

Figure 6-1. EM/EV Bus Configuration



EM/EV employs the ARM AXI (64 bits, 6 layers) as the system bus.
The system bus employs a 3-layer AXI bus switch that consists of one AXI bus switch for the memory controller (MEMC), one for the external memory interface (AB0), and one for the internal SRAM (SRC).

(1) Buses that make up the EM/EV bus system

- Main system bus (AMBA AXI)
- Legacy master bus (AMBA AHB)
- CPU command bus (AMBA APB)
- Display bus (AMBA AXI)

(2) Bus bridges

- AXI bridge for AHB legacy master bus
- AXI to AXI bridge for display bus

(3) Main system bus

- 64-bit 6-layer AMBA AXI bus
- SDRAM × 1 layer

- External memory × 1 layer
- Internal SRAM × 1 layer
- APB bridge × 1 layer

(4) Legacy master bus

- 32-bit AMBA AHB bus

(5) CPU command bus

- 32-bit AMBA APB bus
- Includes security extension

(6) Display bus

- 64-bit AMBA AXI bus

6.2 BUS1 Registers

This register (BUS1_CPU_CONF: E112_0000H) specifies sets the BAND width of the CPU.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		WBW_LIMIT					

7	6	5	4	3	2	1	0
Reserved		RBW_LIMIT					

Name	R/W	Bit No.	After Reset	Description
Reserved	R/W	31:14	0	Reserved. Establish 0.
WBW_LIMIT	R/W	13:8	0	Write band width limit A band width is restricted to 1/(setting value+1). Ex) 0x00 : Without restriction 0x01 : 1/2 0x02 : 1/3 :
Reserved	R/W	7:6	0	Reserved. Establish 0.
RBW_LIMIT	R/W	5:0	0	Read band width limit A band width is restricted to 1/(setting value+1). Ex) 0x00 : Without restriction 0x01 : 1/2 0x02 : 1/3 :

This register (BUS1_M2P_CONF: E112_002CH) specifies sets the BAND width of the CPU.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		WBW_LIMIT					

7	6	5	4	3	2	1	0
Reserved		RBW_LIMIT					

Name	R/W	Bit No.	After Reset	Description
Reserved	R/W	31:14	0	Reserved. Establish 0.
WBW_LIMIT	R/W	13:8	0	Write band width limit A band width is restricted to 1/(setting value+1). Ex) 0x00 : Without restriction 0x01 : 1/2 0x02 : 1/3 :
Reserved	R/W	7:6	0	Reserved. Establish 0.
RBW_LIMIT	R/W	5:0	0	Read band width limit A band width is restricted to 1/(setting value+1). Ex) 0x00 : Without restriction 0x01 : 1/2 0x02 : 1/3 :

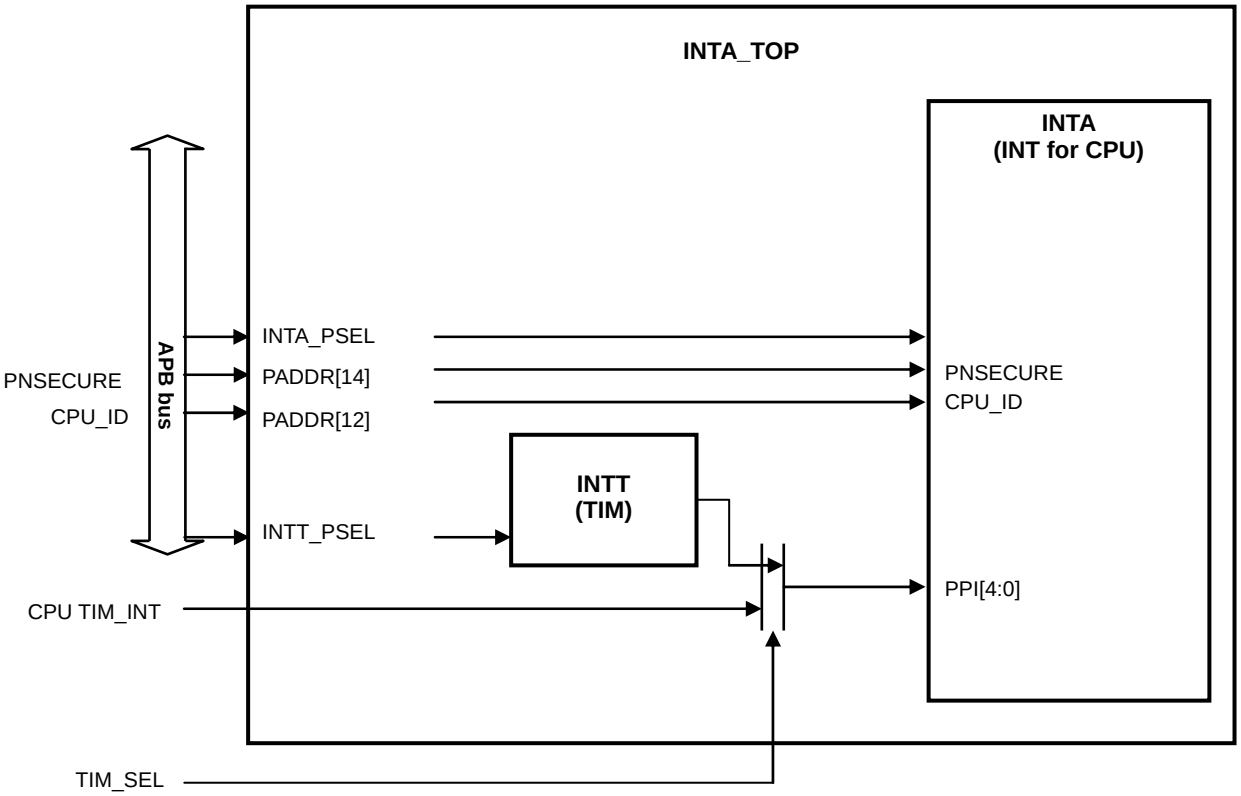
7. Interrupt Control

7.1 Overview

The interrupt control module (INTA) controls interrupts to the CPU.
Table 7-1 shows the interrupt sources assigned to INT[0:165].

- Built-in CortexA-9 GIC (PL390)
- Complies with the AMBA specification (Rev. 2.0)
- Energy efficient
  Automatic clock control is supported, and, if the clock is necessary, a clock request signal is output to the SMU.
- Restriction
  During ICE debugging, automatic clock control must be disabled.
- The INTA module is connected to AHB-APB bridge 1 (PB1) and synchronizes with PCLK. The module has various settings for controlling interrupts, and it reads from and writes to registers. The module complies with the AMBA™ APB specification.

Figure 7-1. INTA Block Diagram



Interruption controller for CPU : GIC
Timer extracted from the CPU (CortexA9) and integrated into INTA : INTT
Module which includes the above : INTA

7.1.1 Interrupt source

(1/4)

Category	INT_No.	Module	INTA Signal Name	Description	Edge/Level
SGI	0	CPU	SGI_0	SGI bit 0	Level
	1		SGI_1	SGI bit 1	Level
	2		SGI_2	SGI bit 2	Level
	3		SGI_3	SGI bit 3	Level
	4		SGI_4	SGI bit 4	Level
	5		SGI_5	SGI bit 5	Level
	6		SGI_6	SGI bit 6	Level
	7		SGI_7	SGI bit 7	Level
	8		SGI_8	SGI bit 8	Level
	9		SGI_9	SGI bit 9	Level
	10		SGI_10	SGI bit 10	Level
	11		SGI_11	SGI bit 11	Level
	12		SGI_12	SGI bit 12	Level
	13		SGI_13	SGI bit 13	Level
	14		SGI_14	SGI bit 14	Level
	15		SGI_15	SGI bit 15	Level
PPI	16		Reserved	–	–
	17		CPU_TIM_INT	CPU timer interrupt	Edge
	18		CPU_WDT_INT	CPU WDT interrupt	Edge
	19		Reserved	–	–
	20		CPU_GTM_INT	CPU global timer interrupt	Edge
	21		Reserved	–	–
	22		Reserved	–	–
	23		Reserved	–	–
	24		Reserved	–	–
	25		Reserved	–	–
	26		Reserved	–	–
	27		Reserved	–	–
	28		Reserved	–	–
	29		Reserved	–	–
	30		Reserved	–	–
	31		Reserved	–	–
SPI	32	CPU0	Register in the INT	–	Level
	33	CPU1	Register in the INT	–	Level
	34	Reserved	Reserved	–	–
	35		Reserved	–	–
	36	IMC	IMC_INT	IMC interrupt	Level
	37	IMCW	IMCW_INT	IMCW interrupt	Level
	38	SRC	SRC_INT	SRC interrupt	Level
	39	Reserved	Reserved	–	–

(2/4)

Category	INT_No.	Module	INTA Signal Name	Description	Edge/Level
SPI	40	BUS1	BUS1_INT[27]	UART #0 interrupt	Level
	41		BUS1_INT[28]	UART #1 interrupt	Level
	42		BUS1_INT[29]	UART #2 interrupt	Level
	43		BUS1_INT[30]	UART #3 interrupt	Level
	44	USIA	SIO0_INT	USI #0 interrupt	Level
	45		SIO1_INT	USI #1 interrupt	Level
	46	USIB	SIO2_INT	USI #2 interrupt	Level
	47		SIO3_INT	USI #3 interrupt	Level
	48		SIO4_INT	USI #4 interrupt	Level
	49		SIO5_INT	USI #5 interrupt	Level
	50	PMU	PMU_INT	PMU interrupt	Level
	51	SMU	SMU_INT	SMU interrupt	Level
	52	LCD	LCD_INT	LCD interrupt	Level
	53	CAM	CAM_INT	CAM interrupt	Level
	54	Reserved	Reserved	–	–
	55	AB	AB_INT_A	AB interrupt	Level
	56	NTS	NTS_INT	NTS interrupt	Level
	57	SD	SDC_SYNC_INT	SDC synchronous interrupt	Level
	58		SDC_ASYNC_INT	SDC asynchronous interrupt	Level
	59		SDI_INT[0]	SDIO #0 interrupt	Level
	60		SDI_INT[1]	SDIO #1 interrupt	Level
	61		SDI_INT[2]	SDIO #2 interrupt	Level
	62	Reserved	Reserved	–	–
	63	A3D	A3D_INT	A3D interrupt	Level
	64	IIC0	IIC0_INT	IIC #0 interrupt	Edge
	65	IIC1	IIC1_INT	IIC #1 interrupt	Edge
	66	DTV	DTV_INT	DTV interrupt	Level
	67	PWM	PWM_INT	PWM interrupt	Level
	68	Reserved	Reserved	–	–
	69	Reserved	Reserved	–	–
	70	Reserved	Reserved	–	–
	71	Reserved	Reserved	–	–
	72	Reserved	Reserved	–	–
	73	Reserved	Reserved	–	–
	74	Reserved	Reserved	–	–
	75	Reserved	Reserved	–	–
	76	Reserved	Reserved	–	–
	77	Reserved	Reserved	–	–
	78	Reserved	Reserved	–	–
	79	Reserved	Reserved	–	–
	80	Reserved	Reserved	–	–
	81	Reserved	Reserved	–	–
	82	Reserved	Reserved	–	–

(3/4)

Category	INT_No.	Module	INTA Signal Name	Description	Edge/Level
SPI	83	CHG	CHG_INT	CHG interrupt	Level
	84	TIM	TI_INT[0]	TI #0 interrupt	Edge
	85		TI_INT[1]	TI #1 interrupt	Edge
	86		TI_INT[2]	TI #2 interrupt	Edge
	87		TI_INT[3]	TI #3 interrupt	Edge
	88		TW_INT[0]	WDT #0 interrupt	Edge
	89		TW_INT[1]	WDT #1 interrupt	Edge
	90		TW_INT[2]	WDT #2 interrupt	Edge
	91		TW_INT[3]	WDT #3 interrupt	Edge
	92		TW_INT[4]	WDT #4 interrupt	Edge
	93		TG_INT[0]	TG #0 interrupt	Edge
	94		TG_INT[1]	TG #1 interrupt	Edge
	95		TG_INT[2]	TG #2 interrupt	Edge
	96		TG_INT[3]	TG #3 interrupt	Edge
	97		TG_INT[4]	TG #4 interrupt	Edge
	98		TG_INT[5]	TG #5 interrupt	Edge
	99	GIO	GIO_A_INT0	GIO #0 interrupt	Level
	100		GIO_A_INT1	GIO #1 interrupt	Level
	101		GIO_A_INT2	GIO #2 interrupt	Level
	102		GIO_A_INT3	GIO #3 interrupt	Level
	103		GIO_A_INT4	GIO #4 interrupt	Level
	104		GIO_A_INT5	GIO #5 interrupt	Level
	105		GIO_A_INT6	GIO #6 interrupt	Level
	106		GIO_A_INT7	GIO #7 interrupt	Level
	107		GIO_A_INT8	GIO #8 interrupt	Level
	108		GIO_A_INT9	GIO #9 interrupt	Level
	109	PDMA	PDMA_INT	PDMA interrupt	Level
	110		Register in the INT	int_liis0	Level
	111		Register in the INT	int_liis1	Level
	112		Register in the INT	int_liis2	Level
	113		Register in the INT	int_liis3	Level
	114	CFI	CFI_INT	CFI interrupt	Level
	115	USB	USB_INTH	USB_Host interrupt	–
	116	BUS1	BUS1_INT[0]	M2M #0 interrupt	Level
	117	Reserved	BUS1_INT[1]	M2M #1 interrupt	Level
	118		BUS1_INT[2]	M2M #2 interrupt	Level
	119		BUS1_INT[3]	M2M #3 interrupt	Level
	120		BUS1_INT[4]	M2M #4 interrupt	Level
	121		BUS1_INT[5]	M2M #5 interrupt	Level
	122		BUS1_INT[6]	M2M #6 interrupt	Level
	123		BUS1_INT[7]	M2M #7 interrupt	Level
	124		BUS1_INT[8]	M2P #0 interrupt	Level

(4/4)

Category	INT_No.	Module	INTA Signal Name	Description	Edge/Level
SPI	125	BUS1	BUS1_INT[9]	M2P #1 interrupt	Level
	126		BUS1_INT[10]	M2P #2 interrupt	Level
	127		BUS1_INT[11]	M2P #3 interrupt	Level
	128		BUS1_INT[12]	M2P #4 interrupt	Level
	129		BUS1_INT[13]	M2P #5 interrupt	Level
	130		BUS1_INT[14]	M2P #6 interrupt	Level
	131		BUS1_INT[15]	M2P #7 interrupt	Level
	132		BUS1_INT[16]	P2M #0 interrupt	Level
	133		BUS1_INT[17]	P2M #1 interrupt	Level
	134		BUS1_INT[18]	P2M #2 interrupt	Level
	135		BUS1_INT[19]	P2M #3 interrupt	Level
	136		BUS1_INT[20]	P2M #4 interrupt	Level
	137		BUS1_INT[21]	P2M #5 interrupt	Level
	138		BUS1_INT[22]	P2M #6 interrupt	Level
	139		BUS1_INT[23]	P2M #7 interrupt	Level
	140		Reserved	–	–
	141		Reserved	–	–
	142		BUS1_INT[26]	ROM interrupt	Level
	143		Reserved	–	–
	144		Reserved	–	–
	145		Reserved	–	–
	146		Reserved	–	–
	147		Reserved	–	–
	148	CPU	COMMTX[0]	COMMTX[0]	Level
	149		COMMTX[1]	COMMTX[1]	Level
	150		COMMRX[0]	COMMRX[0]	Level
	151		COMMRX[1]	COMMRX[1]	Level
	152		PMONIRQ[0]	PMONIRQ[0]	Level
	153		PMONIRQ[1]	PMONIRQ[1]	Level
	154		L2CCINTR[0]	L2CCINTR[0]	Level
	155		L2CCINTR[1]	L2CCINTR[1]	Level
	156		L2CCINTR[2]	L2CCINTR[2]	Level
	157	STI	STI_INT	STI interrupt	Level
	158	USB	USB_INTF[0]	USB_Function #0 interrupt	Level
	159		USB_INTF[1]	USB_Function #1 interrupt	Level
	160	Reserved	Reserved	–	–
	161	Reserved	Reserved	–	–
	162	AB	AB_SEC_INT	AB secure interrupt	Level
	163	MEMC	MEMC_SEC_INT	MEMC secure interrupt	Level
	164	Reserved	Reserved	–	–
	165	AFS	AFS_SEC_INT	AFS secure interrupt	Level

7.1.2 Registers

- The base addresses of the interrupt registers are as follows:
  - INTA: E002_0000H (offset: CPU IF = 0000H, distributer = 8000H)
  - INTT: E003_0000H (offset: general timer = 200H, local timer = 600H)
- Interrupt registers can be accessed via the APB bus, in 32-bit units.

For details about the register functions, see **ARM Generic Interrupt Controller Architecture Specification Architecture version 1.0**.

8. Alternate Pin Function Switching (CHG)

8.1 Register List

Alternate pin functions can be switched by using the registers below.
These registers can only be accessed in 32-bit units.

Base address: E014_0000H (1/3)

Address	Register Name	Symbol	R/W	After Reset
0000H	Boot mode register	CHG_BOOT_MODE	R	–
0004H	P[0:2]/PL OFF data hold control register	CHG_PIN_LAT	R/W	0000_2222H
0008H to 0100H	Reserved	–	–	–
0104H	SDIO[2:0]/SDC interrupt mask register	CHG_CTRL_SDINT	R/W	0000_000FH
0108H	AB0 (ASYNC) boot switch register	CHG_CTRL_AB0_BOOT	R/W	0000_0000H
010CH	Reserved	–	–	–
0110H	1.8 V/3.3 V LCD enable register	CHG_LCD_ENABLE	R/W	0000_0003H
0114H to 01FCH	Reserved	–	–	–
0200H	GPIO[31:0] pin function selection register	CHG_PINSEL_G000	R/W	FFFF_FFFBH
0204H	GPIO[63:32] pin function selection register	CHG_PINSEL_G032	R/W	3E06_0FFFH
0208H	GPIO[95:64] pin function selection register	CHG_PINSEL_G064	R/W	FFFF_FFF0H
020CH	GPIO[127:96] pin function selection register	CHG_PINSEL_G096	R/W	FFFE_07FFH
0210H	GPIO[158:128] pin function selection register	CHG_PINSEL_G128	R/W	787F_FFFFH
0214H to 0280H	Reserved	–	–	–
0284H	3.3 V LCD pin function selection register	CHG_PINSEL_LCD3	R/W	0000_0000H
0288H	UART pin function selection register	CHG_PINSEL_UART	R/W	0000_0000H
028CH	IIC pin function selection register	CHG_PINSEL_IIC	R/W	0000_0000H
0290H	Reserved	–	–	–
0294H	AB pin function selection register	CHG_PINSEL_AB	R/W	0000_0000H
0298H	USI pin function selection register	CHG_PINSEL_USI	R/W	0000_0000H
029CH to 02A4H	Reserved	–	–	–
02A8H	HSI pin function selection register	CHG_PINSEL_HSI	R/W	0000_0000H
02ACH to 02FCH	Reserved	–	–	–
0300H	Pull-up/pull-down/input enable/Schmitt trigger control register 0	CHG_PULL0	R/W	3333_3333H
0304H	Pull-up/pull-down/input enable/Schmitt trigger control register 1	CHG_PULL1	R/W	3300_0003H
0308H	Pull-up/pull-down/input enable/Schmitt trigger control register 2	CHG_PULL2	R/W	3333_3333H
030CH	Pull-up/pull-down/input enable/Schmitt trigger control register 3	CHG_PULL3	R/W	0000_0333H
0310H	Pull-up/pull-down/input enable/Schmitt trigger control register 4	CHG_PULL4	R/W	0333_3333H

(2/3)

Address	Register Name	Symbol	R/W	After Reset
0314H	Pull-up/pull-down/input enable/Schmitt trigger control register 5	CHG_PULL5	R/W	3333_3333H
0318H	Pull-up/pull-down/input enable/Schmitt trigger control register 6	CHG_PULL6	R/W	0333_3333H
031CH	Pull-up/pull-down/input enable/Schmitt trigger control register 7	CHG_PULL7	R/W	0000_0113H
0320H	Pull-up/pull-down/input enable/Schmitt trigger control register 8	CHG_PULL8	R/W	7777_7770H
0324H	Pull-up/pull-down/input enable/Schmitt trigger control register 9	CHG_PULL9	R/W	7777_7777H
0328H	Pull-up/pull-down/input enable/Schmitt trigger control register 10	CHG_PULL10	R/W	0000_3337H
032CH	Pull-up/pull-down/input enable/Schmitt trigger control register 11	CHG_PULL11	R/W	0000_0000H
0330H	Pull-up/pull-down/input enable/Schmitt trigger control register 12	CHG_PULL12	R/W	0033_3333H
0334H	Pull-up/pull-down/input enable/Schmitt trigger control register 13	CHG_PULL13	R/W	3003_3333H
0338H	Pull-up/pull-down/input enable/Schmitt trigger control register 14	CHG_PULL14	R/W	3333_3003H
033CH	Pull-up/pull-down/input enable/Schmitt trigger control register 15	CHG_PULL15	R/W	0033_3333H
0340H	Pull-up/pull-down/input enable/Schmitt trigger control register 16	CHG_PULL16	R/W	0333_3333H
0344H	Pull-up/pull-down/input enable/Schmitt trigger control register 17	CHG_PULL17	R/W	0003_3333H
0348H	Pull-up/pull-down/input enable/Schmitt trigger control register 18	CHG_PULL18	R/W	3003_0033H
034CH	Pull-up/pull-down/input enable/Schmitt trigger control register 19	CHG_PULL19	R/W	3333_3333H
0350H	Pull-up/pull-down/input enable/Schmitt trigger control register 20	CHG_PULL20	R/W	00B3_3733H
0354H	Pull-up/pull-down/input enable/Schmitt trigger control register 21	CHG_PULL21	R/W	3333_3333H
0358H	Pull-up/pull-down/input enable/Schmitt trigger control register 22	CHG_PULL22	R/W	0FF0_F0D3H
035CH to 0360H	Reserved	–	–	–
0364H	Pull-up/pull-down/input enable/Schmitt trigger control register 25	CHG_PULL25	R/W	0000_0303H
0368H to 03FCH	Reserved	–	–	–
0400H	Driving capability selection register 0	CHG_DRIVE0	R/W	0000_0000H
0404H	Driving capability selection register 1	CHG_DRIVE1	R/W	0000_0000H
0408H	Driving capability selection register 2	CHG_DRIVE2	R/W	AAAA_AA2AH
040CH	Driving capability selection register 3	CHG_DRIVE3	R/W	0000_0000H
0410H	Driving capability selection register 4	CHG_DRIVE4	R/W	0000_0000H
0414H	Driving capability selection register 5	CHG_DRIVE5	R/W	0000_0020H

(3/3)

Address	Register Name	Symbol	R/W	After Reset
0418H to 04FCH	Reserved	–	–	–
0500H	Bus hold function on/off switching register	CHG_BUSHOLD	R/W	0000_FFFFH
0504H to 050CH	Reserved	–	–	–
0510H	AB_CLK output selection register	CHG_FLASHCLK_SEL	R/W	0000_0001H
0514H to 05FCH	Reserved	–	–	–
0600H	3.3 V LCD delay/phase setting register	CHG_DELAY_LCD33	R/W	1000_0000H
0604H to 0608H	Reserved	–	–	–
060CH	AB_CLK delay/phase setting register	CHG_DELAY_AB	R/W	0000_1000H
0610H to 0614H	Reserved	–	–	–
0618H	3.3 V ICE delay/phase setting register	CHG_DELAY_ICEA33	R/W	1000_1000H
061CH	1.8 V ICE delay/phase setting register	CHG_DELAY_ICEA18	R/W	1000_1000H
0620H to 07C0H	Reserved	–	–	–
07C4H	CHGREG reset control register (for testing)	CHG_RST_CTRL	R/W	0000_0000H
07C8H to FFFCH	Reserved	–	–	–

8.2 Register details

CHG registers are reset when the PON_DET1 pin is low level.
They are not reset by the system reset pin (SRESETB).

8.2.1 Boot mode register

This register (CHG_BOOT_MODE: E014_0000H) indicates the status of the UTEST, and BOOTSEL pins.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				BOOT_SEL2	BOOT_SEL1	BOOT_SEL0	UTEST

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:4	–	Reserved. If these bits are read, 0 is returned for each bit.
BOOT_SEL[2:0]	R	3:1	–	Indicates the BOOTSEL pin status.
UTEST	R	0	–	Indicates the UTEST pin status. 0: Normal 1: Test UTEST is used for testing of the LSI.

8.2.2 P[0:2] OFF data hold control register

This register (CHG_PIN_LAT: E014_0004H) sets up how to generate power domain boundary latch signals (P2_PINLAT, P1_PINLAT, and P0_PINLAT) that control the signal output to external pins.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		CHG_PL_LAT	LATCH_PL_SEL	Reserved		CHG_P2_LAT	LATCH_P2_SEL

7	6	5	4	3	2	1	0
Reserved		CHG_P1_LAT	LATCH_P1_SEL	Reserved		CHG_P0_LAT	CHG_P0_LAT_SEL

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_PL_LAT	R/W	13	1	0: Output data as is. 1: Output latched data.
LATCH_PL_SEL	R/W	12	0	0: Use the PL_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_PL_LAT bit to latch data.
Reserved	R	11:10	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P2_LAT	R/W	9	1	0: Output data as is. 1: Output latched data.
LATCH_P2_SEL	R/W	8	0	0: Use the P2_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P2_LAT bit to latch data.
Reserved	R	7:6	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P1_LAT	R/W	5	1	0: Output data as is. 1: Output latched data.
LATCH_P1_SEL	R/W	4	0	0: Use the P1_LAT bit of the P1_POWERSW register in the SMU to latch data. 1: Use the CHG_P1_LAT bit to latch data.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_P0_LAT	R/W	1	1	0: Output data as is. 1: Output latched data.
CHG_P0_LAT_SEL	R/W	0	0	0: Use the P0_LAT bit of the P2_POWERSW register in the SMU to latch data. 1: Use the CHG_P0_LAT bit to latch data.

8.2.3 SDIO[2:0]/SDC interrupt mask register

This register (CHG_CTRL_SDINT: E014_0104H) sets up masking of the interrupt signals (ASYNC_INT) for the SDIO[2:0] and SDC macros.

When an interrupt signal is sent from the SD pin (DATA1), it is reported to INTA when the SD macro is not running.

Disable the masking specified in this register after setting up the CHG_PINSEL_*xxx* and CHG_PINSEL_G*xxx* registers.

31	30	29	28	27	26	25	24
Reserved							

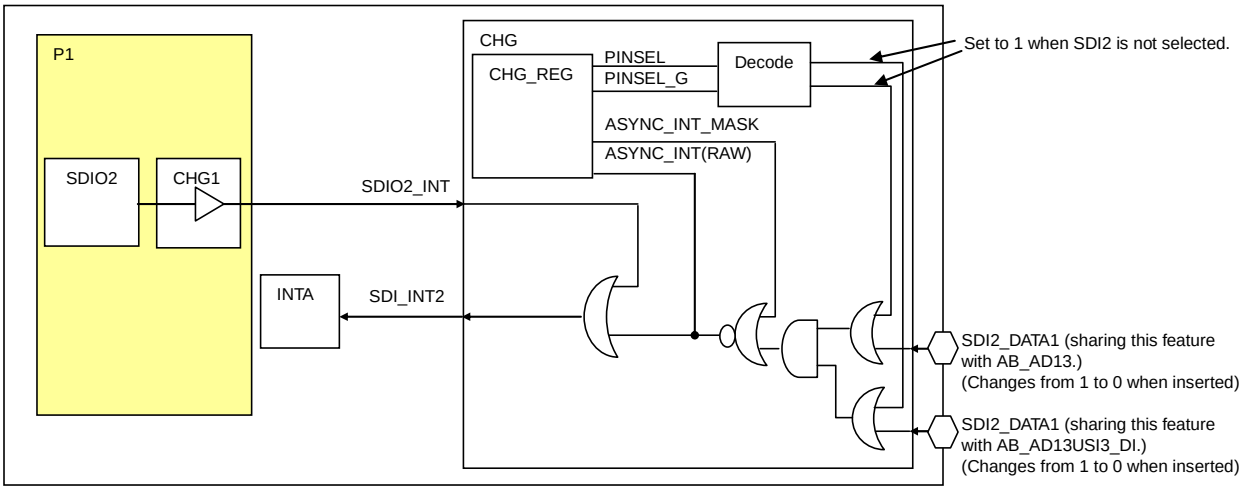
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

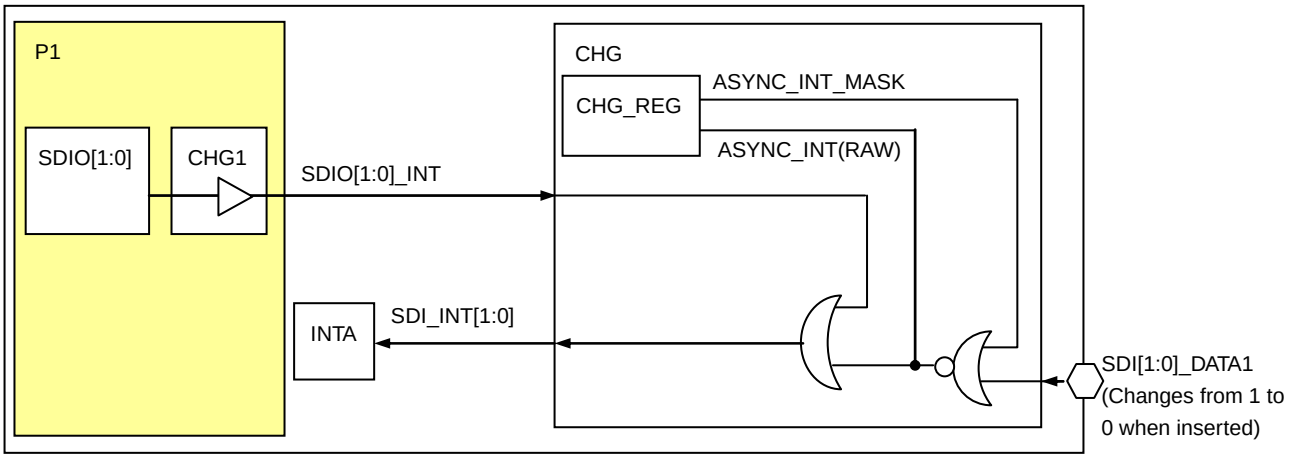
7	6	5	4	3	2	1	0
SDC_ASYNC_INT	SDI2_ASYNC_INT	SDI1_ASYNC_INT	SDI0_ASYNC_INT	SDC_ASYNC_INT_MASK	SDI2_ASYNC_INT_MASK	SDI1_ASYNC_INT_MASK	SDI0_ASYNC_INT_MASK

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:8	–	Reserved. If these bits are read, 0 is returned for each bit.
SDC_ASYNC_INT	R	7	0	Indicates the status of the SDC_ASYNC_INT signal after it is masked. 0: No interrupt 1: The interrupt occurred (when interrupt masking is disabled)
SDI2_ASYNC_INT	R	6	0	Indicates the status of the SDI2_ASYNC_INT signal after it is masked. 0: No interrupt 1: The interrupt occurred (when interrupt masking is disabled)
SDI1_ASYNC_INT	R	5	0	Indicates the status of the SDI1_ASYNC_INT signal after it is masked. 0: No interrupt 1: The interrupt occurred (when interrupt masking is disabled)
SDI0_ASYNC_INT	R	4	0	Indicates the status of the SDI0_ASYNC_INT signal after it is masked. 0: No interrupt 1: The interrupt occurred (when interrupt masking is disabled)
SDC_ASYNC_INT_MASK	R/W	3	1	Specify whether to mask the SDC_ASYNC_INT signal. 0: Disable masking. 1: Mask the interrupt signal (default).
SDI2_ASYNC_INT_MASK	R/W	2	1	Specify whether to mask the SDI2_ASYNC_INT signal. 0: Disable masking. 1: Mask the interrupt signal (default).
SDI1_ASYNC_INT_MASK	R/W	1	1	Specify whether to mask the SDI1_ASYNC_INT signal. 0: Disable masking. 1: Mask the interrupt signal (default).
SDI0_ASYNC_INT_MASK	R/W	0	1	Specify whether to mask the SDI0_ASYNC_INT signal. 0: Disable masking. 1: Mask the interrupt signal (default).

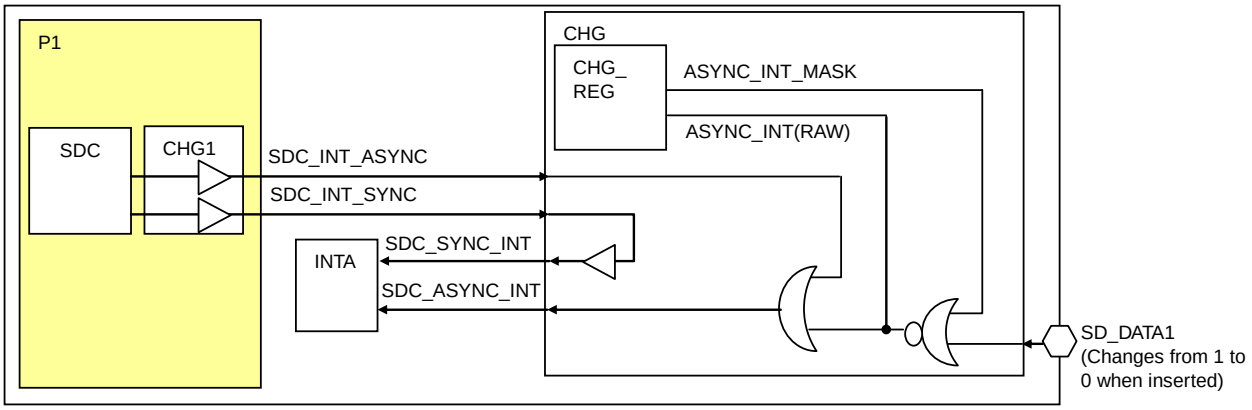
An interrupt signal sent from the external DATA1 pin is detected when the SDIO2 macro is in the reset state (or the power is off). Because this feature is assigned to two pins in the SDIO2 macro, the interrupt is masked using pin selection logic.



An interrupt signal sent from the external DATA1 pin is detected when the SDIO[1:0] macro is in the reset state (or the power is off). This mechanism is provided individually for SDIO0 and SDIO1.



An interrupt signal sent from the external DATA1 pin is detected when the SDC macro is in the reset state (or the power is off).



8.2.4 AB0 (ASYNC) boot switch register

This register (CHG_CTRL_AB0_BOOT: E014_0108H) enables target pin switching (from AB0 to another pin) if a macro is booted from the memory connected to AB0 (ASYNC). Before enabling the setting of the relevant bit, the desired setting must be specified for PINSEL in advance.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						MODE_VINI	VINI_INH

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
MODE_VINI	R	1	–	Indicates the boot mode selected by the BOOTSEL and UTEST bits of the CHG_BOOT_MODE register. 0: AB boot mode (NOR boot) 1: Other mode
VINI_INH	R/W	0	0	Select whether to enable GPIO selection. 0: Mask GPIO selection while in the AB boot mode. 1: Cancel masking of GPIO selection to enable GPIO selection.

8.2.5 1.8 V/3.3 V LCD enable register

This register (CHG_LCD_ENABLE: E014_0110H) specifies whether the 3.3 V LCD or 1.8 V LCD is enabled. After the system is booted up, be sure to clear the LCD18_EN bit to 0.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						LCD18_EN	LCD33_EN

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
LCD18_EN	R/W	1	1	Specify whether to enable the 1.8 V LCD. 0: Disable 1: Enable
LCD33_EN	R/W	0	1	Specify whether to enable the 3.3 V LCD. 0: Disable 1: Enable

8.2.6 GPIO[31:0] pin function selection register

This register (CHG_PINSEL_G000: E014_0200H) selects the GPIO_[31:0] pin functions.
Use the GPIO_[31:0] bits to select the functions of the GPIO_[31:0] pins.
Use the CHG_PINSEL_xx register to select the functions of macros other than GIO.
The setting of the CHG_PINSEL_Gxxx register takes precedence over the setting of the CHG_PINSEL_xxx register.
When using GIO of CHG_PINSEL_Gxxx_LCD33[x] and a terminal with mentioning for a PinSel_GIO section of appendix D, invalidate a terminal for the side which isn't used by CHG_LCD_ENABLE register.

31	30	29	28	27	26	25	24
GPIO_31	GPIO_30	GPIO_29	GPIO_28	GPIO_27	GPIO_26	GPIO_25	GPIO_24

23	22	21	20	19	18	17	16
GPIO_23	GPIO_22	GPIO_21	GPIO_20	GPIO_19	GPIO_18	GPIO_17	GPIO_16

15	14	13	12	11	10	9	8
GPIO_15	GPIO_14	GPIO_13	GPIO_12	GPIO_11	GPIO_10	GPIO_09	GPIO_08

7	6	5	4	3	2	1	0
GPIO_07	GPIO_06	GPIO_05	GPIO_04	GPIO_03	GPIO_02	GPIO_01	GPIO_00

Name	R/W	Bit No.	After Reset	Description
GPIO_[31:0]	R/W	31:0	FFFF_FFFBH	Select the pin functions. 0: Select the functions other than those of GPIO. 1: Select the GPIO functions.

8.2.7 GPIO[63:48] pin function selection register

This register (CHG_PINSEL_G032: E014_0204H) selects the GPIO_[63:32] pin functions.
Use the GPIO_[63:32] bits to select the functions of the GPIO_[63:32] pins.
Use the CHG_PINSEL_xxx register to select the functions of macros other than GIO.
The setting of the CHG_PINSEL_Gxxx register takes precedence over the setting of the CHG_PINSEL_xxx register.

31	30	29	28	27	26	25	24
GPIO_63	GPIO_62	GPIO_61	GPIO_60	GPIO_59	GPIO_58	GPIO_57	GPIO_56

23	22	21	20	19	18	17	16
GPIO_55	GPIO_54	GPIO_53	GPIO_52	GPIO_51	GPIO_50	GPIO_49	GPIO_48

15	14	13	12	11	10	9	8
GPIO_47	GPIO_46	GPIO_45	GPIO_44	GPIO_43	GPIO_42	GPIO_41	GPIO_40

7	6	5	4	3	2	1	0
GPIO_39	GPIO_38	GPIO_37	GPIO_36	GPIO_35	GPIO_34	GPIO_33	GPIO_32

Name	R/W	Bit No.	After Reset	Description
GPIO_[63:32]	R/W	31:0	3E06_0FFFH	Select the pin functions. 0: Select the functions other than those of GPIO. 1: Select the GPIO functions.

8.2.8 GPIO[95:64] pin function selection register

This register (CHG_PINSEL_G064: E014_0208H) selects the GPIO_[95:64] pin functions.
Use the GPIO_[95:64] bits to select the functions of the GPIO_[95:64] pins.
Use the CHG_PINSEL_xxx register to select the functions of macros other than GIO.
The setting of the CHG_PINSEL_Gxxx register takes precedence over the setting of the CHG_PINSEL_xxx register.

31	30	29	28	27	26	25	24
GPIO_9 5	GPIO_94	GPIO_93	GPIO_92	GPIO_91	GPIO_90	GPIO_89	GPIO_ 88

23	22	21	20	19	18	17	16
GPIO_87	GPIO_86	GPIO_85	GPIO_84	GPIO_83	GPIO _82	GPIO_81	GPIO_80

15	14	13	12	11	10	9	8
GPIO_79	GPIO_78	GPIO_77	GPIO_76	GPIO_75	GPIO_74	GPIO_73	GPIO_72

7	6	5	4	3	2	1	0
GPIO_71	GPIO_70	GPIO_69	GPIO_68	GPIO_67	GPIO_66	GPIO_65	GPIO_64

Name	R/W	Bit No.	After Reset	Description
GPIO_[95:64]	R/W	31:0	FFFF_FFFH	Select the pin functions. 0: Select the functions other than those of GPIO. 1: Select the GPIO functions.

8.2.9 GPIO[127:96] pin function selection register

This register (CHG_PINSEL_G096: E014_020CH) selects the GPIO_[127:96] pin functions.
Use the GPIO_[127:96] bits to select the functions of the GPIO_[127:96] pins.
Use the CHG_PINSEL_xxx register to select the functions of macros other than GIO.
The setting of the CHG_PINSEL_Gxxx register takes precedence over the setting of the CHG_PINSEL_xxx register.

31	30	29	28	27	26	25	24
GPIO_127	GPIO_126	GPIO_125	GPIO_124	GPIO_123	GPIO_122	GPIO_121	GPIO_120

23	22	21	20	19	18	17	16
GPIO_119	GPIO_118	GPIO_117	GPIO_116	GPIO_115	GPIO_114	GPIO_113	GPIO_112

15	14	13	12	11	10	9	8
GPIO_111	GPIO_110	GPIO_109	GPIO_108	GPIO_107	GPIO_106	GPIO_105	GPIO_104

7	6	5	4	3	2	1	0
GPIO_103	GPIO_102	GPIO_101	GPIO_100	GPIO_99	GPIO_98	GPIO_97	GPIO_96

Name	R/W	Bit No.	After Reset	Description
GPIO_[127:96]	R/W	31:0	FFFE_07FFH	Select the pin functions. 0: Select the functions other than those of GPIO. 1: Select the GPIO functions.

8.2.10 GPIO[158:128] pin function selection register

This register (CHG_PINSEL_G128: E014_0210H) selects the GPIO_[158:128] pin functions.
Use the GPIO_[158:128] bits to select the functions of the GPIO_[158:128] pins.
Use the CHG_PINSEL_xxx register to select the functions of macros other than GIO.
The setting of the CHG_PINSEL_Gxxx register takes precedence over the setting of the CHG_PINSEL_xxx register.

31	30	29	28	27	26	25	24
Reserved	GPIO_158	GPIO_157	GPIO_156	GPIO_155	GPIO_154	GPIO_153	GPIO_152

23	22	21	20	19	18	17	16
GPIO_151	GPIO_150	GPIO_149	GPIO_148	GPIO_147	GPIO_146	GPIO_145	GPIO_144

15	14	13	12	11	10	9	8
GPIO_143	GPIO_142	GPIO_141	GPIO_140	GPIO_139	GPIO_138	GPIO_137	GPIO_136

7	6	5	4	3	2	1	0
GPIO_135	GPIO_134	GPIO_133	GPIO_132	GPIO_131	GPIO_130	GPIO_129	GPIO_128

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31	–	Reserved. If this bit is read, 0 is returned.
GPIO_[158:128]	R/W	30:0	787F_FFFFH	Select the pin functions. 0: Select the functions other than those of GPIO. 1: Select the GPIO functions.

8.2.11 3.3 V LCD pin function selection register

This register (CHG_PINSEL_LCD3: E014_0284H) selects the 3.3 V LCD pin functions.
When the CHG_PINSEL_G*xxx* register is cleared to 0 (to select functions other than those of GPIO), set up the CHG_PINSEL_*xxx* register to select the pin functions in mode 0 to mode 2.
The setting of the CHG_PINSEL_G*xxx* register takes precedence over the setting of the CHG_PINSEL_*xxx* register.
When using the pin functions in mode 0 to mode 2, select functions other than those of GIO by using the CHG_PINSEL_G*xxx* register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved				CHG_PINSEL_LCD3[11:10]		CHG_PINSEL_LCD3[9:8]	

7	6	5	4	3	2	1	0
CHG_PINSEL_LCD3 [7:6]		CHG_PINSEL_LCD3 [5:4]		CHG_PINSEL_LCD3 [3:2]		CHG_PINSEL_LCD3 [1:0]	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:12	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_PINSEL_ LCD3	R/W	11:0	00b	Select the mode for the 3.3 V LCD pin functions by using 2 bits. 00: Select the pin function in mode 0. 01: Select the pin function in mode 1. 10: Select the pin function in mode 2. 11: Unused.

Remark For details about switching the multi-function pins, see **2.3 Pin Multiplex Function** or **APPEDIX D SIGNAL PINS**.

8.2.12 UART pin function selection register

This register (CHG_PINSEL_UART: E014_0288H) selects the UART pin functions.
The setting of the CHG_PINSEL_G*xxx* register takes precedence over the setting of the CHG_PINSEL_*xxx* register.
When using the pin functions in mode 0 to mode 1, select functions other than those of GIO by using the CHG_PINSEL_G*xxx* register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						CHG_PINSEL_UART[1:0]	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_PINSEL_ UART	R/W	1:0	00b	Select the mode for the UART pin functions by using 2 bits. 00: Select the pin function in mode 0. 01: Select the pin function in mode 1. 10: Unused 11: Unused

Remark For details about switching the multi-function pins, see **2.3 Pin Multiplex Function** or **APPEDIX D SIGNAL PINS**.

8.2.13 IIC pin function selection register

This register (CHG_PINSEL_IIC: E014_028CH) selects the IIC pin functions.

The setting of the CHG_PINSEL_G*xxx* register takes precedence over the setting of the CHG_PINSEL_*xxx* register.

When using the pin functions in mode 0 to mode 1, select functions other than those of GIO by using the CHG_PINSEL_G*xxx* register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						CHG_PINSEL_IIC[1:0]	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_PINSEL_IIC	R/W	1:0	00b	Select the mode for the IIC pin functions by using 2 bits. 00: Select the pin function in mode 0. 01: Select the pin function in mode 1. 10: Unused 11: Unused

Remark For details about switching the multi-function pins, see **2.3 Pin Multiplex Function** or **APPEDIX D SIGNAL PINS**.

8.2.14 AB pin function selection register

This register (CHG_PINSEL_AB: E014_0294H) selects the AB pin functions.

The setting of the CHG_PINSEL_G*xxx* register takes precedence over the setting of the CHG_PINSEL_*xxx* register.

When using the pin functions in mode 0 to mode 3, select functions other than those of GIO by using the CHG_PINSEL_G*xxx* register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
CHG_PINSEL_AB[15:14]		CHG_PINSEL_AB[13:12]		CHG_PINSEL_AB[11:10]		CHG_PINSEL_AB[9:8]	

7	6	5	4	3	2	1	0
CHG_PINSEL_AB[7:6]		CHG_PINSEL_AB[5:4]		CHG_PINSEL_AB[3:2]		CHG_PINSEL_AB[1:0]	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_PINSEL_AB	R/W	15:0	00b	Select the mode for the AB pin functions by using 2 bits. 00: Select the pin function in mode 0. 01: Select the pin function in mode 1. 10: Select the pin function in mode 2. 11: Select the pin function in mode 3.

Remark For details about switching the multi-function pins, see **2.3 Pin Multiplex Function** or **APPEDIX D SIGNAL PINS**.

8.2.15 USI pin function selection register

This register (CHG_PINSEL_USI: E014_0298H) selects the USI pin functions.

The setting of the CHG_PINSEL_G*xxx* register takes precedence over the setting of the CHG_PINSEL_*xxx* register.

When using the pin functions in mode 0 to mode 1, select functions other than those of GIO by using the CHG_PINSEL_G*xxx* register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved						CHG_PINSEL_USI[9:8]	

7	6	5	4	3	2	1	0
CHG_PINSEL_USI[7:6]		CHG_PINSEL_USI[5:4]		CHG_PINSEL_USI[3:2]		CHG_PINSEL_USI[1:0]	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:10	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_PINSEL_USI	R/W	9:0	00b	Select the mode for the USI pin functions by using 2 bits. 00: Select the pin function in mode 0. 01: Select the pin function in mode 1. 10: Unused 11: Unused

Remark For details about switching the multi-function pins, see **2.3 Pin Multiplex Function** or **APPEDIX D SIGNAL PINS**.

8.2.16 HSI pin function selection register

This register (CHG_PINSEL_USI: E014_02A8H) selects the HSI pin functions.

The setting of the CHG_PINSEL_G*xxx* register takes precedence over the setting of the CHG_PINSEL_*xxx* register.

When using the pin functions in mode 0 to mode 1, select functions other than those of GIO by using the CHG_PINSEL_G*xxx* register.

The HSI function is not available.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						CHG_PINSEL_HSI[1:0]	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_PINSEL_HSI	R/W	1:0	00b	Select the mode for the HSI pin functions by using 2 bits. 00: Select the pin function in mode 0. 01: Select the pin function in mode 1. 10: Unused 11: Unused

Remark For details about switching the multi-function pins, see **2.3 Pin Multiplex Function** or **APPEDIX D SIGNAL PINS**.

8.2.17 Pull-up/pull-down/input enable/Schmitt trigger control register 0

This register (CHG_PULL0: E014_0300H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_025_SMT	G_025_CTL	G_025_UDC1	G_025_UDC0	G_024_SMT	G_024_CTL	G_024_UDC1	G_024_UDC0

23	22	21	20	19	18	17	16
G_023_SMT	G_023_CTL	G_023_UDC1	G_023_UDC0	G_022_SMT	G_022_CTL	G_022_UDC1	G_022_UDC0

15	14	13	12	11	10	9	8
G_021_SMT	G_021_CTL	G_021_UDC1	G_021_UDC0	G_020_SMT	G_020_CTL	G_020_UDC1	G_020_UDC0

7	6	5	4	3	2	1	0
G_019_SMT	G_019_CTL	G_019_UDC1	G_019_UDC0	G_018_SMT	G_018_CTL	G_018_UDC1	G_018_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.18 Pull-up/pull-down/input enable/Schmitt trigger control register 1

This register (CHG_PULL1: E014_0304H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_033_SMT	G_033_CTL	G_033_UDC1	G_033_UDC0	G_032_SMT	G_032_CTL	G_032_UDC1	G_032_UDC0

23	22	21	20	19	18	17	16
G_031_SMT	G_031_CTL	G_031_UDC1	G_031_UDC0	G_030_SMT	G_030_CTL	G_030_UDC1	G_030_UDC0

15	14	13	12	11	10	9	8
G_029_SMT	G_029_CTL	G_029_UDC1	G_029_UDC0	G_028_SMT	G_028_CTL	G_028_UDC1	G_028_UDC0

7	6	5	4	3	2	1	0
G_027_SMT	G_027_CTL	G_027_UDC1	G_027_UDC0	G_026_SMT	G_026_CTL	G_026_UDC1	G_026_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	3300_0003H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.19 Pull-up/pull-down/input enable/Schmitt trigger control register 2

This register (CHG_PULL2: E014_0308H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_041_SMT	G_041_CTL	G_041_UDC1	G_041_UDC0	G_040_SMT	G_040_CTL	G_040_UDC1	G_040_UDC0

23	22	21	20	19	18	17	16
G_039_SMT	G_039_CTL	G_039_UDC1	G_039_UDC0	G_038_SMT	G_038_CTL	G_038_UDC1	G_038_UDC0

15	14	13	12	11	10	9	8
G_037_SMT	G_037_CTL	G_037_UDC1	G_037_UDC0	G_036_SMT	G_036_CTL	G_036_UDC1	G_036_UDC0

7	6	5	4	3	2	1	0
G_035_SMT	G_035_CTL	G_035_UDC1	G_035_UDC0	G_034_SMT	G_034_CTL	G_034_UDC1	G_034_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.20 Pull-up/pull-down/input enable/Schmitt trigger control register 3

This register (CHG_PULL3: E014_030CH) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_047_SMT	G_047_CTL	G_047_UDC1	G_047_UDC0	G_046_SMT	G_046_CTL	G_046_UDC1	G_046_UDC0

23	22	21	20	19	18	17	16
G_045_SMT	G_045_CTL	G_045_UDC1	G_045_UDC0	G_044_SMT	G_044_CTL	G_044_UDC1	G_044_UDC0

15	14	13	12	11	10	9	8
Reserved				UART0_SMT	UART0_CTL	UART0_UDC1	UART0_UDC0

7	6	5	4	3	2	1	0
G_043_SMT	G_043_CTL	G_043_UDC1	G_043_UDC0	G_042_SMT	G_042_CTL	G_042_UDC1	G_042_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 11, 7, 3	0000_0333H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable
Reserved	R	15:12	–	Reserved. If these bits are read, 0 is returned for each bit.

8.2.21 Pull-up/pull-down/input enable/Schmitt trigger control register 4

This register (CHG_PULL4: E014_0310H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
Reserved				G_052_SMT	G_052_CTL	G_052_UDC1	G_052_UDC0

23	22	21	20	19	18	17	16
G_051_SMT	G_051_CTL	G_051_UDC1	G_051_UDC0	G_050_SMT	G_050_CTL	G_050_UDC1	G_050_UDC0

15	14	13	12	11	10	9	8
G_049_SMT	G_049_CTL	G_049_UDC1	G_049_UDC0	SD_D_SMT	SD_D_CTL	SD_D_UDC1	SD_D_UDC0

7	6	5	4	3	2	1	0
SD_CM_SMT	SD_CM_CTL	SD_CM_UDC1	SD_CM_UDC0	G_048_SMT	G_048_CTL	G_048_UDC1	G_048_UDC0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	27, 23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	26, 22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	25, 21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	24, 20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.22 Pull-up/pull-down/input enable/Schmitt trigger control register 5

This register (CHG_PULL5: E014_0314H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_060_SMT	G_060_CTL	G_060_UDC1	G_060_UDC0	G_059_SMT	G_059_CTL	G_059_UDC1	G_059_UDC0

23	22	21	20	19	18	17	16
G_058_SMT	G_058_CTL	G_058_UDC1	G_058_UDC0	G_057_SMT	G_057_CTL	G_057_UDC1	G_057_UDC0

15	14	13	12	11	10	9	8
G_056_SMT	G_056_CTL	G_056_UDC1	G_056_UDC0	G_055_SMT	G_055_CTL	G_055_UDC1	G_055_UDC0

7	6	5	4	3	2	1	0
G_054_SMT	G_054_CTL	G_054_UDC1	G_054_UDC0	G_053_SMT	G_053_CTL	G_053_UDC1	G_053_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.23 Pull-up/pull-down/input enable/Schmitt trigger control register 6

This register (CHG_PULL6: E014_0318H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
Reserved				G_067_SMT	G_067_CTL	G_067_UDC1	G_067_UDC0

23	22	21	20	19	18	17	16
G_066_SMT	G_066_CTL	G_066_UDC1	G_066_UDC0	G_065_SMT	G_065_CTL	G_065_UDC1	G_065_UDC0

15	14	13	12	11	10	9	8
G_064_SMT	G_064_CTL	G_064_UDC1	G_064_UDC0	G_063_SMT	G_063_CTL	G_063_UDC1	G_063_UDC0

7	6	5	4	3	2	1	0
G_062_SMT	G_062_CTL	G_062_UDC1	G_062_UDC0	G_061_SMT	G_061_CTL	G_061_UDC1	G_061_UDC0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	27, 23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	26, 22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	25, 21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	24, 20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.24 Pull-up/pull-down/input enable/Schmitt trigger control register 7

This register (CHG_PULL7: E014_031CH) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_075_SMT	G_075_CTL	G_075_UDC1	G_075_UDC0	G_074_SMT	G_074_CTL	G_074_UDC1	G_074_UDC0

23	22	21	20	19	18	17	16
G_073_SMT	G_073_CTL	G_073_UDC1	G_073_UDC0	G_072_SMT	G_072_CTL	G_072_UDC1	G_072_UDC0

15	14	13	12	11	10	9	8
G_071_SMT	G_071_CTL	G_071_UDC1	G_071_UDC0	G_070_SMT	G_070_CTL	G_070_UDC1	G_070_UDC0

7	6	5	4	3	2	1	0
G_069_SMT	G_069_CTL	G_069_UDC1	G_069_UDC0	G_068_SMT	G_068_CTL	G_068_UDC1	G_068_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	0000_0113H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.25 Pull-up/pull-down/input enable/Schmitt trigger control register 8

This register (CHG_PULL8: E014_0320H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_083_SMT	G_083_CTL	G_083_UDC1	G_083_UDC0	G_082_SMT	G_082_CTL	G_082_UDC1	G_082_UDC0

23	22	21	20	19	18	17	16
G_081_SMT	G_081_CTL	G_081_UDC1	G_081_UDC0	G_080_SMT	G_080_CTL	G_080_UDC1	G_080_UDC0

15	14	13	12	11	10	9	8
G_079_SMT	G_079_CTL	G_079_UDC1	G_079_UDC0	G_078_SMT	G_078_CTL	G_078_UDC1	G_078_UDC0

7	6	5	4	3	2	1	0
G_077_SMT	G_077_CTL	G_077_UDC1	G_077_UDC0	G_076_SMT	G_076_CTL	G_076_UDC1	G_076_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	7777_7770H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.26 Pull-up/pull-down/input enable/Schmitt trigger control register 9

This register (CHG_PULL9: E014_0324H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_091_SMT	G_091_CTL	G_091_UDC1	G_091_UDC0	G_090_SMT	G_090_CTL	G_090_UDC1	G_090_UDC0

23	22	21	20	19	18	17	16
G_089_SMT	G_089_CTL	G_089_UDC1	G_089_UDC0	G_088_SMT	G_088_CTL	G_088_UDC1	G_088_UDC0

15	14	13	12	11	10	9	8
G_087_SMT	G_087_CTL	G_087_UDC1	G_087_UDC0	G_086_SMT	G_086_CTL	G_086_UDC1	G_086_UDC0

7	6	5	4	3	2	1	0
G_085_SMT	G_085_CTL	G_085_UDC1	G_085_UDC0	G_084_SMT	G_084_CTL	G_084_UDC1	G_084_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2	1	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.27 Pull-up/pull-down/input enable/Schmitt trigger control register 10

This register (CHG_PULL10: E014_0328H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_099_SMT	G_099_CTL	G_099_UDC1	G_099_UDC0	G_098_SMT	G_098_CTL	G_098_UDC1	G_098_UDC0

23	22	21	20	19	18	17	16
G_097_SMT	G_097_CTL	G_097_UDC1	G_097_UDC0	G_096_SMT	G_096_CTL	G_096_UDC1	G_096_UDC0

15	14	13	12	11	10	9	8
G_095_SMT	G_095_CTL	G_095_UDC1	G_095_UDC0	G_094_SMT	G_094_CTL	G_094_UDC1	G_094_UDC0

7	6	5	4	3	2	1	0
G_093_SMT	G_093_CTL	G_093_UDC1	G_093_UDC0	G_092_SMT	G_092_CTL	G_092_UDC1	G_092_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	0000_3337H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.28 Pull-up/pull-down/input enable/Schmitt trigger control register 11

This register (CHG_PULL11: E014_032CH) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved				G_104_SMT	G_104_CTL	G_104_UDC1	G_104_UDC0

15	14	13	12	11	10	9	8
G_103_SMT	G_103_CTL	G_103_UDC1	G_103_UDC0	G_102_SMT	G_102_CTL	G_102_UDC1	G_102_UDC0

7	6	5	4	3	2	1	0
G_101_SMT	G_101_CTL	G_101_UDC1	G_101_UDC0	G_100_SMT	G_100_CTL	G_100_UDC1	G_100_UDC0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:20	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	17, 13, 9, 5, 1	0	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	16, 12, 8, 4, 0	0	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.29 Pull-up/pull-down/input enable/Schmitt trigger control register 12

This register (CHG_PULL12: E014_0330H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
G_106_SMT	G_106_CTL	G_106_UDC1	G_106_UDC0	G_105_SMT	G_105_CTL	G_105_UDC1	G_105_UDC0

15	14	13	12	11	10	9	8
USI0_CS0_SMT	USI0_CS0_CTL	USI0_CS0_UDC1	USI0_CS0_UDC0	USI0_DO_SMT	USI0_DO_CTL	USI0_DO_UDC1	USI0_DO_UDC0

7	6	5	4	3	2	1	0
USI0_DI_SMT	USI0_DI_CTL	USI0_DI_UDC1	USI0_DI_UDC0	USI0_CK_SMT	USI0_CK_CTL	USI0_CK_UDC1	USI0_CK_UDC0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:24	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.30 Pull-up/pull-down/input enable/Schmitt trigger control register 13

This register (CHG_PULL13: E014_0334H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_009_SMT	G_009_CTL	G_009_UDC1	G_009_UDC0	G_008_SMT	G_008_CTL	G_008_UDC1	G_008_UDC0

23	22	21	20	19	18	17	16
G_007_SMT	G_007_CTL	G_007_UDC1	G_007_UDC0	G_006_SMT	G_006_CTL	G_006_UDC1	G_006_UDC0

15	14	13	12	11	10	9	8
USI1_CS0_SMT	USI1_CS0_CTL	USI1_CS0_UDC1	USI1_CS0_UDC0	G_108_SMT	G_108_CTL	G_108_UDC1	G_108_UDC0

7	6	5	4	3	2	1	0
G_107_SMT	G_107_CTL	G_107_UDC1	G_107_UDC0	USI1_CK_SMT	USI1_CK_CTL	USI1_CK_UDC1	USI1_CK_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	3003_3333H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.31 Pull-up/pull-down/input enable/Schmitt trigger control register 14

This register (CHG_PULL14: E014_0338H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_017_SMT	G_017_CTL	G_017_UDC1	G_017_UDC0	G_016_SMT	G_016_CTL	G_016_UDC1	G_016_UDC0

23	22	21	20	19	18	17	16
G_015_SMT	G_015_CTL	G_015_UDC1	G_015_UDC0	G_014_SMT	G_014_CTL	G_014_UDC1	G_014_UDC0

15	14	13	12	11	10	9	8
G_013_SMT	G_013_CTL	G_013_UDC1	G_013_UDC0	G_012_SMT	G_012_CTL	G_012_UDC1	G_012_UDC0

7	6	5	4	3	2	1	0
G_011_SMT	G_011_CTL	G_011_UDC1	G_011_UDC0	G_010_SMT	G_010_CTL	G_010_UDC1	G_010_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	3003_3003H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.32 Pull-up/pull-down/input enable/Schmitt trigger control register 15

This register (CHG_PULL15: E014_033CH) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
G_114_SMT	G_114_CTL	G_114_UDC1	G_114_UDC0	G_113_SMT	G_113_CTL	G_113_UDC1	G_113_UDC0

15	14	13	12	11	10	9	8
G_112_SMT	G_112_CTL	G_112_UDC1	G_112_UDC0	G_111_SMT	G_111_CTL	G_111_UDC1	G_111_UDC0

7	6	5	4	3	2	1	0
G_110_SMT	G_110_CTL	G_110_UDC1	G_110_UDC0	G_109_SMT	G_109_CTL	G_109_UDC1	G_109_UDC0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:24	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.33 Pull-up/pull-down/input enable/Schmitt trigger control register 16

This register (CHG_PULL16: E014_0340H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
Reserved				G_121_SMT	G_121_CTL	G_121_UDC1	G_121_UDC0

23	22	21	20	19	18	17	16
G_120_SMT	G_120_CTL	G_120_UDC1	G_120_UDC0	G_119_SMT	G_119_CTL	G_119_UDC1	G_119_UDC0

15	14	13	12	11	10	9	8
G_118_SMT	G_118_CTL	G_118_UDC1	G_118_UDC0	G_117_SMT	G_117_CTL	G_117_UDC1	G_117_UDC0

7	6	5	4	3	2	1	0
G_116_SMT	G_116_CTL	G_116_UDC1	G_116_UDC0	G_115_SMT	G_115_CTL	G_115_UDC1	G_115_UDC0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	27, 23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	26, 22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	25, 21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	24, 20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.34 Pull-up/pull-down/input enable/Schmitt trigger control register 17

This register (CHG_PULL17: E014_0344H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved				G_126_SMT	G_126_CTL	G_126_UDC1	G_126_UDC0

15	14	13	12	11	10	9	8
G_125_SMT	G_125_CTL	G_125_UDC1	G_125_UDC0	G_124_SMT	G_124_CTL	G_124_UDC1	G_124_UDC0

7	6	5	4	3	2	1	0
G_123_SMT	G_123_CTL	G_123_UDC1	G_123_UDC0	G_122_SMT	G_122_CTL	G_122_UDC1	G_122_UDC0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:20	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.35 Pull-up/pull-down/input enable/Schmitt trigger control register 18

This register (CHG_PULL18: E014_0348H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_134_SMT	G_134_CTL	G_134_UDC1	G_134_UDC0	G_133_SMT	G_133_CTL	G_133_UDC1	G_133_UDC0

23	22	21	20	19	18	17	16
G_132_SMT	G_132_CTL	G_132_UDC1	G_132_UDC0	G_131_SMT	G_131_CTL	G_131_UDC1	G_131_UDC0

15	14	13	12	11	10	9	8
G_130_SMT	G_130_CTL	G_130_UDC1	G_130_UDC0	G_129_SMT	G_129_CTL	G_129_UDC1	G_129_UDC0

7	6	5	4	3	2	1	0
G_128_SMT	G_128_CTL	G_128_UDC1	G_128_UDC0	G_127_SMT	G_127_CTL	G_127_UDC1	G_127_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	3003_0033H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.36 Pull-up/pull-down/input enable/Schmitt trigger control register 19

This register (CHG_PULL19: E014_034CH) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_142_SMT	G_142_CTL	G_142_UDC1	G_142_UDC0	G_141_SMT	G_141_CTL	G_141_UDC1	G_141_UDC0

23	22	21	20	19	18	17	16
G_140_SMT	G_140_CTL	G_140_UDC1	G_140_UDC0	G_139_SMT	G_139_CTL	G_139_UDC1	G_139_UDC0

15	14	13	12	11	10	9	8
G_138_SMT	G_138_CTL	G_138_UDC1	G_138_UDC0	G_137_SMT	G_137_CTL	G_137_UDC1	G_137_UDC0

7	6	5	4	3	2	1	0
G_136_SMT	G_136_CTL	G_136_UDC1	G_136_UDC0	G_135_SMT	G_135_CTL	G_135_UDC1	G_135_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.37 Pull-up/pull-down/input enable/Schmitt trigger control register 20

This register (CHG_PULL20: E014_0350H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
Reserved				G_154_SMT	G_154_CTL	G_154_UDC1	G_154_UDC0

23	22	21	20	19	18	17	16
G_005_SMT	G_005_CTL	G_005_UDC1	G_005_UDC0	G_004_SMT	G_004_CTL	G_004_UDC1	G_004_UDC0

15	14	13	12	11	10	9	8
G_003_SMT	G_003_CTL	G_003_UDC1	G_003_UDC0	G_002_SMT	G_002_CTL	G_002_UDC1	G_002_UDC0

7	6	5	4	3	2	1	0
G_001_SMT	G_001_CTL	G_001_UDC1	G_001_UDC0	G_000_SMT	G_000_CTL	G_000_UDC1	G_000_UDC0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	27, 23, 19, 15, 11, 7, 3	00B3_3733H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	26, 22, 18, 14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	25, 21, 17, 13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	24, 20, 16, 12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.38 Pull-up/pull-down/input enable/Schmitt trigger control register 21

This register (CHG_PULL21: E014_0354H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_150_SMT	G_150_CTL	G_150_UDC1	G_150_UDC0	G_149_SMT	G_149_CTL	G_149_UDC1	G_149_UDC0

23	22	21	20	19	18	17	16
G_148_SMT	G_148_CTL	G_148_UDC1	G_148_UDC0	G_147_SMT	G_147_CTL	G_147_UDC1	G_147_UDC0

15	14	13	12	11	10	9	8
G_146_SMT	G_146_CTL	G_146_UDC1	G_146_UDC0	G_145_SMT	G_145_CTL	G_145_UDC1	G_145_UDC0

7	6	5	4	3	2	1	0
G_144_SMT	G_144_CTL	G_144_UDC1	G_144_UDC0	G_143_SMT	G_143_CTL	G_143_UDC1	G_143_UDC0

Name	R/W	Bit No.	After Reset	Description
*xxx*_SMT	R/W	31, 27, 23, 19, 15, 11, 7, 3	0	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 26, 22, 18, 14, 10, 6, 2	0	Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 25, 21, 17, 13, 9, 5, 1	1	Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 24, 20, 16, 12, 8, 4, 0	1	Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.39 Pull-up/pull-down/input enable/Schmitt trigger control register 22

This register (CHG_PULL22: E014_0358H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
G_153_SMT	G_153_CTL	G_153_UDC1	G_153_UDC0	Reserved			

23	22	21	20	19	18	17	16
JT_DEN_SMT	JT_DEN_CTL	JT_DEN_ UDC1	JT_DEN_ UDC0	G_152_SMT	G_152_CTL	G_152_UDC1	G_152_UDC0

15	14	13	12	11	10	9	8
JT_RST_ SMT	JT_RST_ CTL	JT_RST_ UDC1	JT_RST_ UDC0	G_151_SMT	G_151_CTL	G_151_UDC1	G_151_UDC0

7	6	5	4	3	2	1	0
JT_SMT	JT_CTL	JT_UDC1	JT_UDC0	Reserved			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	27:24	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	31, 23, 19, 15, 11, 7, 3	0FF0_F0D0H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	30, 22, 18, 14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	29, 21, 17, 13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	28, 20, 16, 12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable
Reserved	R	3:0	–	Reserved. If these bits are read, 0 is returned for each bit.

8.2.40 Pull-up/pull-down/input enable/Schmitt trigger control register 25

This register (CHG_PULL25: E014_0364H) sets up pulling up, pulling down, input enabling, and Schmitt control for pins in 4-bit units.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
G_158_SMT	G_158_CTL	G_158_UDC1	G_158_UDC0	G_157_SMT	G_157_CTL	G_157_UDC1	G_157_UDC0

7	6	5	4	3	2	1	0
G_156_SMT	G_156_CTL	G_156_UDC1	G_156_UDC0	G_155_SMT	G_155_CTL	G_155_UDC1	G_155_UDC0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
*xxx*_SMT	R/W	15, 11, 7, 3	0303H	Specify whether to use a Schmitt trigger. 0: Do not use a Schmitt trigger (normal input). 1: Use a Schmitt trigger.
*xxx*_CTL	R/W	14, 10, 6, 2		Specify whether to enable input to pins. 0: Mask input. 1: Enable input.
*xxx*_UDC1	R/W	13, 9, 5, 1		Specify whether to pull pins up or down. 0: Pull up, 1: Pull down
*xxx*_UDC0	R/W	12, 8, 4, 0		Specify whether to enable specifying the pin pull-up or pull-down setting. 0: Disable, 1: Enable

8.2.41 Driving capability selection register 0

This register (CHG_DRIVE0: E014_0400H) selects the IO buffer driving capability for pins in 2-bit units.

31	30	29	28	27	26	25	24
LCD_15[1:0]		LCD_14[1:0]		LCD_13[1:0]		LCD_12[1:0]	

23	22	21	20	19	18	17	16
LCD_11[1:0]		LCD_10[1:0]		LCD_9[1:0]		LCD_8[1:0]	

15	14	13	12	11	10	9	8
LCD_7[1:0]		LCD_6[1:0]		LCD_5[1:0]		LCD_4[1:0]	

7	6	5	4	3	2	1	0
LCD_3[1:0]		LCD_2[1:0]		Reserved			

Name	R/W	Bit No.	After Reset	Description
LCD_15[1:0]	R/W	31:30	00b	Select the driving capability.
LCD_14[1:0]	R/W	29:28	00b	00: 4 mA (initial value)
LCD_13[1:0]	R/W	27:26	00b	01: 6 mA
LCD_12[1:0]	R/W	25:24	00b	10: 8 mA
LCD_11[1:0]	R/W	23:22	00b	11: 12 mA
LCD_10[1:0]	R/W	21:20	00b	
LCD_9[1:0]	R/W	19:18	00b	
LCD_8[1:0]	R/W	17:16	00b	
LCD_7[1:0]	R/W	15:14	00b	
LCD_6[1:0]	R/W	13:12	00b	
LCD_5[1:0]	R/W	11:10	00b	
LCD_4[1:0]	R/W	9:8	00b	
LCD_3[1:0]	R/W	7:6	00b	
LCD_2[1:0]	R/W	5:4	00b	
Reserved	R	3:0	–	Reserved. If these bits are read, 0 is returned for each bit.

8.2.42 Driving capability selection register 1

This register (CHG_DRIVE1: E014_0404H) selects the IO buffer driving capability for pins in 2-bit units.

31	30	29	28	27	26	25	24
SD_1[1:0]		SD_0[1:0]		IIC1[1:0]		IIC0[1:0]	

23	22	21	20	19	18	17	16
Reserved				SDI1_1[1:0]		SDI1_0[1:0]	

15	14	13	12	11	10	9	8
SDI0_2[1:0]		SDI0_1[1:0]		SDI0_0[1:0]		LCD_20[1:0]	

7	6	5	4	3	2	1	0
LCD_19[1:0]		LCD_18[1:0]		LCD_17[1:0]		LCD_16[1:0]	

Name	R/W	Bit No.	After Reset	Description
SD_1[1:0]	R/W	31:30	00b	Select the driving capability.
SD_0[1:0]	R/W	29:28	00b	00: 4 mA (initial value)
IIC1[1:0]	R/W	27:26	00b	01: 6 mA
IIC0[1:0]	R/W	25:24	00b	10: 8 mA 11: 12 mA
Reserved	R	23:20	–	Reserved. If these bits are read, 0 is returned for each bit.
SDI1_1[1:0]	R/W	19:18	00b	Select the driving capability.
SDI1_0[1:0]	R/W	17:16	00b	00: 4 mA (initial value)
SDI0_2[1:0]	R/2	15:14	00b	01: 6 mA
SDI0_1[1:0]	R/W	13:12	00b	10: 8 mA
SDI0_0[1:0]	R/W	11:10	00b	11: 12 mA
LCD_20[1:0]	R/W	9:8	00b	
LCD_19[1:0]	R/W	7:6	00b	
LCD_18[1:0]	R/W	5:4	00b	
LCD_17[1:0]	R/W	3:2	00b	
LCD_16[1:0]	R/W	1:0	00b	

8.2.43 Driving capability selection register 2

This register (CHG_DRIVE2: E014_0408H) selects the IO buffer driving capability for pins in 2-bit units.

31 30	29 28	27 26	25 24
AB_15[1:0]	AB_14[1:0]	AB_13[1:0]	AB_12[1:0]

23 22	21 20	19 18	17 16
AB_11[1:0]	AB_10[1:0]	AB_9[1:0]	AB8[1:0]

15 14	13 12	11 10	9 8
AB_7[1:0]	AB_6[1:0]	AB_5[1:0]	AB_4[1:0]

7 6	5 4	3 2	1 0
AB_3[1:0]	AB_21:0]	AB_1[1:0]	AB_0[1:0]

Name	R/W	Bit No.	After Reset	Description
AB_15[1:0]	R/W	31:30	10b	Select the driving capability.
AB_14[1:0]	R/W	29:28	10b	00: 4 mA (Initial value)
AB_13[1:0]	R/W	27:26	10b	01: 6 mA
AB_12[1:0]	R/W	25:24	10b	10: 8 mA
AB_11[1:0]	R/W	23:22	10b	11: 12 mA
AB_10[1:0]	R/W	21:20	10b	
AB_9[1:0]	R/W	19:18	10b	
AB_8[1:0]	R/W	17:16	10b	
AB_7[1:0]	R/W	15:14	10b	
AB_6[1:0]	R/W	13:12	10b	
AB_5[1:0]	R/W	11:10	10b	
AB_4[1:0]	R/W	9:8	10b	
AB_3[1:0]	R/W	7:6	00b	
AB_2[1:0]	R/W	5:4	10b	
AB_1[1:0]	R/W	3:2	10b	
AB_0[1:0]	R/W	1:0	10b	

8.2.44 Driving capability selection register 3

This register (CHG_DRIVE3: E014_040CH) selects the IO buffer driving capability for pins in 2-bit units.

31	30	29	28	27	26	25	24
Reserved				NTSC_1[1:0]		NTSC_0[1:0]	

23	22	21	20	19	18	17	16
PWM[1:0]		GPIO_0[1:0]		USI3_1[1:0]		USI3_0[1:0]	

15	14	13	12	11	10	9	8
USI2_3[1:0]		USI2_2[1:0]		USI2_1[1:0]		USI2_0[1:0]	

7	6	5	4	3	2	1	0
USI1_1[1:0]		USI1_0[1:0]		USI0_1[1:0]		USI0_0[1:0]	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
NTSC_1[1:0]	R/W	27:26	00b	Select the driving capability.
NTSC_0[1:0]	R/W	25:24	00b	00: 4 mA (initial value)
PWM[1:0]	R/W	23:22	00b	01: 6 mA
GPIO_0[1:0]	R/W	21:20	00b	10: 8 mA
USI3_1[1:0]	R/W	19:18	00b	11: 12 mA
USI3_0[1:0]	R/W	17:16	00b	
USI2_3[1:0]	R/W	15:14	00b	
USI2_2[1:0]	R/W	13:12	00b	
USI2_1[1:0]	R/W	11:10	00b	
USI2_0[1:0]	R/W	9:8	00b	
USI1_1[1:0]	R/W	7:6	00b	
USI1_0[1:0]	R/W	5:4	00b	
USI0_1[1:0]	R/W	3:2	00b	
USI0_0[1:0]	R/W	1:0	00b	

8.2.45 Driving capability selection register 4

This register (CHG_DRIVE4: E014_0410H) selects the IO buffer driving capability for pins in 2-bit units.

31	30	29	28	27	26	25	24
Reserved				GPIO_10[1:0]		GPIO_9[1:0]	

23	22	21	20	19	18	17	16
GPIO_8[1:0]		GPIO_7[1:0]		GPIO_6[1:0]		GPIO_5[1:0]	

15	14	13	12	11	10	9	8
GPIO_4[1:0]		GPIO_3[1:0]		GPIO_2[1:0]		GPIO_1[1:0]	

7	6	5	4	3	2	1	0
CAM_3[1:0]		CAM_2[1:0]		CAM_1[1:0]		CAM_0[1:0]	

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:28	–	Reserved. If these bits are read, 0 is returned for each bit.
GPIO_10[1:0]	R/W	27:26	00b	Select the driving capability.
GPIO_9[1:0]	R/W	25:24	00b	00: 4 mA (initial value)
GPIO_8[1:0]	R/W	23:22	00b	01: 6 mA
GPIO_7[1:0]	R/W	21:20	00b	10: 8 mA
GPIO_6[1:0]	R/W	19:18	00b	11: 12 mA
GPIO_5[1:0]	R/W	17:16	00b	
GPIO_4[1:0]	R/W	15:14	00b	
GPIO_3[1:0]	R/W	13:12	00b	
GPIO_2[1:0]	R/W	11:10	00b	
GPIO_1[1:0]	R/W	9:8	00b	
CAM_3[1:0]	R/W	7:6	00b	
CAM_2[1:0]	R/W	5:4	00b	
CAM_1[1:0]	R/W	3:2	00b	
CAM_0[1:0]	R/W	1:0	00b	

8.2.46 Driving capability selection register 5

This register (CHG_DRIVE5: E014_0414H) selects the IO buffer driving capability for pins in 2-bit units.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
UART_2[1:0]		UART_1[1:0]		UART_0[1:0]		LP[1:0]	

7	6	5	4	3	2	1	0
USB[1:0]		JT[1:0]		Reserved			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
UART_2[1:0]	R/W	15:14	00b	Select the driving capability.
UART_1[1:0]	R/W	13:12	00b	00: 4 mA (initial value)
UART_0[1:0]	R/W	11:10	00b	01: 6 mA
LP[1:0]	R/W	9:8	00b	10: 8 mA
USB[1:0]	R/W	7:6	00b	11: 12 mA
JT[1:0]	R/W	5:4	10b	
Reserved	R	3:0	–	Reserved. If these bits are read, 0 is returned for each bit.

8.2.47 Bus hold function on/off switching register

This register (CHG_BUSHOLD: E014_0500H) specifies whether to enable or disable the bus hold function of the AB_AD pin.

31	30	29	28	27	26	25	24
BUSHOLD_GPIO[7:0]							

23	22	21	20	19	18	17	16
BUSHOLD_CAM[7:0]							

15	14	13	12	11	10	9	8
BUSHOLD_AB[15:8]							

7	6	5	4	3	2	1	0
BUSHOLD_AB[7:0]							

Name	R/W	Bit No.	After Reset	Description
BUSHOLD_GPIO[7:0]	R/W	31:24	00H	Specify whether to enable or disable the bus hold function of the pins sharing functions with GPIO[017:010]. 0: Disable, 1: Enable The BUSHOLD_GPIO7 bit controls GPIO_017.
BUSHOLD_CAM[7:0]	R/W	23:16	00H	Specify whether to enable or disable the bus hold function of the pins sharing functions with CAM_YUV[7:0]. 0: Disable, 1: Enable The BUSHOLD_CAM7 bit controls CAM_YUV7.
BUSHOLD_AB[15:0]	R/W	15:0	FFFFH	Specify whether to enable or disable the bus hold function of the AB_AD[15:0] pins. 0: Disable, 1: Enable The BUSHOLD_AB15 bit controls AB_AD15.

8.2.48 AB_CLK output selection register

This register (CHG_FLASHCLK_SEL: E014_0510H) selects the module that outputs AB_CKL.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							FLASHCLK_SEL

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
FLASHCLK_SEL	R/W	0	1	Select the module that outputs AB_CLK. 0: AB 1: SMU (default)

8.2.49 3.3 V LCD delay/phase setting register

This register (CHG_DELAY_LCD33: E014_0600H) specifies the phase and delay for the 3.3 V LCD signals.

31	30	29	28	27	26	25	24
Reserved			PXCLK33_ PHASESEL	PXCLK33_DLYSEL[11:8]			

23	22	21	20	19	18	17	16
PXCLK33_DLYSEL[7:0]							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
PXCLK33_PHASE SEL	R/W	28	1	Specify the phase of LCD3_PXCLK and YUV3_CLK_O. 0: Inverted, 1: Normal
PXCLK33_DLYSEL	R/W	27:16	000H	Specify the amount of delay for LCD3_PXCLK and YUV3_CLK_O. Bit 27 26 25 24 23 22 21 20 19 18 17 16 Delay 0 0 ps 0 1 500 ps 0 1 1 1 ns 0 1 1 1 1.5 ns 0 1 1 1 1 2 ns 0 1 1 1 1 1 2.5 ns 0 1 1 1 1 1 1 3 ns 0 1 1 1 1 1 1 1 3.5 ns 0 1 1 1 1 1 1 1 1 4 ns 0 1 1 1 1 1 1 1 1 1 4.5 ns 0 1 1 1 1 1 1 1 1 1 1 5 ns 0 1 1 1 1 1 1 1 1 1 1 1 5.5 ns 1 1 1 1 1 1 1 1 1 1 1 1 6 ns
Reserved	R	15:0	–	Reserved. If these bits are read, 0 is returned for each bit.

8.2.50 AB_CLK delay/phase setting register

This register (CHG_DELAY_AB: E014_060CH) specifies the phase and delay for AB_CLK.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved			AB_PHASESEL	AB_DLYSEL[11:8]			

7	6	5	4	3	2	1	0
AB_DLYSEL[7:0]							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:13	–	Reserved. If these bits are read, 0 is returned for each bit.
AB_PHASESEL	R/W	12	1	Specify the phase of AB_CLK. 0: Inverted, 1: Normal
AB_DLYSEL[11:0]	R/W	11:0	000H	Specify the amount of delay for AB_CLK. Bit11 10 9 8 7 6 5 4 3 2 1 0 Delay 0 0 ps 0 1 500 ps 0 1 1 1 ns 0 1 1 1 1.5 ns 0 1 1 1 1 2 ns 0 1 1 1 1 1 2.5 ns 0 1 1 1 1 1 1 3 ns 0 1 1 1 1 1 1 1 3.5 ns 0 1 1 1 1 1 1 1 1 4 ns 0 1 1 1 1 1 1 1 1 1 4.5 ns 0 1 1 1 1 1 1 1 1 1 1 5 ns 0 1 1 1 1 1 1 1 1 1 1 1 5.5 ns 1 1 1 1 1 1 1 1 1 1 1 1 6 ns

8.2.51 3.3 V ICE delay/phase setting register

This register (CHG_DELAY_ICEA33: E014_0618H) specifies the phase and delay for the 3.3 V ICE signals.

31	30	29	28	27	26	25	24
Reserved			TCLK33_PHASESEL	TCLK33_DLYSEL[11:8]			

23	22	21	20	19	18	17	16
TCLK33_DLYSEL[7:0]							

15	14	13	12	11	10	9	8
Reserved			TCTL33_PHASESEL	TCTL33_DLYSEL[11:8]			

7	6	5	4	3	2	1	0
TCTL33_DLYSEL[7:0]							

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
TCLK33_PHASESEL	R/W	28	1	Specify the phase of 3.3 V TRACECLK. 0: Inverted, 1: Normal
TCLK33_DLYSEL[11:0]	R/W	27:16	000H	Specify the amount of delay for 3.3 V TRACECLK. Bit 27 26 25 24 23 22 21 20 19 18 17 16 Delay 0 0 ps 0 1 500 ps 0 1 1 1 ns 0 1 1 1 1.5 ns 0 1 1 1 1 2 ns 0 1 1 1 1 1 2.5 ns 0 1 1 1 1 1 1 3 ns 0 1 1 1 1 1 1 1 3.5 ns 0 1 1 1 1 1 1 1 1 4 ns 0 1 1 1 1 1 1 1 1 1 4.5 ns 0 1 1 1 1 1 1 1 1 1 1 5 ns 0 1 1 1 1 1 1 1 1 1 1 1 5.5 ns 1 1 1 1 1 1 1 1 1 1 1 1 6 ns
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
TCTL33_PHASE SEL	R/W	12	1	Specify the phase of 3.3 V TRACECTL. 0: Inverted, 1: Normal
TCTL33_DLYSEL [11:0]	R/W	11:0	000H	Specify the amount of delay for 3.3 V TRACECTL. Bit11 10 9 8 7 6 5 4 3 2 1 0 Delay 0 0 ps 0 1 500 ps 0 1 1 1 ns 0 1 1 1 1.5 ns 0 1 1 1 1 2 ns 0 1 1 1 1 1 2.5 ns 0 1 1 1 1 1 1 3 ns 0 1 1 1 1 1 1 1 3.5 ns 0 1 1 1 1 1 1 1 1 4 ns 0 1 1 1 1 1 1 1 1 1 4.5 ns 0 1 1 1 1 1 1 1 1 1 1 5 ns 0 1 1 1 1 1 1 1 1 1 1 1 5.5 ns 1 1 1 1 1 1 1 1 1 1 1 1 6 ns

8.2.52 1.8 V ICE delay/phase setting register

This register (CHG_DELAY_ICEA18: E014_061CH) specifies the phase and delay for the 1.8 V ICE signals.

31	30	29	28	27	26	25	24
Reserved			TCLK18_PHASESEL	TCLK18_DLYSEL[11:8]			

23	22	21	20	19	18	17	16
TCLK18_DLYSEL[7:0]							

15	14	13	12	11	10	9	8
Reserved			TCTL18_PHASESEL	TCTL18_DLYSEL[11:8]			

7	6	5	4	3	2	1	0
TCTL18__DLYSEL[7:0]							

(1/2)

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
TCLK18_PHASESEL	R/W	28	1	Specify the phase of 1.8 V TRACECLK. 0: Inverted, 1: Normal
TCLK18_DLYSEL[11:0]	R/W	27:16	000H	Specify the amount of delay for 1.8 V TRACECLK. Bit 27 26 25 24 23 22 21 20 19 18 17 16 Delay 0 0 ps 0 1 500 ps 0 1 1 1 ns 0 1 1 1 1.5 ns 0 1 1 1 1 2 ns 0 1 1 1 1 1 2.5 ns 0 1 1 1 1 1 1 3 ns 0 1 1 1 1 1 1 1 3.5 ns 0 1 1 1 1 1 1 1 1 4 ns 0 1 1 1 1 1 1 1 1 1 4.5 ns 0 1 1 1 1 1 1 1 1 1 1 5 ns 0 1 1 1 1 1 1 1 1 1 1 1 5.5 ns 1 1 1 1 1 1 1 1 1 1 1 1 6 ns
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit No.	After Reset	Description
TCTL18_PHASE SEL	R/W	12	1	Specify the phase of 1.8 V TRACECTL. 0: Inverted, 1: Normal
TCTL18_DLYSEL [11:0]	R/W	11:0	000H	Specify the amount of delay for 1.8 V TRACECTL. Bit11 10 9 8 7 6 5 4 3 2 1 0 Delay 0 0 ps 0 1 500 ps 0 1 1 1 ns 0 1 1 1 1.5 ns 0 1 1 1 1 2 ns 0 1 1 1 1 1 2.5 ns 0 1 1 1 1 1 1 3 ns 0 1 1 1 1 1 1 1 3.5 ns 0 1 1 1 1 1 1 1 1 4 ns 0 1 1 1 1 1 1 1 1 1 4.5 ns 0 1 1 1 1 1 1 1 1 1 1 5 ns 0 1 1 1 1 1 1 1 1 1 1 1 5.5 ns 1 1 1 1 1 1 1 1 1 1 1 1 6 ns

8.2.53 CHGREG reset control register (for testing)

This register (CHG_RST_CTRL: E014_07C4H) specifies the signal used to reset CHGREG registers.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							CHG_RST_ CTRL

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
CHG_RST_CTRL	R/W	0	0	Specify the signal used to reset CHGREG registers. 1: SRESETB and SMU_CHGRSTZ 0: SMU_CHGRSTZ (a signal equivalent to PONDET)

APPENDIX A. Register List

A.1 Timers (TI0, TI1, TI2, TI3, TW0, TW1, TW2, TW3, TW4, TG0, TG1, TG2, TG3, TG4, TG5)

Base address: E000_0000H

PB1_PADDR[31:0]	Module	PB1_PADDR[31:0]	Module
0000H	TI0	1400H	TW4
0100H	TI1	2000H	TG0
0200H	TI2	2100H	TG1
0300H	TI3	2200H	TG2
1000H	TW0	2300H	TG3
1100H	TW1	2400H	TG4
1200H	TW2	2500H	TG5
1300H	TW3		

Address	Register Name	Symbol	R/W	After Reset
00H	Timer operation register	xxx_OP	R/W	0000_0000H
04H	Timer clear register	xxx_CLR	W	0000_0000H
08H	Timer value setting register	xxx_SET	R/W	0000_0000H
0CH	Real count read register	xxx_RCR	R	0000_0000H
10H	Reserved	–	–	–
14H	Timer value setting monitor register	xxx_SCLR	R/W	0000_0000H
18H	One-shot startup register	xxx_ONE	W	0000_0000H
1CH	INT asserted period setting register	xxx_INT	R/W	0000_0000H
20H to FCH	Reserved	–	–	–

(xxx = TI0, TI1, TI2, TI3, TW0, TW1, TW2, TW3, TW4, TG0, TG1, TG2, TG3, TG4, or TG5)

A.2 Unified Serial Interface (SIO0 to SIO5)

Base address

SIO0: E012_0000H

SIO1: E001_0000H

SIO2: E10C_0000H

SIO3: E10D_0000H

SIO4: E10E_0000H

SIO5: E10F_0000H

(1) Mode setting registers

Address	Register Name	Symbol	R/W	After Reset
0000H	Mode selection enable register	SIO_SWITCH_EN	R/W	0000_0000H
0004H	Mode selection register	SIO_MODE_SWITCH	R/W	0000_0000H
0008H to 0FFCH	Reserved	–	–	–

(2) SPI registers

Address	Register Name	Symbol	R/W	After Reset
1000H	SPI mode register	SPI_MODE	R/W	0000_0002H
1004H	SPI polarity register	SPI_POL	R/W	0000_7000H
1008H	SPI Control register	SPI_CONTROL	R/W	0000_8040H
100CH	Reserved	–	–	–
1010H	SPI transmit data register	SPI_TX_DATA	W	0000_0000H
1014H	SPI receive data register	SPI_RX_DATA	R	0000_00xxH
1018H	SPI interrupt status register	SPI_STATUS	R	0000_0000H
101CH	SPI interrupt raw status register	SPI_RAW_STATUS	R	0000_0000H
1020H	SPI interrupt enable set register	SPI_ENSET	R/W	0000_0000H
1024H	SPI interrupt enable clear register	SPI_ENCLR	W	0000_0000H
1028H	SPI interrupt source clear register	SPI_FFCLR	W	0000_0000H
102CH	Reserved	–	–	–
1030H	SPI reception FIFO pointer register	SPI_RX_FIFO_P	R	0000_0000H
1034H	SPI control register 2	SPI_CONTROL2	R/W	0000_0000H
1038H	SPI CS fixed value setting register	SPI_TIECS	R/W	0000_0000H
103CH to 1FFCH	Reserved	–	–	–

(3) Audio registers

Address	Register Name	Symbol	R/W	After Reset
2000H	PCM operation mode setting register	PCM_FUNC_SEL	R/W	0000_0000H
2004H	PCM data transfer enable set register	PCM_TXRX_EN	R/W	0000_0000H
2008H	PCM data transfer enable clear register	PCM_TXRX_DIS	W	0000_0000H
200CH	PCM data transfer cycle setting register	PCM_CYCLE	R/W	0000_0000H
2010H	PCM interrupt raw status register	PCM_RAW	R	0000_0000H
2014H	PCM interrupt status register	PCM_STATUS	R	0000_0000H
2018H	PCM interrupt enable set register	PCM_ENSET	R/W	0000_0000H
201CH	PCM interrupt enable clear register	PCM_ENCLR	W	–
2020H	PCM interrupt clear register	PCM_CLEAR	W	–
2024H	PCM transmission data register	PCM_TXQ	R/W	0000_0000H
2028H	PCM reception data register	PCM_RXQ	R	xxxx_xxxxH
202CH	PCM FIFO counter register	PCM_FIFO_P	R	0000_0000H
2030H	PCM data transfer cycle setting register 2	PCM_CYCLE2	R/W	0000_0000H
2034H	Reserved	–	–	–
2038H	PCM AC97 reset assert register	PCM_AC97_RESET	R/W	0000_0000H
2040H to FFFCH	Reserved	–	–	–

A.3 Interrupt Interface (INTA)

Base address: E002_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	CPU Interface Control Register	ICCICR	R/W	0000_0000H
0004H	Interrupt Priority Mask Register	ICCPMR	R/W	0000_0000H
0008H	Binary Point Register	ICCBPR	R/W	0000_0000H to 0000_0003H
000CH	Interrupt Acknowledge Register	ICCIAR	R	0000_03FFH
0010H	End of Interrupt Register	ICCEOIR	W	–
0014H	Running Priority Register	ICCRPR	R	0000_00FFH
0018H	Highest Pending Interrupt Register	ICCHPIR	R	0000_03FFH
001CH	Aliased Binary Point Register	ICCABPR	R/W	0000_0000H
0020H to 003CH	Reserved	–	–	–
0040H to 00CFH	IMPLEMENTATION DEFINED Register	–	–	–
00D0H to 00F8H	Reserved	–	–	–
00FCH	CPU Interface Identification Register	ICCIIDR	R	IMPLEMENTATION DEFINED
0100H to 7FFCH	Reserved	–	–	–
8000H	Distributor Control Register	ICDDCR	R/W	0000_0000H
8004H	Interrupt Controller Type Register	ICDICTR	R	IMPLEMENTATION DEFINED
8008H	Distributor Implementer Identification Register	ICDIIDR	R	IMPLEMENTATION DEFINED
800CH to 807CH	Reserved	–	–	–
8080H	Interrupt Security Register	ICDISR	R/W	IMPLEMENTATION DEFINED
8084H to 80FCH				0000_0000H
8100H to 817CH	Interrupt Set-Enable Register	ICDISER	R/W	IMPLEMENTATION DEFINED
8180H to 81FCH	Interrupt Clear-Enable Register	ICDICER	R/W	IMPLEMENTATION DEFINED
8200H to 827CH	Interrupt Set-Pending Register	ICDISPR	R/W	0000_0000H
8280H to 82FCH	Interrupt Clear-Pending Register	ICDICPR	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
8300H to 837CH	Active Bit Register	ICDABR	R	0000_0000H
8380H to 83FCH	Reserved	–	–	–
8400H to 87F8H	Interrupt Priority Register	ICDIPR	R/W	0000_0000H
87FCH	Reserved	–	–	–
8800H to 881CH	Interrupt Processor Targets Register	ICDIPTR	R	IMPLEMENTATION DEFINED
8820H to 8BF8H			R/W	0000_0000H
8BFCH	Reserved	–	–	–
8C00H to 8CFCH	Interrupt Configuration Register	ICDICFR	R/W	IMPLEMENTATION DEFINED
8D00H to 8DFCH	IMPLEMENTATION DEFINED Register	–	–	–
8E00H to 8EFCH	Reserved	–	–	–
8F00H	Software Generated Interrupt Register	ICDSGIR	W	–
8F04H to 8FCCH	Reserved	–	–	–
8FD0H to 8FFCH	Identification Register	ICDIIDR	R	IMPLEMENTATION DEFINED
9000H to FFFCH	Reserved	–	–	–

A.4 LCD Interface

Base address: E004_0000H

(1) Function setting registers

Address	Register Name	Symbol	R/W	After Reset
0000H	Control register	LCD_CONTROL	R/W	0000_0000H
0004H	Simple QoS setting register	LCD_QOS	R/W	0000_0000H
0008H	Data request cycle register	LCD_DATAREQ	R/W	0000_0000H
000CH	Reserved	–	–	–

(2) Display start registers

Address	Register Name	Symbol	R/W	After Reset
0010H	Display register	LCD_LCDOUT	R/W	0000_0000H
0014H	Access bus select register	LCD_BUSSEL	R/W	0000_0000H
0018H	Status register	LCD_STATUS	R	0000_0000H
001CH	Fixed-color output value register	LCD_BACKCOLOR	R/W	0000_0000H

(3) Frame buffer setting registers

Address	Register Name	Symbol	R/W	After Reset
0020H	Display area address register	LCD_AREAADR_ODD	R/W	0000_0000H
0024H	Display area address register	LCD_AREAADR_EVEN	R/W	0000_0000H
0028H	Address addition value register	LCD_HOFFSET	R/W	0000_0000H
002CH	Input format register	LCD_IFORMAT	R/W	0000_0000H
0030H	Simple resize register	LCD_RESIZE	R/W	0000_0000H
0034H to 003CH	Reserved	–	–	–

(4) Display setting registers

Address	Register Name	Symbol	R/W	After Reset
0040H	Horizontal direction total register	LCD_HTOTAL	R/W	0000_0000H
0044H	Horizontal direction display area register	LCD_HAREA	R/W	0000_0000H
0048H	Horizontal synchronization edge 1 register	LCD_HEDGE1	R/W	0000_0000H
004CH	Horizontal synchronization edge 2 register	LCD_HEDGE2	R/W	0000_0000H
0050H	Vertical direction total register	LCD_VTOTAL	R/W	0000_0000H
0054H	Vertical direction display area register	LCD_VAREA	R/W	0000_0000H
0058H	Vertical synchronization edge 1 register	LCD_VEDGE1	R/W	0000_0000H
005CH	Vertical synchronization edge 2 register	LCD_VEDGE2	R/W	0000_0000H

(5) Interrupt control registers

Address	Register Name	Symbol	R/W	After Reset
0060H	Interrupt status register	LCD_INTSTATUS	R	0000_0000H
0064H	Interrupt raw status register	LCD_INTRAWSTATUS	R	0000_0000H
0068H	Interrupt enable set register	LCD_INTENSET	R/W	0000_0000H
006CH	Interrupt enable clear register	LCD_INTENCLR	W	0000_0000H
0070H	Interrupt source clear register	LCD_INTFFCLR	W	0000_0000H
0074H	Frame count interrupt setting register	LCD_FRAMECOUNT	R/W	0000_0000H
0078H to 007CH	Reserved	–	–	–

(6) YUV output relationship registers

Address	Register Name	Symbol	R/W	After Reset
0080H	RGB2YUV transform coefficient register Y0	LCD_COEF_Y0	R/W	0000_0000H
0084H	RGB2YUV transform coefficient register Y1	LCD_COEF_Y1	R/W	0000_0000H
0088H	RGB2YUV transform coefficient register Y2	LCD_COEF_Y2	R/W	0000_0000H
008CH	RGB2YUV transform coefficient register Y3	LCD_COEF_Y3	R/W	0000_0000H
0090H	RGB2YUV transform coefficient register U0	LCD_COEF_U0	R/W	0000_0000H
0094H	RGB2YUV transform coefficient register U1	LCD_COEF_U1	R/W	0000_0000H
0098H	RGB2YUV transform coefficient register U2	LCD_COEF_U2	R/W	0000_0000H
009CH	RGB2YUV transform coefficient register U3	LCD_COEF_U3	R/W	0000_0000H
00A0H	RGB2YUV transform coefficient register V0	LCD_COEF_V0	R/W	0000_0000H
00A4H	RGB2YUV transform coefficient register V1	LCD_COEF_V1	R/W	0000_0000H
00A8H	RGB2YUV transform coefficient register V2	LCD_COEF_V2	R/W	0000_0000H
00ACH	RGB2YUV transform coefficient register V3	LCD_COEF_V3	R/W	0000_0000H
00B0H to 00BCH	Reserved	–	–	–
00C0H	BYTELANE register	LCD_BYTELANE	R/W	0000_0000H
00C4H to 00CCH	Reserved	–	–	–
00D0H	Vertical synchronization signal control register	LCD_VSYNC_CONT	R/W	0000_0000H
00D4H	Reserved	–	–	–
00D8H	Vertical synchronization edge offset register (Odd field)	LCD_VOFFSET_ODD	R/W	0000_0000H
00DCH	Vertical synchronization edge offset register (Even field)	LCD_VOFFSET_EVEN	R/W	0000_0000H
00E0H	Vertical direction total register (Even field)	LCD_VAREA_EVEN	R/W	0000_0000H
00E4H	Reserved	–	–	–
00E8H	Vertical synchronization edge 1 register (Even field)	LCD_VEDGE1_EVEN	R/W	0000_0000H
00ECH	Vertical synchronization edge 2 register (Even field)	LCD_VEDGE2_EVEN	R/W	0000_0000H
00F0H to 01FCH	Reserved	–	–	–

(7) Cursor-relationship registers

Address	Register Name	Symbol	R/W	After Reset
0200H	Cursor enable register	LCD_CURSOR_EN	R/W	0000_0000H
0204H	Cursor operation register	LCD_CURSOR_OPE	R/W	0000_0000H
0208H	Cursor horizontal position register	LCD_CURSOR_POSH	R/W	0000_0000H
020CH	Cursor vertical position register	LCD_CURSOR_POSV	R/W	0000_0000H
0210H	Cursor data RAM select register	LCD_CURSOR_RAMSEL	R/W	0000_0000H
0214H	Cursor status register	LCD_CURSOR_STATUS	R	0000_0000H
0218H to 03FCH	Reserved	–	–	–
0400H to 07FCH	Cursor palette RAM register	LCD_CURSOR_TABLE	R/W	Undefined (RAM)
0800H to 00FFCH	Reserved	–	–	–
1000H to 1FFCH	Cursor data RAM 0 register	LCD_CURSOR_DATA0	R/W	Undefined (RAM)
2000H to 2FFCH	Cursor data RAM 1 register	LCD_CURSOR_DATA1	R/W	Undefined (RAM)
3000H to FFFCH	Reserved	–	–	–

A.5 General-Purpose I/O Interface (GIO)

Base address: E005_0000H

Register addresses of each GPIO port

Symbol	GPIO_31-0 GIO_xxx = GIO_000	GPIO_63-32 GIO_xxx = GIO_032	GPIO_95-64 GIO_xxx = GIO_064	GPIO_127-96 GIO_xxx = GIO_096	GPIO_158-128 GIO_xxx = GIO_128
GIO_XXX_E1	0000H	0080H	0100H	0180H	0200H
GIO_XXX_E0	0004H	0084H	0104H	0184H	0204H
GIO_XXX_EM	0004H	0084H	0104H	0184H	0204H
GIO_XXX_OL	0008H	0088H	0108H	0188H	0208H
GIO_XXX_OH	000CH	008CH	010CH	018CH	020CH
GIO_XXX_I	0010H	0090H	0110H	0190H	0210H
GIO_XXX_IIA	0014H	0094H	0114H	0194H	0214H
GIO_XXX_IEN	0018H	0098H	0118H	0198H	0218H
GIO_XXX_IDS	001CH	009CH	011CH	019CH	021CH
GIO_XXX_IIM	001CH	009CH	011CH	019CH	021CH
GIO_XXX_RAW	0020H	00A0H	0120H	01A0H	0220H
GIO_XXX_MST	0024H	00A4H	0124H	01A4H	0224H
GIO_XXX_IIR	0028H	00A8H	0128H	01A8H	0228H
GIO_XXX_GSW	003CH	00BCH	013CH	01BCH	023CH
GIO_XXX_IDT0	0040H	00C0H	0140H	01C0H	0240H
GIO_XXX_IDT1	0044H	00C4H	0144H	01C4H	0244H
GIO_XXX_IDT2	0048H	00C8H	0148H	01C8H	0248H
GIO_XXX_IDT3	004CH	00CCH	014CH	01CCH	024CH
GIO_XXX_RAWBL	0050H	00D0H	0150H	01D0H	0250H
GIO_XXX_RAWBH	0054H	00D4H	0154H	01D4H	0254H
GIO_XXX_IRBL	0058H	00D8H	0158H	01D8H	0258H
GIO_XXX_IRBH	005CH	00DCH	015CH	01DCH	025CH

Address	Register Name	Symbol	R/W	After Reset
0000H	Port switch setting register (output setting)	GIO_xxx_E1	W	0000_0000H
0004H	Port switch setting/status register (input setting)	GIO_xxx_E0	W	0000_0000H
0004H	Port status monitor register	GIO_xxx_EM	R	0000_0000H
0008H	Output data setting register (lower 16 bits)	GIO_xxx_OL	W	0000_0000H
000CH	Output data setting register (higher 16 bits)	GIO_xxx_OH	W	0000_0000H
0010H	Input data read register	GIO_xxx_I	R	Note
0014H	Input port interrupt enable specification register	GIO_xxx_IIA	R/W	0000_0000H
0018H	Input port interrupt enable register (mask cancel)	GIO_xxx_IEN	W	0000_0000H
001CH	Input port interrupt disable register (mask setting)	GIO_xxx_IDS	W	0000_0000H
001CH	Input port interrupt enable monitor register	GIO_xxx_IIM	R	0000_0000H
0020H	Input port interrupt raw status register	GIO_xxx_RAW	R	0000_0000H
0024H	Input port interrupt maskable status register	GIO_xxx_MST	R	0000_0000H
0028H	Input port interrupt source reset register	GIO_xxx_IIR	W	0000_0000H
002CH-0038H	Reserved	–	–	–
003CH	INT_FIQ pin connection register	GIO_xxx_GSW	R/W	0000_0000H
0040H	Input port interrupt detection mode register (bits 7 to 0)	GIO_xxx_IDT0	R/W	0000_0000H
0044H	Input port interrupt detection mode register (bits 15 to 8)	GIO_xxx_IDT1	R/W	0000_0000H
0048H	Input port interrupt detection mode register (bits 23 to 16)	GIO_xxx_IDT2	R/W	0000_0000H
004CH	Input port interrupt detection mode register (bits 31 to 24)	GIO_xxx_IDT3	R/W	0000_0000H
0050H	Interrupt status register (in both edge detection mode) (lower 16 bits)	GIO_xxx_RAWBL	R	0000_0000H
0054H	Interrupt status register (in both edge detection mode) (higher 16 bits)	GIO_xxx_RAWBH	R	0000_0000H
0058H	Interrupt source clear register (in both edge detection mode) (lower 16 bits)	GIO_xxx_IRBL	W	0000_0000H
005CH	Interrupt source clear register (in both edge detection mode) (higher 16 bits)	GIO_xxx_IRBH	W	0000_0000H
0060H to FFFCH	Reserved	–	–	–

Note The reset value is determined according to the external pin status.

A.6 I²C Interface (IIC0, IIC1)

Base address

IIC0: E007_0000H

IIC1: E10A_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	IICx enable operation register	IIC_IICACTx	R/W	0000H
0004H	IICx shift register	IIC_IICx	R/W	0000H
0008H	IICx control register	IIC_IICCx	R/W	0000H
000CH	Slave address register	IIC_SVAx	R/W	0000H
0010H	IICx transfer clock selection register	IIC_IICCLx	R/W	0004H
0014H	IICx function extension register	IIC_IICXx	R/W	0000H
0018H	IICx state register	IIC_IICSx	R	0000H
001CH	IICx state register (Read-only register for emulation)	IIC_IICSEx	R	0000H
0020H	IICx flag register	IIC_IICFx	R/W	0000H
0024H to FFFCH	Reserved	–	–	–

Note x = 0 or 1.

A.7 LP-DDR/ DDR2 Controller (MEMC)

Base address: E00A_0000H

(1) Request controller and system cache configuration registers

Address	Register Name	Symbol	R/W	After Reset
0000H	Cache disable/prefetch per master register	MEMC_CACHE_MODE	R/W	0000_0000H
0004H	Reserved	–	–	–
0008H	Degenerate function register	MEMC_DEGFUN	R/W	0000_0000H
000CH to 0FFCH	Reserved	–	–	–

(2) Memory request scheduler configuration register

Address	Register Name	Symbol	R/W	After Reset
1000H	Memory request scheduling mode register	MEMC_REQSCH	R/W	0000_0000H
1004H to 1FFCH	Reserved	–	–	–

(3) External memory controller registers

Address	Register Name	Symbol	R/W	After Reset
2000H	Memory connection setting register	MEMC_DDR_CONFIGF	R/W	0000_0808H
2004H	AC timing setting register 1	MEMC_DDR_CONFIGA1	R/W	5444_3203H
2008H	AC timing setting register 2	MEMC_DDR_CONFIGA2	R/W	00DA_0040H
200CH	Software command issuance register 1	MEMC_DDR_CONFIGC1	R/W	4040_0033H
2010H	Software command issuance register 2	MEMC_DDR_CONFIGC2	R/W	0000_0340H
2014H	Refresh setting register 1	MEMC_DDR_CONFIGR1	R/W	0FFF_0FFFH
2018H	Refresh setting register 2	MEMC_DDR_CONFIGR2	R/W	1F1F_FCFCH
201CH	Refresh setting register 3	MEMC_DDR_CONFIGR3	R/W	0000_FCFCH
2020H	Automatic DQS timing adjustment register 1	MEMC_DDR_CONFIGT1	R/W	0000_0003H
2024H	Automatic DQS timing adjustment register 2	MEMC_DDR_CONFIGT2	R/W	0000_0000H
2028H	Reserved	–	–	–
202CH	Memory status check register	MEMC_DDR_STATE8	R/W	0000_0000H
2030H	IO configuration register	MEMC_DDR_CONFIGD	R/W	0000_8000H
2034H	Reserved	–	–	–
2038H	Drive capability switch register 1	MEMC_DDR_CONFIGZD	R/W	0000_0000H
203CH	Drive capability switch register 2	MEMC_DDR_CONFIGZC	R/W	0000_0000H
2040H	Drive capability switch register 3	MEMC_DDR_CONFIGZA	R/W	0000_0000H
2044H to FFFCH	Reserved	–	–	–

A.8 PDMA

Base address: E00F_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	PDMA/DMA selection register (exclusively switched)	PDMA_DMA_SEL	R/W	0000_0000H
0004H	Transfer start/reserve register (used for both starting and reserving transfer)	PDMA_CONT	W	0000_0000H
0008H	Status register (stopped/transferring/reserved)	PDMA_STATUS	R	0000_0000H
000CH	Reservation cancel register	PDMA_RSV_CANCEL	W	0000_0000H
0010H	Forced end register	PDMA_END	W	0000_0000H
0014H to 001CH	Reserved	–	–	–
0020H	Transfer start address register (for reservation, 4-byte alignment)	PDMA_RSV_ADD	R/W	0000_0000H
0024H	Transfer length register (for reservation, in word (4 bytes) units)	PDMA_RSV_LENG	R/W	0000_0000H
0028H	Transfer start address register (during transfer, 4-byte alignment)	PDMA_RUN_ADD	R	0000_0000H
002CH	Transfer length register (during transfer, in word (4 bytes) units)	PDMA_RUN_LENG	R	0000_0000H
0030H	Interrupt status register	PDMA_INT_STATUS	R	0000_0000H
0034H	Interrupt raw status register	PDMA_INT_RAW_STATUS	R	0000_0000H
0038H	Interrupt enable set register	PDMA_INT_ENABLE	R/W	0000_0000H
003CH	Interrupt enable clear register	PDMA_INT_ENABLE_CL	W	0000_0000H
0040H	Interrupt source clear register	PDMA_INT_REQ_CL	W	0000_0001H
0044H to 004CH	Reserved	–	–	–
0050H	Address pointer register (during transfer, 4-byte alignment)	PDMA_RUN_ADP	R	0000_0000H
0054H	Halfword swap register	PDMA_HWORD_SWAP	R/W	0000_0000H
0058H	Temporary register (can be used for reservation management)	PDMA_TMP	R/W	0000_0000H
005CH	AXI address pointer (for debugging)	PDMA_AXI_ADP	R	0000_0000H
0060H to FFFCH	Reserved	–	–	–

A.9 Power Management Unit (PMU)

Base address: E010_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Reserved	–	–	–
0004H	Program counter (command RAM address) register	PMU_PC	R/W	0000_0000H
0008H	PMU start register	PMU_START	R/W	0000_0000H
0010H to 002CH	Reserved	–	–	–
0030H	Power-on sequence start PC register	PMU_POWER_ON_PC	R/W	0000_0000H
0034H to 005CH	Reserved	–	–	–
0060H	Watchdog timer count enable register	PMU_WDT_COUNT_EN	R/W	0000_0000H
0064H	Watchdog timer count limit register	PMU_WDT_COUNT_LMT	R/W	0003_FFFFH
0068H	Interrupt handler PC register	PMU_INT_HANDLER_PC	R/W	0000_0000H
0070H	Program status register	PMU_PSR	R	0000_0000H
0074H	TRIG_WAIT command status register	PMU_TRIG_STATUS	R	0000_0000H
0078H	General-purpose register A	PMU_REGA	R	0000_0000H
007CH	General-purpose register B	PMU_REGB	R	0000_0000H
0080H	CPU interrupt status register	PMU_INTSTATUS_A	R	0000_0000H
0084H	CPU interrupt raw status register	PMU_INTRAWSTATUS_A	R	0000_0000H
0088H	CPU interrupt enable set register	PMU_INTENSET_A	R/W	0000_0000H
008CH	CPU interrupt enable clear register	PMU_INTENCLR_A	W	0000_0000H
0090H	CPU interrupt source clear register	PMU_INTFFCLR_A	W	0000_0000H
0094H to 00A4H	Reserved	–	–	–
00A8H	PC error address register	PMU_PCERR	R/W	0000_0000H
00ACH	Security error address register	PMU_SECERRADR	R/W	0000_0000H
00B0H to 00FCH	Reserved	–	–	–
0100H to 013CH	Command buffer FF register	PMU_CMD_BUF_FF	R/W	–
0140H to 0FFCH	Reserved	–	–	–
1000H to 27FCH	Command buffer RAM register	PMU_CMD_BUF_RAM	R/W	–
2800H to FFFCH	Reserved	–	–	–

A.10 System Management Unit (SMU)

Base address: E011_0000H

(1) S1 domain registers

Address	Register Name	Symbol	R/W	After Reset
0000H	CPU reset control register 0	CPU_RSTCTRL0	R/W	0000_001FH
0004H	CPU reset control register 1	CPU_RSTCTRL1	R/W	0000_0003H
0008H	Reserved	–	–	–
000CH	GIO reset control register	GIO_RSTCTRL	R/W	0000_0000H
0010H	INTA reset control register	INTA_RSTCTRL	R/W	0000_0001H
0014H	CHG reset control register	CHG_RSTCTRL	R/W	0000_0001H
0018H	CHG1 reset control register	CHG1_RSTCTRL	R/W	0000_0000H
001CH	BUS0 reset control register	BUS0_RSTCTRL	R/W	0000_0001H
0020H	BUS1 reset control register	BUS1_RSTCTRL	R/W	0000_0001H
0024H	PBL0 reset control register	PBL0_RSTCTRL	R/W	0000_0001H
0028H	PBL1 reset control register	PBL1_RSTCTRL	R/W	0000_0001H
002CH	AHB reset control register	AHB_RSTCTRL	R/W	0000_0001H
0030H	P2M reset control register	P2M_RSTCTRL	R/W	0000_0000H
0034H	M2P reset control register	M2P_RSTCTRL	R/W	0000_0000H
0038H	M2M reset control register	M2M_RSTCTRL	R/W	0000_0000H
003CH	PMU reset control register	PMU_RSTCTRL	R/W	0000_0000H
0040H	SRC reset control register	SRC_RSTCTRL	R/W	0000_0001H
0044H	ROM reset control register	ROM_RSTCTRL	R/W	0000_0001H
0048H	AB0 reset control register	AB0_RSTCTRL	R/W	0000_0001H
004CH	MEMC reset control register	MEMC_RSTCTRL	R/W	0000_0000H
0050H	LCD reset control register	LCD_RSTCTRL	R/W	0000_0000H
0054H	IMC reset control register	IMC_RSTCTRL	R/W	0000_0000H
0058H	IMCW reset control register	IMCW_RSTCTRL	R/W	0000_0000H
005CH	SIZ reset control register	SIZ_RSTCTRL	R/W	0000_0000H
0060H	ROT reset control register	ROT_RSTCTRL	R/W	0000_0000H
0064H	Reserved	–	–	–
0068H	AVE reset control register	AVE_RSTCTRL	R/W	0000_0000H
006CH	A3D reset control register	A3D_RSTCTRL	R/W	0000_0000H
0070H	DTV reset control register	DTV_RSTCTRL	R/W	0000_0000H
0074H	NTS reset control register	NTS_RSTCTRL	R/W	0000_0000H
0078H	CAM reset control register	CAM_RSTCTRL	R/W	0000_0000H
007CH to 0084H	Reserved	–	–	–
0088H	PWM reset control register	PWM_RSTCTRL	R/W	0000_0000H
008CH	USIAS0 reset control register	USIAS0_RSTCTRL	R/W	0000_0000H
0090H	USIAS1 reset control register	USIAS1_RSTCTRL	R/W	0000_0000H
0094H	USIAU0 reset control register	USIAU0_RSTCTRL	R/W	0000_0000H
0098H	Reserved	–	–	–

Address	Register Name	Symbol	R/W	After Reset
009CH	USIBS2 reset control register	USIBS2_RSTCTRL	R/W	0000_0000H
00A0H	USIBS3 reset control register	USIBS3_RSTCTRL	R/W	0000_0000H
00A4H	USIBS4 reset control register	USIBS4_RSTCTRL	R/W	0000_0000H
00A8H	USIBS5 reset control register	USIBS5_RSTCTRL	R/W	0000_0000H
00ACH	USIBU1 reset control register	USIBU2_RSTCTRL	R/W	0000_0000H
00B0H	USIBU2 reset control register	USIBU2_RSTCTRL	R/W	0000_0000H
00B4H	USIBU3 reset control register	USIBU3_RSTCTRL	R/W	0000_0000H
00B8H	Reserved	–	–	–
00BCH	SDIO0 reset control register	SDIO0_RSTCTRL	R/W	0000_0000H
00C0H	SDIO1 reset control register	SDIO1_RSTCTRL	R/W	0000_0000H
00C4H	SDIO2 reset control register	SDIO2_RSTCTRL	R/W	0000_0000H
00C8H	SDC reset control register	SDC_RSTCTRL	R/W	0000_0000H
00CCH	Reserved	–	–	–
00D0H	CFI reset control register	CFI_RSTCTRL	R/W	0000_0000H
00D4H to 00D8H	Reserved	–	–	–
00DCH	IIC0 reset control register	IIC0_RSTCTRL	R/W	0000_0000H
00E0H	IIC1 reset control register	IIC1_RSTCTRL	R/W	0000_0000H
00E4H	USB0 reset control register	USB0_RSTCTRL	R/W	0000_0000H
00E8H	USB1 reset control register	USB1_RSTCTRL	R/W	0000_0000H
00ECH	TI0 reset control register	TI0_RSTCTRL	R/W	0000_0000H
00F0H	TI1 reset control register	TI1_RSTCTRL	R/W	0000_0000H
00F4H	TI2 reset control register	TI2_RSTCTRL	R/W	0000_0000H
00F8H	IT3 reset control register	TI3_RSTCTRL	R/W	0000_0000H
00FCH	TW0 reset control register	TW0_RSTCTRL	R/W	0000_0000H
0100H	TW1 reset control register	TW1_RSTCTRL	R/W	0000_0000H
0104H	TW2 reset control register	TW2_RSTCTRL	R/W	0000_0000H
0108H	TW3 reset control register	TW3_RSTCTRL	R/W	0000_0000H
010CH	TG0 reset control register	TG0_RSTCTRL	R/W	0000_0000H
0110H	TG1 reset control register	TG1_RSTCTRL	R/W	0000_0000H
0114H	TG2 reset control register	TG2_RSTCTRL	R/W	0000_0000H
0118H	TG3 reset control register	TG3_RSTCTRL	R/W	0000_0000H
011CH	TG4 reset control register	TG4_RSTCTRL	R/W	0000_0000H
0120H	TG5 reset control register	TG5_RSTCTRL	R/W	0000_0000H
0124H	STI reset control register	STI_RSTCTRL	R/W	0000_0000H
0128H	Reserved	–	–	–
012CH	AFS reset control register	AFS_RSTCTRL	R/W	0000_0000H
0130H to 013CH	Reserved	–	–	–
0140H	TW4 reset control register	TW4_RSTCTRL	R/W	0000_0000H
0144H	Reserved	–	–	–
0148H	PDMA reset control register	PDMA_RSTCTRL	R/W	0000_0000H
014CH to 0150H	Reserved	–	–	–

Address	Register Name	Symbol	R/W	After Reset
0154H	CPU0 safe reset control register	CPU_SAFE_RESET0	R/W	0000_001FH
0158H	CPU1 safe reset control register	CPU_SAFE_RESET1	R/W	0000_0003H
015CH	Reserved	–	–	–
0160H	USB0 safe reset control register	USB0_SAFE_RESET	R/W	0000_0001H
0164H	USB1 safe reset control register	USB1_SAFE_RESET	R/W	0000_0001H
0168H	DTV safe reset control register	DTV_SAFE_RESET	R/W	0000_0001H
016CH	CFI safe reset control register	CFI_SAFE_RESET	R/W	0000_0001H
0170H	SDC safe reset control register	SDC_SAFE_RESET	R/W	0000_0001H
0174H	SDIO0 safe reset control register	SDIO0_SAFE_RESET	R/W	0000_0001H
0178H	SDIO1 safe reset control register	SDIO1_SAFE_RESET	R/W	0000_0001H
017CH	SDIO2 safe reset control register	SDIO2_SAFE_RESET	R/W	0000_0001H
0180H	USIA safe reset control register	USIA_SAFE_RESET	R/W	0000_0001H
0184H	USIB safe reset control register	USIB_SAFE RESET	R/W	0000_0001H
0188H	Reserved	–	–	–
018CH	CAM safe reset control register	CAM_SAFE_RESET	R/W	0000_0001H
0190H to 0198H	Reserved	–	–	–
019CH	AHB safe reset control register	AHB_SAFE_RESET	R/W	0000_0001H
01A0H	A3D safe reset control register	A3D_SAFE_RESET	R/W	0000_0001H
01A4H	AVE safe reset control register	AVE_SAFE_RESET	R/W	0000_0001H
01A8H	SIZ safe reset control register	SIZ_SAFE_RESET	R/W	0000_0001H
01ACH	ROT safe reset control register	ROT_SAFE_RESET	R/W	0000_0001H
01B0H	IMC safe reset control register	IMC_SAFE_RESET	R/W	0000_0001H
01B4H	IMCW safe reset control register	IMCW_SAFE_RESET	R/W	0000_0001H
01B8H	M2M safe reset control register	M2M_SAFE_RESET	R/W	0000_0001H
01BCH	M2P safe reset control register	M2P_SAFE_RESET	R/W	0000_0001H
01C0H	P2M safe reset control register	P2M_SAFE_RESET	R/W	0000_0001H
01C4H	Reserved	–	–	–
01C8H	Reset clock control specification register	RSTZ_CLKREQ	R/W	1F1F_1F1FH
01CCH	Reserved	–	–	–
01D0H	Watchdog timer forced reset control register	WDT_INT_RESET	R/W	0000_0000H
01D4H to 01D8H	Reserved	–	–	–
01DCH	Software interrupt source setting register	SFTWARE_INTGEN	R	0000_0000H
01E0H	Interrupt status register	INT_STATUS	R	0000_0000H
01E4H	Interrupt raw status register	INT_RAW_STATUS	R	0000_0000H
01E8H	Interrupt enable set register	INT_ENSET	R/W	0000_0000H
01ECH	Interrupt enable clear register	INT_ENCLR	R	0000_0000H
01F0H	Interrupt clear register	INT_CLEAR	R	0000_0000H
01F4H to 01FCH	Reserved	–	–	–
0200H	System PLL1 setting register 0	PLL1CTRL0	R/W	0001_04DDH
0204H	System PLL1 setting register 1	PLL1CTRL1	R/W	0000_00FFH
0208H	System PLL2 setting register 0	PLL2CTRL0	R/W	0000_0079H

Address	Register Name	Symbol	R/W	After Reset
020CH	System PLL2 setting register 1	PLL2CTRL1	R/W	0000_00FFH
0210H	System PLL3 setting register 0	PLL3CTRL0	R/W	0000_0037H
0214H	System PLL3 setting register 1	PLL3CTRL1	R/W	0000_0000H
0218H	PLL4 serial clock setting register 0	PLL4CTRL0	R/W	0000_0079H
021CH	PLL4 serial clock setting register 1	PLL4CTRL1	R/W	0000_00FFH
0220H	System OSC0 setting register	OSC0CTRL1	R/W	0000_00FFH
0224H	System OSC1 setting register	OSC1CTRL1	R/W	0000_00FFH
0228H	PLL lockup time setting register 0	PLLLOCKTIME0	R/W	0022_0022H
022CH	PLL lockup time setting register 1	PLLLOCKTIME1	R/W	0022_0032H
0230H	OSC lockup time setting register	OSCLOCKTIME	R/W	0022_0022H
0234H	PLL status register	PLL_STATUS	R	0000_0000H
0238H	ROSC setting register	ROSCCTRL1	R/W	0000_0000H
023CH to 0244H	Reserved	–	–	–
0248H	OSC setting register	OSC_CX	R/W	0000_0000H
024CH to 02ECH	Reserved	–	–	–
02F0H	Automatic PLL standby mode register	AUTO_PLL_STANDBY	R/W	0000_0002H
02F4H	Automatic mode transition enable register	AUTO_MODE_EN	R/W	0000_0000H
02F8H to 02FCH	Reserved	–	–	–
0300H	Clock mode select register	CLK_MODE_SEL	R/W	0000_0F00H
0304H	SMU-MEMC handshaking switch register	MEMC_HAND_SHAKE_FAKE	R/W	0000_0000H
0308H to 0318H	Reserved	–	–	–
031CH	PLL select register	CKMODE_PLLSEL	R/W	D00C_0000H
0320H	Normal mode A clock frequency division setting register	NORMALA_DIV	R/W	0531_5100H
0324H	Normal mode B clock frequency division setting register	NORMALB_DIV	R/W	0531_5100H
0328H	Normal mode C clock frequency division setting register	NORMALC_DIV	R/W	0531_5100H
032CH	Normal mode D clock frequency division setting register	NORMALD_DIV	R/W	0531_5100H
0330H	Power-on mode clock frequency division setting register	POWERON_DIV	R/W	0777_7707H
0334H	Economy mode clock frequency division setting register	ECONOMY_DIV	R/W	0531_5100H
0338H	Sleep mode clock frequency division setting register	SLEEP_DIV	R/W	0555_5500H
033CH to 034CH	Reserved	–	–	–
0350H	MEMC_CLK270 switch register	MEMCCLK270_SEL	R/W	0000_0000H
0354H	Reserved	–	–	–
0358H	CPU_CLK synchronous/asynchronous switch register	CPUCLK_SYNCSET	R/W	0003_0101H
035CH	CPU_CLK source clock select register	CPUCLK_ASYNC_MODE	R/W	0000_0100H
0360H	AB_CLK delay adjustment register	FLA_CLK_DLY	R/W	0000_1000H
0364H	AB_CLK stop status setting register	FLASHCLK_CTRL	R/W	0000_0000H
0368H to 037CH	Reserved	–	–	–

Address	Register Name	Symbol	R/W	After Reset
0380H	AHB macro clock control register 0	AHBCLKCTRL0	R/W	0000_0000H
0384H	AHB macro clock control register 1	AHBCLKCTRL1	R/W	0000_0000H
0388H	AHB macro clock control register 2	AHBCLKCTRL2	R/W	0000_0000H
038CH	AHB macro clock control register 3	AHBCLKCTRL3	R/W	0000_0000H
0390H	APB macro clock control register 0	APBCLKCTRL0	R/W	1173_0331H
0394H	APB macro clock control register 1	APBCLKCTRL1	R/W	0133_3137H
0398H	APB macro clock control register 2	APBCLKCTRL2	R/W	1331_6FFFH
039CH	Asynchronous macro clock control register	CLKCTRL	R/W	0000_0000H
03A0H	AVE macro clock control register	AVECLKCTRL	R/W	0000_0000H
03A4H to 03C4H	Reserved	–	–	–
03C8H	Access start timing setting register0	ACNT0	R/W	0000_0000H
03CCH	Access start timing setting register1	ACNT1	R/W	0000_0000H
03D0H	Transaction states register	TRANEXIST	R	0000_0000H
03D4H to 03FCH	Reserved	–	–	–
0400H	CPU clock gate control register	CPUGCLKCTRL	R/W	0000_0007H
0404H	Reserved	–	–	–
0408H	GIO clock gate control register	GIOGCLKCTRL	R/W	0000_0003H
040CH	INTA clock gate control register	INTAGCLKCTRL	R/W	0000_0007H
0410H	CHG clock gate control register	CHGGCLKCTRL	R/W	0000_0003H
0414H	BUS0 clock gate control register	BUS0GCLKCTRL	R/W	0000_0003H
0418H	BUS1 clock gate control register	BUS1GCLKCTRL	R/W	0000_0003H
041CH	PBL0 clock gate control register	PBL0GCLKCTRL	R/W	0000_0001H
0420H	PBL1 clock gate control register	PBL1GCLKCTRL	R/W	0000_0001H
0424H	AHB clock gate control register	AHBGCLKCTRL	R/W	0000_0003H
0428H	P2M clock gate control register	P2MGCLKCTRL	R/W	0000_0007H
042CH	M2P clock gate control register	M2PGCLKCTRL	R/W	0000_0007H
0430H	M2M clock gate control register	M2MGCLKCTRL	R/W	0000_0003H
0434H	PMU clock gate control register	PMUGCLKCTRL	R/W	0000_0003H
0438H	SRC clock gate control register	SRCGCLKCTRL	R/W	0000_0001H
043CH	ROM clock gate control register	ROMGCLKCTRL	R/W	0000_0001H
0440H	AB clock gate control register	ABGCLKCTRL	R/W	0000_0001H
0444H	FLA clock gate control register	FLAGCLKCTRL	R/W	0000_0000H
0448H	MEMC clock gate control register	MEMCGCLKCTRL	R/W	0000_000FH
044CH	LCD clock gate control register	LCDGCLKCTRL	R/W	0000_000BH
0450H	IMC clock gate control register	IMCGCLKCTRL	R/W	0000_0003H
0454H	IMCW clock gate control register	IMCWGCLKCTRL	R/W	0000_0003H
0458H	SIZ clock gate control register	SIZGCLKCTRL	R/W	0000_0003H
045CH	ROT clock gate control register	ROTGCLKCTRL	R/W	0000_0003H
0460H	Reserved	–	–	–
0464H	AVE clock gate control register	AVEGCLKCTRL	R/W	0000_0005H
0468H	A3D clock gate control register	A3DGCLKCTRL	R/W	0000_0003H

Address	Register Name	Symbol	R/W	After Reset
046CH	DTV clock gate control register	DTVGCLKCTRL	R/W	0000_0007H
0470H	NTS clock gate control register	NTSGCLKCTRL	R/W	0000_0003H
0474H	CAM clock gate control register	CAMGCLKCTRL	R/W	0000_0003H
0478H to 0480H	Reserved	–	–	–
0484H	PWM clock gate control register	PWMGCLKCTRL	R/W	0000_0001H
0488H	Reserved	–	–	–
048CH	IIC0 clock gate control register	IIC0GCLKCTRL	R/W	0000_0001H
0490H	IIC1 clock gate control register	IIC1GCLKCTRL	R/W	0000_0001H
0494H	USB clock gate control register	USBGCLKCTRL	R/W	0000_0003H
0498H	USIAS0 clock gate control register	USIAS0GCLKCTRL	R/W	0000_0007H
049CH	USIAS1 clock gate control register	USIAS1GCLKCTRL	R/W	0000_0005H
04A0H	USIAU0 clock gate control register	USIAU0GCLKCTRL	R/W	0000_0003H
04A4H	Reserved	–	–	–
04A8H	USIBS2 clock gate control register	USIBS2GCLKCTRL	R/W	0000_0005H
04ACH	USIBS3 clock gate control register	USIBS3GCLKCTRL	R/W	0000_0005H
04B0H	USIBS4 clock gate control register	USIBS4GCLKCTRL	R/W	0000_0005H
04B4H	USIBS5 clock gate control register	USIBS5GCLKCTRL	R/W	0000_0005H
04B8H	USIBU1 clock gate control register	USIBU1GCLKCTRL	R/W	0000_0001H
04BCH	USIBU2 clock gate control register	USIBU2GCLKCTRL	R/W	0000_0001H
04C0H	USIBU3 clock gate control register	USIBU3GCLKCTRL	R/W	0000_0001H
04C4H	Reserved	–	–	–
04C8H	SDIO0 clock gate control register	SDIO0GCLKCTRL	R/W	0000_0005H
04CCH	SDIO1 clock gate control register	SDIO1GCLKCTRL	R/W	0000_0005H
04D0H	SDIO2 clock gate control register	SDIO2GCLKCTRL	R/W	0000_0005H
04D4H	SDC clock gate control register	SDCGCLKCTRL	R/W	0000_0005H
04D8H	Reserved	–	–	–
04DCH	CFI clock gate control register	CFIGCLKCTRL	R/W	0000_0006H
04E0H to 04E8H	Reserved	–	–	–
04ECH	TI0 clock gate control register	TI0GCLKCTRL	R/W	0000_0001H
04F0H	TI1 clock gate control register	TI1GCLKCTRL	R/W	0000_0001H
04F4H	TI2 clock gate control register	TI2GCLKCTRL	R/W	0000_0001H
04F8H	TI3 clock gate control register	TI3GCLKCTRL	R/W	0000_0001H
04FCH	TG0 clock gate control register	TG0GCLKCTRL	R/W	0000_0001H
0500H	TG1 clock gate control register	TG1GCLKCTRL	R/W	0000_0001H
0504H	TG2 clock gate control register	TG2GCLKCTRL	R/W	0000_0001H
0508H	TG3 clock gate control register	TG3GCLKCTRL	R/W	0000_0001H
050CH	TG4 clock gate control register	TG4GCLKCTRL	R/W	0000_0001H
0510H	TG5 clock gate control register	TG5GCLKCTRL	R/W	0000_0001H
0514H	TW0 clock gate control register	TW0GCLKCTRL	R/W	0000_0001H
0518H	TW1 clock gate control register	TW1GCLKCTRL	R/W	0000_0001H
051CH	TW2 clock gate control register	TW2GCLKCTRL	R/W	0000_0001H

Address	Register Name	Symbol	R/W	After Reset
0520H	TW3 clock gate control register	TW3GCLKCTRL	R/W	0000_0001H
0524H	TIM clock gate control register	TIMGCLKCTRL	R/W	0000_0001H
0528H	STI clock gate control register	STIGCLKCTRL	R/W	0000_0003H
052CH	Reserved	–	–	–
0530H	AFS clock gate control register	AFSGCLKCTRL	R/W	0000_0003H
0534H to 0538H	Reserved	–	–	–
053CH	REF clock gate control register	REFGCLKCTRL	R/W	0000_0000H
0540H	TW4 clock gate control register	TW4GCLKCTRL	R/W	0000_0001H
0544H to 0550H	Reserved	–	–	–
0554H	PDMA clock gate control register	PDMAGCLKCTRL	R/W	0000_0001H
0558H to 05FCH	Reserved	–	–	–
0600H	TW0_TIN/TI0_TIN setting register	TWI0TIN_SEL	R/W	0001_0001H
0604H	TW1_TIN/TI1_TIN setting register	TWI1TIN_SEL	R/W	0001_0001H
0608H	TW2_TIN/TI2_TIN setting register	TWI2TIN_SEL	R/W	0001_0001H
060CH	TW3_TIN/TI3_TIN setting register	TWI3TIN_SEL	R/W	0001_0001H
0610H	TG0-TG5_TIN setting register	TGNTIN_SEL	R/W	0011_1111H
0614H	Timer clock frequency division setting register	TIMCLKDIV	R/W	0000_00FFH
0618H	USIA_SCLK clock frequency division setting register	USIASCLKDIV	R/W	000F_000FH
061CH	USIB_SCLK clock frequency division setting register	USIBSCLKDIV	R/W	0000_0005H
0620H	Reserved	–	–	–
0624H	IIC_SCLK frequency division setting register	IICSCLKDIV	R/W	002F_002FH
0628H	USB_SCLK frequency division setting register	USBSCLKDIV	R/W	0007_0000H
062CH	MEMC_RCLK frequency division setting register	MEMCRCLKDIV	R/W	0000_000FH
0630H	LCD_LCLK frequency division setting register	LCDLCLKDIV	R/W	0000_0009H
0634H to 0644H	Reserved	–	–	–
0648H	SDIO0_SCLK frequency division setting register	SDIO0SCLKDIV	R/W	0000_0005H
064CH	SDIO1_SCLK frequency division setting register	SDIO1SCLKDIV	R/W	0000_0005H
0650H	SDIO2_SCLK frequency division setting register	SDIO2SCLKDIV	R/W	0000_0005H
0654H	USIB0_SCLK frequency division setting register	USIB0SCLKDIV	R/W	000F_000FH
0658H	USIB1_SCLK frequency division setting register	USIB1SCLKDIV	R/W	000F_000FH
065CH	USIB2_SCLK frequency division setting register	USIB2SCLKDIV	R/W	0005_0005H
0660H	USIB3_SCLK frequency division setting register	USIB3SCLKDIV	R/W	0000_0005H
0664H to 0668H	Reserved	–	–	–
066CH	PWM_PWCLK frequency division setting register	PWMPWCLKDIV	R/W	0013_0013H
0670H	CAM_SCLK frequency division setting register	CAMSCLKDIV	R/W	0000_0019H
0674H to 0678H	Reserved	–	–	–
067CH	A3D_CORE_CLK frequency division setting register	A3DCORECLKDIV	R/W	0000_0000H
0680H	AVE_CCLK frequency division setting register	AVECCLKDIV	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
0684H	QR_CLK frequency division setting register	QRCLKDIV	R/W	0000_0001H
0688H	STI_SCLK source select register	STI_CLKSEL	R/W	0000_0000H
068CH	REF_CLKO frequency division setting register	REFCLKDIV	R/W	0000_0005H
0690H to 0694H	Reserved	–	–	–
0698H	TW4_TIN setting register	TW4TIN_SEL	R/W	0000_0001H
069CH	INTA_TCLK setting register	INTA_CLKSEL	R/W	0000_0000H
06A0H to 06DCH	Reserved	–	–	–
06E0H	32.768 kHz clock status register	CLK32_STATUS	R	0000_0000H
06E4H to 06ECH	Reserved	–	–	–
06F0H	Clock stop instruction signal status register	CLKSTOPSIG_ST	R	0000_0000H
06F4H to 06FCH	Reserved	–	–	–
0700H	Automatic frequency switch control REQMASK0 register	CKRQMODE_MASK0	R/W	0001_0000H
0704H	Automatic frequency switch control REQMASK1 register	CKRQMODE_MASK1	R/W	7FFE_FFFFH
0708H	Automatic frequency switch control register	CKRQ_MODE	R/W	F000_0000H
070CH	Reserved	–	–	–
0710H	Automatic frequency control FIFO space mode setting register	DFS_FIFOMODE	R/W	0000_0000H
0714H	Automatic frequency switch control register	DFS_FIFO_REQMASK	R/W	0000_0007H
0718H	Automatic frequency control LCD_FIFO threshold register	LCD_FIFOTHRESHOLD	R/W	0000_0000H
071CH	Automatic frequency control CAM_FIFO threshold register	CAM_FIFOTHRESHOLD	R/W	0000_0000H
0720H to 072CH	Reserved	–	–	–
0730H	Automatic frequency control domain clock division switch mode register	AUTO_DMDIVCNG_MODE	R/W	0000_0000H
0734H	Automatic frequency control domain clock division switch parameter register	AUTO_DMDIVCNG_PARAM	R/W	0531_5100H
0738H to 07BCH	Reserved	–	–	–
07C0H	General-purpose register 0	GENERAL_REG0	R/W	0000_0000H
07C4H	General-purpose register 1	GENERAL_REG1	R/W	0000_0000H
07C8H to 07ECH	Reserved	–	–	–
07F0H	Low power register	LOWPWR	R/W	0000_0000H
07F4H	PLL power stabilization time setting register	PLLVDDWAIT	R/W	0000_0000H
07F8H to 07FCH	Reserved	–	–	–
0800H	P0 power switch, R-FF/R-RAM control register	P0_POWERSW	R/W	3300_0000H
0804H	Reserved	–	–	–
0808H	PU power switch, R-FF/R-RAM control register	PU_POWERSW	R/W	3300_0000H
080CH	PM power switch, R-FF/R-RAM control register	PM_POWERSW	R/W	3300_0000H

Address	Register Name	Symbol	R/W	After Reset
0810H	PL power switch, R-FF/R-RAM control register	PL_POWERSW	R/W	3300_0000H
0814H	Reserved	–	–	–
0818H	P1 power switch, R-FF/R-RAM control register	P1_POWERSW	R/W	3300_0000H
081CH	P2 power switch, R-FF/R-RAM control register	P2_POWERSW	R/W	3300_0000H
0820H	PG power switch, R-FF/R-RAM control register	PG_POWERSW	R/W	3300_0000H
0824H	PV power switch, R-FF/R-RAM control register	PV_POWERSW	R/W	3300_0000H
0828H	PR power switch control register	PR_POWERSW	R/W	0001_0000H
082CH	Power domain status monitor register	POWER_STATUS	R	0000_0000H
0830H	Power switch control sequencer status monitor register	SEQ_BUSY	R	0000_0000H
0834H	Automatic P0 power control register	P0_SWON	R/W	0000_0001H
0838H	Reserved	–	–	–
083CH	Automatic PU power control register	PU_SWON	R/W	0000_0001H
0840H	Automatic PM power control register	PM_SWON	R/W	0000_0001H
0844H	Automatic PL power control register	PL_SWON	R/W	0000_0001H
0848H	Reserved	–	–	–
084CH	Automatic P1 power control register	P1_SWON	R/W	0000_0001H
0850H	Automatic P2 power control register	P2_SWON	R/W	0000_0001H
0854H	Automatic PG power control register	PG_SWON	R/W	0000_0001H
0858H	Automatic PV power control register	PV_SWON	R/W	0000_0001H
085CH	Automatic PR power control register	PR_SWON	R/W	0000_0001H
0860H	P0 power RFF/RRAM control signal input interval setting register 0	P0_RFF_PARA0	R/W	0404_0404H
0864H	P0 power RFF/RRAM control signal input interval setting register 1	P0_RFF_PARA1	R/W	0004_0404H
0868H	P0 power turn-on interval setting register	P0_PWSW_PARA	R/W	0000_0085H
086CH to 0874H	Reserved	–	–	–
0878H	PU power RFF/RRAM control signal input interval setting register 0	PU_RFF_PARA0	R/W	0404_0404H
087CH	PU power RFF/RRAM control signal input interval setting register 1	PU_RFF_PARA1	R/W	0004_0404H
0880H	PU power turn-on interval setting register	PU_PWSW_PARA	R/W	0000_0085H
0884H	PM power RFF/RRAM control signal input interval setting register 0	PM_RFF_PARA0	R/W	0404_0404H
0888H	PM power RFF/RRAM control signal input interval setting register 1	PM_RFF_PARA1	R/W	0004_0404H
088CH	PM power turn-on interval setting register	PM_PWSW_PARA	R/W	0000_0085H
0890H	PL power RFF/RRAM control signal input interval setting register 0	PL_RFF_PARA0	R/W	0404_0404H
0894H	PL power RFF/RRAM control signal input interval setting register 1	PL_RFF_PARA1	R/W	0004_0404H
0898H	PL power turn-on interval setting register	PL_PWSW_PARA	R/W	0000_0085H
089CH to 08A4H	Reserved	–	–	–
08A8H	P1 power RFF/RRAM control signal input interval setting	P1_RFF_PARA0	R/W	0404_0404H

Address	Register Name	Symbol	R/W	After Reset
	register 0			
08ACH	P1 power RFF/RRAM control signal input interval setting register 1	P1_RFF_PARA1	R/W	0004_0B04H
08B0H	P1 power turn-on interval setting register	P1_PWSW_PARA	R/W	0000_0085H
08B4H	P2 power RFF/RRAM control signal input interval setting register 0	P2_RFF_PARA0	R/W	0404_0404H
08B8H	P2 power RFF/RRAM control signal input interval setting register 1	P2_RFF_PARA1	R/W	0004_0B04H
08BCH	P2 power turn-on interval setting register	P2_PWSW_PARA	R/W	0000_0085H
08C0H	PG power RFF/RRAM control signal input interval setting register 0	PG_RFF_PARA0	R/W	0404_0404H
08C4H	PG power RFF/RRAM control signal input interval setting register 1	PG_RFF_PARA1	R/W	0004_0404H
08C8H	PG power turn-on interval setting register	PG_PWSW_PARA	R/W	0000_0085H
08CCH	PV power RFF/RRAM control signal input interval setting register 0	PV_RFF_PARA0	R/W	0404_0404H
08D0H	PV power RFF/RRAM control signal input interval setting register 1	PV_RFF_PARA1	R/W	0004_0404H
08D4H	PV power turn-on interval setting register	PV_PWSW_PARA	R/W	0000_0085H
08D8H	PR power RFF/RRAM control signal input interval setting register 0	PR_RFF_PARA0	R/W	0000_0004H
08DCH	PR power RFF/RRAM control signal input interval setting register 1	PR_RFF_PARA1	R/W	0000_0004H
08E0H	PR power turn-on interval setting register	PR_PWSW_PARA	R/W	0000_0085H
08E4H to 0988H	Reserved	–	–	–
098CH	CPU RAM power switch register	CPU_PWSW_L2RAM	R/W	0000_0000H
0990H	CPU logic power switch register	CPU_PWSW_LOGIC	R/W	0000_0000H
0994H	CPU RAM power switch register	CPU_PWSW_L1RAM	R/W	0000_0000H
0998H	CPU RAM PD control register	CPU_SRAM_PD	R/W	0000_0000H
099CH	CPU power switch control register	CPU_PWSW_CTRL	R/W	0000_0007H
09A0H	CPU power status register	CPU_POWER_STATUS	R	0000_0000H
09A4H	CPU power switch sequencer status register	CPU_SEQ_BUSY	R	0000_0000H
09A8H to 09B0H	Reserved	–	–	–
09B4H	QR WFE setting register	QR_WFE	R/W	0000_0000H
09B8H	QR WFI setting register	QR_WFI	R/W	0000_0000H
09BCH	CPU NEON enable register	CPU_NEON_ENABLE	R/W	0000_0003H
09C0H	Reserved	–	–	–
09C4H	QR DSIIDEOFF setting register	QR_DSIIDEOFF	R/W	0000_0000H
09C8H to 09CCH	Reserved	–	–	–
09D0H	CPU DS0 power automatic control register	DS0_SWON	R/W	0000_0001H
09D4H	CPU DS1 power automatic control register	DS1_SWON	R/W	0000_0001H
09D8H	CPU HM power automatic control register	HM_SWON	R/W	0000_0001H
09DCH	CPU PE0 power automatic control register	PE0_SWON	R/W	0000_0001H

Address	Register Name	Symbol	R/W	After Reset
09E0H	CPU PE1 power automatic control register	PE1_SWON	R/W	0000_0001H
09E4H	CPU NE0 power automatic control register	NE0_SWON	R/W	0000_0001H
09E8H	CPU NE1 power automatic control register	NE1_SWON	R/W	0000_0001H
09ECH	PC power RFF control parameter register 0	PC_RFF_PARA0	R/W	0000_0404H
09F0H	PC power switch control parameter register	PC_PWSW_PARA	R/W	0000_0085H
09F4H	QR WAIT count setting register	QR_WAITCNT	R/W	0000_0000H
09F8H to 0A2CH	Reserved	–	–	–
0A30H	PMU interrupt source control register	PMU_INTCTRL	R/W	0000_0000H
0A34H to 0A48H	Reserved	–	–	–
0A4CH	CPU ASSOCIATIVITY setting register0	CPU_ASSOCIATIVITY	R/W	0000_0000H
0A50H	CPU WAYSIZE setting register	CPU_WAYSIZE	R/W	0000_0002H
0A54H	CPU CFGADDRSET setting register1	CPU_CFGADDRSET	R/W	0000_0000H
0A58H	CPU CFGADDRFILT setting register	CPU_CFGADDRFILT	R/W	0000_0000H
0A5CH	Reserved	–	–	–
0A60H	CPU SCU address filter enable register	CPU_FILTEREN	R/W	0000_0000H
0A64H	CPU SCU access address setting register	CPU_FILTERADDR	R/W	0000_0000H
0A68H to 0A6CH	Reserved	–	–	–
0A70H	CPU COH setting register	CPU_COH	R/W	0000_0000H
0A74H to 0ADCH	Reserved	–	–	–
0AE0H	ICEREG_DATA[31:0] read register	ICEREG_DATA0	R	0000_0000H
0AE4H	ICEREG_DATA[63:32] read register	ICEREG_DATA1	R	0000_0000H
0AE8H	ICEREG_DATA[95:64] read register	ICEREG_DATA2	R	0000_0000H
0AECH	ICEREG_DATA[127:96] read register	ICEREG_DATA3	R	0000_0000H
0AF0H	ICEREG_DATA[159:128] read register	ICEREG_DATA4	R	0000_0000H
0AF4H	ICEREG_DATA[191:160] read register	ICEREG_DATA5	R	0000_0000H
0AF8H	ICEREG_DATA[223:192] read register	ICEREG_DATA6	R	0000_0000H
0AFCH	ICEREG_DATA[255:224] read register	ICEREG_DATA7	R	00FA_0000H
0B00H	CP15S disable status register	R_CP15SDISABLE	R	0111_0100H
0B04H to 1008H	Reserved	–	–	–
100CH	SMU control register	SMU_CONTROL	R/W	0000_0000H
1010H	Automatic frequency switch control REQMASK2 register	CKRQMODE_MASK2	R/W	0000_0000H
1014H	Reserved	–	–	–
1018H	MEMC hand shake enable register	MEMCHSENA_AFRQ	R/W	0000_0000H
101CH to 1FFCH	Reserved	–	–	–
2000H	Chip revision register	CHIP_REVISION	R/W	0000_0030H
2004H to FFFCH	Reserved	–	–	–

(2) S2 domain registers

Address	Register Name	Symbol	R/W	After Reset
0000H	CP15S disable setting register	CP15SDISABLE	R/W	0111_0100H
0004H	CPU SCU secure register protect setting register	CPU_CFGSDISABLE	R/W	0000_0000H
0008H	INT_TIMSEL control register	INT_TIMSEL	R/W	0000_0000H
000CH to FFFCH	Reserved	–	–	–

A.11 Alternate Function Switching (CHG)

Base address: E014_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Boot mode register	CHG_BOOT_MODE	R	–
0004H	P[0:2]/PL OFF data hold control register	CHG_PIN_LAT	R/W	0000_2222H
0008H to 0100H	Reserved	–	–	–
0104H	SDIO[2:0]/SDC interrupt mask register	CHG_CTRL_SDINT	R/W	0000_000FH
0108H	AB0 (ASYNC) boot switch register	CHG_CTRL_AB0_BOOT	R/W	0000_0000H
010CH	Reserved	–	–	–
0110H	1.8 V/3.3 V LCD enable register	CHG_LCD_ENABLE	R/W	0000_0003H
0114H to 01FCH	Reserved	–	–	–
0200H	GPIO[31:0] pin function selection register	CHG_PINSEL_G000	R/W	FFFF_FFFBH
0204H	GPIO[63:32] pin function selection register	CHG_PINSEL_G032	R/W	3E06_0FFFH
0208H	GPIO[95:64] pin function selection register	CHG_PINSEL_G064	R/W	FFFF_FFF0H
020CH	GPIO[127:96] pin function selection register	CHG_PINSEL_G096	R/W	FFFE_07FFH
0210H	GPIO[158:128] pin function selection register	CHG_PINSEL_G128	R/W	787F_FFFFH
0214H to 0280H	Reserved	–	–	–
0284H	3.3 V LCD pin function selection register	CHG_PINSEL_LCD3	R/W	0000_0000H
0288H	UART pin function selection register	CHG_PINSEL_UART	R/W	0000_0000H
028CH	IIC pin function selection register	CHG_PINSEL_IIC	R/W	0000_0000H
0290H	Reserved	–	–	–
0294H	AB pin function selection register	CHG_PINSEL_AB	R/W	0000_0000H
0298H	USI pin function selection register	CHG_PINSEL_USI	R/W	0000_0000H
029CH to 02A4H	Reserved	–	–	–
02A8H	HSI pin function selection register	CHG_PINSEL_HSI	R/W	0000_0000H
02ACH to 02FCH	Reserved	–	–	–
0300H	Pull-up/pull-down/input enable/Schmitt trigger control register 0	CHG_PULL0	R/W	3333_3333H
0304H	Pull-up/pull-down/input enable/Schmitt trigger control register 1	CHG_PULL1	R/W	3300_0003H
0308H	Pull-up/pull-down/input enable/Schmitt trigger control register 2	CHG_PULL2	R/W	3333_3333H
030CH	Pull-up/pull-down/input enable/Schmitt trigger control register 3	CHG_PULL3	R/W	0000_0333H
0310H	Pull-up/pull-down/input enable/Schmitt trigger control register 4	CHG_PULL4	R/W	0333_3333H
0314H	Pull-up/pull-down/input enable/Schmitt trigger control register 5	CHG_PULL5	R/W	3333_3333H
0318H	Pull-up/pull-down/input enable/Schmitt trigger control register 6	CHG_PULL6	R/W	0333_3333H

Address	Register Name	Symbol	R/W	After Reset
031CH	Pull-up/pull-down/input enable/Schmitt trigger control register 7	CHG_PULL7	R/W	0000_0113H
0320H	Pull-up/pull-down/input enable/Schmitt trigger control register 8	CHG_PULL8	R/W	7777_7770H
0324H	Pull-up/pull-down/input enable/Schmitt trigger control register 9	CHG_PULL9	R/W	7777_7777H
0328H	Pull-up/pull-down/input enable/Schmitt trigger control register 10	CHG_PULL10	R/W	0000_3337H
032CH	Pull-up/pull-down/input enable/Schmitt trigger control register 11	CHG_PULL11	R/W	0000_0000H
0330H	Pull-up/pull-down/input enable/Schmitt trigger control register 12	CHG_PULL12	R/W	0033_3333H
0334H	Pull-up/pull-down/input enable/Schmitt trigger control register 13	CHG_PULL13	R/W	3003_3333H
0338H	Pull-up/pull-down/input enable/Schmitt trigger control register 14	CHG_PULL14	R/W	3333_3003H
033CH	Pull-up/pull-down/input enable/Schmitt trigger control register 15	CHG_PULL15	R/W	0033_3333H
0340H	Pull-up/pull-down/input enable/Schmitt trigger control register 16	CHG_PULL16	R/W	0333_3333H
0344H	Pull-up/pull-down/input enable/Schmitt trigger control register 17	CHG_PULL17	R/W	0003_3333H
0348H	Pull-up/pull-down/input enable/Schmitt trigger control register 18	CHG_PULL18	R/W	3003_0033H
034CH	Pull-up/pull-down/input enable/Schmitt trigger control register 19	CHG_PULL19	R/W	3333_3333H
0350H	Pull-up/pull-down/input enable/Schmitt trigger control register 20	CHG_PULL20	R/W	00B3_3733H
0354H	Pull-up/pull-down/input enable/Schmitt trigger control register 21	CHG_PULL21	R/W	3333_3333H
0358H	Pull-up/pull-down/input enable/Schmitt trigger control register 22	CHG_PULL22	R/W	0FF0_F0D3H
035CH to 0360H	Reserved	–	–	–
0364H	Pull-up/pull-down/input enable/Schmitt trigger control register 25	CHG_PULL25	R/W	0000_0303H
0368H to 03FCH	Reserved	–	–	–
0400H	Driving capability selection register 0	CHG_DRIVE0	R/W	0000_0000H
0404H	Driving capability selection register 1	CHG_DRIVE1	R/W	0000_0000H
0408H	Driving capability selection register 2	CHG_DRIVE2	R/W	AAAA_AA2AH
040CH	Driving capability selection register 3	CHG_DRIVE3	R/W	0000_0000H
0410H	Driving capability selection register 4	CHG_DRIVE4	R/W	0000_0000H
0414H	Driving capability selection register 5	CHG_DRIVE5	R/W	0000_0020H
0418H to 04FCH	Reserved	–	–	–
0500H	Bus hold function on/off switching register	CHG_BUSHOLD	R/W	0000_FFFFH
0504H to	Reserved	–	–	–

Address	Register Name	Symbol	R/W	After Reset
050CH				
0510H	AB_CLK output selection register	CHG_FLASHCLK_SEL	R/W	0000_0000H
0514H to 05FCH	Reserved	–	–	–
0600H	3.3 V LCD delay/phase setting register	CHG_DELAY_LCD33	R/W	1000_0000H
0604H to 0608H	Reserved	–	–	–
060CH	AB_CLK delay/phase setting register	CHG_DELAY_AB	R/W	0000_1000H
0610H to 0614H	Reserved	–	–	–
0618H	3.3 V ICE delay/phase setting register	CHG_DELAY_ICEA33	R/W	1000_1000H
061CH	1.8 V ICE delay/phase setting register	CHG_DELAY_ICEA18	R/W	1000_1000H
0620H to 07C0H	Reserved	–	–	–
07C4H	CHGREG reset control register (for testing)	CHG_RST_CTRL	R/W	0000_0000H
07C8H to FFFCH	Reserved	–	–	–

A.12 System Timer (STI)

Base address: E018_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Control register	STI_CONTROL	R/W ,W	0000_0000H
0004H to 000CH	Reserved	–	–	–
0010H	Timer compare register A (higher 16 bits)	STI_COMPA_H	R/W	0000_FFFFH
0014H	Timer compare register A (lower 32 bits)	STI_COMPA_L	R/W	FFFF_FFFFH
0018H	Timer compare register B (higher 16 bits)	STI_COMPB_H	R/W	0000_FFFFH
001CH	Timer compare register B (lower 32 bits)	STI_COMPB_L	R/W	FFFF_FFFFH
0020H	Synchronous timer count value register (higher 16 bits)	STI_COUNT_H	R	0000_0000H
0024H	Synchronous timer count value register (lower 32 bits)	STI_COUNT_L	R	0000_0000H
0028H	Asynchronous timer count value register (higher 16 bits)	STI_COUNT_RAW_H	R	0000_0000H
002CH	Asynchronous timer count value register (lower 32 bits)	STI_COUNT_RAW_L	R	0000_0000H
0030H	Counter value set register (higher 16 bits)	STI_SET_H	R/W ,W	0000_0000H
0034H	Counter value set register (lower 32 bits)	STI_SET_L	R/W	0000_0000H
0038H to 003CH	Reserved	–	–	–
0040H	Interrupt status register	STI_INTSTATUS	R	0000_0000H
0044H	Interrupt raw status register	STI_INTRAWSTATUS	R	0000_0000H
0048H	Interrupt enable set register	STI_INTENSET	R,W	0000_0000H
004CH	Interrupt enable clear register	STI_INTENCLR	W	0000_0000H
0050H	Interrupt source clear register	STI_INTFFCLR	W	0000_0000H
0054H to FFFCH	Reserved	–	–	–

A.13 UART Interface (UART)

Base address: UART0: E102_0000H
UART1: E103_0000H
UART2: E104_0000H
UART3: E105_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Receive buffer register	RBR	R	Undefined
	Transmit hold register	THR	W	
0004H	Interrupt enable register	IER	R/W	0000H
0008H	Interrupt identification register	IIR	R	0001H
000CH	FIFO control register	FCR	R/W	0000H
0010H	Line control register	LCR	R/W	0000H
0014H	Modem control register	MCR	R/W	0000H
0018H	Line status register	LSR	R	0060H
001CH	Modem status register	MSR	R	000xH Note
0020H	Scratch register	SCR	R/W	0000H
0024H	Divisor latch LS byte register	DLL	R/W Note2	0000H
0028H	Divisor latch MS byte register	DLM	R/W Note2	0000H
002CH	Hardware control register	HCR0	R/W	0000H
0030H	Hardware status register 2	HCR2	R	0000H
0034H	Hardware status register 3	HCR3	R	0000H
0038H to FFFCH	Reserved	–	–	–

Note. The value depends on the connected device.

A.14 DMA Controller (DMAC)

(1) M2P (Memory-to-peripheral) registers

Base address: E107_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	DMA start control register	CONT	W	0000_0000H
0004H	DMA control status register	CONTSTATUS	R	0000_0000H
0008H	DMA end control register	END	W	0000_0000H
000CH-00FCH	Reserved	–	–	–
0100H	Interrupt status register (LCH0 to LCH3)	LCH0LCH3_INT_CONT	R	0000_0000H
0104H	Interrupt raw status register (LCH0 to LCH3)	LCH0LCH3_INT_RAW	R	0000_0000H
0108H	Interrupt enable set register (LCH0 to LCH3)	LCH0LCH3_INT_ENABLE	R/W	0000_0000H
010CH	Interrupt enable clear register (LCH0 to LCH3)	LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
0110H	Interrupt source clear register (LCH0 to LCH3)	LCH0LCH3_INT_REQ_CL	W	0000_0000H
0114H-011CH	Reserved	–	–	–
0120H	Interrupt status register (LCH4 to LCH7)	LCH4LCH7_INT_CONT	R	0000_0000H
0124H	Interrupt raw status register (LCH4 to LCH7)	LCH4LCH7_INT_RAW	R	0000_0000H
0128H	Interrupt enable set register (LCH4 to LCH7)	LCH4LCH7_INT_ENABLE	R/W	0000_0000H
012CH	Interrupt enable clear register (LCH4 to LCH7)	LCH4LCH7_INT_ENABLE_CL	W	0000_0000H
0130H	Interrupt source clear register (LCH4 to LCH7)	LCH4LCH7_INT_REQ_CL	W	0000_0000H
0134H-0FFCH	Reserved	–	–	–
1000H	LCH0 source address register (start address)	LCH0_AADD	R/W	0000_0000H
1004H	LCH0 source address pointer register	LCH0_AADP	R	0000_0000H
1008H	LCH0 source address offset register	LCH0_AOFF	R/W	0000_0000H
100CH	LCH0 source block size register	LCH0_ASIZE	R/W	0000_0000H
1010H	LCH0 source block count regiaster	LCH0_ASIZE_COUNT	R/W	0000_0000H
1014H-101CH	Reserved	–	–	–
1020H	LCH0 destination address register (start address)	LCH0_BADD	R/W	0000_0000H
1024H-103CH	Reserved	–	–	–
1040H	LCH0 length register	LCH0_LENG	R/W	0000_0000H
1044H	LCH0 read length count register	LCH0_LENG_RCOUNT	R	0000_0000H
1048H	LCH0 write length count register	LCH0_LENG_WCOUNT	R	0000_0000H
104CH	Reserved	–	–	–
1050H	LCH0 mode register	LCH0_MODE	R/W	E4E4_0000H
1054H	LCH0 timer register	LCH0_TIME	R/W	0000_0000H
1058H	LCH0 timer count register	LCH0_TIME_COUNT	R	0000_0000H
105CH	LCH0 physical channel register	LCH0_PCH	R/W	0000_0000H
1060H-10FCH	Reserved	–	–	–
1100H	LCH1 source address register (start address)	LCH1_AADD	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
1104H	LCH1 source address pointer register	LCH1_AADP	R	0000_0000H
1108H	LCH1 source address offset register	LCH1_AOFF	R/W	0000_0000H
110CH	LCH1 source block size register	LCH1_ASIZE	R/W	0000_0000H
1110H	LCH1 source block count regiaster	LCH1_ASIZE_COUNT	R/W	0000_0000H
1114H-111CH	Reserved	–	–	–
1120H	LCH1 destination address register (start address)	LCH1_BADD	R/W	0000_0000H
1124H-113CH	Reserved	–	–	–
1140H	LCH1 length register	LCH1_LENG	R/W	0000_0000H
1144H	LCH1 read length count register	LCH1_LENG_RCOUNT	R	0000_0000H
1148H	LCH1 write length count register	LCH1_LENG_WCOUNT	R	0000_0000H
114CH	Reserved	–	–	–
1150H	LCH1 mode register	LCH1_MODE	R/W	E4E4_0000H
1154H-1158H	Reserved	–	–	–
115CH	LCH1 physical channel register	LCH1_PCH	R/W	0000_0000H
1160H-11FCH	Reserved	–	–	–
1200H	LCH2 source address register (start address)	LCH2_AADD	R/W	0000_0000H
1204H	LCH2 source address pointer register	LCH2_AADP	R	0000_0000H
1208H	LCH2 source address offset register	LCH2_AOFF	R/W	0000_0000H
120CH	LCH2 source block size register	LCH2_ASIZE	R/W	0000_0000H
1210H	LCH2 source block count regiaster	LCH2_ASIZE_COUNT	R/W	0000_0000H
1214H-121CH	Reserved	–	–	–
1220H	LCH2 destination address register (start address)	LCH2_BADD	R/W	0000_0000H
1224H-123CH	Reserved	–	–	–
1240H	LCH2 length register	LCH2_LENG	R/W	0000_0000H
1244H	LCH2 read length count register	LCH2_LENG_RCOUNT	R	0000_0000H
1248H	LCH2 write length count register	LCH2_LENG_WCOUNT	R	0000_0000H
124CH	Reserved	–	–	–
1250H	LCH2 mode register	LCH2_MODE	R/W	E4E4_0000H
1254H-1258H	Reserved	–	–	–
125CH	LCH2 physical channel register	LCH2_PCH	R/W	0000_0000H
1260H-12FCH	Reserved	–	–	–
1300H	LCH3 source address register (start address)	LCH3_AADD	R/W	0000_0000H
1304H	LCH3 source address pointer register	LCH3_AADP	R	0000_0000H
1308H	LCH3 source address offset register	LCH3_AOFF	R/W	0000_0000H
130CH	LCH3 source block size register	LCH3_ASIZE	R/W	0000_0000H
1310H	LCH3 source block count regiaster	LCH3_ASIZE_COUNT	R/W	0000_0000H
1314H-131CH	Reserved	–	–	–

Address	Register Name	Symbol	R/W	After Reset
1320H	LCH3 destination address register (start address)	LCH3_BADD	R/W	0000_0000H
1324H-133CH	Reserved	–	–	–
1340H	LCH3 length register	LCH3_LENG	R/W	0000_0000H
1344H	LCH3 read length count register	LCH3_LENG_RCOUNT	R	0000_0000H
1348H	LCH3 write length count register	LCH3_LENG_WCOUNT	R	0000_0000H
134CH	Reserved	–	–	–
1350H	LCH3 mode register	LCH3_MODE	R/W	E4E4_0000H
1354H-1358H	Reserved	–	–	–
135CH	LCH3 physical channel register	LCH3_PCH	R/W	0000_0000H
1360H-13FCH	Reserved	–	–	–
1400H	LCH4 source address register (start address)	LCH4_AADD	R/W	0000_0000H
1404H	LCH4 source address pointer register	LCH4_AADP	R	0000_0000H
1408H	LCH4 source address offset register	LCH4_AOFF	R/W	0000_0000H
140CH	LCH4 source block size register	LCH4_ASIZE	R/W	0000_0000H
1410H	LCH4 source block count regiaster	LCH4_ASIZE_COUNT	R/W	0000_0000H
1414H-141CH	Reserved	–	–	–
1420H	LCH4 destination address register (start address)	LCH4_BADD	R/W	0000_0000H
1424H-143CH	Reserved	–	–	–
1440H	LCH4 length register	LCH4_LENG	R/W	0000_0000H
1444H	LCH4 read length count register	LCH4_LENG_RCOUNT	R	0000_0000H
1448H	LCH4 write length count register	LCH4_LENG_WCOUNT	R	0000_0000H
144CH	Reserved	–	–	–
1450H	LCH4 mode register	LCH4_MODE	R/W	E4E4_0000H
1454H-1458H	Reserved	–	–	–
145CH	LCH4 physical channel register	LCH4_PCH	R/W	0000_0000H
1460H-14FCH	Reserved	–	–	–
1500H	LCH5 source address register (start address)	LCH5_AADD	R/W	0000_0000H
1504H	LCH5 source address pointer register	LCH5_AADP	R	0000_0000H
1508H	LCH5 source address offset register	LCH5_AOFF	R/W	0000_0000H
150CH	LCH5 source block size register	LCH5_ASIZE	R/W	0000_0000H
1510H	LCH5 source block count regiaster	LCH5_ASIZE_COUNT	R/W	0000_0000H
1514H-151CH	Reserved	–	–	–
1520H	LCH5 destination address register (start address)	LCH5_BADD	R/W	0000_0000H
1524H-153CH	Reserved	–	–	–
1540H	LCH5 length register	LCH5_LENG	R/W	0000_0000H
1544H	LCH5 read length count register	LCH5_LENG_RCOUNT	R	0000_0000H
1548H	LCH5 write length count register	LCH5_LENG_WCOUNT	R	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
154CH	Reserved	–	–	–
1550H	LCH5 mode register	LCH5_MODE	R/W	E4E4_0000H
1554H-1558H	Reserved	–	–	–
155CH	LCH5 physical channel register	LCH5_PCH	R/W	0000_0000H
1560H-15FCH	Reserved	–	–	–
1600H	LCH6 source address register (start address)	LCH6_AADD	R/W	0000_0000H
1604H	LCH6 source address pointer register	LCH6_AADP	R	0000_0000H
1608H	LCH6 source address offset register	LCH6_AOFF	R/W	0000_0000H
160CH	LCH6 source block size register	LCH6_ASIZE	R/W	0000_0000H
1610H	LCH6 source block count regiaster	LCH6_ASIZE_COUNT	R/W	0000_0000H
1614H-161CH	Reserved	–	–	–
1620H	LCH6 destination address register (start address)	LCH6_BADD	R/W	0000_0000H
1624H-163CH	Reserved	–	–	–
1640H	LCH6 length register	LCH6_LENG	R/W	0000_0000H
1644H	LCH6 read length count register	LCH6_LENG_RCOUNT	R	0000_0000H
1648H	LCH6 write length count register	LCH6_LENG_WCOUNT	R	0000_0000H
164CH	Reserved	–	–	–
1650H	LCH6 mode register	LCH6_MODE	R/W	E4E4_0000H
1654H-1658H	Reserved	–	–	–
165CH	LCH6 physical channel register	LCH6_PCH	R/W	0000_0000H
1660H-16FCH	Reserved	–	–	–
1700H	LCH7 source address register (start address)	LCH7_AADD	R/W	0000_0000H
1704H	LCH7 source address pointer register	LCH7_AADP	R	0000_0000H
1708H	LCH7 source address offset register	LCH7_AOFF	R/W	0000_0000H
170CH	LCH7 source block size register	LCH7_ASIZE	R/W	0000_0000H
1710H	LCH7 source block count regiaster	LCH7_ASIZE_COUNT	R/W	0000_0000H
1714H-171CH	Reserved	–	–	–
1720H	LCH7 destination address register (start address)	LCH7_BADD	R/W	0000_0000H
1724H-173CH	Reserved	–	–	–
1740H	LCH7 length register	LCH7_LENG	R/W	0000_0000H
1744H	LCH7 read length count register	LCH7_LENG_RCOUNT	R	0000_0000H
1748H	LCH7 write length count register	LCH7_LENG_WCOUNT	R	0000_0000H
174CH	Reserved	–	–	–
1750H	LCH7 mode register	LCH7_MODE	R/W	E4E4_0000H
1754H-1758H	Reserved	–	–	–
175CH	LCH7 physical channel register	LCH7_PCH	R/W	0000_0000H
1760H-	Reserved	–	–	–

Address	Register Name	Symbol	R/W	After Reset
FFFCH				

(2) P2M (Peripheral-to-memory) registers

Base address: E108_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	DMA start control register	CONT	W	0000_0000H
0004H	DMA control status register	CONTSTATUS	R	0000_0000H
0008H	DMA end control register	END	W	0000_0000H
000CH-00FCH	Reserved	–	–	–
0100H	Interrupt status register (LCH0 to LCH3)	LCH0LCH3_INT_CONT	R	0000_0000H
0104H	Interrupt raw status register (LCH0 to LCH3)	LCH0LCH3_INT_RAW	R	0000_0000H
0108H	Interrupt enable set register (LCH0 to LCH3)	LCH0LCH3_INT_ENABLE	R/W	0000_0000H
010CH	Interrupt enable clear register (LCH0 to LCH3)	LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
0110H	Interrupt source clear register (LCH0 to LCH3)	LCH0LCH3_INT_REQ_CL	W	0000_0000H
0114H-011CH	Reserved	–	–	–
0120H	Interrupt status register (LCH4 to LCH7)	LCH4LCH7_INT_CONT	R	0000_0000H
0124H	Interrupt raw status register (LCH4 to LCH7)	LCH4LCH7_INT_RAW	R	0000_0000H
0128H	Interrupt enable set register (LCH4 to LCH7)	LCH4LCH7_INT_ENABLE	R/W	0000_0000H
012CH	Interrupt enable clear register (LCH4 to LCH7)	LCH4LCH7_INT_ENABLE_CL	W	0000_0000H
0130H	Interrupt source clear register (LCH4 to LCH7)	LCH4LCH7_INT_REQ_CL	W	0000_0000H
0134H-0FFCH	Reserved	–	–	–
1000H	LCH0 source address register (start address)	LCH0_AADD	R/W	0000_0000H
1004H-101CH	Reserved	–	–	–
1020H	LCH0 destination address register (start address)	LCH0_BADD	R/W	0000_0000H
1024H	LCH0 destination address pointer register	LCH0_BADP	R	0000_0000H
1028H	LCH0 destination address offset register	LCH0_BOFF	R/W	0000_0000H
102CH	LCH0 destination block size register	LCH0_BSIZE	R/W	0000_0000H
1030H	LCH0 destination block count register	LCH0_BSIZE_COUNT	R/W	0000_0000H
1034H-103CH	Reserved	–	–	–
1040H	LCH0 length register	LCH0_LENG	R/W	0000_0000H
1044H	LCH0 read length count register	LCH0_LENG_RCOUNT	R	0000_0000H
1048H	LCH0 write length count register	LCH0_LENG_WCOUNT	R	0000_0000H
104CH	Reserved	–	–	–
1050H	LCH0 mode register	LCH0_MODE	R/W	E4E4_0000H
1054H	LCH0 timer register	LCH0_TIME	R/W	0000_0000H
1058H	LCH0 timer count register	LCH0_TIME_COUNT	R	0000_0000H
105CH	LCH0 physical channel register	LCH0_PCH	R/W	0000_0000H
1060H-10FCH	Reserved	–	–	–

Address	Register Name	Symbol	R/W	After Reset
1100H	LCH1 source address register (start address)	LCH1_AADD	R/W	0000_0000H
1104H-111CH	Reserved	–	–	–
1120H	LCH1 destination address register (start address)	LCH1_BADD	R/W	0000_0000H
1124H	LCH1 destination address pointer register	LCH1_BADP	R	0000_0000H
1128H	LCH1 destination address offset register	LCH1_BOFF	R/W	0000_0000H
112CH	LCH1 destination block size register	LCH1_BSIZE	R/W	0000_0000H
1130H	LCH1 destination block count register	LCH1_BSIZE_COUNT	R/W	0000_0000H
1134H-113CH	Reserved	–	–	–
1140H	LCH1 length register	LCH1_LENG	R/W	0000_0000H
1144H	LCH1 read length count register	LCH1_LENG_RCOUNT	R	0000_0000H
1148H	LCH1 write length count register	LCH1_LENG_WCOUNT	R	0000_0000H
114CH	Reserved	–	–	–
1150H	LCH1 mode register	LCH1_MODE	R/W	E4E4_0000H
1154H-1158H	Reserved	–	–	–
115CH	LCH1 physical channel register	LCH1_PCH	R/W	0000_0000H
1160H-11FCH	Reserved	–	–	–
1200H	LCH2 source address register (start address)	LCH2_AADD	R/W	0000_0000H
1204H-121CH	Reserved	–	–	–
1220H	LCH2 destination address register (start address)	LCH2_BADD	R/W	0000_0000H
1224H	LCH2 destination address pointer register	LCH2_BADP	R	0000_0000H
1228H	LCH2 destination address offset register	LCH2_BOFF	R/W	0000_0000H
122CH	LCH2 destination block size register	LCH2_BSIZE	R/W	0000_0000H
1230H	LCH2 destination block count register	LCH2_BSIZE_COUNT	R/W	0000_0000H
1234H-123CH	Reserved	–	–	–
1240H	LCH2 length register	LCH2_LENG	R/W	0000_0000H
1244H	LCH2 read length count register	LCH2_LENG_RCOUNT	R	0000_0000H
1248H	LCH2 write length count register	LCH2_LENG_WCOUNT	R	0000_0000H
124CH	Reserved	–	–	–
1250H	LCH2 mode register	LCH2_MODE	R/W	E4E4_0000H
1254H-1258H	Reserved	–	–	–
125CH	LCH2 physical channel register	LCH2_PCH	R/W	0000_0000H
1260H-12FCH	Reserved	–	–	–
1300H	LCH3 source address register (start address)	LCH3_AADD	R/W	0000_0000H
1304H-131CH	Reserved	–	–	–
1320H	LCH3 destination address register (start address)	LCH3_BADD	R/W	0000_0000H
1324H	LCH3 destination address pointer register	LCH3_BADP	R	0000_0000H
1328H	LCH3 destination address offset register	LCH3_BOFF	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
132CH	LCH3 destination block size register	LCH3_BSIZE	R/W	0000_0000H
1330H	LCH3 destination block count register	LCH3_BSIZE_COUNT	R/W	0000_0000H
1334H-133CH	Reserved	–	–	–
1340H	LCH3 length register	LCH3_LENG	R/W	0000_0000H
1344H	LCH3 read length count register	LCH3_LENG_RCOUNT	R	0000_0000H
1348H	LCH3 write length count register	LCH3_LENG_WCOUNT	R	0000_0000H
134CH	Reserved	–	–	–
1350H	LCH3 mode register	LCH3_MODE	R/W	E4E4_0000H
1354H-1358H	Reserved	–	–	–
135CH	LCH3 physical channel register	LCH3_PCH	R/W	0000_0000H
1360H-13FCH	Reserved	–	–	–
1400H	LCH4 source address register (start address)	LCH4_AADD	R/W	0000_0000H
1404H-141CH	Reserved	–	–	–
1420H	LCH4 destination address register (start address)	LCH4_BADD	R/W	0000_0000H
1424H	LCH4 destination address pointer register	LCH4_BADP	R	0000_0000H
1428H	LCH4 destination address offset register	LCH4_BOFF	R/W	0000_0000H
142CH	LCH4 destination block size register	LCH4_BSIZE	R/W	0000_0000H
1430H	LCH4 destination block count register	LCH4_BSIZE_COUNT	R/W	0000_0000H
1434H-143CH	Reserved	–	–	–
1440H	LCH4 length register	LCH4_LENG	R/W	0000_0000H
1444H	LCH4 read length count register	LCH4_LENG_RCOUNT	R	0000_0000H
1448H	LCH4 write length count register	LCH4_LENG_WCOUNT	R	0000_0000H
144CH	Reserved	–	–	–
1450H	LCH4 mode register	LCH4_MODE	R/W	E4E4_0000H
1454H-1458H	Reserved	–	–	–
145CH	LCH4 physical channel register	LCH4_PCH	R/W	0000_0000H
1460H-14FCH	Reserved	–	–	–
1500H	LCH5 source address register (start address)	LCH5_AADD	R/W	0000_0000H
1504H-151CH	Reserved	–	–	–
1520H	LCH5 destination address register (start address)	LCH5_BADD	R/W	0000_0000H
1524H	LCH5 destination address pointer register	LCH5_BADP	R	0000_0000H
1528H	LCH5 destination address offset register	LCH5_BOFF	R/W	0000_0000H
152CH	LCH5 destination block size register	LCH5_BSIZE	R/W	0000_0000H
1530H	LCH5 destination block count register	LCH5_BSIZE_COUNT	R/W	0000_0000H
1534H-153CH	Reserved	–	–	–
1540H	LCH5 length register	LCH5_LENG	R/W	0000_0000H
1544H	LCH5 read length count register	LCH5_LENG_RCOUNT	R	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
1548H	LCH5 write length count register	LCH5_LENG_WCOUNT	R	0000_0000H
154CH	Reserved	–	–	–
1550H	LCH5 mode register	LCH5_MODE	R/W	E4E4_0000H
1554H-1558H	Reserved	–	–	–
155CH	LCH5 physical channel register	LCH5_PCH	R/W	0000_0000H
1560H-15FCH	Reserved	–	–	–
1600H	LCH6 source address register (start address)	LCH6_AADD	R/W	0000_0000H
1604H-161CH	Reserved	–	–	–
1620H	LCH6 destination address register (start address)	LCH6_BADD	R/W	0000_0000H
1624H	LCH6 destination address pointer register	LCH6_BADP	R	0000_0000H
1628H	LCH6 destination address offset register	LCH6_BOFF	R/W	0000_0000H
162CH	LCH6 destination block size register	LCH6_BSIZE	R/W	0000_0000H
1630H	LCH6 destination block count register	LCH6_BSIZE_COUNT	R/W	0000_0000H
1634H-163CH	Reserved	–	–	–
1640H	LCH6 length register	LCH6_LENG	R/W	0000_0000H
1644H	LCH6 read length count register	LCH6_LENG_RCOUNT	R	0000_0000H
1648H	LCH6 write length count register	LCH6_LENG_WCOUNT	R	0000_0000H
164CH	Reserved	–	–	–
1650H	LCH6 mode register	LCH6_MODE	R/W	E4E4_0000H
1654H-1658H	Reserved	–	–	–
165CH	LCH6 physical channel register	LCH6_PCH	R/W	0000_0000H
1660H-16FCH	Reserved	–	–	–
1700H	LCH7 source address register (start address)	LCH7_AADD	R/W	0000_0000H
1704H-171CH	Reserved	–	–	–
1720H	LCH7 destination address register (start address)	LCH7_BADD	R/W	0000_0000H
1724H	LCH7 destination address pointer register	LCH7_BADP	R	0000_0000H
1728H	LCH7 destination address offset register	LCH7_BOFF	R/W	0000_0000H
172CH	LCH7 destination block size register	LCH7_BSIZE	R/W	0000_0000H
1730H	LCH7 destination block count register	LCH7_BSIZE_COUNT	R/W	0000_0000H
1734H-173CH	Reserved	–	–	–
1740H	LCH7 length register	LCH7_LENG	R/W	0000_0000H
1744H	LCH7 read length count register	LCH7_LENG_RCOUNT	R	0000_0000H
1748H	LCH7 write length count register	LCH7_LENG_WCOUNT	R	0000_0000H
174CH	Reserved	–	–	–
1750H	LCH7 mode register	LCH7_MODE	R/W	E4E4_0000H
1754H-1758H	Reserved	–	–	–
175CH	LCH7 physical channel register	LCH7_PCH	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
1760H-FFFCH	Reserved	–	–	–

(3) M2M (Memory-to-memory) registers

Base address: E109_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	DMA start control register	CONT	W	0000_0000H
0004H	DMA control status register	CONTSTATUS	R	0000_0000H
0008H	DMA end control register	END	W	0000_0000H
000CH-00FCH	Reserved	–	–	–
0100H	Interrupt status register (LCH0 to LCH3)	LCH0LCH3_INT_CONT	R	0000_0000H
0104H	Interrupt raw status register (LCH0 to LCH3)	LCH0LCH3_INT_RAW	R	0000_0000H
0108H	Interrupt enable set register (LCH0 to LCH3)	LCH0LCH3_INT_ENABLE	R/W	0000_0000H
010CH	Interrupt enable clear register (LCH0 to LCH3)	LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
0110H	Interrupt source clear register (LCH0 to LCH3)	LCH0LCH3_INT_REQ_CL	W	0000_0000H
0114H-011CH	Reserved	–	–	–
0120H	Interrupt status register (LCH4 to LCH7)	LCH4LCH7_INT_CONT	R	0000_0000H
0124H	Interrupt raw status register (LCH4 to LCH7)	LCH4LCH7_INT_RAW	R	0000_0000H
0128H	Interrupt enable set register (LCH4 to LCH7)	LCH4LCH7_INT_ENABLE	R/W	0000_0000H
012CH	Interrupt enable clear register (LCH4 to LCH7)	LCH4LCH7_INT_ENABLE_CL	W	0000_0000H
0130H	Interrupt source clear register (LCH4 to LCH7)	LCH4LCH7_INT_REQ_CL	W	0000_0000H
0134H-0FFCH	Reserved	–	–	–
1000H	LCH0 source address register (start address)	LCH0_AADD	R/W	0000_0000H
1004H	LCH0 source address pointer register	LCH0_AADP	R	0000_0000H
1008H	LCH0 source address offset register	LCH0_AOFF	R/W	0000_0000H
100CH	Reserved	–	–	–
1010H	LCH0 source block count register	LCH0_ASIZE_COUNT	R/W	0000_0000H
1014H-101CH	Reserved	–	–	–
1020H	LCH0 destination address register (start address)	LCH0_BADD	R/W	0000_0000H
1024H	LCH0 destination address pointer register	LCH0_BADP	R	0000_0000H
1028H	LCH0 destination address offset register	LCH0_BOFF	R/W	0000_0000H
102CH	Reserved	–	–	–
1030H	LCH0 destination block count register	LCH0_BSIZE_COUNT	R/W	0000_0000H
1034H-103CH	Reserved	–	–	–
1040H	LCH0 length register	LCH0_LENG	R/W	0000_0000H
1044H	LCH0 read length count register	LCH0_LENG_RCOUNT	R	0000_0000H
1048H	LCH0 write length count register	LCH0_LENG_WCOUNT	R	0000_0000H
104CH	LCH0 block size register	LCH0_SIZE	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
1050H	LCH0 mode register	LCH0_MODE	R/W	E4E4_0000H
1054H-10FCH	Reserved	–	–	–
1100H	LCH1 source address register (start address)	LCH1_AADD	R/W	0000_0000H
1104H	LCH1 source address pointer register	LCH1_AADP	R	0000_0000H
1108H	LCH1 source address offset register	LCH1_AOFF	R/W	0000_0000H
110CH	Reserved	–	–	–
1110H	LCH1 source block count register	LCH1_ASIZE_COUNT	R/W	0000_0000H
1114H-111CH	Reserved	–	–	–
1120H	LCH1 destination address register (start address)	LCH1_BADD	R/W	0000_0000H
1124H	LCH1 destination address pointer register	LCH1_BADP	R	0000_0000H
1128H	LCH1 destination address offset register	LCH1_BOFF	R/W	0000_0000H
112CH	Reserved	–	–	–
1130H	LCH1 destination block count register	LCH1_BSIZE_COUNT	R/W	0000_0000H
1134H-113CH	Reserved	–	–	–
1140H	LCH1 length register	LCH1_LENG	R/W	0000_0000H
1144H	LCH1 read length count register	LCH1_LENG_RCOUNT	R	0000_0000H
1148H	LCH1 write length count register	LCH1_LENG_WCOUNT	R	0000_0000H
114CH	LCH1 block size register	LCH1_SIZE	R/W	0000_0000H
1150H	LCH1 mode register	LCH1_MODE	R/W	E4E4_0000H
1154H-11FCH	Reserved	–	–	–
1200H	LCH2 source address register (start address)	LCH2_AADD	R/W	0000_0000H
1204H	LCH2 source address pointer register	LCH2_AADP	R	0000_0000H
1208H	LCH2 source address offset register	LCH2_AOFF	R/W	0000_0000H
120CH	Reserved	–	–	–
1210H	LCH2 source block count register	LCH2_ASIZE_COUNT	R/W	0000_0000H
1214H-121CH	Reserved	–	–	–
1220H	LCH2 destination address register (start address)	LCH2_BADD	R/W	0000_0000H
1224H	LCH2 destination address pointer register	LCH2_BADP	R	0000_0000H
1228H	LCH2 destination address offset register	LCH2_BOFF	R/W	0000_0000H
122CH	Reserved	–	–	–
1230H	LCH2 destination block count register	LCH2_BSIZE_COUNT	R/W	0000_0000H
1234H-123CH	Reserved	–	–	–
1240H	LCH2 length register	LCH2_LENG	R/W	0000_0000H
1244H	LCH2 read length count register	LCH2_LENG_RCOUNT	R	0000_0000H
1248H	LCH2 write length count register	LCH2_LENG_WCOUNT	R	0000_0000H
124CH	LCH2 block size register	LCH2_SIZE	R/W	0000_0000H
1250H	LCH2 mode register	LCH2_MODE	R/W	E4E4_0000H
1254H-12FCH	Reserved	–	–	–

Address	Register Name	Symbol	R/W	After Reset
1300H	LCH3 source address register (start address)	LCH3_AADD	R/W	0000_0000H
1304H	LCH3 source address pointer register	LCH3_AADP	R	0000_0000H
1308H	LCH3 source address offset register	LCH3_AOFF	R/W	0000_0000H
130CH	Reserved	–	–	–
1310H	LCH3 source block count register	LCH3_ASIZE_COUNT	R/W	0000_0000H
1314H-131CH	Reserved	–	–	–
1320H	LCH3 destination address register (start address)	LCH3_BADD	R/W	0000_0000H
1324H	LCH3 destination address pointer register	LCH3_BADP	R	0000_0000H
1328H	LCH3 destination address offset register	LCH3_BOFF	R/W	0000_0000H
132CH	Reserved	–	–	–
1330H	LCH3 destination block count register	LCH3_BSIZE_COUNT	R/W	0000_0000H
1334H-133CH	Reserved	–	–	–
1340H	LCH3 length register	LCH3_LENG	R/W	0000_0000H
1344H	LCH3 read length count register	LCH3_LENG_RCOUNT	R	0000_0000H
1348H	LCH3 write length count register	LCH3_LENG_WCOUNT	R	0000_0000H
134CH	LCH3 block size register	LCH3_SIZE	R/W	0000_0000H
1350H	LCH3 mode register	LCH3_MODE	R/W	E4E4_0000H
1354H-13FCH	Reserved	–	–	–
1400H	LCH4 source address register (start address)	LCH4_AADD	R/W	0000_0000H
1404H	LCH4 source address pointer register	LCH4_AADP	R	0000_0000H
1408H	LCH4 source address offset register	LCH4_AOFF	R/W	0000_0000H
140CH	Reserved	–	–	–
1410H	LCH4 source block count register	LCH4_ASIZE_COUNT	R/W	0000_0000H
1414H-141CH	Reserved	–	–	–
1420H	LCH4 destination address register (start address)	LCH4_BADD	R/W	0000_0000H
1424H	LCH4 destination address pointer register	LCH4_BADP	R	0000_0000H
1428H	LCH4 destination address offset register	LCH4_BOFF	R/W	0000_0000H
142CH	Reserved	–	–	–
1430H	LCH4 destination block count register	LCH4_BSIZE_COUNT	R/W	0000_0000H
1434H-143CH	Reserved	–	–	–
1440H	LCH4 length register	LCH4_LENG	R/W	0000_0000H
1444H	LCH4 read length count register	LCH4_LENG_RCOUNT	R	0000_0000H
1448H	LCH4 write length count register	LCH4_LENG_WCOUNT	R	0000_0000H
144CH	LCH4 block size register	LCH4_SIZE	R/W	0000_0000H
1450H	LCH4 mode register	LCH4_MODE	R/W	E4E4_0000H
1454H-14FCH	Reserved	–	–	–
1500H	LCH5 source address register (start address)	LCH5_AADD	R/W	0000_0000H
1504H	LCH5 source address pointer register	LCH5_AADP	R	0000_0000H
1508H	LCH5 source address offset register	LCH5_AOFF	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
150CH	Reserved	–	–	–
1510H	LCH5 source block count register	LCH5_ASIZE_COUNT	R/W	0000_0000H
1514H-151CH	Reserved	–	–	–
1520H	LCH5 destination address register (start address)	LCH5_BADD	R/W	0000_0000H
1524H	LCH5 destination address pointer register	LCH5_BADP	R	0000_0000H
1528H	LCH5 destination address offset register	LCH5_BOFF	R/W	0000_0000H
152CH	Reserved	–	–	–
1530H	LCH5 destination block count register	LCH5_BSIZE_COUNT	R/W	0000_0000H
1534H-153CH	Reserved	–	–	–
1540H	LCH5 length register	LCH5_LENG	R/W	0000_0000H
1544H	LCH5 read length count register	LCH5_LENG_RCOUNT	R	0000_0000H
1548H	LCH5 write length count register	LCH5_LENG_WCOUNT	R	0000_0000H
154CH	LCH5 block size register	LCH5_SIZE	R/W	0000_0000H
1550H	LCH5 mode register	LCH5_MODE	R/W	E4E4_0000H
1554H-15FCH	Reserved	–	–	–
1600H	LCH6 source address register (start address)	LCH6_AADD	R/W	0000_0000H
1604H	LCH6 source address pointer register	LCH6_AADP	R	0000_0000H
1608H	LCH6 source address offset register	LCH6_AOFF	R/W	0000_0000H
160CH	Reserved	–	–	–
1610H	LCH6 source block count register	LCH6_ASIZE_COUNT	R/W	0000_0000H
1614H-161CH	Reserved	–	–	–
1620H	LCH6 destination address register (start address)	LCH6_BADD	R/W	0000_0000H
1624H	LCH6 destination address pointer register	LCH6_BADP	R	0000_0000H
1628H	LCH6 destination address offset register	LCH6_BOFF	R/W	0000_0000H
162CH	Reserved	–	–	–
1630H	LCH6 destination block count register	LCH6_BSIZE_COUNT	R/W	0000_0000H
1634H-163CH	Reserved	–	–	–
1640H	LCH6 length register	LCH6_LENG	R/W	0000_0000H
1644H	LCH6 read length count register	LCH6_LENG_RCOUNT	R	0000_0000H
1648H	LCH6 write length count register	LCH6_LENG_WCOUNT	R	0000_0000H
164CH	LCH6 block size register	LCH6_SIZE	R/W	0000_0000H
1650H	LCH6 mode register	LCH6_MODE	R/W	E4E4_0000H
1654H-16FCH	Reserved	–	–	–
1700H	LCH7 source address register (start address)	LCH7_AADD	R/W	0000_0000H
1704H	LCH7 source address pointer register	LCH7_AADP	R	0000_0000H
1708H	LCH7 source address offset register	LCH7_AOFF	R/W	0000_0000H
170CH	Reserved	–	–	–
1710H	LCH7 source block count register	LCH7_ASIZE_COUNT	R/W	0000_0000H
1714H-	Reserved	–	–	–

Address	Register Name	Symbol	R/W	After Reset
171CH				
1720H	LCH7 destination address register (start address)	LCH7_BADD	R/W	0000_0000H
1724H	LCH7 destination address pointer register	LCH7_BADP	R	0000_0000H
1728H	LCH7 destination address offset register	LCH7_BOFF	R/W	0000_0000H
172CH	Reserved	–	–	–
1730H	LCH7 destination block count register	LCH7_BSIZE_COUNT	R/W	0000_0000H
1734H-173CH	Reserved	–	–	–
1740H	LCH7 length register	LCH7_LENG	R/W	0000_0000H
1744H	LCH7 read length count register	LCH7_LENG_RCOUNT	R	0000_0000H
1748H	LCH7 write length count register	LCH7_LENG_WCOUNT	R	0000_0000H
174CH	LCH7 block size register	LCH7_SIZE	R/W	0000_0000H
1750H	LCH7 mode register	LCH7_MODE	R/W	E4E4_0000H
1754H to FFFCH	Reserved	–	–	–

A.15 Camera Interface (CAM)

Base address: E10B_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	INT status register	CA_STATUS	R	0000_0000H
0004H	INT raw status register	CA_RAWSTATUS	R	0000_0000H
0008H	INT enable set register	CA_ENSET	R/W	0000_0000H
000CH	INT enable clear register	CA_ENCLR	W	0000_0000H
0010H	INT source clear register	CA_FFCLR	W	0000_0000H
0014H	Error address register	CA_ERRORADR	R/W	0000_0000H
0018H to 001CH	Reserved	–	–	–
0020H	Camera control register	CA_CSR	R/W	0000_0000H
0024H to 002CH	Reserved	–	–	–
0030H	Transfer start X coordinate register	CA_X1R	R/W	0000_0000H
0034H	Transfer end X coordinate register	CA_X2R	R/W	0000_0000H
0038H	Transfer start Y coordinate register	CA_Y1R	R/W	0000_0000H
003CH	Transfer end Y coordinate register	CA_Y2R	R/W	0000_0000H
0040H	Luminance signal offset register	CA_BNZR	R/W	0000_0000H
0044H	Luminance signal gain register	CA_BNGR	R/W	0000_0080H
0048H	U color difference signal offset register	CA_CBZR	R/W	0000_0000H
004CH	U color difference signal gain register	CA_CBGR	R/W	0000_0080H
0050H	V color difference signal offset register	CA_CRZR	R/W	0000_0000H
0054H	V color difference signal gain register	CA_CRGR	R/W	0000_0080H
0058H to 07CH	Reserved	–	–	–
0080H	Transfer control register	CA_DMACNT	R/W	0000_0000H
0084H	Transfer frame register	CA_FRAME	R/W	0000_0005H
0088H	Transfer request register	CA_DMAREQ	R/W	0000_0000H
008CH	Transfer request cancellation register	CA_DMASTOP	W	0000_0000H
0090H to 00FCH	Reserved	–	–	–
0100H	Address addition value register (main frame)	CA_LINESIZE_MAIN	R/W	0000_0000H
0104H	Horizontal reduction ratio register (main frame)	CA_XRATIO_MAIN	R/W	0000_0000H
0108H	Vertical reduction ratio register (main frame)	CA_YRATIO_MAIN	R/W	0000_0000H
010CH	Horizontal transfer size register (main frame)	CA_DMAX_MAIN	R/W	0000_0000H
0110H	Vertical transfer size register (main frame)	CA_DMAY_MAIN	R/W	0000_0000H
0114H	Y plane transfer address register (A frame)	CA_YPLANE_A	R/W	0000_0000H
0118H	UV plane transfer address register (A frame)	CA_UVPLANE_A	R/W	0000_0000H
011CH	Y plane transfer address register (B frame)	CA_YPLANE_B	R/W	0000_0000H
0120H	UV plane transfer address register (B frame)	CA_UVPLANE_B	R/W	0000_0000H

Address	Register Name	Symbol	R/W	After Reset
0124H to 0224H	Reserved	–	–	–
022CH	Module control register	CA_MODULECONT	R/W	0000_0000H
0230H	Update register	CA_UPDATE	R/W	0000_0000H
0234H	Horizontal/vertical flip control register	CA_MIRROR	R/W	0000_0000H
0238H	Byte lane control register (dedicated to YUV 422 Interleave)	CA_OD_BYTELANE	R/W	0000_00E4H
023CH	Reserved	–	–	–
0240H	Transfer end X coordinate register (dedicated to enable signal sampling mode)	CA_X3R	R/W	0000_0000H
0244H	V plane transfer address register (A frame)	CA_VPLANE_A	R/W	0000_0000H
0248H	V plane transfer address register (B frame)	CA_VPLANE_B	R/W	0000_0000H
024CH to 0250H	Reserved	–	–	–
0254H	Byte lane control register 2 (for video-system macros)	CA_OD_BYTELANE2	R/W	0000_E4E4H
0258H	Simple QoS setting register	CA_QOS	R/W	0000_0000H
025CH to FFFCH	Reserved	–	–	–

A.16 Pulse Width Modulation Interface

Base address: E113_0000H

(1) Control registers (PWM0)

Address	Register Name	Symbol	R/W	After Reset
0000H	PWM operation start/stop register	PWM_CH0_CTRL	R/W	0000_0000H
0004H	PWM0 mode control register	PWM_CH0_MODE	R/W	0000_0000H
0008H to 000CH	Reserved	–	–	–

(2) Setting registers (PWM0)

Address	Register Name	Symbol	R/W	After Reset
0010H	Channel 0 counter 0 delay setting register	PWM_CH0_DELAY0	R/W	0000_0000H
0014H	Channel 0 counter 0 leading edge setting register	PWM_CH0_LEDGE0	R/W	0000_0000H
0018H	Channel 0 counter 0 trailing edge setting register	PWM_CH0_TEDGE0	R/W	0000_0000H
001CH	Channel 0 counter 0 total cycle setting register	PWM_CH0_TOTAL0	R/W	0000_0000H
0020H	Channel 0 counter 0 loop count setting register	PWM_CH0_LOOP0	R/W	0000_0000H
0024H to 003CH	Reserved	–	–	–
0040H	Channel 0 counter 1 delay setting register	PWM_CH0_DELAY1	R/W	0000_0000H
0044H	Channel 0 counter 1 leading edge setting register	PWM_CH0_LEDGE1	R/W	0000_0000H
0048H	Channel 0 counter 1 trailing edge setting register	PWM_CH0_TEDGE1	R/W	0000_0000H
004CH	Channel 0 counter 1 total cycle setting register	PWM_CH0_TOTAL1	R/W	0000_0000H
0050H	Channel 0 counter 1 loop count setting register	PWM_CH0_LOOP1	R/W	0000_0000H
0054H to 07CH	Reserved	–	–	–
0080H	Channel 0 counter 2 delay setting register	PWM_CH0_DELAY2	R/W	0000_0000H
0084H	Channel 0 counter 2 leading edge setting register	PWM_CH0_LEDGE2	R/W	0000_0000H
0088H	Channel 0 counter 2 trailing edge setting register	PWM_CH0_TEDGE2	R/W	0000_0000H
008CH	Channel 0 counter 2 total cycle setting register	PWM_CH0_TOTAL2	R/W	0000_0000H
0090H	Channel 0 counter 2 loop count setting register	PWM_CH0_LOOP2	R/W	0000_0000H
0094H to 00FCH	Reserved	–	–	–

(3) Control registers (PWM1)

Address	Register Name	Symbol	R/W	After Reset
0100H	PWM operation start/stop register	PWM_CH1_CTRL	R/W	0000_0000H
0104H	PWM0 mode control register	PWM_CH1_MODE	R/W	0000_0000H
0108H to 010CH	Reserved	–	–	–

(4) Setting registers (PWM1)

Address	Register Name	Symbol	R/W	After Reset
0110H	Channel 1 counter 0 delay setting register	PWM_CH1_DELAY0	R/W	0000_0000H
0114H	Channel 1 counter 0 leading edge setting register	PWM_CH1_LEDGE0	R/W	0000_0000H
0118H	Channel 1 counter 0 trailing edge setting register	PWM_CH1_TEDGE0	R/W	0000_0000H
011CH	Channel 1 counter 0 total cycle setting register	PWM_CH1_TOTAL0	R/W	0000_0000H
0120H	Channel 1 counter 0 loop count setting register	PWM_CH1_LOOP0	R/W	0000_0000H
0124H to 013CH	Reserved	–	–	–
0140H	Channel 1 counter 1 delay setting register	PWM_CH1_DELAY1	R/W	0000_0000H
0144H	Channel 1 counter 1 leading edge setting register	PWM_CH1_LEDGE1	R/W	0000_0000H
0148H	Channel 1 counter 1 trailing edge setting register	PWM_CH1_TEDGE1	R/W	0000_0000H
014CH	Channel 1 counter 1 total cycle setting register	PWM_CH1_TOTAL1	R/W	0000_0000H
0150H	Channel 1 counter 1 loop count setting register	PWM_CH1_LOOP1	R/W	0000_0000H
0154H to 017CH	Reserved	–	–	–
0180H	Channel 1 counter 2 delay setting register	PWM_CH1_DELAY2	R/W	0000_0000H
0184H	Channel 1 counter 2 leading edge setting register	PWM_CH1_LEDGE2	R/W	0000_0000H
0188H	Channel 1 counter 2 trailing edge setting register	PWM_CH1_TEDGE2	R/W	0000_0000H
018CH	Channel 1 counter 2 total cycle setting register	PWM_CH1_TOTAL2	R/W	0000_0000H
0190H	Channel 1 counter 2 loop count setting register	PWM_CH1_LOOP2	R/W	0000_0000H
0194H to 03FCH	Reserved	–	–	–

(5) Interrupt registers

Address	Register Name	Symbol	R/W	After Reset
0400H	PWM interrupt status register	PWM_INTSTATUS	R	0000_0000H
0404H	PWM interrupt raw status register	PWM_INTRAWSTATUS	R	0000_0000H
0408H	PWM interrupt enable set register	PWM_INTENSET	R/W	0000_0000H
040CH	PWM interrupt enable clear register	PWM_INTENCLR	W	0000_0000H
0410H	PWM interrupt source clear register	PWM_INTFFCLR	W	0000_0000H
0414H to FFFCH	Reserved	–	–	–

A.17 Digital Terrestrial TV Interface (DTV)

Base address: E115_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Interrupt status register	DT_STATUS	R	0000_0000H
0004H	Interrupt raw status register	DT_RAWSTATUS	R	0000_0000H
0008H	Interrupt enable set register	DT_ENSET	R/W	0000_0000H
000CH	Interrupt enable clear register	DT_ENCLR	W	0000_0000H
0010H	Interrupt source clear register	DT_FFCLR	W	0000_0000H
0014H	Error address register	DT_ERRORADR	R/W	0000_0000H
0018H to 001CH	Reserved	–	–	–
0020H	Transfer control register	DT_DMACNT	R/W	0000_0003H
0024H	Transfer request register	DT_DMAREQ	R/W	0000_0000H
0028H	Transfer request cancellation register	DT_DMASTOP	W	0000_0000H
002CH	Start address register	DT_START	R/W	0000_0000H
0030H	Buffer size register	DT_BUFSIZE	R/W	0000_0000H
0034H	Blank size register	DT_BLANK	R/W	0000_0000H
0038H	Current packet register	DT_CURRENT	R	0000_0000H
003CH	DMA completion interrupt setting register	DT_INTCONT	R/W	0000_0000H
0040H	Module control register	DT_MODULECONT	R/W	0000_0000H
0044H	DTVPSYNC/DTVVLD polarity designation register	DT_SIGNALINVERT	R/W	0000_0000H
0048H	Input pin status monitor register	DT_MONITOR	R	0000_0000H
004CH to FFFCH	Reserved	–	–	–

A.18 Resizer (SIZ)

Base address: E118_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Horizontal pixel count setting register	SRCHSIZE	R/W	0000_0000H
0004H	Vertical pixel count setting register	SRCVSIZE	R/W	0000_0000H
0008H	Pixel format setting register	SRCFMT	R/W	0000_0000H
000CH	Horizontal destination setting register 1	DSTHSIZE	R/W	0000_0000H
0010H	Vertical destination setting register 1	DSTVSIZE	R/W	0000_0000H
0014H	Destination skip setting register	DSTHSKIP	R/W	0000_0000H
0018H	Destination address (YRGB) setting register	DSTADRYRGB	R/W	0000_0000H
001CH	Destination address (UV) setting register	DSTADRUV	R/W	0000_0000H
0020H	Destination address (V) setting register	DSTADRV	R/W	0000_0000H
0024H	Destination format setting register	DSTFMT	R/W	0000_0000H
0028H	Destination byte lane setting register	DSTBL	R/W	0000_00E4H
002CH	Horizontal magnification setting register	DSTHSTEP	R/W	0000_0100H
0030H	Vertical magnification setting register	DSTVSTEP	R/W	0000_0100H
0034H	Filtering option setting register	FILTOPT	R/W	0000_0000H
0038H	Horizontal destination setting register 2	DSTHCROP	R/W	0000_0000H
003CH	Vertical destination setting register 2	DSTVCROP	R/W	0000_0000H
0040H	Rotation channel destination address (YRGB) setting register	ROTDSTADRYRGB	R/W	0000_0000H
0044H	Rotation channel destination address (UV) setting register	ROTDSTADRUV	R/W	0000_0000H
0048H	Rotation channel function setting register	ROTMODE	R/W	0000_0000H
004CH	Rotation channel destination format setting register	ROTDSTFMT	R/W	0000_0000H
0050H	Status register	STAT	R	0000_0000H
0054H	Filtering coefficient setting register 0	FILT0	R/W	00f8_0008H
0058H	Filtering coefficient setting register 1	FILT1	R/W	00e8_0018H
005CH	Filtering coefficient setting register 2	FILT2	R/W	00d8_0028H
0060H	Filtering coefficient setting register 3	FILT3	R/W	00c8_0038H
0064H	Filtering coefficient setting register 4	FILT4	R/W	00b8_0048H
0068H	Filtering coefficient setting register 5	FILT5	R/W	00a8_0058H
006CH	Filtering coefficient setting register 6	FILT6	R/W	0098_0068H
0070H	Filtering coefficient setting register 7	FILT7	R/W	0088_0078H
0074H	Color conversion coefficient	COEF_R0	R/W	0000_03FBH
0078H	Color conversion coefficient	COEF_R1	R/W	0000_05D1H
007CH	Color conversion coefficient	COEF_R2	R/W	0000_05DBH
0080H	Color conversion coefficient	COEF_R3	R/W	0000_027CH
0084H	Color conversion coefficient	COEF_G0	R/W	0000_028FH
0088H	Color conversion coefficient	COEF_G1	R/W	0000_063FH
008CH	Color conversion coefficient	COEF_G2	R/W	0000_077FH
0090H	Color conversion coefficient	COEF_G3	R/W	0000_07CFH
0094H	Color conversion coefficient	COEF_B0	R/W	0000_05FCH

0098H	Color conversion coefficient	COEF_B1	R/W	0000_05DAH
009CH	Color conversion coefficient	COEF_B2	R/W	0000_0193H
00A0H	Color conversion coefficient	COEF_B3	R/W	0000_03D3H
00A4H to FFFCH	Reserved	–	–	–

A.19 HD Video Decoder (AVE)

Base address: E119_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	BIT run start	CodeRun	W	0000_0000H
0004H	Code Download Data register	CodeDownLoad	W	0000_0000H
0008H	Host Interrupt Request to BIT	HostIntReq	W	0000_0000H
000CH	BIT Interrupt Clear	BitIntClear	W	0000_0000H
0010H	BIT Interrupt Status	BitIntSts	R	0000_0000H
0014H	Obsolete	Obsolete		0000_0000H
0018H	BIT Current PC	BitCurPc	R	0000_0000H
001CH to 00FCH	Reserved	–	–	–
0100H	CODE Table SDRAM Address	CodeBufAdddr	R/W	–
0104H	Working Buffer SDRAM Address	WorkBufAddr	R/W	–
0108H	Argument / return Parameter Buffer SDRAM Address	ParaBufAddr	R/W	–
010CH	Bitstream Buffer Control	BitStreamCtrl	R/W	–
0110H	Frame Memory Control	FrameMemCtrl	R/W	–
0114H	Decoder Function Control	DecFuncCtrl	R/W	–
0118H to 011CH	Reserved	–	–	–
0120H	Bitstream Buffer Read Address of Run Index 0	BitStreamRdPtr0	R/W	–
0124H	Bitstream Buffer Write Address of Run Index 0	BitStreamWrPtr0	R/W	–
0128H	Bitstream Buffer Read Address of Run Index 1	BitStreamRdPtr1	R/W	–
012CH	Bitstream Buffer Write Address of Run Index 1	BitStreamWrPtr1	R/W	–
0130H	Bitstream Buffer Read Address of Run Index 2	BitStreamRdPtr2	R/W	–
0134H	Bitstream Buffer Write Address of Run Index 2	BitStreamWrPtr2	R/W	–
0138H	Bitstream Buffer Read Address of Run Index 3	BitStreamRdPtr3	R/W	–
013CH	Bitstream Buffer Write Address of Run Index 3	BitStreamWrPtr3	R/W	–
0140H	Internal scratch RAM Configuration	AXI_SRAM_USE	R/W	–
0144H to 014CH	Reserved	–	–	–
0150H	Display use flag of frame buffer for Run Index 0	BitFrameDisFlag0	R/W	–
0154H	Display use flag of frame buffer for Run Index 1	BitFrameDisFlag1	R/W	–
0158H	Display use flag of frame buffer for Run Index 2	BitFrameDisFlag2	R/W	–
015CH	Display use flag of frame buffer for Run Index 3	BitFrameDisFlag3	R/W	–
0160H	Processor Busy Flag	BusyFlag	R	–
0164H	Run Command	RunCommand	R/W	–
0168H	Run Process Index	RunIndex	R/W	–
016CH	Run Decoder Standard	RunCodStd	R/W	–
0170H	Interrupt Enable	IntEnable	R/W	–
0174H	Interrupt Reason	IntReason	R/W	–
0178H	Run Decoder Auxiliary Standard	RunAuxStd	R/W	–
017CH	Reserved	–	–	–

0180H to 01D0H	Command I/O Registers	CMD I/O	R/W	–
01D4H to FFFCH	Reserved	–	–	–

A.20 ITU-R BT.656 Interface (NTS)

Base address: E121_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Control register	NTS_CONTROL	R/W	0000_0000H
0004H	Display register	NTS_OUT	R/W	0000_0000H
0008H	Status register	NTS_STATUS	R	0000_0000H
000CH	Display area address register YA	NTS_YAREAAD_A	R/W	0000_0000H
0010H	Display area address register YB	NTS_YAREAAD_B	R/W	0000_0000H
0014H	Display area address register YC	NTS_YAREAAD_C	R/W	0000_0000H
0018H	Display area address register UVA	NTS_UVAREAAD_A	R/W	0000_0000H
001CH	Display area address register UVB	NTS_UVAREAAD_B	R/W	0000_0000H
0020H	Display area address register UVC	NTS_UVAREAAD_C	R/W	0000_0000H
0024H	Address addition value register	NTS_HOFFSET	R/W	0000_0000H
0028H	Frame select register	NTS_FRAMESEL	R/W	0000_0001H
002CH to 005CH	Reserved	–	–	–
0060H	Interrupt status register	NTS_INTSTATUS	R	0000_0000H
0064H	Interrupt raw status register	NTS_INTRAWSTATUS	R	0000_0000H
0068H	Interrupt enable set register	NTS_INTENSET	R/W	0000_0000H
006CH	Interrupt enable clear register	NTS_INTENCLR	W	0000_0000H
0070H	Interrupt source clear register	NTS_INTFFCLR	W	0000_0000H
0074H	Error address register	NTS_ERRORADR	R/W	0000_0000H
0078H	Software reset register	NTS_SWRESET	R/W	0000_0000H
007CH to FFFCH	Reserved	–	–	–

A.21 Rotator (ROT)

Base address: E122_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	Rotation setting register (CH0)	MODE_CH0	R/W	0000_0000H
0004H	Horizontal source image size setting register (CH0)	SRCHSIZE_CH0	R/W	0000_0000H
0008H	Vertical source image size setting register (CH0)	SRCVSIZE_CH0	R/W	0000_0000H
000CH	Source format setting register (CH0)	SRCFMT_CH0	R/W	0000_0000H
0010H	Destination address (YRGB) setting register (CH0)	DSTADRYRGB_CH0	R/W	0000_0000H
0014H	Destination address (UV) setting register (CH0)	DSTADRUV_CH0	R/W	0000_0000H
0018H	Destination address (V) setting register (CH0)	DSTADRV_CH0	R/W	0000_0000H
001CH	Destination image byte lane setting register (CH0)	DSTBL_CH0	R/W	0000_00E4H
0020H	Rotation setting register (CH1)	MODE_CH1	R/W	0000_0000H
0024H	Horizontal source image size setting register (CH1)	SRCHSIZE_CH1	R/W	0000_0000H
0028H	Vertical source image size setting register (CH1)	SRCVSIZE_CH1	R/W	0000_0000H
002CH	Source format setting register (CH1)	SRCFMT_CH1	R/W	0000_0000H
0030H	Destination address (YRGB) setting register (CH1)	DSTADRYRGB_CH1	R/W	0000_0000H
0034H	Destination address (UV) setting register (CH1)	DSTADRUV_CH1	R/W	0000_0000H
0038H	Destination address (V) setting register (CH1)	DSTADRUV_CH1	R/W	0000_0000H
003CH	Destination image byte lane setting register (CH1)	DSTBL_CH1	R/W	0000_00E4H
0040H	Histogram control register	HISTCTRL	R/W	–
0044H	Histogram value clear register	HISTCLR	R/W	0000_0000H
0048H	Histogram value count register 0	HIST0	R	0000_0000H
004CH	Histogram value count register 1	HIST1	R	0000_0000H
0050H	Histogram value count register 2	HIST2	R	0000_0000H
0054H	Histogram value count register 3	HIST3	R	0000_0000H
0058H	Histogram value count register 4	HIST4	R	0000_0000H
005CH	Histogram value count register 5	HIST5	R	0000_0000H
0060H	Histogram value count register 6	HIST6	R	0000_0000H
0064H	Histogram value count register 7	HIST7	R	0000_0000H
0068H to FFFCH	Reserved	–	–	–

A.22 Image Composer (IMC/IMCW)

IMC Base address: E126_0000H
IMCW Base address: E127_0000H

Caution : Among addresses 000H to FFFCH, the addresses not listed in the following tables are reserved. Writing to reserved areas is prohibited. An undefined value is returned for read access.

(1) Function setting registers

Address	Register Name	Symbol	R/W	After Reset
0000H	Control register	IMC_CONTROL	R/W	0000_0000H
0004H	Update reserve register	IMC_REFRESH	R/W	0000_0000H
0008H	Data request threshold register	IMC_DATAREQ	R/W	0000_0100H
000CH	Reserved	–	–	–

(2) Image synthesis startup registers

Address	Register Name	Symbol	R/W	After Reset
0010H	Startup reserved register	IMC_START	R/W	0000_0000H
0014H	Status register	IMC_STATUS	R	0000_0000H
0018H	CPU double buffer control register	IMC_CPUBUFSEL	R/W	0000_0000H
001CH	Forced termination register	IMC_STOP	W	0000_0000H

(3) Gamma correction registers

Address	Register Name	Symbol	R/W	After Reset
0020H	Gamma correction control register	IMC_GAMMA_EN	R/W	0000_0000H
0024H	Gamma correction table address register	IMC_GAMMA_ADR	R/W	0000_0000H
0028H	Gamma correction table data register	IMC_GAMMA_DATA	R/W	xxxx_xxxxH
002CH to 003CH	Reserved	–	–	–

(4) Register for immediate startup settings

Address	Register Name	Symbol	R/W	After Reset
0040H	Display area start address register	IMC_WB_AREAADR_P	R/W	0000_0000H
0044H	Address addition value register	IMC_WB_HOFFSET	R/W	0000_0000H
0048H	Format register	IMC_WB_FORMAT	R/W	0000_0000H
004CH	WB image size register	IMC_WB_SIZE	R/W	0000_0000H
0050H	Display area start address register	IMC_WB_AREAADR_Q	R/W	0000_0000H
0054H	WB double buffer control register	IMC_WB_BUFSEL	R/W	0000_0000H
0058H	WB memory frame start position register	IMC_WB_MPOSITION	R/W	0000_0000H
005CH	WB memory frame size register	IMC_WB_MSIZE	R/W	0000_0000H
0060H	Fixed color register	IMC_BACKCOLOR	R/W	0000_0000H
0064H	WB bytelane register	IMC_WB_BYTELANE	R/W	0000_E400H
0068H to 006CH	Reserved	–	–	–
0070H	WB output scanning mode register	IMC_WB_SCANMODE	R/W	0000_0000H
0074H to 0FFCH	Reserved	–	–	–

(5) Register for settings common to all layers

Address	Register Name	Symbol	R/W	After Reset
0100H	Output image horizontal/vertical flip setting register	IMC_MIRROR	R/W	0000_0000H
0104H	Y gain offset register	IMC_YGAINOFFSET	R/W	0000_0080H
0108H	U gain offset register	IMC_UGAINOFFSET	R/W	0000_0080H
010CH	V gain offset register	IMC_VGAINOFFSET	R/W	0000_0080H
0110H	YUV2RGB conversion mode register	IMC_YUV2RGB	R/W	0000_0000H
0114H	Custom coefficient register (Coef R0)	IMC_COEF_R0	R/W	0000_0000H
0118H	Custom coefficient register (Coef R1)	IMC_COEF_R1	R/W	0000_0000H
011CH	Custom coefficient register (Coef R2)	IMC_COEF_R2	R/W	0000_0000H
0120H	Custom coefficient register (Coef R3)	IMC_COEF_R3	R/W	0000_0000H
0124H	Custom coefficient register (Coef G0)	IMC_COEF_G0	R/W	0000_0000H
0128H	Custom coefficient register (Coef G1)	IMC_COEF_G1	R/W	0000_0000H
012CH	Custom coefficient register (Coef G2)	IMC_COEF_G2	R/W	0000_0000H
0130H	Custom coefficient register (Coef G3)	IMC_COEF_G3	R/W	0000_0000H
0134H	Custom coefficient register (Coef B0)	IMC_COEF_B0	R/W	0000_0000H
0138H	Custom coefficient register (Coef B1)	IMC_COEF_B1	R/W	0000_0000H
013CH	Custom coefficient register (Coef B2)	IMC_COEF_B2	R/W	0000_0000H
0140H	Custom coefficient register (Coef B3)	IMC_COEF_B3	R/W	0000_0000H
0144H to 014CH	Reserved	–	–	–
0150H	Alpha select register 0	IMC_ALPHASEL0	R/W	0000_0000H
0154H	Alpha select register 1	IMC_ALPHASEL1	R/W	0000_0000H
0158H to 015CH	Reserved	–	–	–
0160H	Burst enable register	IMC_BURST_EN	R/W	0000_0101H
0164H	Maximum burst length switching threshold register	IMC_THRESHOLD	R/W	0000_1010H
0168H to 01FCH	Reserved	–	–	–

(6) L0 setting registers

Address	Register Name	Symbol	R/W	After Reset
0200H	L0 input image control register	IMC_L0_CONTROL	R/W	0000_0000H
0204H	L0 format register	IMC_L0_FORMAT	R/W	0000_0000H
0208H	L0 double buffer control register	IMC_L0_BUFSEL	R/W	0000_0000H
020CH	L0 byte lane register	IMC_L0_BYTELANE	R/W	0000_E400H
0210H	L0 transparency color control register	IMC_L0_KEYENABLE	R/W	0000_0000H
0214H	L0 transparency color register	IMC_L0_KEYCOLOR	R/W	0000_0000H
0218H	L0 alpha register	IMC_L0_ALPHA	R/W	0000_0000H
021CH	Reserved	–	–	–
0220H	L0 resize register	IMC_L0_RESIZE	R/W	0000_0000H
0224H	L0 horizontal/vertical flip setting register	IMC_L0_MIRROR	R/W	0000_0000H
0228H to 022CH	Reserved	–	–	–
0230H	L0 input address addition value register	IMC_L0_OFFSET	R/W	0000_0000H
0234H	L0 frame buffer start address register (P)	IMC_L0_FRAMEADR_P	R/W	0000_0000H
0238H to 023CH	Reserved	–	–	–
0240H	L0 frame buffer start address register (Q)	IMC_L0_FRAMEADR_Q	R/W	0000_0000H
0244H to 024CH	Reserved	–	–	–
0250H	L0 display position register	IMC_L0_POSITION	R/W	0000_0000H
0254H	L0 display size register	IMC_L0_SIZE	R/W	0000_0000H
0258H to 025CH	Reserved	–	–	–
0260H	L0 memory frame start position register	IMC_L0_MPOSITION	R/W	0000_0000H
0264H	L0 memory frame size register	IMC_L0_MSIZE	R/W	0000_0000H
0268H to 026CH	Reserved	–	–	–
0270H	L0 input scanning mode register	IMC_L0_SCANMODE	R/W	0000_0000H
0274H to 02FCH	Reserved	–	–	–

(7) L1A setting registers

Address	Register Name	Symbol	R/W	After Reset
0300H	L1A input image control register	IMC_L1A_CONTROL	R/W	0000_0000H
0304H	L1A format register	IMC_L1A_FORMAT	R/W	0000_0000H
0308H	L1A double buffer control register	IMC_L1A_BUFSEL	R/W	0000_0000H
030CH	L1A byte lane register	IMC_L1A_BYTELANE	R/W	0000_E400H
0310H	L1A transparency color control register	IMC_L1A_KEYENABLE	R/W	0000_0000H
0314H	L1A transparency color register	IMC_L1A_KEYCOLOR	R/W	0000_0000H
0318H	L1A alpha register	IMC_L1A_ALPHA	R/W	0000_0000H
031CH	Reserved	–	–	–
0320H	L1A resize register	IMC_L1A_RESIZE	R/W	0000_0000H
0324H	L1A horizontal/vertical flip setting register	IMC_L1A_MIRROR	R/W	0000_0000H
0328H to 032CH	Reserved	–	–	–
0330H	L1A input address addition value register	IMC_L1A_OFFSET	R/W	0000_0000H
0334H	L1A frame buffer start address register (P)	IMC_L1A_FRAMEADR_P	R/W	0000_0000H
0338H to 033CH	Reserved	–	–	–
0340H	L1A frame buffer start address register (Q)	IMC_L1A_FRAMEADR_Q	R/W	0000_0000H
0344H to 034CH	Reserved	–	–	–
0350H	L1A display position register	IMC_L1A_POSITION	R/W	0000_0000H
0354H	L1A display size register	IMC_L1A_SIZE	R/W	0000_0000H
0358H to 035CH	Reserved	–	–	–
0360H	L1A memory frame start position register	IMC_L1A_MPOSITION	R/W	0000_0000H
0364H	L1A memory frame buffer size register	IMC_L1A_MSIZE	R/W	0000_0000H
0368H to 036CH	Reserved	–	–	–
0370H	L1A input scanning mode register	IMC_L1A_SCANMODE	R/W	0000_0000H
0374H to 03FCH	Reserved	–	–	–

(8) L1B setting registers

Address	Register Name	Symbol	R/W	After Reset
0400H	L1B input image control register	IMC_L1B_CONTROL	R/W	0000_0000H
0404H	L1B format register	IMC_L1B_FORMAT	R/W	0000_0000H
0408H	L1B double buffer control register	IMC_L1B_BUFSEL	R/W	0000_0000H
040CH	L1B byte lane register	IMC_L1B_BYTELANE	R/W	0000_E400H
0410H	L1B transparency color control register	IMC_L1B_KEYENABLE	R/W	0000_0000H
0414H	L1B transparency color register	IMC_L1B_KEYCOLOR	R/W	0000_0000H
0418H	L1B alpha register	IMC_L1B_ALPHA	R/W	0000_0000H
041CH	Reserved	–	–	–
0420H	L1B resize register	IMC_L1B_RESIZE	R/W	0000_0000H
0424H	L1B horizontal/vertical flip setting register	IMC_L1B_MIRROR	R/W	0000_0000H
0428H to 042CH	Reserved	–	–	–
0430H	L1B input address addition value register	IMC_L1B_OFFSET	R/W	0000_0000H
0434H	L1B frame buffer start address register (P)	IMC_L1B_FRAMEADR_P	R/W	0000_0000H
0438H to 043CH	Reserved	–	–	–
0440H	L1B frame buffer start address register (Q)	IMC_L1B_FRAMEADR_Q	R/W	0000_0000H
0444H to 044CH	Reserved	–	–	–
0450H	L1B display position register	IMC_L1B_POSITION	R/W	0000_0000H
0454H	L1B display size register	IMC_L1B_SIZE	R/W	0000_0000H
0458H to 045CH	Reserved	–	–	–
0460H	L1B memory frame start position register	IMC_L1B_MPOSITION	R/W	0000_0000H
0464H	L1B memory frame buffer size register	IMC_L1B_MSIZE	R/W	0000_0000H
0468H to 046CH	Reserved	–	–	–
0470H	L1B input scanning mode register	IMC_L1B_SCANMODE	R/W	0000_0000H
0474H to 04FCH	Reserved	–	–	–

(9) L1C setting registers

Address	Register Name	Symbol	R/W	After Reset
0500H	L1C input image control register	IMC_L1C_CONTROL	R/W	0000_0000H
0504H	L1C format register	IMC_L1C_FORMAT	R/W	0000_0000H
0508H	L1C double buffer control register	IMC_L1C_BUFSEL	R/W	0000_0000H
050CH	L1C byte lane register	IMC_L1C_BYTELANE	R/W	0000_E400H
0510H	L1C transparency color control register	IMC_L1C_KEYENABLE	R/W	0000_0000H
0514H	L1C transparency color register	IMC_L1C_KEYCOLOR	R/W	0000_0000H
0518H	L1C alpha register	IMC_L1C_ALPHA	R/W	0000_0000H
051CH	Reserved	–	–	–
0520H	L1C resize register	IMC_L1C_RESIZE	R/W	0000_0000H
0524H	L1C horizontal/vertical flip setting register	IMC_L1C_MIRROR	R/W	0000_0000H
0528H to 052CH	Reserved	–	–	–
0530H	L1C input address addition value register	IMC_L1C_OFFSET	R/W	0000_0000H
0534H	L1C frame buffer start address register (P)	IMC_L1C_FRAMEADR_P	R/W	0000_0000H
0538H to 053CH	Reserved	–	–	–
0540H	L1C frame buffer start address register (Q)	IMC_L1C_FRAMEADR_Q	R/W	0000_0000H
0544H to 054CH	Reserved	–	–	–
0550H	L1C display position register	IMC_L1C_POSITION	R/W	0000_0000H
0554H	L1C display size register	IMC_L1C_SIZE	R/W	0000_0000H
0558H to 055CH	Reserved	–	–	–
0560H	L1C memory frame start position register	IMC_L1C_MPOSITION	R/W	0000_0000H
0564H	L1C memory frame buffer size register	IMC_L1C_MSIZE	R/W	0000_0000H
0568H to 056CH	Reserved	–	–	–
0570H	L1C input scanning mode register	IMC_L1C_SCANMODE	R/W	0000_0000H
0574H to 05FCH	Reserved	–	–	–

(10) L2A setting registers

Address	Register Name	Symbol	R/W	After Reset
0600H	L2A input image control register	IMC_L2A_CONTROL	R/W	0000_0000H
0604H	L2A format register	IMC_L2A_FORMAT	R/W	0000_0000H
0608H	L2A double buffer control register	IMC_L2A_BUFSEL	R/W	0000_0000H
060CH	L2A byte lane register	IMC_L2A_BYTELANE	R/W	0000_E4E4H
0610H to 061CH	Reserved	–	–	–
0620H	L2A resize register	IMC_L2A_RESIZE	R/W	0000_0000H
0624H	L2A horizontal/vertical flip control register	IMC_L2A_MIRROR	R/W	0000_0000H
0628H to 062CH	Reserved	–	–	–
0630H	L2A input address addition value register	IMC_L2A_OFFSET	R/W	0000_0000H
0634H	L2A frame buffer start address register (YP)	IMC_L2A_FRAMEADR_YP	R/W	0000_0000H
0638H	L2A frame buffer start address register (UP)	IMC_L2A_FRAMEADR_UP	R/W	0000_0000H
063CH	L2A frame buffer start address register (VP)	IMC_L2A_FRAMEADR_VP	R/W	0000_0000H
0640H	L2A frame buffer start address register (YQ)	IMC_L2A_FRAMEADR_YQ	R/W	0000_0000H
0644H	L2A frame buffer start address register (UQ)	IMC_L2A_FRAMEADR_UQ	R/W	0000_0000H
0648H	L2A frame buffer start address register (VQ)	IMC_L2A_FRAMEADR_VQ	R/W	0000_0000H
064CH	Reserved	–	–	–
0650H	L2A display position register	IMC_L2A_POSITION	R/W	0000_0000H
0654H	L2A display size register	IMC_L2A_SIZE	R/W	0000_0000H
0658H to 065CH	Reserved	–	–	–
0660H	L2A memory frame start position register	IMC_L2A_MPOSITION	R/W	0000_0000H
0664H	L2A memory frame buffer size register	IMC_L2A_MSIZE	R/W	0000_0000H
0668H to 066CH	Reserved	–	–	–
0670H	L2A input scanning mode register	IMC_L2A_SCANMODE	R/W	0000_0000H
0674H to 06FCH	Reserved	–	–	–

(11) L2B setting registers

Address	Register Name	Symbol	R/W	After Reset
0700H	L2B input image control register	IMC_L2B_CONTROL	R/W	0000_0000H
0704H	L2B format register	IMC_L2B_FORMAT	R/W	0000_0000H
0708H	L2B double buffer control register	IMC_L2B_BUFSEL	R/W	0000_0000H
070CH	L2B byte lane register	IMC_L2B_BYTELANE	R/W	0000_E4E4H
0710H to 071CH	Reserved	–	–	–
0720H	L2B resize register	IMC_L2B_RESIZE	R/W	0000_0000H
0724H	L2B horizontal/vertical flip control register	IMC_L2B_MIRROR	R/W	0000_0000H
0728H to 072CH	Reserved	–	–	–
0730H	L2B input address addition value register	IMC_L2B_OFFSET	R/W	0000_0000H
0734H	L2B frame buffer start address register (YP)	IMC_L2B_FRAMEADR_YP	R/W	0000_0000H
0738H	L2B frame buffer start address register (UP)	IMC_L2B_FRAMEADR_UP	R/W	0000_0000H
073CH	L2B frame buffer start address register (VP)	IMC_L2B_FRAMEADR_VP	R/W	0000_0000H
0740H	L2B frame buffer start address register (YQ)	IMC_L2B_FRAMEADR_YQ	R/W	0000_0000H
0744H	L2B frame buffer start address register (UQ)	IMC_L2B_FRAMEADR_UQ	R/W	0000_0000H
0748H	L2B frame buffer start address register (VQ)	IMC_L2B_FRAMEADR_VQ	R/W	0000_0000H
074CH	Reserved	–	–	–
0750H	L2B display position register	IMC_L2B_POSITION	R/W	0000_0000H
0754H	L2B display size register	IMC_L2B_SIZE	R/W	0000_0000H
0758H to 075CH	Reserved	–	–	–
0760H	L2B memory frame start position register	IMC_L2B_MPOSITION	R/W	0000_0000H
0764H	L2B memory frame buffer size register	IMC_L2B_MSIZE	R/W	0000_0000H
0768H to 076CH	Reserved	–	–	–
0770H	L2B input scanning mode register	IMC_L2B_SCANMODE	R/W	0000_0000H
0774H to 07FCH	Reserved	–	–	–

(12) BG setting registers

Address	Register Name	Symbol	R/W	After Reset
0800H	Reserved	–	–	–
0804H	BG format register	IMC_BG_FORMAT	R/W	0000_0000H
0808H	BG double buffer control register	IMC_BG_BUFSEL	R/W	0000_0000H
080CH	BG byte lane register	IMC_BG_BYTELANE	R/W	0000_E400H
0820H	BG resize register	IMC_BG_RESIZE	R/W	0000_0000H
0824H	BG horizontal/vertical flip setting register	IMC_BG_MIRROR	R/W	0000_0000H
0828H to 082CH	Reserved	–	–	–
0830H	BG input address addition value register	IMC_BG_OFFSET	R/W	0000_0000H
0834H	BG frame buffer start address register (P)	IMC_BG_FRAMEADR_P	R/W	0000_0000H
0838H to 083CH	Reserved	–	–	–
0840H	BG frame buffer start address register (Q)	IMC_BG_FRAMEADR_Q	R/W	0000_0000H
0844H to 085CH	Reserved	–	–	–
0860H	BG memory frame start position register	IMC_BG_MPOSITION	R/W	0000_0000H
0864H	BG memory frame buffer size register	IMC_BG_MSIZE	R/W	0000_0000H
0868H to 086CH	Reserved	–	–	–
0870H	BG input scanning mode register	IMC_BG_SCANMODE	R/W	0000_0000H
0874H to 08FCH	Reserved	–	–	–

(13) Interrupt control registers

Address	Register Name	Symbol	R/W	After Reset
0900H	Interrupt status register	IMC_INTSTATUS	R	0000_0000H
0904H	Interrupt raw status register	IMC_INTRAWSTATUS	R	0000_0000H
0908H	Interrupt enable set register	IMC_INTENSET	R/W	0000_0000H
090CH	Interrupt enable clear register	IMC_INTENCLR	W	0000_0000H
0910H	Interrupt source clear register	IMC_INTFFCLR	W	0000_0000H
0914H	AXI read error address register	IMC_ERRORADR_R	R/W	0000_0000H
0918H	AXI write error address register	IMC_ERRORADR_W	R/W	0000_0000H
091CH	AXI write error address register	IMC_ERRORADR_SW	R/W	0000_0000H
0920H to FFFCH	Reserved	–	–	–

(14) Other registers

Address	Register Name	Symbol	R/W	After Reset
FFFCH	Composition register	IMC_COMP	R/W	0000_0000H

A.23 SD Card Interface

Base address: E210_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	SD card command register	SDC_CMD	R/W	0000_0000H
0004H	SD card port select register	SDC_PORT	R/W	0000_0100H
0008H	SD card command parameter register 0	SDC_ARG0	R/W	0000_0000H
000CH	SD card command parameter register 1	SDC_ARG1	R/W	0000_0000H
0010H	SD card stop register	SDC_STOP	R/W	0000_0000H
0014H	SD card transfer sector count register	SDC_SECCNT	R/W	0000_0000H
0018H	SD card response register 0	SDC_RSP0	R	0000_0000H
001CH	SD card response register 1	SDC_RSP1	R	0000_0000H
0020H	SD card response register 2	SDC_RSP2	R	0000_0000H
0024H	SD card response register 3	SDC_RSP3	R	0000_0000H
0028H	SD card response register 4	SDC_RSP4	R	0000_0000H
002CH	SD card response register 5	SDC_RSP5	R	0000_0000H
0030H	SD card response register 6	SDC_RSP6	R	0000_0000H
0034H	SD card response register 7	SDC_RSP7	R	0000_0000H
0038H	SD card information register 1	SDC_INFO1	R/W, R	Undefined (0000_068DH)
003CH	SD card information register 2	SDC_INFO2	R/W, R	Undefined (0000_2080H)
0040H	SD card information mask register 1	SDC_INFO1_MASK	R/W	0000_031DH
0044H	SD card information mask register 2	SDC_INFO2_MASK	R/W	0000_8B7FH
0048H	SD card transfer clock control register	SDC_CLK_CTRL	R/W	0000_0020H
004CH	SD card transfer data size register	SDC_SIZE	R/W	0000_0200H
0050H	SD card option setting register	SDC_OPTION	R/W	0000_00EEH
0054H	Reserved	–	–	–
0058H	SD card error interrupt status register 1	SDC_ERR_STS1	R	0000_2000H
005CH	SD card error interrupt status register 2	SDC_ERR_STS2	R	0000_0000H
0060H	SD card data buffer 0 register	SDC_BUF0	R/W	Undefined
0064H	Reserved	–	–	–
0068H	SDIO mode setting register	SDC_SDIO_MODE	R/W	0000_0000H
006CH	SDIO information register	SDC_SDIO_INFO1	R/W	0000_0000H
0070H	SDIO information mask register	SDC_SDIO_INFO1_MASK	R/W	0000_C007H
0074H-01BCH	Reserved	–	–	–
01C0H	SDC software reset control register	SDC_SOFT_RST	R/W	0000_0000H
01C4H-01E0H	Reserved	–	–	–
0200H	SDC use register	SDC_USER	R/W, R	0000_0004H
0204H	SDC use register 2	SDC_USER2	R/W	0000_0000H

0208H-0210H	Reserved	–	–	–
0214H	AHB bus interface control register	SDC_BUSIF_CTRL	R/W, R	0000_0000H
0218H	Reserved	–	–	–
021CH	DMA mask setting register	SDC_DMAMSK_CTRL	R/W	0000_000FH
0220H	SD write transfer data storage address	SDC_TXMEM_ADDR0L	R/W	0000_0000H
0224H	Reserved	–	–	–
0228H	SD read transfer data storage address	SDC_RXMEM_ADDR0L	R/W	0000_0000H
022CH	Reserved	–	–	–
0230H	SD sector length setting register	SDC_SECTOR_LENGTH0	R/W	0000_0000H
0234H-023CH	Reserved	–	–	–
0240H	SD block length setting register	SDC_BLOCK_LENGTH0	R/W	0000_0000H
0244H-025CH	Reserved	–	–	–
0260H	DMA startup register	SDC_TRANS_START	R/W	0000_0000H
0264H-026CH	Reserved	–	–	–
0270H	Interrupt mask register	SDC_INT_MSK	R/W	0000_000FH
0274H	Interrupt factor RAW register	SDC_INT_RAW	R/W	0000_000FH
0278H	Interrupt factor register	SDC_INT_ORG	R/W	0000_000FH
027CH	Interrupt factor clear register	SDC_INT_CLR	R/W	0000_000FH
0274H-028CH	Reserved	–	–	–
0290H	SD write transfer data storage address	SDC_TXMEM_ADDR0H	R/W	0000_0000H
0294H	Reserved	–	–	–
0298H	SD read transfer data storage address	SDC_RXMEM_ADDR0H	R/W	0000_0000H
0300H	DMA mode SD buffer register	SDC_DMASD	R/W	0000_0000H
0304H to FFFCH	Reserved	–	–	–

A.24 CF Card Interface

Base address: E220_0000H

Address	Register Name	Symbol	R/W	After Reset
C000H	Control register 0	Control-0	R/W	0000_8000H
C004H	Control register 1	Control-1	R/W	0000_0000H
0008H	Reserved	–	–	–
C00CH	Interrupt register	Interrupt	R/W	0000_0000H
C010H	Status register	Status	R	0000_07FEH
C014H	Reserved	–	–	–
C018H	Timing register 1	Timing-1	R/W	0000_0000H
C01CH to C020H	Reserved	–	–	–
C024H	Version register 0	Version-0	R	0000_2007H
C028H	Version register 1	Version-1	R	0000_0222H
C02CH	Data register	DATA	R/W	0000_0000H
C030H	Reserved	–	–	–
C034H	Extension register 0	Extension-0	R/W	0000_0000H
C038H	Extension register 1	Extension-1	R	0000_0002H
C03CH to C044H	Reserved	–	–	–
E000H	Reset control register	RESET_CTRL	R/W	0000_0000H
E004H	Bus interface control register	BUSIF_CTRL	R/W	0000_0000H
E008H	TXMEM address register	TXMEM_ADDR	R/W	3000_8000H
E00CH	RXMEM address register	RXMEM_ADDR	R/W	3000_C000H
E010H	PIO address register	PIO_ADDR	R/W	0000_0000H
E014H	Reserved	–	–	–
E01CH	Block length register	BLOCK_LENGTH	R/W	0000_0001H
E020H	Block index register	BLOCK_INDEX	R/W	0000_0000H
E024H	Transfer start register	TRANS_START	R/W	0000_0000H
E028H, E02CH	Reserved	–	–	–
E034H	Interrupt raw status register	INT_RAW	R	0000_0001H
E038H	Interrupt report register	INT_ORG	R	0000_0000H
E03CH	Interrupt clear register	INT_CLR	W	0000_0000H

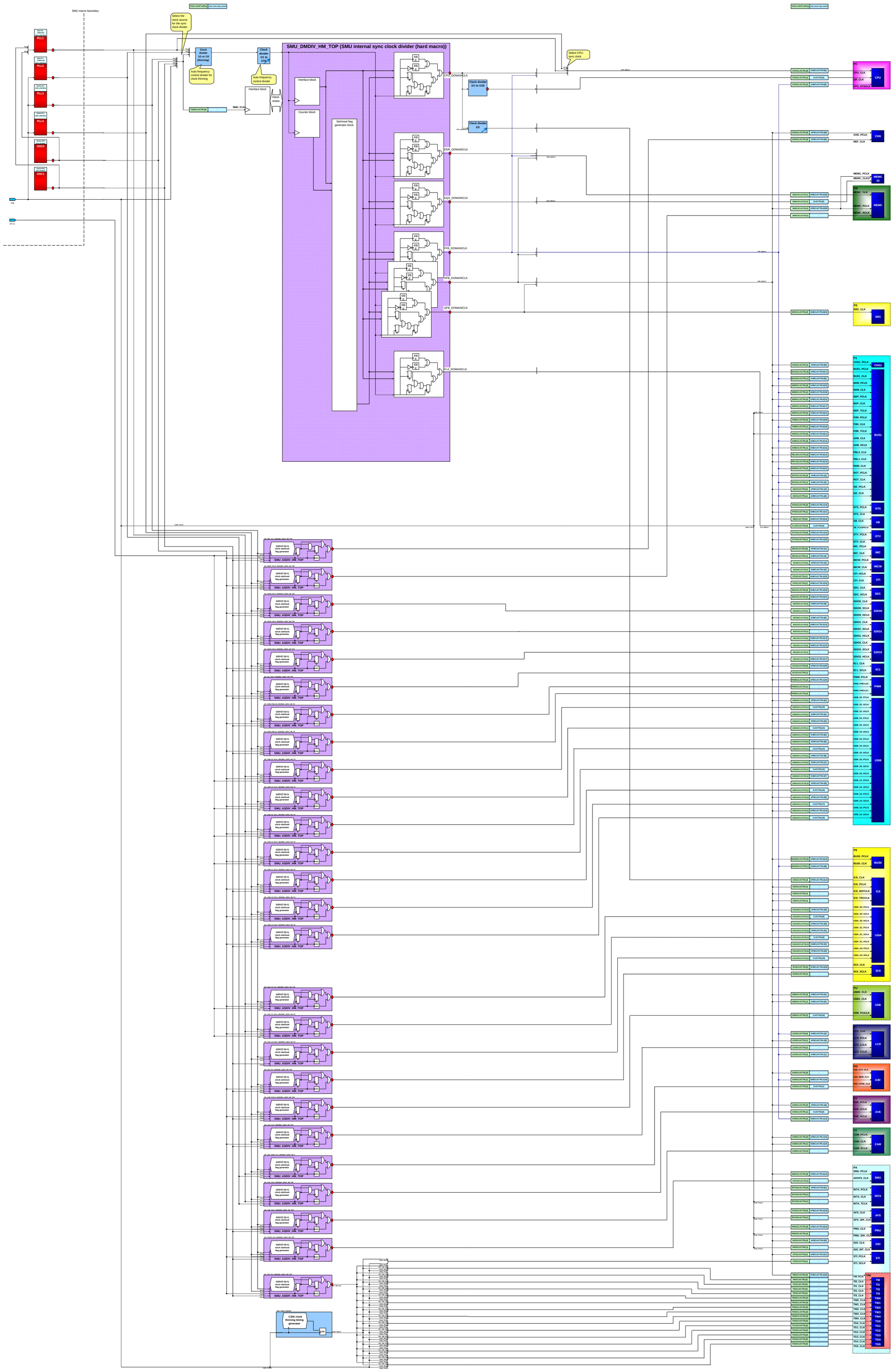
A.25 SDIO Interface

Base address: SDIO0 : E290_0000H
SDIO1 : E2A0_0000H
SDIO2 : E2B0_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H to 0002H	Reserved	–	–	–
0004H	Block size register	SDIO_BLKSIZE	R/W	0000H
0006H	Block count register	SDIO_BLKCOUNT	R/W	0000H
0008H	Argument setting register 0	SDIO_ARG0	R/W	0000H
000AH	Argument setting register 1	SDIO_ARG1	R/W	0000H
000CH	Transfer mode setting register	SDIO_MODE	R/W	0000H
000EH	Command setting register	SDIO_CMD	R/W	0000H
0010H	Response register 0	SDIO_RSP0	R	0000H
0012H	Response register 1	SDIO_RSP1	R	0000H
0014H	Response register 2	SDIO_RSP2	R	0000H
0016H	Response register 3	SDIO_RSP3	R	0000H
0018H	Response register 4	SDIO_RSP4	R	0000H
001AH	Response register 5	SDIO_RSP5	R	0000H
001CH	Response register 6	SDIO_RSP6	R	0000H
001EH	Response register 7	SDIO_RSP7	R	00H
0020H	Buffer data port register 0	SDIO_BUF0	R/W	–
0022H	Buffer data port register 1	SDIO_BUF1	R/W	–
0024H	State register 0	SDIO_STATE0	R	0000H
0026H	State register 1	SDIO_STATE1	R	000AH
0028H	Host control setting register	SDIO_HOST	R/W	00H
0029H	Power control setting register	SDIO_POWER	R/W	00H
002AH	Block gap control setting register	SDIO_BLKGAP	R/W	00H
002BH	Wakeup control setting register	SDIO_WAKEUP	R/W	00H
002CH	Clock control setting register	SDIO_CLKCTRL	R/W	0002H
002EH	Timeout setting register	SDIO_TIMEOUT	R/W	00H
002FH	Software reset setting register	SDIO_SOFTRST	R/W	00H
0030H	Normal interrupt status register	SDIO_NRMINT_STS	R, R/W	0000H
0032H	Error interrupt status register	SDIO_ERRINT_STS	R/W	0000H
0034H	Normal interrupt status enable register	SDIO_NRMINT_STSEN	R/W	0000H
0036H	Error interrupt status enable register	SDIO_ERRINT_STSEN	R/W	0000H
0038H	Normal interrupt signal enable register	SDIO_NRMINT_SIGEN	R/W	0000H
003AH	Error interrupt signal enable register	SDIO_ERRINT_SIGEN	R/W	0000H
003CH	Automatic CMD12 issuance error register	SDIO_CMD12_ERR	R	0000_0000H
003EH	Reserved	–	–	–
0040H	Capability register 0	SDIO_CAP0	R	32B2H
0042H	Capability register 1	SDIO_CAP1	R	07FDH

0044H to 004EH	Reserved	–	–	–
0050H	CMD12 error interrupt force event register	SDIO_CMD12ERR_FORCE	R	0000H
0052H	Error interrupt force event register	SDIO_ERRINT_FORCE	R	0000H
0054H	ADMA1/2 error status register	SDIO_ADMA_ERR	R	0000H
0056H	Reserved	–	–	–
0058H	ADMA1/2 system address register 0 (lower 16 bits)	SDIO_ADMA_SYSADD0	R/W	0000_0000H
005AH	ADMA1/2 system address register 1 (higher 16 bits)	SDIO_ADMA_SYSADD1	R/W	0000_0000H
005CH to 007EH	Reserved	–	–	–
0080H	CE-ATA control register	SDIO_CEATA	R, R/W	0000_0010H
0082H to 00FAH	Reserved	–	–	–
00FCH	Slot interrupt status register	SDIO_SLOTINT_STS	R	00FFH
00FEH	Host controller version register	SDIO_HOSTVER	R	E101H
0100H	AHB IF control register 0	SDIO_AMBA0	R/W	0000_0000H
0102H	Reserved	–	–	–
0104H	AHB IF control register 1	SDIO_AMBA1	R/W	0000_0000H
0106H to DFFEH	Reserved	–	–	–
E000H	Clock delay setting register	SDIO_DLYCYRL	R/W	0000_0000H
E002H	Reserved	–	–	–
E004H	Module port setting register0	SDIO_GPIO0	R/W	0000_8000H
E006H	Reserved	–	–	–
E008H	Module port setting register1	SDIO_GPIO1	R/W	4000_0000H
E00AH to EFFCH	Reserved	–	–	–
F000H	Module enable register	SDIO_MODEN	R/W	0000_0000H
F002H to FFFEH	Reserved	–	–	–

APPENDIX B Clock Tree



APPENDIX C. Boot Loader

C.1 Overview

This chapter describes the boot loader in ROM, which performs the starting processing of EM/EV.
EM/EV has the following two ROM boot modes:

- SD boot: Copies Miniboot from SD to SRAM.
- eMMC boot: Copies Miniboot from eMMC to SRAM.

C.1.1 Restrictions

- SD boot: The SD card must be initialized in the FAT16 (more than 32 MB) or FAT32 format.
  Only formats in which each sector is 512 bytes and each cluster is 64 KB or less are supported.
  LBA format is not supported.
- eMMC boot: If multiple devices are connected, Miniboot is loaded from the eMMC that has the smallest CID.

C.1.2 Cautions

<1> This boot loader uses only the internal SRAM as RAM. (The setting of DDR is specified in the Miniboot that is loaded by this boot loader to SRAM.)

<2> UART0 is used for outputting messages.

<3> SMU_GENERAL_REG0 is used when multiple CPUs are running. For details, see **C.4.1 (1) CPU_ID check processing in common block**.

<4> An SD card cannot be inserted while booting up from an SD card. Booting up in this way is only possible if an SD card is already inserted.

C.2 Operational Overview

The boot loader in ROM requires the boot processing described below.
It's the sequence which does boot mode judgment just after the start by a boot loader in the ROM and transfers to processing of each boot mode.
Processing is moved to the address stocked in BOOT_JUMP_ADDR after processing completion by each boot mode.

The setting of UART0 used by each boot mode commonness is as follows.

Source clock : PLL3
Baud rate : 9600bps
Data length : 8bit
Parity bit : none
Stop bit : 1bit
Flow control : none

C.2.1 SD boot

(1) Specification

After developing MiniBoot stocked in an SD by following specification to an SRAM, processing is moved to MiniBoot.

・The SD card connected to the SD card interface is used.

・The source clock (HFB domain, 14.336 MHz) is used as the macro clock.

・The boot loader runs on the macro clock divided by 64 (= 224 kHz) until initialization (CMD9 issuance). After initialization, the boot loader runs on the macro clock divided by 2 (= 7.168 MHz).

・To keep the system waiting for SD initialization, input a clock for 1 ms.

・A response to the SD_SEND_OP_COND command is used to switch between sector and byte access.

・The boot loader accesses the SD card in bit units.

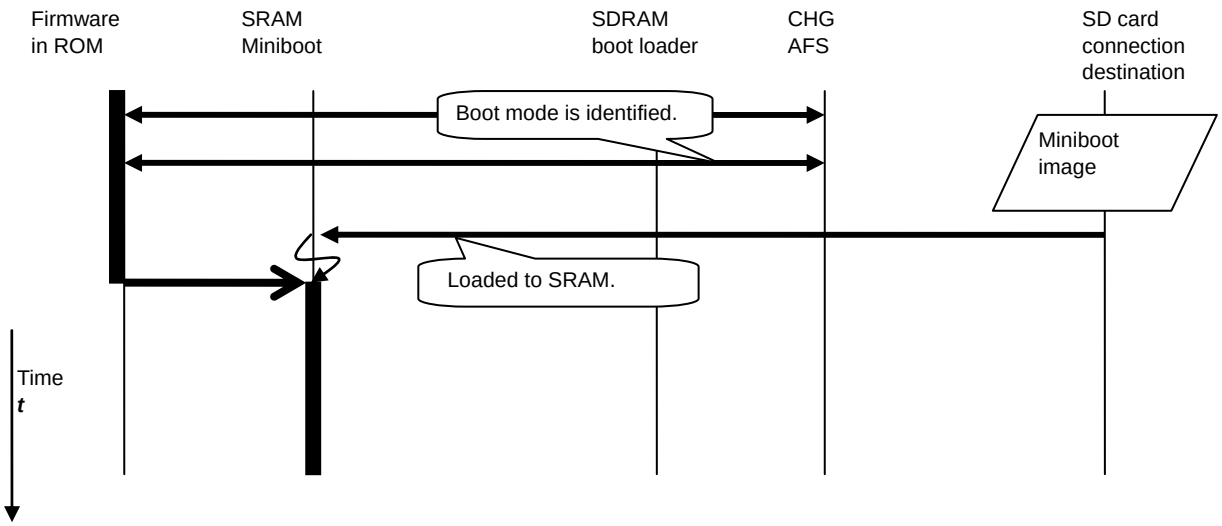
・The host PC searches for sdboot.bin in the root directory of the SD card, which is in the FAT16 (more than 32 MB) or FAT32 format, and then copies this file to the SRAM. However, only formats in which each sector is 512 bytes and each cluster is 64 KB or less are supported.

・The maximum file size of sdboot.bin is 64 KB.

・UART0 is used for outputting messages.

(2) Sequence

If SD boot is identified according to the settings of the CHG_BOOT_MODE register in CHG and the AFS_DATA3 register in AFS, the Miniboot image in the SD card is written to SRAM and execution jumps to the Miniboot.



The processing sequence is as follows.

<1> Initializes UART.

<2> Initializes the SD card interface of EM/EV.

<3> Input a wait signal for 1 ms.

<4> Turns on the power to the SD card.

<5> Acquires MBR and FAT information from the SD card.

<6> Copies the Miniboot file image written to the SD card (file name: `sdboot.bin`) to SRAM.

<7> Jumps to the address stored in the BOOT_JUMP_ADDR register.

C.2.2 eMMC boot

(1) Specification

After developing MiniBoot stocked in eMMC by following specification to an SRAM, processing is moved to MiniBoot.

・eMMC connected to the SDIO0 macro is used.

・The source clock (PLL3) divided by 16 is used as the macro clock.

・The boot loader runs on the macro clock divided by 64 (= 224 kHz) until initialization (CMD6 issuance). After initialization, the boot loader runs on the undivided macro clock (= 14.336 MHz).

・To keep the system waiting for eMMC initialization, input a clock for 1 ms.

・A response to the SEND_OP_COND command is used to switch between sector and byte access.

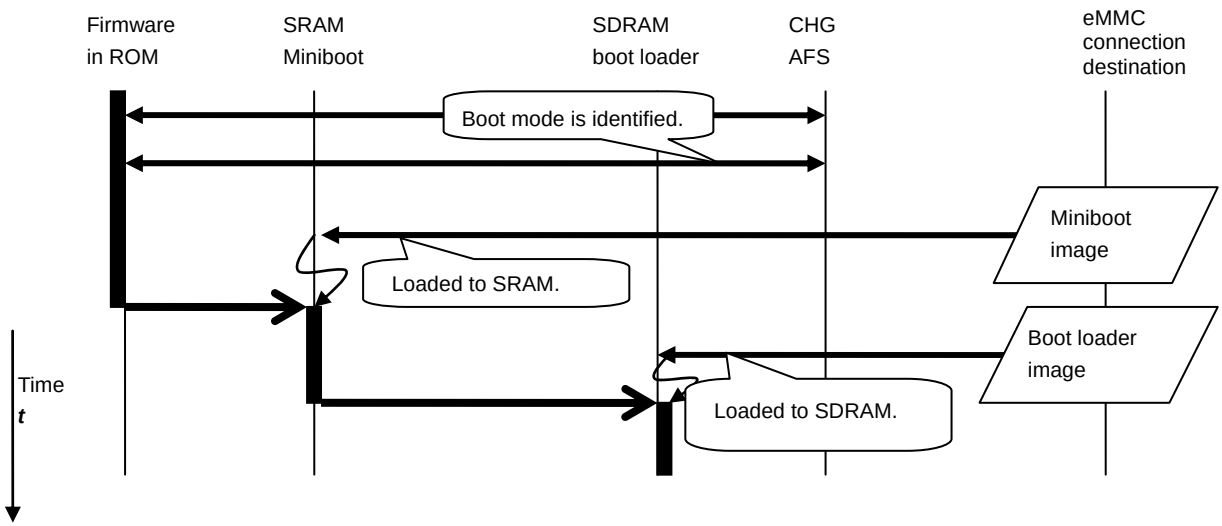
・The boot loader accesses eMMC in 4-bit units.

・The boot loader reads the master boot record (MBR) from the eMMC in which RCA is set to 01H (the smallest CID), and reads 8 KB from the LBA of the first active partition table.

・UART0 is used for outputting messages.

(2) Sequence

If eMMC boot is identified according to the settings of the CHG_BOOT_MODE register in CHG and the AFS_DATA3 register in AFS, the Miniboot image in eMMC with RCA = 01 is written to SRAM and execution jumps to the Miniboot.



The processing sequence is as follows.

<1> Initializes UART.

<2> Initializes the SDIO0 interface of EM/EV.

<3> Input a wait signal for 1 ms.

<4> Turns on the power to the eMMC device.

<5> Acquires MBR information from the eMMC device with RCA = 01H.

<6> Copies 8 KB from the LBA of the first active partition table to SRAM.

(If there is no active partition table, the first partition table is used.)

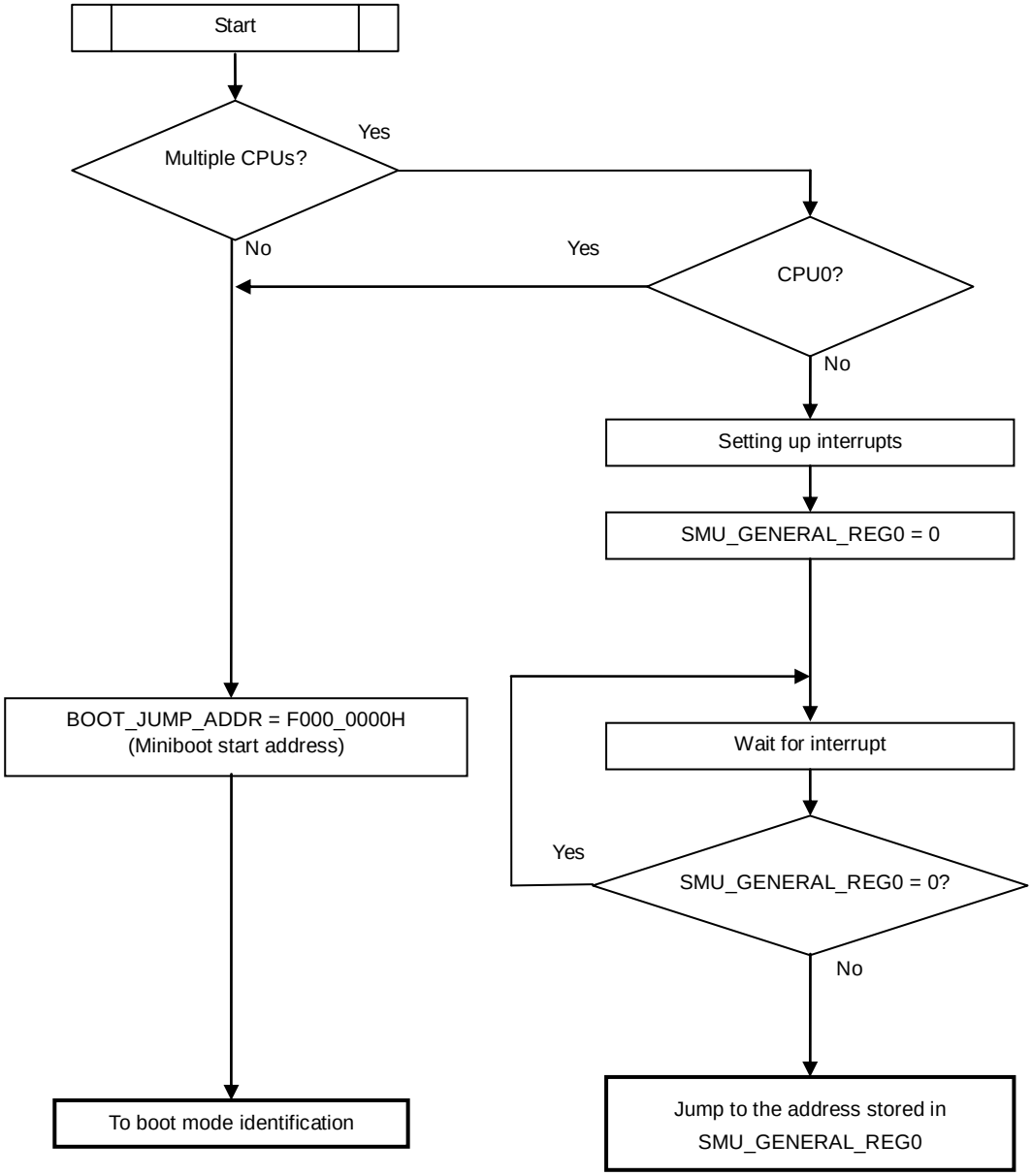
<7> Jumps to Miniboot.

C.3 Processing Flow

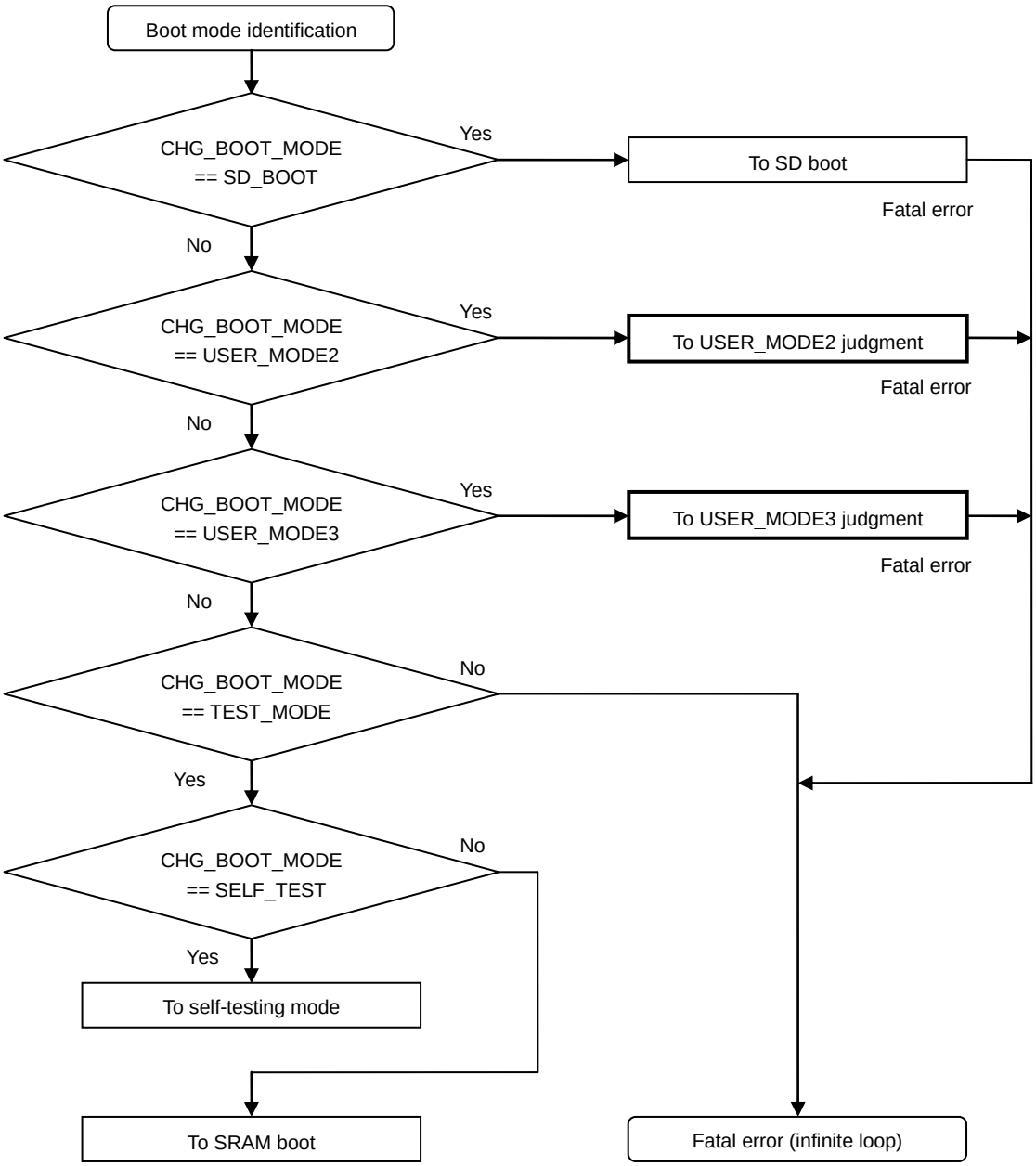
This chapter provides details about the overall operation of the ROM-internal boot loader and provides flowcharts. The processing immediately after starting up EM/EV is assumed to be the common block, and, after identifying the operating mode in this block, each type of boot processing is performed.

C.3.1 ROM-internal boot loader common processing

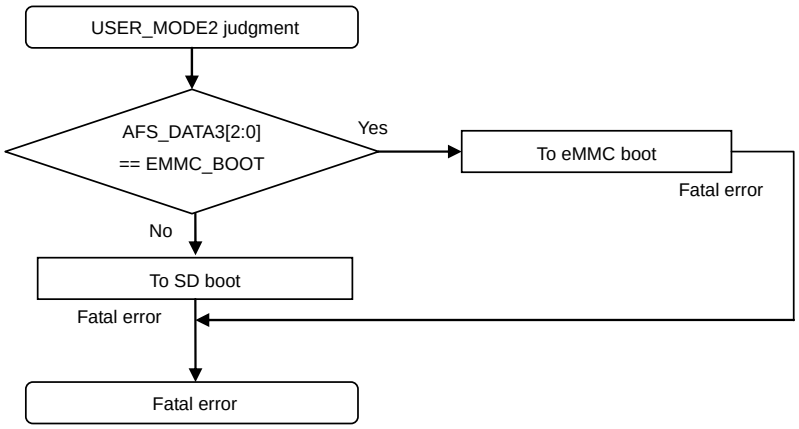
(1) CPU_ID check processing in common block



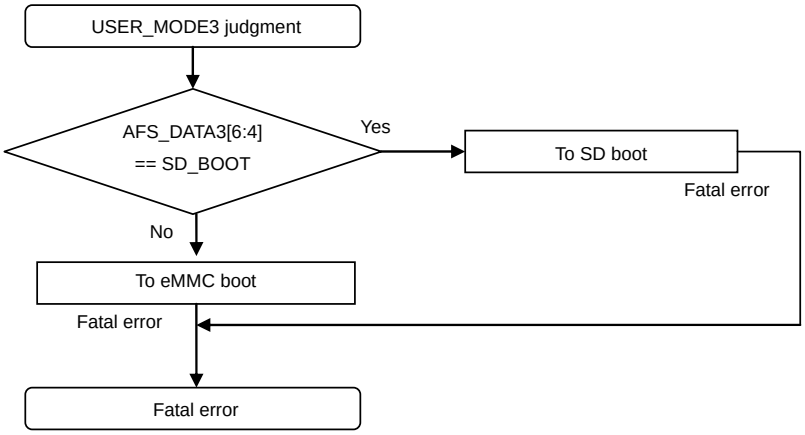
(2) Common boot mode identification



(3) USER MODE2 judgment



(4) USER MODE3 judgment



(5) Registers used in the common block

Register settings for basic ROM-internal boot loader processing

In the common block, the following registers are referenced to select the boot processing:

Register Name	Address	Available bit	Value	Description
CHG_BOOT_MODE	E014_0000H	0000_000FH	0000_000AH	eSD boot
		0000_0007H	0000_0000H	–
			0000_0002H	USER BOOT2
			0000_0004H	USER BOOT3
			0000_0006H	Test mode
AFS_DATA3	E00C_002CH	0000_0007H	0000_0000H	[USER BOOT2] SD boot
			0000_0001H	[USER BOOT2] eMMC boot
			0000_0002H	–
			0000_0003H	–
			0000_0004H	–
		0000_0070H	0000_0000H	[USER BOOT3] eMMC boot
			0000_0010H	[USER BOOT3] SD boot
			0000_0020H	–
			0000_0030H	–
			0000_0040H	–
AFS_DATA2	E00C_0028H	C000_0000H	8000_0000H	CPU0 disable
			4000_0000H	CPU1 disable
			0000_0000H	Dual CPU enable

Remarks The items in brackets are only referenced if the items are enabled.

The registers and settings for when UART0 is used are as follows:

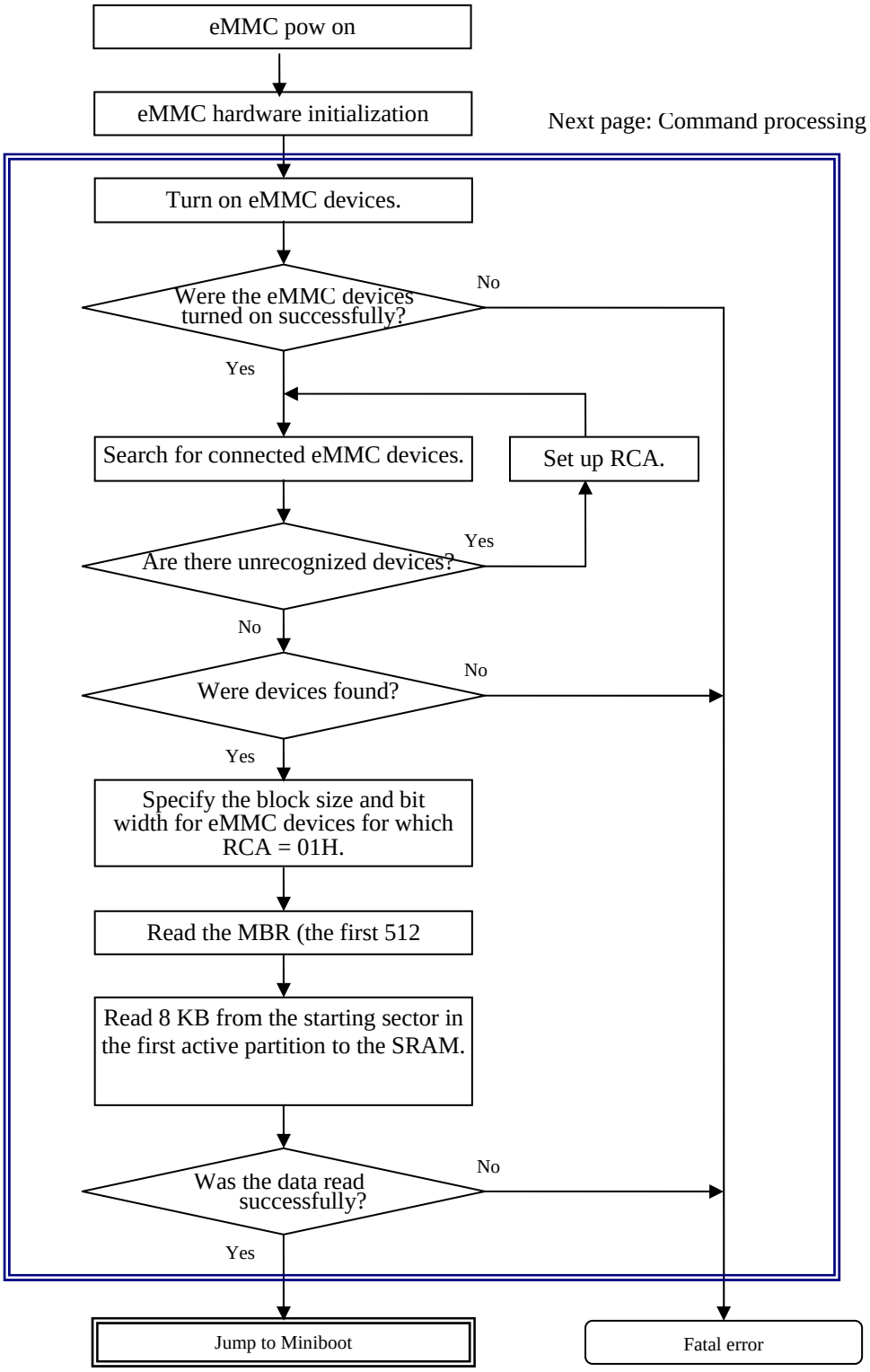
No.	Register Name	Address	Specified Value	Remark
1	SMU_USIAU0GCLKCTRL	E011_04A0H	FFFF_FFFDH	Stop USIA_U0_SCLK.
2	SMU_USIAU0SCLKDIV	E011_061CH	0000_0000H	PLL3 undivided
3	SMU_USIAU0GCLKCTRL	E011_04A0H	FFFF_FFFFH	Supply USIA_U0_SCLK.
4	UART0_IER	E102_0004H	0000H	Disable interrupts.
5	UART0_LCR	E102_0010H	0083H	DLAB = on
6	UART0_DLL	E102_0024H	00D5H	9,600 bps
7	UART0_DLM	E102_0028H	0005H	9,600 bps
8	UART0_LCR	E102_0010H	0003H	DLAB off, 8-bit transfer
9	UART0_MCR	E102_0014H	0003H	RTS, DTR on
10	UART0_FCR	E102_000CH	0006H	Reset transmission/reception FIFO

The registers set up in the common block and their values are as follows (in order of setup):

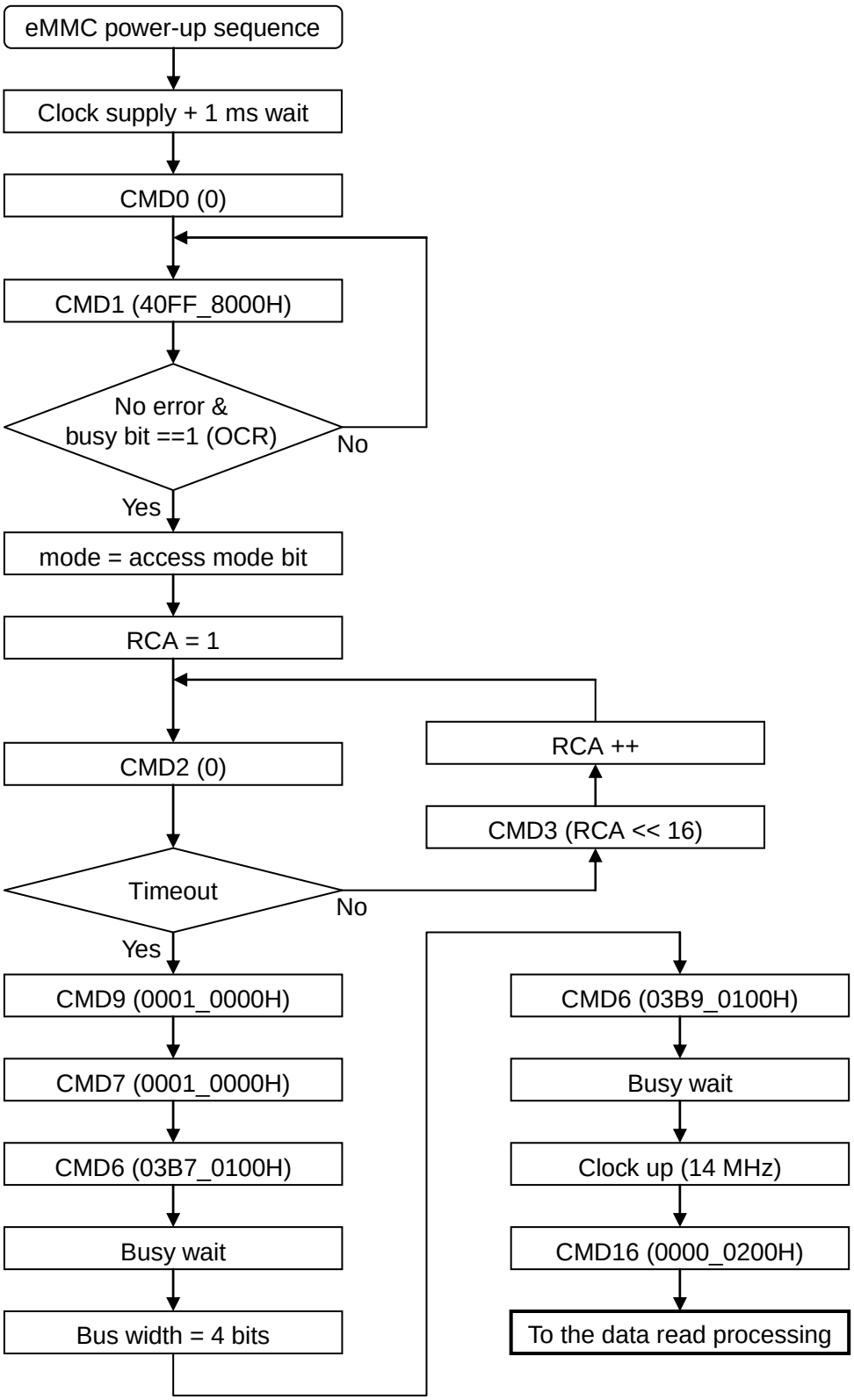
No.	Register Name	Address	Specified Value	Remark
1	INTA_ICCICR	E002_0000H	0000_0003H	When there are multiple CPUs and CPU 1 is running
	INTA_ICCIPMR	E002_0004H	0000_00F0H	
	SMU_GENERAL_REG0	E011_07C0H	0000_0000H	
	INTA_ICCEOIR	E002_0010H	Value read from INTA_ICCIAR (E002_000CH)	
2	–	–	–	–
3	SMU_AVEGCLKCTRL	E011_0464H	0000_0000H	Disable the AVE macro clock.
4	SMU_A3DGCLKCTRL	E011_0468H	0000_0000H	Disable the A3D macro clock.
5	SMU_USBGCLKCTRL	E011_0494H	0000_0000H	Disable the USB macro clock.
6	–	–	–	–
7	SMU_GIO_RSTCTRL	E011_000CH	FFFF_FFFFH	End the GIO macro reset.
8	SMU_INTA_RSTCTRL	E011_0010H	FFFF_FFFFH	End the INTA macro reset.
9	SMU_CHG_RSTCTRL	E011_0014H	FFFF_FFFFH	End the CHG macro reset.
10	SMU_CHG1_RSTCTRL	E011_0018H	FFFF_FFFFH	End the CHG1 macro reset.
11	SMU_ROM_RSTCTRL	E011_0044H	FFFF_FFFFH	End the ROM macro reset.
12	SMU_MEMC_RSTCTRL	E011_004CH	FFFF_FFFFH	End the MEMC macro reset.
13	–	–	–	–
14	SMU_TI0_RSTCTRL	E011_00ECH	FFFF_FFFFH	End the TI0 macro reset.
15	SMU_TW0_RSTCTRL	E011_00FCH	FFFF_FFFFH	End the TW0 macro reset.
16	SMU_TG0_RSTCTRL	E011_010CH	FFFF_FFFFH	End the TG0 macro reset.
17	SMU_AB0_RSTCTRL	E011_0048H	FFFF_FFFFH	End the AB0 macro reset.
18	SMU_SDIO0_RSTCTRL	E011_00BCH	FFFF_FFFFH	End the SDIO0 macro reset.
19	SMU_SDC_RSTCTRL	E011_00C8H	FFFF_FFFFH	End the SDC macro reset.
20	–	–	–	–
21	CHG_P1_LAT	E014_0004H	0000_2222H	Set up unmasked output.
22	–	–	–	–
23	INTA_ICDICR	E0028_000H	0000_0000H	Disable interrupts.

C.3.2 eMMC boot processing

(1) eMMC boot processing

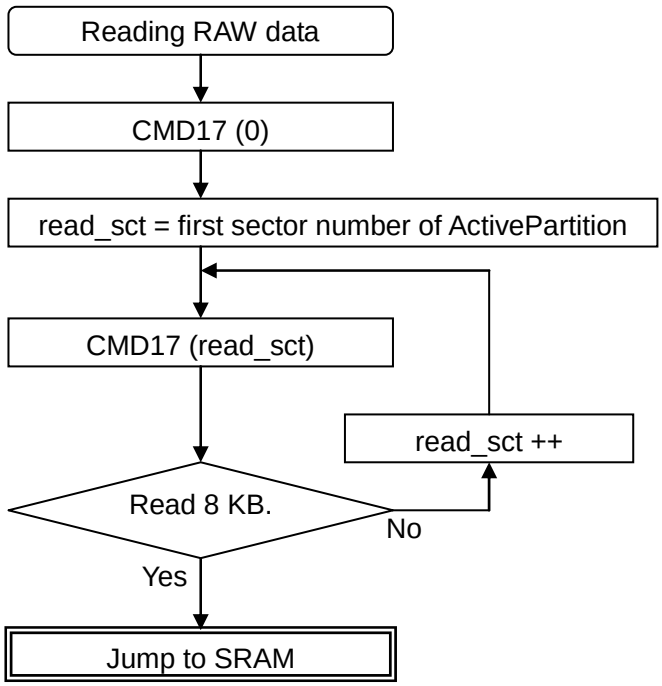


Command processing (1/2)



Remark When issuing a command other than CMD1, the boot processing stops if an error occurs.

Command processing (2/2)



(2) Registers and settings for eMMC boot

Booting up from eMMC hardware is selected by specifying the following combination of register settings (in the USER BOOT2 or USER BOOT3 mode):

Boot Mode	Register Name	Address	Available bit	Value
USER BOOT2	CHG_BOOT_MODE	E014_0000H	bit[2:0]	0000_0002H
	AFS_DATA3	E00C_002CH	bit[2:0]	0000_0001H
USER BOOT3	CHG_BOOT_MODE	E014_0000H	bit[2:0]	0000_0004H
	AFS_DATA3	E00C_002CH	bit[6:4]	0000_0000H

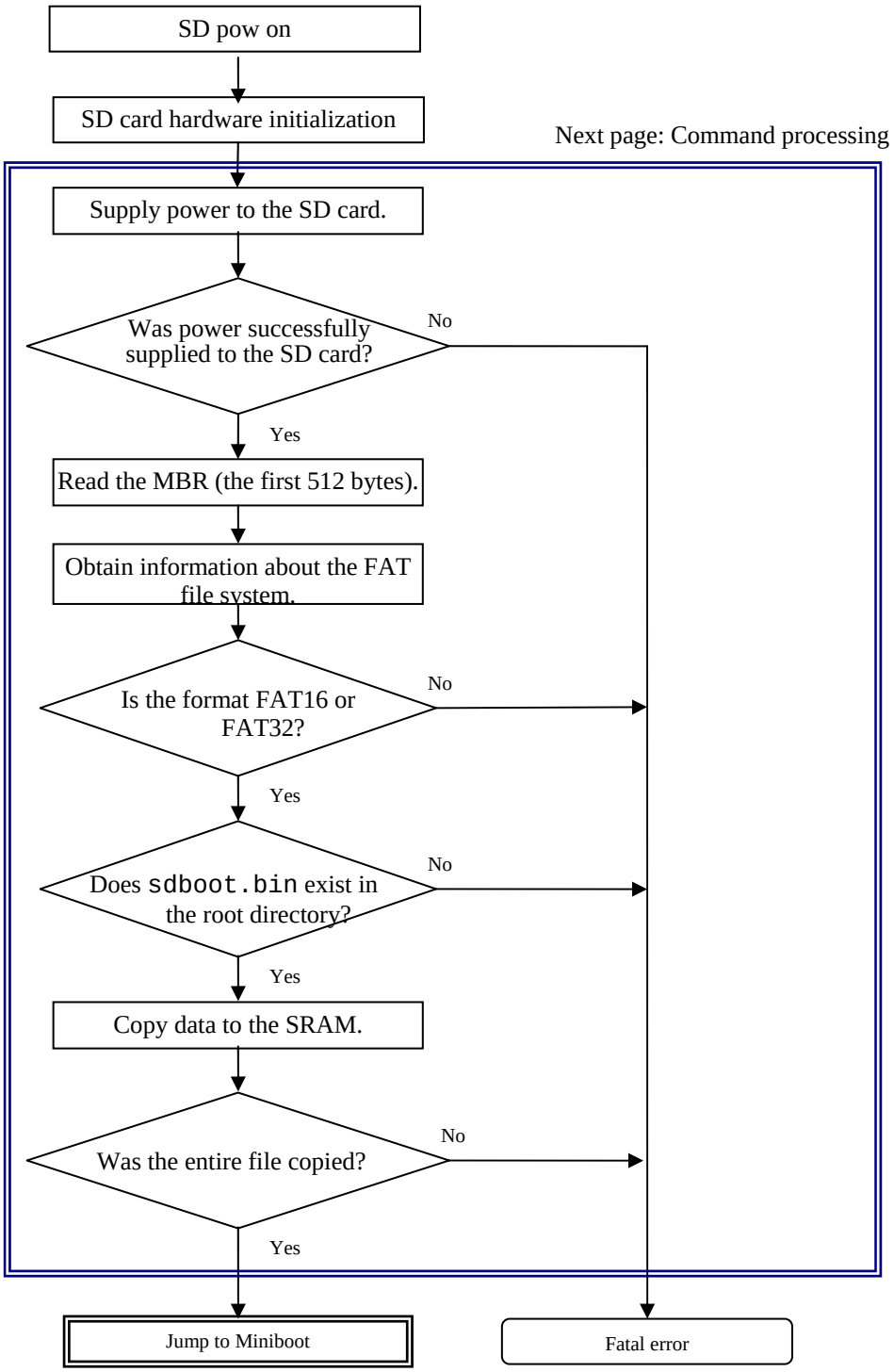
The registers that are specified when an eMMC boot is executed are shown below (in that order).

No.	Register Name	Address	Specified Value	Remark
1	SMU_SDIO0GCLKCTRL	E011_04C8H	FFFF_FFFDH	Supply SDIO0 CLK, SDIO0_HCLK
2	CHG_PINSEL_SD	E014_0290H	0000_0000H (0000_000CH)	Switch the pin function from eMMC to mode 0.
3	CHG_PINSEL_G032	E014_0204H	0000_0000H (1FFC_0000H)	Switch the pin function to SDIO0 mode. GPIO_[050:060] → SDIO0
4	CHG_DRIVE1	E014_0404H	0000_5400H (0000_FC00H)	Change the SDIO0 drive capability. SDI0_CKO,SDI0_CKI, SDI0_CMD, SDI0_DATA[0:7]: 6 mA
5	CHG_PULL4	E014_0310H	0DC0_0000H (0FFF_0000H)	Change settings for SDIO. SDI0_CKO: CMOS, input masked, no pull SDI0_CKI: Schmitt trigger, input not masked, no pull SDI0_CMD: Schmitt trigger, input not masked, pull up
6	CHG_PULL5	E014_0314H	DDDD_DDDDH	Change settings for SDIO. SDI0_DATA[0:7]: Schmitt trigger, input not masked, pull up
7	SMU_SDIO0SCLKDIV	E011_0648H	0000_000FH	PLL3, 1/16
8	SMU_SDIO0GCLKCTRL	E011_04C8H	FFFF_FFFFH	Supply SDIO0 SCLK.

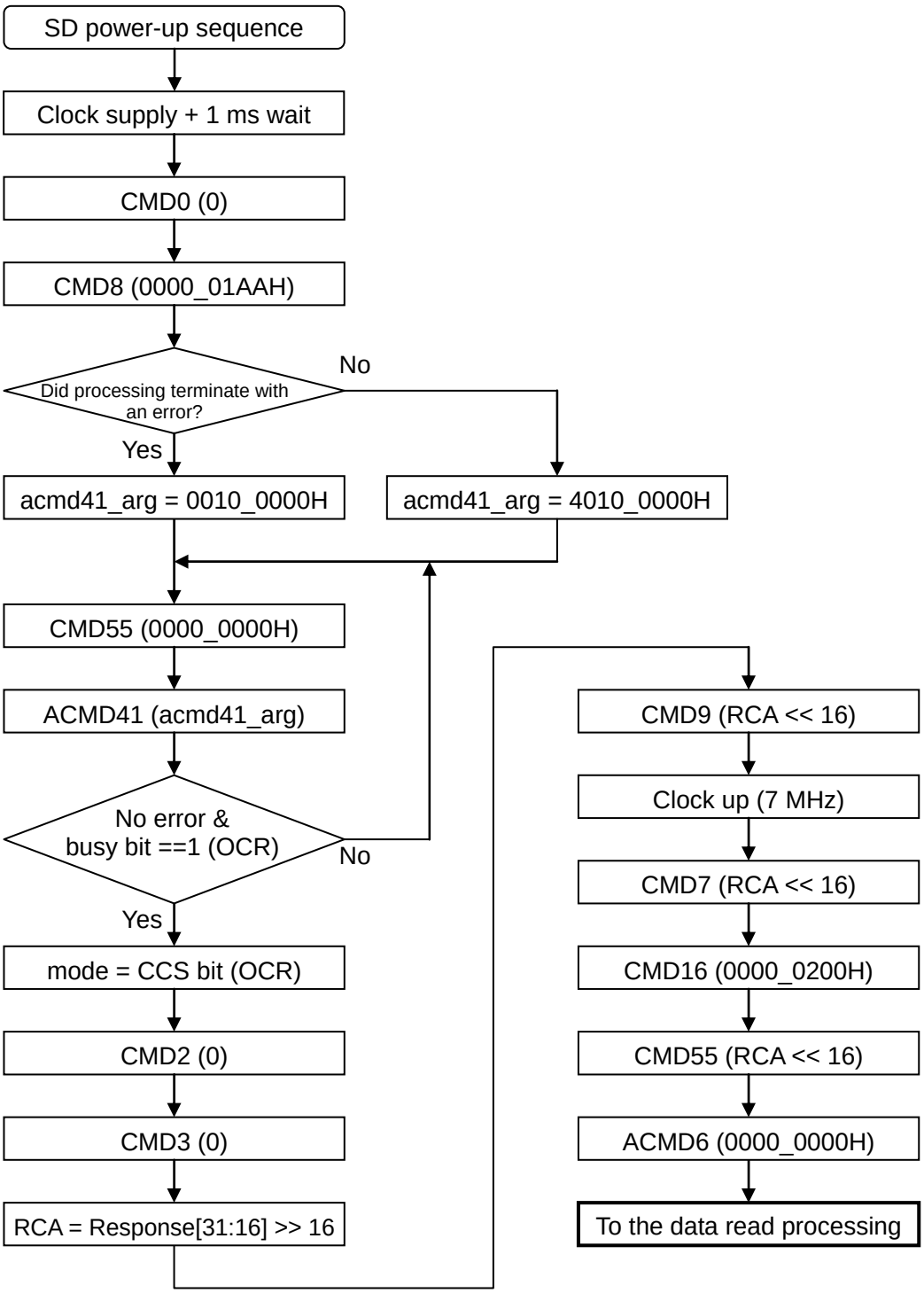
Remark The contents of brackets for fields to which values are written indicate valid bits.

C.3.3 SD boot processing

(1) SD boot processing

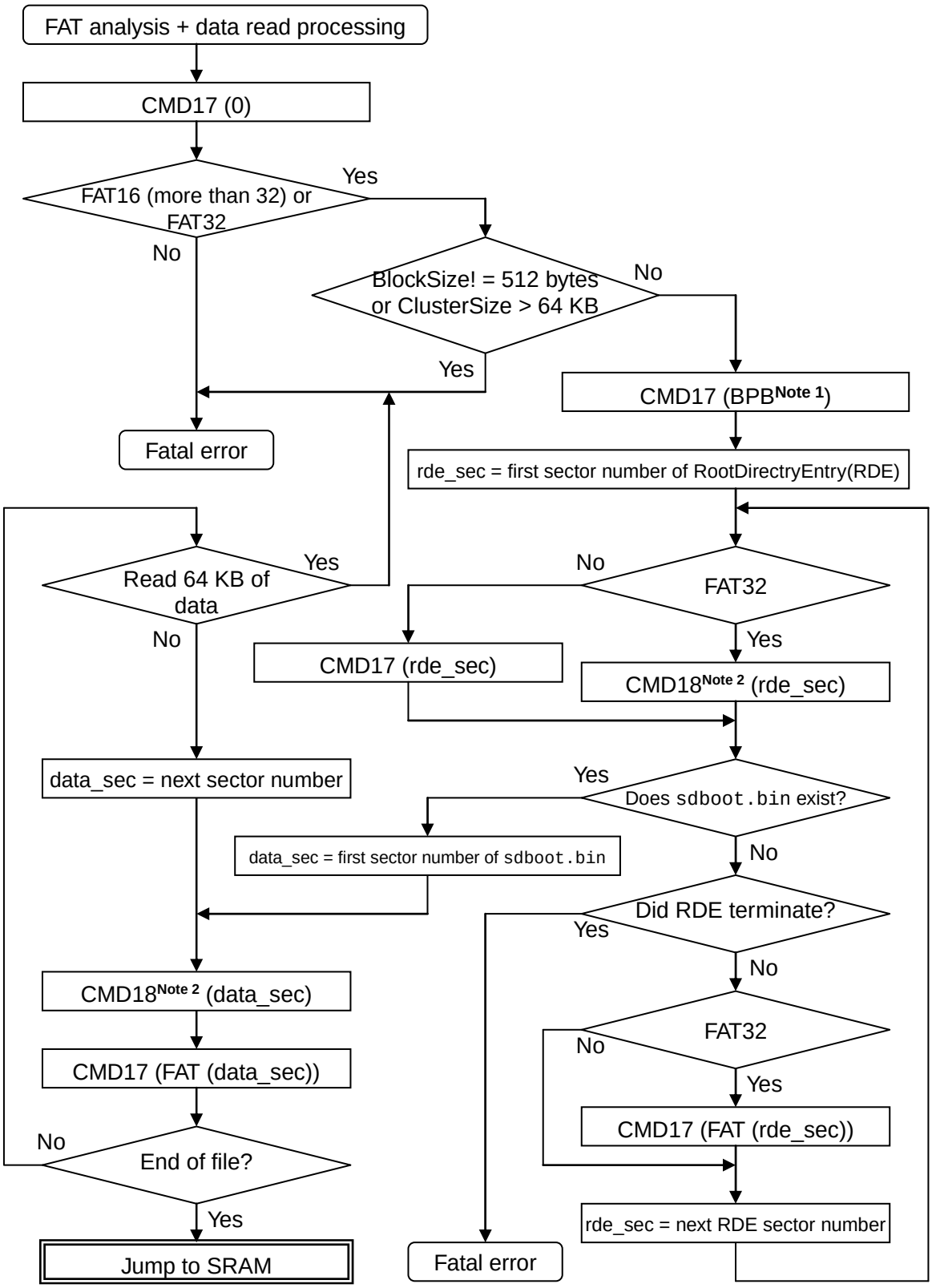


Command processing (1/2)



Remark When issuing a command other than CMD8 or ACMD41, the boot processing stops if an error occurs.

Command processing (2/2)



Notes 1. BPB: First partition sector number read from the MBR partition table

2. CMD18 reads one cluster.

(2) FAT information when booting up from an SD card

The FAT information obtained when booting up from the ROM is stored in the SRAM (the beginning of the work area) as a `fat_info_t` structure. The `root_entry` member of this structure is used to decide between FAT16 and FAT32.

■ `fat_info_t` structure

Type	Member Name	Description
`int`	`bpb_sec_pos`	BPB storage sector number
`int`	`fat_sec_pos`	First FAT sector number
`int`	`rde_sec_pos`	FAT16: First RDE sector number FAT32: First RDE cluster number
`int`	`user_sec_pos`	First user area sector number
`int`	`byte_per_sec`	Number of bytes per sector
`int`	`sec_per_clus`	Number of sectors per cluster
`int`	`root_entry`	FAT16: RDE number (not 0) FAT32: 0
`int`	`sec_per_fat`	Number of sectors per FAT
`int`	`sec_rde_size`	FAT16: RDE size FAT32: 0
`int`	`reserved`	–
`int`	`reserved`	–

(3) Registers and settings for SD boot

Booting up from an SD card is selected by specifying the following combination of register settings (in the USER BOOT2 or USER BOOT3 mode):

Boot Mode	Register Name	Address	Available bit	Value
USER BOOT2	CHG_BOOT_MODE	E014_0000H	0000_0007H	0000_0002H
	AFS_DATA3	E00C_002CH	0000_0007H	0000_0000H
USER BOOT3	CHG_BOOT_MODE	E014_0000H	0000_0007H	0000_0004H
	AFS_DATA3	E00C_002CH	0000_0070H	0000_0010H

The registers that are specified when an SD boot is executed are shown below (in that order).

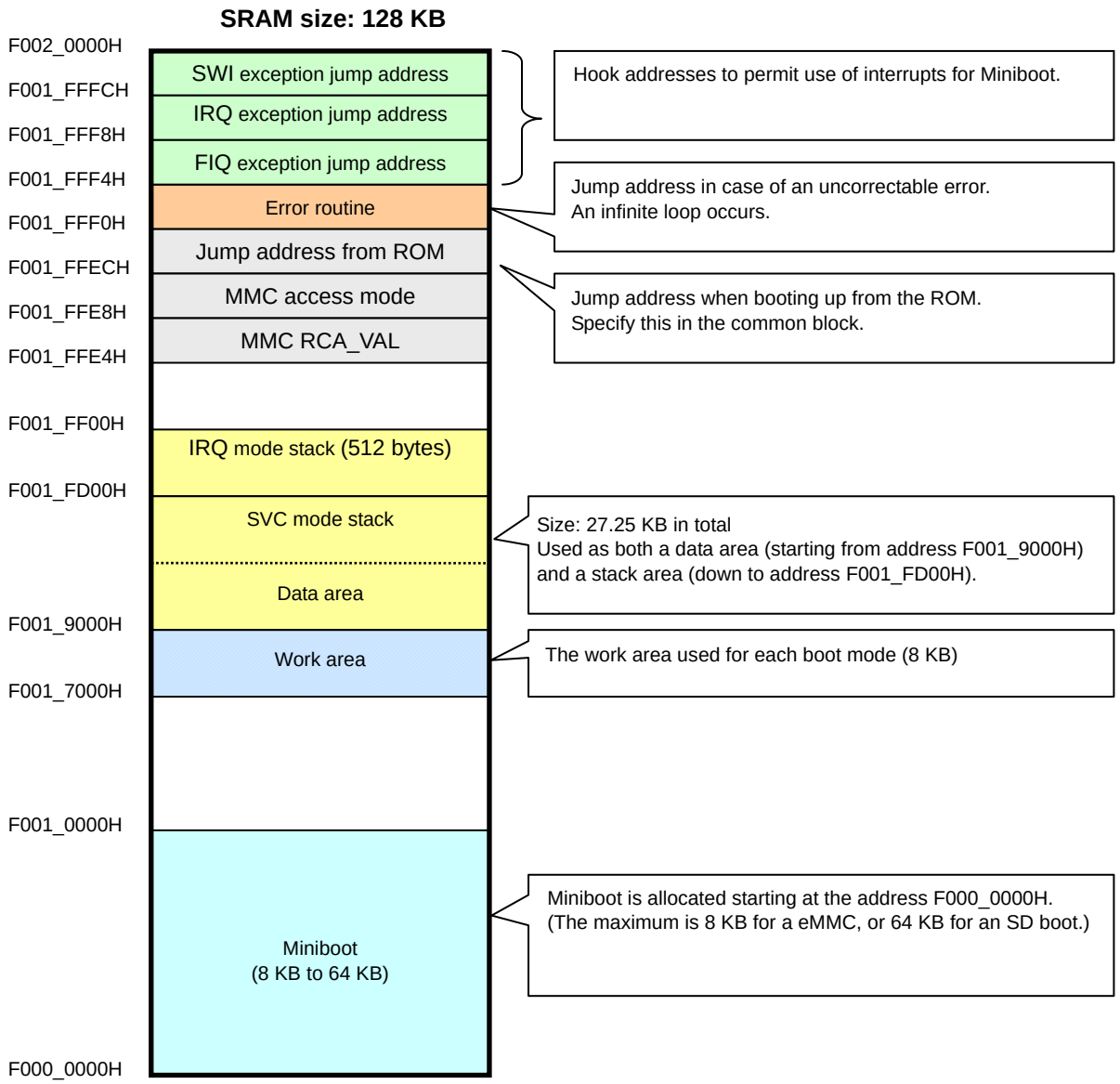
No.	Register Name	Address	Specified Value	Remark
1	CHG_PINSEL_SD	E014_0290H	0000_0000H (0000_0003H)	Switch the SD pin function to mode 0.
2	CHG_PINSEL_G032	E014_0204H	0000_0000H (0001_0000H)	Switch the pin function to SD mode. GPIO_P048 → SD
3	CHG_DRIVE1	E014_0404H	5000_0000H (F000_0000H)	Change the SD drive capability. SD_CKO, SD_CKI, SD_CMD, SD_DATA[0:3]: 6 mA
4	CHG_PULL4	E014_0310H	0000_0DDCH (0000_0FFFH)	Change settings for SD. SD_CKI: Schmitt trigger, input not masked, no pull SD_CMD, SD_DATA[0:3]: Schmitt trigger, input not masked, pull up
5	SMU_SDCGCLKCTRL	E011_04D4H	FFFF_FFFDH	Supply SDC CLK/HCLK

Remark The contents of brackets for fields to which values are written indicate valid bits.

C.4 Memory Allocation

C.4.1 SRAM

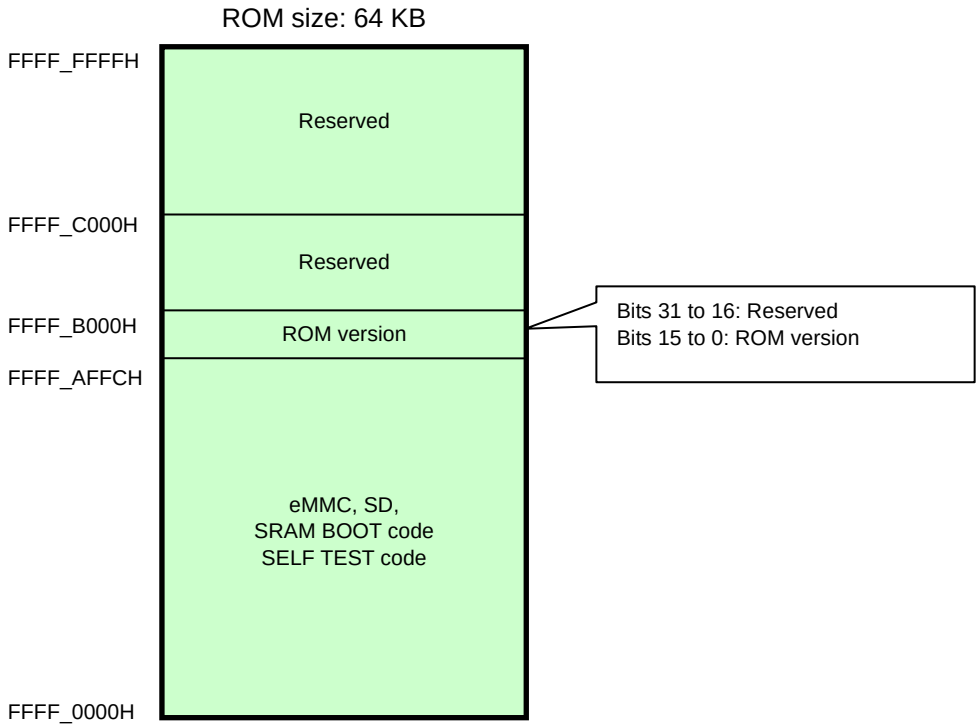
The memory allocations of the internal SRAM used by this ROM boot loader are shown below.



Work area

- When booting up from an SD card, FAT information (described in **C.3.4 (2) FAT information when booting up from an SD card**) is stored at the beginning of the work area.
- When booting up from eMMC hardware, the MBR (512 bytes) is stored at the beginning of the work area.

C.4.2 ROM


ROM size: 64 KB
FFFF_FFFFH
Reserved
FFFF_C000H
Reserved
FFFF_B000H
ROM version
FFFF_AFFCH
eMMC, SD,
SRAM BOOT code
SELF TEST code
FFFF_0000H
Bits 31 to 16: Reserved
Bits 15 to 0: ROM version

APPENDIX D Signal Pins

Pin No.	PinName	I/O	I/O power	Mode0		Mode1		Mode2		Mode3		GPIO	Default Mode	PinSel	PinSel_GIO	Pull Note1	Drive Note2	Reset					Standby		Buffer Type
				Name	I/O	Name	I/O	Name	I/O	Name	I/O							IO	Output	Input mask	pu/pd	Drive	Output	Input	
B22	LCD3_PXCLK	IO	3.3V	LCD3_PXCLK	O	YUV3_CLK_O	O					GPIO_018	GPIO_018	CHG_PINSEL_LCD3[1:0]	CHG_PINSEL_G000_LCD33[18]	G_018	LCD_7	I	-	M	PD	4	PD	L	G
C21	GPIO_019	IO	3.3V									GPIO_019	GPIO_019	-	CHG_PINSEL_G000_LCD33[19]	G_019	LCD_8	I	-	M	PD	4	PD	L	G
A21	LCD3_CLK_I	IO	3.3V	LCD3_CLK_I	I	YUV3_CLK_I	I					GPIO_020	GPIO_020	CHG_PINSEL_LCD3[1:0]	CHG_PINSEL_G000[20]	G_020	LCD_9	I	-	M	PD	4	PD	L	G
B21	LCD3_HS	IO	3.3V	LCD3_HS	O	YUV3_HS	O					GPIO_021	GPIO_021		CHG_PINSEL_G000_LCD33[21]	G_021	LCD_10	I	-	M	PD	4	PD	L	G
C20	LCD3_VS	IO	3.3V	LCD3_VS	O	YUV3_VS	O					GPIO_022	GPIO_022		CHG_PINSEL_G000_LCD33[22]	G_022	LCD_11	I	-	M	PD	4	PD	L	G
D19	LCD3_DE	IO	3.3V	LCD3_DE	O	YUV3_DE	O					GPIO_023	GPIO_023		CHG_PINSEL_G000_LCD33[23]	G_023	LCD_12	I	-	M	PD	4	PD	L	G
D20	GPIO_024	IO	3.3V									GPIO_024	GPIO_024	-	CHG_PINSEL_G000[24]	G_024	LCD_13	I	-	M	PD	4	PD	L	G
E20	GPIO_025	IO	3.3V									GPIO_025	GPIO_025	-	CHG_PINSEL_G000[25]	G_025	LCD_14	I	-	M	PD	4	PD	L	G
F16	GPIO_026	IO	3.3V									GPIO_026	GPIO_026	-	CHG_PINSEL_G000[26]	G_026	LCD_15	I	-	M	PD	4	PD	L	G
F17	GPIO_027	IO	3.3V									GPIO_027	GPIO_027	-	CHG_PINSEL_G000[27]	G_027	LCD_16	I	-	M	-	4	Hi-Z	L	H
F18	GPIO_028	IO	3.3V									GPIO_028	GPIO_028	-	CHG_PINSEL_G000[28]	G_028	LCD_17	I	-	M	-	4	Hi-Z	L	H
G18	GPIO_029	IO	3.3V									GPIO_029	GPIO_029	-	CHG_PINSEL_G000[29]	G_029	LCD_18	I	-	M	-	4	Hi-Z	L	H
H18	GPIO_030	IO	3.3V									GPIO_030	GPIO_030	-	CHG_PINSEL_G000[30]	G_030	LCD_19	I	-	M	-	4	Hi-Z	L	H
J18	GPIO_031	IO	3.3V									GPIO_031	GPIO_031	-	CHG_PINSEL_G000[31]	G_031	LCD_20	I	-	M	-	4	Hi-Z	L	H
A20	LCD3_R0	IO	3.3V	LCD3_R0	O							GPIO_032	GPIO_032	-	CHG_PINSEL_G032_LCD33[0]	G_032	LCD_2	I	-	M	PD	4	PD	L	G
B20	LCD3_R1	IO	3.3V	LCD3_R1	O							GPIO_033	GPIO_033	-	CHG_PINSEL_G032_LCD33[1]	G_033		I	-	M	PD	4	PD	L	G
A19	LCD3_R2	IO	3.3V	LCD3_R2	O							GPIO_034	GPIO_034	-	CHG_PINSEL_G032_LCD33[2]	G_034		I	-	M	PD	4	PD	L	G
B19	LCD3_R3	IO	3.3V	LCD3_R3	O							GPIO_035	GPIO_035	-	CHG_PINSEL_G032_LCD33[3]	G_035		I	-	M	PD	4	PD	L	G
C19	LCD3_R4	IO	3.3V	LCD3_R4	O							GPIO_036	GPIO_036	-	CHG_PINSEL_G032_LCD33[4]	G_036		I	-	M	PD	4	PD	L	G
B18	LCD3_R5	IO	3.3V	LCD3_R5	O							GPIO_037	GPIO_037	-	CHG_PINSEL_G032_LCD33[5]	G_037	LCD_3	I	-	M	PD	4	PD	L	G
C18	LCD3_R6	IO	3.3V	LCD3_R6	O			TP33_CLK	O			GPIO_038	GPIO_038	CHG_PINSEL_LCD3[9:8]	CHG_PINSEL_G032_LCD33[6]	G_038	LCD_4	I	-	M	PD	4	PD	L	G
D18	LCD3_R7	IO	3.3V	LCD3_R7	O			TP33_CTRL	O			GPIO_039	GPIO_039		CHG_PINSEL_G032_LCD33[7]	G_039	LCD_5	I	-	M	PD	4	PD	L	G
A18	LCD3_G0	IO	3.3V	LCD3_G0	O	YUV3_D0	O	TP33_DATA0	O			GPIO_040	GPIO_040	CHG_PINSEL_LCD3[11:10]	CHG_PINSEL_G032_LCD33[8]	G_040	LCD_6	I	-	M	PD	4	PD	L	G
A17	LCD3_G1	IO	3.3V	LCD3_G1	O	YUV3_D1	O	TP33_DATA1	O			GPIO_041	GPIO_041		CHG_PINSEL_G032_LCD33[9]	G_041		I	-	M	PD	4	PD	L	G
B17	LCD3_G2	O	3.3V	LCD3_G2	O	YUV3_D2	O	TP33_DATA2	O			-	LCD3_G2		-	-		O	L	M	-	4	PD	L	G
C17	LCD3_G3	O	3.3V	LCD3_G3	O	YUV3_D3	O	TP33_DATA3	O			-	LCD3_G3		-	-		O	L	M	-	4	PD	L	G
D17	LCD3_G4	O	3.3V	LCD3_G4	O	YUV3_D4	O	TP33_DATA4	O			-	LCD3_G4		-	-		O	L	M	-	4	PD	L	G
B16	LCD3_G5	O	3.3V	LCD3_G5	O	YUV3_D5	O	TP33_DATA5	O			-	LCD3_G5		-	-		O	L	M	-	4	PD	L	G
C16	LCD3_G6	O	3.3V	LCD3_G6	O	YUV3_D6	O	TP33_DATA6	O			-	LCD3_G6		-	-		O	L	M	-	4	PD	L	G
D16	LCD3_G7	O	3.3V	LCD3_G7	O	YUV3_D7	O	TP33_DATA7	O			-	LCD3_G7		-	-		O	L	M	-	4	PD	L	G
A16	LCD3_B0	IO	3.3V	LCD3_B0	O	YUV3_D8	O	TP33_DATA8	O			GPIO_042	GPIO_042		CHG_PINSEL_G032_LCD33[10]	G_042		I	-	M	PD	4	PD	L	G
A15	LCD3_B1	IO	3.3V	LCD3_B1	O	YUV3_D9	O	TP33_DATA9	O			GPIO_043	GPIO_043		CHG_PINSEL_G032_LCD33[11]	G_043		I	-	M	PD	4	PD	L	G
B15	LCD3_B2	O	3.3V	LCD3_B2	O	YUV3_D10	O	TP33_DATA10	O			-	LCD3_B2		-	-		O	L	M	-	4	PD	L	G
C15	LCD3_B3	O	3.3V	LCD3_B3	O	YUV3_D11	O	TP33_DATA11	O			-	LCD3_B3		-	-		O	L	M	-	4	PD	L	G
D15	LCD3_B4	O	3.3V	LCD3_B4	O	YUV3_D12	O	TP33_DATA12	O			-	LCD3_B4		-	-		O	L	M	-	4	PD	L	G
B14	LCD3_B5	O	3.3V	LCD3_B5	O	YUV3_D13	O	TP33_DATA13	O			-	LCD3_B5		-	-		O	L	M	-	4	PD	L	G
C14	LCD3_B6	O	3.3V	LCD3_B6	O	YUV3_D14	O	TP33_DATA14	O			-	LCD3_B6		-	-		O	L	M	-	4	PD	L	G
D14	LCD3_B7	O	3.3V	LCD3_B7	O	YUV3_D15	O	TP33_DATA15	O			-	LCD3_B7		-	-		O	L	M	-	4	PD	L	G
V13	UART0_RX	I	1.8V/3.3V	UART0_RX	I							-	UART0_RX	-	-	UART0	-	I	-	M	PD	4	PD	L	J
V12	UART0_TX	O	1.8V/3.3V	UART0_TX	O							-	UART0_TX	-	-	-	UART_0	O	H	M	-	4	PU	L	I
Y11	UART1_RX	IO	1.8V/3.3V	UART1_RX	I							GPIO_155	GPIO_155	-	CHG_PINSEL_G128[27]	G_155	UART_1	I	-	M	PD	4	PD	L	J
Y10	UART1_TX	IO	1.8V/3.3V	UART1_TX	O							GPIO_156	GPIO_156	-	CHG_PINSEL_G128[28]	G_156		I	-	M	-	4	Hi-Z	L	K
AA10	UART1_CTSB	IO	1.8V/3.3V	UART1_CTSB	I	UART2_RX	I					GPIO_157	GPIO_157	CHG_PINSEL_UART[1:0]	CHG_PINSEL_G128[29]	G_157	UART_2	I	-	M	PD	4	PD	L	J
AB10	UART1_RTSB	IO	1.8V/3.3V	UART1_RTSB	O	UART2_TX	O					GPIO_158	GPIO_158		CHG_PINSEL_G128[30]	G_158		I	-	M	-	4	Hi-Z	L	K
AA9	IIC0_SCL	IO	1.8V/3.3V	IIC0_SCL	OT							GPIO_044	IIC0_SCL	-	CHG_PINSEL_G032[12]	G_044	IIC0	I	-	M	-	4	Hi-Z	L	K
AA8	IIC0_SDA	IO	1.8V/3.3V	IIC0_SDA	OT							GPIO_045	IIC0_SDA	-	CHG_PINSEL_G032[13]	G_045		I	-	M	-	4	Hi-Z	L	K
Y9	IIC1_SCL	IO	1.8V/3.3V	IIC1_SCL	OT	UART3_RX	I					GPIO_046	IIC1_SCL	CHG_PINSEL_IIC[1:0]	CHG_PINSEL_G032[14]	G_046	IIC1	I	-	M	-	4	Hi-Z	L	K
Y8	IIC1_SDA	IO	1.8V/3.3V	IIC1_SDA	OT	UART3_TX	O					GPIO_047	IIC1_SDA		CHG_PINSEL_G032[15]	G_047		I	-	M	-	4	Hi-Z	L	K
AC20	SD_CKO	O	3.3V	SD_CKO	O							-	SD_CKO	-	-	-	SD_0	O	L	M	-	4	PD	L	G
AC19	SD_CKI	IO	3.3V	SD_CKI	I							GPIO_048	SD_CKI	-	CHG_PINSEL_G032[16]	G_048	SD_1	I	-	M	PD	4	PD	L	G
AB17	SD_CMD	IO	3.3V	SD_CMD	I/O							-	SD_CMD	-	-	SD_CM		I	-	M	PD	4	PD	L	G
Y18	SD_DATA0	IO	3.3V	SD_DATA0	I/O							-	SD_DATA0	-	-	SD_D		I	-	M	PD	4	PD	L	G
AA18	SD_DATA1	IO	3.3V	SD_DATA1	I/O							-	SD_DATA1	-	-	SD_D		I	-	M	PD	4	PD	L	G
Y17	SD_DATA2	IO	3.3V	SD_DATA2	I/O							-	SD_DATA2	-	-	SD_D		I	-	M	PD	4	PD	L	G
AA17	SD_DATA3	IO	3.3V	SD_DATA3	I/O							-	SD_DATA3	-	-	SD_D		I	-	M	PD	4	PD	L	G
AB16	GPIO_049	IO	3.3V									GPIO_049	GPIO_049	-	CHG_PINSEL_G032[17]	G_049		I	-	M	PD	4	PD	L	G
AB18	SDI0_CKO	IO	3.3V	SDI0_CKO	O							GPIO_050	GPIO_050	-	CHG_PINSEL_G032[18]	G_050	SDI0_0	I	-	M	PD	4	PD	L	G
AC18	SDI0_CKI	IO	3.3V	SDI0_CKI	I							GPIO_051	SDI0_CKI	-	CHG_PINSEL_G032[19]	G_051	SDI0_1	I	-	M	PD	4	PD	L	G
Y12	SDI0_CMD	IO	3.3V	SDI0_CMD	I/O							GPIO_052	SDI0_CMD	-	CHG_PINSEL_G032[20]	G_052		I	-	M	PD	4	PD	L	G
AA13	SDI0_DATA0	IO	3.3V	SDI0_DATA0	I/O							GPIO_053	SDI0_DATA0	-	CHG_PINSEL_G032[21]	G_053		I	-	M	PD	4	PD	L	G
Y13	SDI0_DATA1	IO	3.3V	SDI0_DATA1	I/O							GPIO_054	SDI0_DATA1	-	CHG_PINSEL_G032[22]	G_054		I	-	M	PD	4	PD	L	G
AA14	SDI0_DATA2	IO	3.3V	SDI0_DATA2	I/O							GPIO_055	SDI0_DATA2	-	CHG_PINSEL_G032[23]	G_055		I	-	M	PD	4	PD	L	G
Y14	SDI0_DATA3	IO	3.3V	SDI0_DATA3	I/O							GPIO_056	SDI0_DATA3	-	CHG_PINSEL_G032[24]	G_056		I	-	M	PD	4	PD	L	G
AA15	SDI0_DATA4	IO	3.3V	SDI0_DATA4	I/O							GPIO_057	GPIO_057	-	CHG_PINSEL_G032[25]	G_057	SDI0_2	I	-	M	PD	4	PD	L	G
Y15	SDI0_DATA5	IO	3.3V	SDI0_DATA5	I/O							GPIO_058	GPIO_058	-	CHG_PINSEL_G032[26]	G_058		I	-	M	PD	4	PD	L	G
AA16	SDI0_DATA6	IO	3.3V	SDI0_DATA6	I/O							GPIO_059	GPIO_059	-	CHG_PINSEL_G032[27]	G_059		I	-	M	PD	4	PD	L	G
Y16	SDI0_DATA7	IO	3.3V	SDI0_DATA7	I/O							GPIO_060	GPIO_060	-	CHG_PINSEL_G032[28]	G_060		I	-	M	PD	4	PD	L	G
AB22	SDI1_CKO	IO	3.3V	SDI1_CKO	O							GPIO_061	GPIO_061	-	CHG_PINSEL_G032[29]	G_061	SDI1_0	I	-	M	PD	4	PD	L	G
AA23	SDI1_CKI	IO	3.3V	SDI1_CKI	I							GPIO_062	SDI1_CKI	-	CHG_PINSEL_G032[30]	G_062	SDI1_1	I	-	M	PD	4	PD	L	G
AC21	SDI1_CMD	IO	3.3V	SDI1_CMD	I/O							GPIO_063	SDI1_CMD	-	CHG_PINSEL_G032[31]	G_063		I	-	M	PD	4	PD	L	G
AB21	SDI1_DATA0	IO	3.3V	SDI1_DATA0	I/O							GPIO_064	SDI1_DATA0	-	CHG_PINSEL_G064[0]	G_064		I	-	M	PD	4	PD	L	G
AB20	SDI1_DATA1	IO	3.3V	SDI1_DATA1	I/O							GPIO_065	SDI1_DATA1	-	CHG_PINSEL_G064[1]	G_065		I	-	M	PD	4	PD	L	G
AB19	SDI1_DATA2	IO	3.3V	SDI1_DATA2	I/O							GPIO_066	SDI1_DATA2	-	CHG_PINSEL_G064[2]	G_066		I	-	M	PD	4	PD	L	G
AA19	SDI1_DATA3	IO	3.3V	SDI1_DATA3	I/O							GPIO_067	SDI1_DATA3	-	CHG_PINSEL_G064[3]	G_067		I	-	M	PD	4	PD	L	G
J23	AB_CLK	IO	3.3V	AB_CLK	O							GPIO_068	GPIO_068	-	CHG_PINSEL_G064[4]	G_068	AB_0	I	-	M	PD	8	PD	L	G
D21	AB_CSB0	IO	3.3V	AB_CSB0	O							GPIO_069	GPIO_069	-	CHG_PINSEL_G064[5]	G_069	AB_1	I	-	M	PU	8	PU	L	F
E21	AB_CSB1	IO	3.3V	AB_CSB1	O							GPIO_070	GPIO_070	-	CHG_PINSEL_G064[6]	G_070		I	-	M	PU	8	PU	L	F
F20	AB_CSB2	IO	3.3V	AB_CSB2	O			CF_CSB0	O			GPIO_071	GPIO_071	CHG_PINSEL_AB[1:0]	CHG_PINSEL_G064[7]	G_071	AB_2	I	-	M	-	8	Hi-Z	L	H
G20	AB_CSB3	IO	3.3V	AB_CSB3	O			CF_CSB1	O			GPIO_072	GPIO_072		CHG_PINSEL_G064[8]	G_072		I	-	M	-	8	Hi-Z	L	H
J20	AB_RDB	IO	3.3V	AB_RDB	O			CF_IORDB	O			GPIO_073	GPIO_073		CHG_PINSEL_G064[9]	G_073		I	-	M	-	8	Hi-Z	L	H
H20	AB_WRB	IO	3.3V	AB_WRB	O			CF_IOWRB	O			GPIO_074	GPIO_074		CHG_PINSEL_G064[10]	G_074		I	-	M	-	8	Hi-Z	L	H
L20	AB_WAIT	IO	3.3V	AB_WAIT	I			CF_IORDY	I			GPIO_075	GPIO_075		CHG_PINSEL_G064[11]	G_075	AB_3	I	-	M	-	4	Hi-Z	L	H
K20	AB_ADV	IO	3.3V	AB_ADV	O			CF_RESET	O			GPIO_076	GPIO_076		CHG_PINSEL_G064[12]	G_076	AB_4	I	-	M	-	8	Hi-Z	L	H
C23	AB_AD0	IO	3.3V	AB_AD0	I/O			CF_D00	I/O			GPIO_077	GPIO_077		CHG_PINSEL_G064[13]	G_077	AB_5	I	-	T	PD	8	PD	L	G
C22	AB_AD1	IO	3.3V	AB_AD1	I/O			CF_D01	I/O			GPIO_078	GPIO_078		CHG_PINSEL_G064[14]	G_078		I	-	T	PD	8	PD	L	G
D23	AB_AD2	IO	3.3V	AB_AD2	I/O			CF_D02	I/O			GPIO_079	GPIO_079		CHG_PINSEL_G064[15]	G_079		I	-	T	PD	8	PD	L	G
D22	AB_AD3	IO	3.3V	AB_AD3	I/O			CF_D03	I/O			GPIO_080	GPIO_080		CHG_PINSEL_G064[16]	G_080		I	-	T	PD	8	PD	L	G
E23	AB_AD4	IO	3.3V	AB_AD4	I/O			CF_D04	I/O			GPIO_081	GPIO_081		CHG_PINSEL_G064[17]	G_081		I	-	T	PD	8	PD	L	G
E22	AB_AD5	IO	3.3V	AB_AD5	I/O			CF_D05	I/O			GPIO_082	GPIO_082		CHG_PINSEL_G064[18]	G_082		I	-	T	PD	8	PD	L	G
F23	AB_AD6	IO	3.3V	AB_AD6	I/O			CF_D06	I/O			GPIO_083	GPIO_083		CHG_PINSEL_G064[19]	G_083		I	-	T	PD	8	PD	L	G
F22	AB_AD7	IO	3.3V	AB_AD7	I/O			CF_D07	I/O			GPIO_084	GPIO_084		CHG_PINSEL_G064[20]	G_084		I	-	T	PD	8	PD	L	G
F21	AB_AD8	IO	3.3V	AB_AD8	I/O	DTV_BCLK	I	CF_D08	I/O	USI5_CLK	I/O	GPIO_085	GPIO_085	CHG_PINSEL_AB[3:2]	CHG_PINSEL_G064[21]	G_085	AB_6	I	-	T	PD	8	PD	L	G
G23	AB_AD9	IO	3.3V	AB_AD9	I/O	DTV_PSYNC	I	CF_D09	I/O	USI5_DI	I	GPIO_086	GPIO_086		CHG_PINSEL_G064[22]	G_086	AB_7	I	-	T	PD	8	PD	L	G
G22	AB_AD10	IO	3.3V	AB_AD10	I/O	DTV_VALID	I	CF_D10	I/O	USI5_DO	O	GPIO_087	GPIO_087		CHG_PINSEL_G064[23]	G_087		I	-	T	PD	8	PD	L	G
G21	AB_AD11	IO	3.3V	AB_AD11	I/O	DTV_DATA	I	CF_D11	I/O	USI5_CS0	I/O	GPIO_088	GPIO_088		CHG_PINSEL_G064[24]	G_088		I	-	T	PD	8	PD	L	G
H23	AB_AD12	IO	3.3V	AB_AD12	I/O	SDI2_DATA0	I/O	CF_D12	I/O	USI5_CS1	O	GPIO_089	GPIO_089	CHG_PINSEL_AB[5:4]	CHG_PINSEL_G064[25]	G_089	AB_8	I	-	T	PD	8	PD	L	G
H22	AB_AD13	IO	3.3V	AB_AD13	I/O	SDI2_DATA1	I/O	CF_D13	I/O	USI5_CS2	O	GPIO_090	GPIO_090		CHG_PINSEL_G064[26]	G_090		I	-	T	PD	8	PD	L	G
H21	AB_AD14	IO	3.3V	AB_AD14	I/O	SDI2_DATA2	I/O	CF_D14	I/O			GPIO_091	GPIO_091	CHG_PINSEL_AB[7:6]	CHG_PINSEL_G064[27]	G_091	AB_9	I	-	T	PD	8	PD	L	G
J22	AB_AD15	IO	3.3V	AB_AD15	I/O	SDI2_DATA3	I/O	CF_D15	I/O			GPIO_092	GPIO_092		CHG_PINSEL_G064[28]	G_092		I	-	T	PD	8	PD	L	G
J21	AB_A17	IO	3.3V	AB_A17	O			CF_A00	O			GPIO_093	GPIO_093	CHG_PINSEL_AB[1:0]	CHG_PINSEL_G064[29]	G_093	AB_10	I	-	M	PD	8	PD	L	G
K21	AB_A18	IO	3.3V	AB_A18	O			CF_A01	O			GPIO_094	GPIO_094		CHG_PINSEL_G064[30]	G_094		I	-	M	PD	8	PD	L	G
L21	AB_A19	IO	3.3V	AB_A19	O			CF_A02	O			GPIO_095	GPIO_095		CHG_PINSEL_G064[31]	G_095		I	-	M	PD	8	PD	L	G
M21	AB_A20	IO	3.3V	AB_A20	O							GPIO_096	GPIO_096	-	CHG_PINSEL_G096[0]	G_096		I	-	M	-	8	Hi-Z	L	H
N21	AB_A21	IO	3.3V	AB_A21	O	SDI2_CKO	O	CF_INTRQ	I			GPIO_097	GPIO_097	CHG_PINSEL_AB[9:8]	CHG_PINSEL_G096[1]	G_097	AB_11	I	-	M	-	8	Hi-Z	L	H
M20	AB_A22	IO	3.3V	AB_A22	O	SDI2_CKI	I					GPIO_098	GPIO_098		CHG_PINSEL_G096[2]	G_098	AB_12	I	-	M	-	8	Hi-Z	L	H
N20	AB_A23	IO	3.3V	AB_A23	O	SDI2_CMD	I/O					GPIO_099	GPIO_099		CHG_PINSEL_G096[3]	G_099		I	-	M	-	8	Hi-Z	L	H
L18	AB_A24	IO	3.3V	AB_A24	O			CF_INPACKB	I			GPIO_100	GPIO_100	CHG_PINSEL_AB[11:10]	CHG_PINSEL_G096[4]	G_100	AB_13	I	-	M	-	8	Hi-Z	L	H
M18	AB_A25	IO	3.3V	AB_A25	O			CF_CDB1	I			GPIO_101	GPIO_101		CHG_PINSEL_G096[5]	G_101	AB_14	I	-	M	-	8	Hi-Z	L	H
N18	AB_A26	IO	3.3V	AB_A26	O			CF_CDB2	I			GPIO_102	GPIO_102		CHG_PINSEL_G096[6]	G_102		I	-	M	-	8	Hi-Z	L	H
L17	AB_A27	IO	3.3V	AB_A27	O			AB_BEN0	O			GPIO_103	GPIO_103	CHG_PINSEL_AB[13:12]	CHG_PINSEL_G096[7]	G_103	AB_15	I	-	M	-	8	Hi-Z	L	H
M17	AB_A28	IO	3.3V	AB_A28	O			AB_BEN1	O			GPIO_104	GPIO_104		CHG_PINSEL_G096[8]	G_104		I	-	M	-	8	Hi-Z	L	H
B6	USI0_CLK	IO	1.8V/3.3V	USI0_CLK	I/O							-	USI0_CLK	-	-	USI0_CK	USI0_0	I	-	M	PD	4	PD	L	L
B10	USI0_DI	I	1.8V/3.3V	USI0_DI	I							-	USI0_DI	-	-	USI0_DI	-	I	-	M	PD	4	PD	L	L
B11	USI0_DO	O	1.8V/3.3V	USI0_DO	O							-	USI0_DO	-	-	USI0_DO	USI0_1	I	-	M	PD	4	PD	L	L
B7	USI0_CS0	IO	1.8V/3.3V	USI0_CS0	I/O							-	USI0_CS0	-	-	USI0_CS0		I	-	M	PD	4	PD	L	L
B8	USI0_CS1	IO	1.8V/3.3V	USI0_CS1	O							GPIO_105	GPIO_105	-	CHG_PINSEL_G096[9]	G_105		I	-	M	PD	4	PD	L	L
B9	USI0_CS2	IO	1.8V/3.3V	USI0_CS2	O							GPIO_106	GPIO_106	-	CHG_PINSEL_G096[10]	G_106		I	-	M	PD	4	PD	L	L
C9	USI1_CLK	IO	1.8V/3.3V	USI1_CLK	I/O							-	USI1_CLK	-	-	USI1_CK	USI1_0	I	-	M	PD	4	PD	L	J
C10	USI1_DI	IO	1.8V/3.3V	USI1_DI	I							GPIO_107	USI1_DI	-	CHG_PINSEL_G096[11]	G_107	USI1_1	I	-	M	PD	4	PD	L	J
D10	USI1_DO	IO	1.8V/3.3V	USI1_DO	O							GPIO_108	USI1_DO	-	CHG_PINSEL_G096[12]	G_108		I	-	M	PD	4	PD	L	J
D11	USI1_CS0	IO	1.8V/3.3V	USI1_CS0	I/O							-	USI1_CS0	-	-	USI1_CS0		I	-	M	PD	4	PD	L	J
AB5	USI2_CLK	IO	1.8V/3.3V	USI2_CLK	I/O	DTV_BCLK	I					GPIO_109	USI2_CLK	CHG_PINSEL_USI[1:0]	CHG_PINSEL_G096[13]	G_109	USI2_0	I	-	M	PD	4	PD	L	L
AA6	USI2_DI	IO	1.8V/3.3V	USI2_DI	I	DTV_PSYNC	I					GPIO_110	USI2_DI		CHG_PINSEL_G096[14]	G_110	USI2_1	I	-	M	PD	4	PD	L	L
AA5	USI2_DO	IO	1.8V/3.3V	USI2_DO	O	DTV_VALID	I					GPIO_111	USI2_DO		CHG_PINSEL_G096[15]	G_111		I	-	M	PD	4	PD	L	L
Y7	USI2_CS0	IO	1.8V/3.3V	USI2_CS0	I/O	DTV_DATA	I					GPIO_112	USI2_CS0		CHG_PINSEL_G096[16]	G_112		I	-	M	PD	4	PD	L	L
AA7	USI2_CS1	IO	1.8V/3.3V	USI2_CS1	O	USI4_CS0	I/O					GPIO_113	GPIO_113	CHG_PINSEL_USI[3:2]	CHG_PINSEL_G096[17]	G_113	USI2_2	I	-	M	PD	4	PD	L	L
Y6	USI2_CS2	IO	1.8V/3.3V	USI2_CS2	O	USI4_CS1	O					GPIO_114	GPIO_114		CHG_PINSEL_G096[18]	G_114	USI2_3	I	-	M	PD	4	PD	L	L
AC5	USI3_CLK	IO	1.8V/3.3V	USI3_CLK	I/O	USI0_CS3	O					GPIO_115	GPIO_115	CHG_PINSEL_USI[5:4]	CHG_PINSEL_G096[19]	G_115	USI3_0	I	-	M	PD	4	PD	L	L
AC4	USI3_DI	IO	1.8V/3.3V	USI3_DI	I	USI0_CS4	O					GPIO_116	GPIO_116		CHG_PINSEL_G096[20]	G_116	USI3_1	I	-	M	PD	4	PD	L	L
AC3	USI3_DO	IO	1.8V/3.3V	USI3_DO	O	USI0_CS5	O					GPIO_117	GPIO_117		CHG_PINSEL_G096[21]	G_117		I	-	M	PD	4	PD	L	L
AB4	USI3_CS0	IO	1.8V/3.3V	USI3_CS0	I/O	USI0_CS6	O					GPIO_118	GPIO_118		CHG_PINSEL_G096[22]	G_118		I	-	M	PD	4	PD	L	L
AB3	GPIO_119	IO	1.8V/3.3V			USI4_CLK	I/O					GPIO_119	GPIO_119	CHG_PINSEL_USI[7:6]	CHG_PINSEL_G096[23]	G_119	GPIO_0	I	-	M	PD	4	PD	L	L
AA4	PWM0	IO	1.8V/3.3V	PWM0	O	USI4_DI	I					GPIO_120	GPIO_120	CHG_PINSEL_USI[9:8]	CHG_PINSEL_G096[24]	G_120	PWM	I	-	M	PD	4	PD	L	L
Y5	PWM1	IO	1.8V/3.3V	PWM1	O	USI4_DO	O					GPIO_121	GPIO_121		CHG_PINSEL_G096[25]	G_121		I	-	M	PD	4	PD	L	L
V20	NTSC_CLK	IO	3.3V	NTSC_CLK	I							GPIO_122	GPIO_122	-	CHG_PINSEL_G096[26]	G_122	NTSC_0	I	-	M	PD	4	PD	L	G
P20	NTSC_DATA0	IO	3.3V	NTSC_DATA0	O							GPIO_123	GPIO_123	-	CHG_PINSEL_G096[27]	G_123		I	-	M	PD	4	PD	L	G
P18	NTSC_DATA1	IO	3.3V	NTSC_DATA1	O							GPIO_124	GPIO_124	-	CHG_PINSEL_G096[28]	G_124		I	-	M	PD	4	PD	L	G
R20	NTSC_DATA2	IO	3.3V	NTSC_DATA2	O							GPIO_125	GPIO_125	-	CHG_PINSEL_G096[29]	G_125		I	-	M	PD	4	PD	L	G
R18	NTSC_DATA3	IO	3.3V	NTSC_DATA3	O							GPIO_126	GPIO_126	-	CHG_PINSEL_G096[30]	G_126		I	-	M	PD	4	PD	L	G
T20	NTSC_DATA4	IO	3.3V	NTSC_DATA4	O							GPIO_127	GPIO_127	-	CHG_PINSEL_G096[31]	G_127	NTSC_1	I	-	M	PD	4	PD	L	G
T18	NTSC_DATA5	IO	3.3V	NTSC_DATA5	O							GPIO_128	GPIO_128	-	CHG_PINSEL_G128[0]	G_128		I	-	M	PD	4	PD	L	G
U20	NTSC_DATA6	IO	3.3V	NTSC_DATA6	O							GPIO_129	GPIO_129	-	CHG_PINSEL_G128[1]	G_129		I	-	M	-	4	Hi-Z	L	H
U18	NTSC_DATA7	IO	3.3V	NTSC_DATA7	O							GPIO_130	GPIO_130	-	CHG_PINSEL_G128[2]	G_130		I	-	M	-	4	Hi-Z	L	H

**Note1 : This section shows bit name of CHG_PULLxx register

Pin No.	PinName	I/O	I/O power	Mode0		Mode1		Mode2		Mode3		GPIO	Default Mode	PinSel	PinSel_GIO	Pull Note1	Drive Note2	Reset					Standby		Buffer Type
				Name	I/O	Name	I/O	Name	I/O	Name	I/O							IO	Output	Input mask	pu/pd	Drive	Output	Input	
W23	CAM_CLKO	IO	3.3V	CAM_CLKO	O							GPIO_131	GPIO_131	-	CHG_PINSEL_G128[3]	G_131	CAM_0	I	-	M	PD	4	PD	L	G
Y23	CAM_CLKI	IO	3.3V	CAM_CLKI	I							GPIO_132	GPIO_132	-	CHG_PINSEL_G128[4]	G_132	CAM_1	I	-	M	-	4	Hi-Z	L	H
W22	CAM_VS	IO	3.3V	CAM_VS	I							GPIO_133	GPIO_133	-	CHG_PINSEL_G128[5]	G_133		I	-	M	-	4	Hi-Z	L	H
V21	CAM_HS	IO	3.3V	CAM_HS	I							GPIO_134	GPIO_134	-	CHG_PINSEL_G128[6]	G_134	CAM_2	I	-	M	PD	4	PD	L	G
T21	CAM_YUV0	IO	3.3V	CAM_YUV0	I							GPIO_135	GPIO_135	-	CHG_PINSEL_G128[7]	G_135	CAM_3	I	-	M	PD	4	PD	L	G
T22	CAM_YUV1	IO	3.3V	CAM_YUV1	I							GPIO_136	GPIO_136	-	CHG_PINSEL_G128[8]	G_136		I	-	M	PD	4	PD	L	G
T23	CAM_YUV2	IO	3.3V	CAM_YUV2	I							GPIO_137	GPIO_137	-	CHG_PINSEL_G128[9]	G_137		I	-	M	PD	4	PD	L	G
U21	CAM_YUV3	IO	3.3V	CAM_YUV3	I							GPIO_138	GPIO_138	-	CHG_PINSEL_G128[10]	G_138		I	-	M	PD	4	PD	L	G
U22	CAM_YUV4	IO	3.3V	CAM_YUV4	I							GPIO_139	GPIO_139	-	CHG_PINSEL_G128[11]	G_139		I	-	M	PD	4	PD	L	G
U23	CAM_YUV5	IO	3.3V	CAM_YUV5	I							GPIO_140	GPIO_140	-	CHG_PINSEL_G128[12]	G_140		I	-	M	PD	4	PD	L	G
V22	CAM_YUV6	IO	3.3V	CAM_YUV6	I							GPIO_141	GPIO_141	-	CHG_PINSEL_G128[13]	G_141		I	-	M	PD	4	PD	L	G
V23	CAM_YUV7	IO	3.3V	CAM_YUV7	I							GPIO_142	GPIO_142	-	CHG_PINSEL_G128[14]	G_142		I	-	M	PD	4	PD	L	G
V10	GPIO_000	IO	1.8V/3.3V									GPIO_000	GPIO_000	-	CJH_PINSEL_G000[0]	G_000	GPIO_1	I	-	M	PD	4	PD	L	L
U10	GPIO_001	IO	1.8V/3.3V									GPIO_001	GPIO_001	-	CJH_PINSEL_G000[1]	G_001		I	-	M	PD	4	PD	L	L
V9	GPIO_002	IO	1.8V/3.3V	JT_SEL	I							GPIO_002	GPIO_002	-	CJH_PINSEL_G000[2]	G_002	GPIO_2	I	-	T	PD	4	PD	L	L
U9	GPIO_003	IO	1.8V/3.3V	ERR_RST_REQB	O							GPIO_003	GPIO_003	-	CJH_PINSEL_G000[3]	G_003	GPIO_3	I	-	M	PD	4	PD	L	L
V8	GPIO_004	IO	1.8V/3.3V	REF_CLKO	O							GPIO_004	GPIO_004	-	CJH_PINSEL_G000[4]	G_004	GPIO_4	I	-	M	PD	4	PD	L	L
U8	GPIO_005	IO	1.8V/3.3V	EXT_CLKI	I							GPIO_005	GPIO_005	-	CJH_PINSEL_G000[5]	G_005	GPIO_5	I	-	M	PD	4	PD	L	L
V18	GPIO_006	IO	3.3V									GPIO_006	GPIO_006	-	CJH_PINSEL_G000[6]	G_006	GPIO_6	I	-	M	PD	4	PD	L	G
V17	GPIO_007	IO	3.3V									GPIO_007	GPIO_007	-	CJH_PINSEL_G000[7]	G_007	GPIO_7	I	-	M	-	4	Hi-Z	L	H
V16	GPIO_008	IO	3.3V									GPIO_008	GPIO_008	-	CJH_PINSEL_G000[8]	G_008		I	-	M	-	4	Hi-Z	L	H
V15	GPIO_009	IO	3.3V									GPIO_009	GPIO_009	-	CJH_PINSEL_G000[9]	G_009	GPIO_8	I	-	M	PD	4	PD	L	G
AA22	GPIO_010	IO	3.3V									GPIO_010	GPIO_010	-	CJH_PINSEL_G000[10]	G_010	GPIO_9	I	-	M	PD	4	PD	L	G
AA21	GPIO_011	IO	3.3V									GPIO_011	GPIO_011	-	CJH_PINSEL_G000[11]	G_011	GPIO_10	I	-	M	-	4	Hi-Z	L	H
AA20	GPIO_012	IO	3.3V									GPIO_012	GPIO_012	-	CJH_PINSEL_G000[12]	G_012		I	-	M	-	4	Hi-Z	L	H
Y21	GPIO_013	IO	3.3V									GPIO_013	GPIO_013	-	CJH_PINSEL_G000[13]	G_013		I	-	M	PD	4	PD	L	G
Y20	GPIO_014	IO	3.3V									GPIO_014	GPIO_014	-	CJH_PINSEL_G000[14]	G_014		I	-	M	PD	4	PD	L	G
Y19	GPIO_015	IO	3.3V									GPIO_015	GPIO_015	-	CJH_PINSEL_G000[15]	G_015		I	-	M	PD	4	PD	L	G
W21	GPIO_016	IO	3.3V									GPIO_016	GPIO_016	-	CJH_PINSEL_G000[16]	G_016		I	-	M	PD	4	PD	L	G
W20	GPIO_017	IO	3.3V									GPIO_017	GPIO_017	-	CJH_PINSEL_G000[17]	G_017		I	-	M	PD	4	PD	L	G
K22	HSI_CAWAKE Note3	IO	1.8V	HSI_CAWAKE Note3	I	USI5_CLK	I/O					GPIO_143	GPIO_143	CHG_PINSEL_HSI[1:0]	CHG_PINSEL_G128[15]	G_143	HSI_0	I	-	M	PD	4	PD	L	C
K23	HSI_CADATA Note3	IO	1.8V	HSI_CADATA Note3	I	USI5_DO	O					GPIO_144	GPIO_144		CHG_PINSEL_G128[16]	G_144	HSI_1	I	-	M	PD	4	PD	L	C
L23	HSI_CAFLAG Note3	IO	1.8V	HSI_CAFLAG Note3	I	USI5_CS0	I/O					GPIO_145	GPIO_145		CHG_PINSEL_G128[17]	G_145		I	-	M	PD	4	PD	L	C
L22	HSI_ACREADY Note3	IO	1.8V	HSI_ACREADY Note3	O	USI5_CS1	O					GPIO_146	GPIO_146		CHG_PINSEL_G128[18]	G_146		I	-	M	PD	4	PD	L	C
N22	HSI_ACWAKE Note3	IO	1.8V	HSI_ACWAKE Note3	O	USI5_CS2	O					GPIO_147	GPIO_147		CHG_PINSEL_G128[19]	G_147		I	-	M	PD	4	PD	L	C
N23	HSI_ACDATA Note3	IO	1.8V	HSI_ACDATA Note3	O	USI5_CS3	O					GPIO_148	GPIO_148		CHG_PINSEL_G128[20]	G_148		I	-	M	PD	4	PD	L	C
M23	HSI_ACFLAG Note3	IO	1.8V	HSI_ACFLAG Note3	O	USI5_CS4	O					GPIO_149	GPIO_149		CHG_PINSEL_G128[21]	G_149		I	-	M	PD	4	PD	L	C
M22	HSI_CAREADY Note3	IO	1.8V	HSI_CAREADY Note3	I	USI5_DI	I					GPIO_150	GPIO_150		CHG_PINSEL_G128[22]	G_150		I	-	M	PD	4	PD	L	C
A11	JT_TCK	I	1.8V	JT_TCK	I							-	JT_TCK	-	-	PD	-	I	-	T	PD	4	PD	L	C
F14	JT_TMS	IO	1.8V	JT_TMS	I/O							-	JT_TMS	-	-	JT	JT	I	-	T	PU	8	PU	L	B
D13	JT_TDO	IO	1.8V	JT_TDO	O							GPIO_151	JT_TDO	-	CHG_PINSEL_G128[23]	G_151		O	L	M	-	8	L	L	E
C11	JT_TRSTB	I	1.8V	JT_TRSTB	I							-	JT_TRSTB	-	-	JT_RST	-	I	-	T	PD	4	PD	L	C
C13	JT_TDI	I	1.8V	JT_TDI	I							-	JT_TDI	-	-	PU	-	I	-	T	PU	4	PU	L	B
F13	JT_TDOEN	IO	1.8V	JT_TDOEN	O							GPIO_152	JT_TDOEN	-	CHG_PINSEL_G128[24]	G_152	JT	O	L	M	-	8	L	L	E
D12	JT_DBG_EN	I	1.8V	JT_DBG_EN	I							-	JT_DBG_EN	-	-	JT_DEN	-	I	-	T	PD	4	PD	L	C
C12	NC	I	1.8V									-	-	-	-	-	-	I		-	PD	-	PD	L	C
AB13	USB_DP1	IO	3.3V	USB_DP1	I/O							-	USB_DP1	-	-	-	-	I	-	-	-	-	-	-	-
AC13	USB_DM1	IO	3.3V	USB_DM1	I/O							-	USB_DM1	-	-	-	-	I	-	-	-	-	-	-	-
AB9	USB_DP2	IO	3.3V	USB_DP2	I/O							-	USB_DP2	-	-	-	-	I	-	-	-	-	-	-	-
AC9	USB_DM2	IO	3.3V	USB_DM2	I/O							-	USB_DM2	-	-	-	-	I	-	-	-	-	-	-	-
AA12	USB_VBUS	I	3.3V	USB_VBUS	I							GPIO_153	USB_VBUS	-	CHG_PINSEL_G128[25]	G_153	USB	I	-	M	-	4	Hi-Z	L	H
P23	NC	I	1.8V									-	-	-	-	-	-	I	-	-	-	-	-	L	-
P22	NC	I	1.8V									-	-	-	-	-	-	I	-	-	-	-	-	L	-
R23	NC	I	1.8V									-	-	-	-	-	-	I	-	-	-	-	-	L	-
R22	NC	I	1.8V									-	-	-	-	-	-	I	-	-	-	-	-	L	-
F12	BOOTSEL0	I	1.8V	BOOTSEL0	I							-	BOOTSEL0	-	-	SMT	-	I	-	T	-	4	Hi-Z	-	A
G11	BOOTSEL1	I	1.8V	BOOTSEL1	I							-	BOOTSEL1	-	-	SMT	-	I	-	T	-	4	Hi-Z	-	A
F11	BOOTSEL2	I	1.8V	BOOTSEL2	I							-	BOOTSEL2	-	-	SMT	-	I	-	T	-	4	Hi-Z	-	A
C6	UTEST	I	1.8V	UTEST	I							-	UTEST	-	-	SMT	-	I	-	T	-	4	Hi-Z	-	A
D6	TE1	I	1.8V	TE1	I							-	TE1	-	-	PD	-	I	-	T	PD	-	-	-	N
D7	TE2	I	1.8V	TE2	I							-	TE2	-	-	PD	-	I	-	T	PD	-	-	-	O
F8	TRSTB	I	1.8V	TRSTB	I							-	TRSTB	-	-	PD	-	I	-	T	PD	4	PD	L	C
C5	NECTESTIO	O	3.3V	NECTESTIO	O							-	NECTESTIO	-	-	-	-	O					-	-	-
A13	PONDET	I	1.8V	PONDET	I							-	PONDET	-	-	-	-	I	-	T	-	-	-	-	M
B12	SRESETB	I	1.8V	SRESETB	I							-	SRESETB	-	-	SMT	-	I	-	T	-	4	Hi-Z	L	D
A5	C32K	I	1.8V	C32K	I							-	C32K	-	-	SMT	-	I	-	T	-	4	Hi-Z	-	A
A12	LOWPWR	O	1.8V	LOWPWR	O							GPIO_154	LOWPWR	-	CHG_PINSEL_G128[26]	G_154	LP	O	L	M	-	4	L	L	E
A9	OSC0_XT1	I	1.8V	OSC0_XT1	I							-	OSC0_XT1	-	-	PD	-	I	-	-	PD	-	-	L	P
A8	OSC0_XT2	I/O	1.8V	OSC0_XT2	I/O							-	OSC0_XT2	-	-	PU	-	I	-	-	PU	-	-	L	P
AC15	OSC1_XT1	I	1.8V	OSC1_XT1	I							-	OSC1_XT1	-	-	PD	-	I	-	-	PD	-	-	L	P
AC16	OSC1_XT2	I/O	1.8V	OSC1_XT2	I/O							-	OSC1_XT2	-	-	PU	-	I	-	-	PU	-	-	L	P
B3	AFS_ARSTB	I	1.8V	AFS_ARSTB	I							-	AFS_ARSTB	-	-	SMT	-	I	-	T	-	4	Hi-Z	-	A
M1	DDR_CK	O	1.8V	DDR_CK	O							-	DDR_CK	-	-	-	-	O	-	-	-	-	Hi-Z	-	R
M2	DDR_CKB	O	1.8V	DDR_CKB	O							-	DDR_CKB	-	-	-	-	O	-	-	-	-	Hi-Z	-	R
L7	DDR_CS0B	O	1.8V	DDR_CS0B	O							-	DDR_CS0B	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
J6	DDR_CS1B	O	1.8V	DDR_CS1B	O							-	DDR_CS1B	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
L1	DDR_CKE0	O	1.8V	DDR_CKE0	O							-	DDR_CKE0	-	-	-	-	O	-	-	-	-	L	-	Q
N1	DDR_CKE1	O	1.8V	DDR_CKE1	O							-	DDR_CKE1	-	-	-	-	O	-	-	-	-	L	-	Q
N6	DDR_CKERSTB	I	1.8V	DDR_CKERSTB	I							-	DDR_CKERSTB	-	-	-	-	I	-	-	-	-	-	-	U
M6	DDR_ODT Note4	O	1.8V	DDR_ODT Note4	O							-	DDR_ODT Note4	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
L6	DDR_RASB	O	1.8V	DDR_RASB	O							-	DDR_RASB	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
K6	DDR_CASB	O	1.8V	DDR_CASB	O							-	DDR_CASB	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
M4	DDR_WEB	O	1.8V	DDR_WEB	O							-	DDR_WEB	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
K2	DDR_BA0	O	1.8V	DDR_BA0	O							-	DDR_BA0	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
L4	DDR_BA1	O	1.8V	DDR_BA1	O							-	DDR_BA1	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
K1	DDR_BA2	O	1.8V	DDR_BA2	O							-	DDR_BA2	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
J1	DDR_A0	O	1.8V	DDR_A0	O							-	DDR_A0	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
L3	DDR_A1	O	1.8V	DDR_A1	O							-	DDR_A1	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
J2	DDR_A2	O	1.8V	DDR_A2	O							-	DDR_A2	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
K3	DDR_A3	O	1.8V	DDR_A3	O							-	DDR_A3	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
R3	DDR_A4	O	1.8V	DDR_A4	O							-	DDR_A4	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
R2	DDR_A5	O	1.8V	DDR_A5	O							-	DDR_A5	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
P4	DDR_A6	O	1.8V	DDR_A6	O							-	DDR_A6	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
P2	DDR_A7	O	1.8V	DDR_A7	O							-	DDR_A7	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
P3	DDR_A8	O	1.8V	DDR_A8	O							-	DDR_A8	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
R1	DDR_A9	O	1.8V	DDR_A9	O							-	DDR_A9	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
K4	DDR_A10	O	1.8V	DDR_A10	O							-	DDR_A10	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
N3	DDR_A11	O	1.8V	DDR_A11	O							-	DDR_A11	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
P1	DDR_A12	O	1.8V	DDR_A12	O							-	DDR_A12	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
N4	DDR_A13	O	1.8V	DDR_A13	O							-	DDR_A13	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
L2	DDR_A14	O	1.8V	DDR_A14	O							-	DDR_A14	-	-	-	-	O	-	-	-	-	Hi-Z	-	Q
D1	DDR_DM0	O	1.8V	DDR_DM0	O							-	DDR_DM0	-	-	-	-	O	-	-	-	-	Hi-Z	L	S
G3	DDR_DM1	O	1.8V	DDR_DM1	O							-	DDR_DM1	-	-	-	-	O	-	-	-	-	Hi-Z	L	S
U4	DDR_DM2	O	1.8V	DDR_DM2	O							-	DDR_DM2	-	-	-	-	O	-	-	-	-	Hi-Z	L	S
Y1	DDR_DM3	O	1.8V	DDR_DM3	O							-	DDR_DM3	-	-	-	-	O	-	-	-	-	Hi-Z	L	S
E1	DDR_DQS0	I/O	1.8V	DDR_DQS0	I/O							-	DDR_DQS0	-	-	-	-	I/O	-	-	-	-	Hi-Z	L	T
E2	DDR_DQS0B	I/O	1.8V	DDR_DQS0B	I/O							-	DDR_DQS0B	-	-	-	-	I/O	-	-	-	-	Hi-Z	L	T
F1	DDR_DQS1	I/O	1.8V	DDR_DQS1	I/O							-	DDR_DQS1	-	-	-	-	I/O	-	-	-	-	Hi-Z	L	T
F2	DDR_DQS1B	I/O	1.8V	DDR_DQS1B	I/O							-	DDR_DQS1B	-	-	-	-	I/O	-	-	-	-	Hi-Z	L	T
V1	DDR_DQS2	I/O	1.8V	DDR_DQS2	I/O							-	DDR_DQS2	-	-	-	-	I/O	-	-	-	-	Hi-Z	L	T
V2	DDR_DQS2B	I/O	1.8V	DDR_DQS2B	I/O							-	DDR_DQS2B	-	-	-	-	I/O	-	-	-	-	Hi-Z	L	T
W1	DDR_DQS3	I/O	1.8V	DDR_DQS3	I/O							-	DDR_DQS3	-	-	-	-	I/O	-	-	-	-	Hi-Z	L	T
W2	DDR_DQS3B	I/O	1.8V	DDR_DQS3B	I/O							-	DDR_DQS3B	-	-	-	-	I/O	-	-	-	-	Hi-Z	L	T
C2	DDR_DQ0	I/O	1.8V	DDR_DQ0	I/O							-	DDR_DQ0	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
D4	DDR_DQ1	I/O	1.8V	DDR_DQ1	I/O							-	DDR_DQ1	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
C3	DDR_DQ2	I/O	1.8V	DDR_DQ2	I/O							-	DDR_DQ2	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
E3	DDR_DQ3	I/O	1.8V	DDR_DQ3	I/O							-	DDR_DQ3	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
D2	DDR_DQ4	I/O	1.8V	DDR_DQ4	I/O							-	DDR_DQ4	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
E4	DDR_DQ5	I/O	1.8V	DDR_DQ5	I/O							-	DDR_DQ5	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
D3	DDR_DQ6	I/O	1.8V	DDR_DQ6	I/O							-	DDR_DQ6	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
C1	DDR_DQ7	I/O	1.8V	DDR_DQ7	I/O							-	DDR_DQ7	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
G2	DDR_DQ8	I/O	1.8V	DDR_DQ8	I/O							-	DDR_DQ8	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
G4	DDR_DQ9	I/O	1.8V	DDR_DQ9	I/O							-	DDR_DQ9	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
H4	DDR_DQ10	I/O	1.8V	DDR_DQ10	I/O							-	DDR_DQ10	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
G1	DDR_DQ11	I/O	1.8V	DDR_DQ11	I/O							-	DDR_DQ11	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
H1	DDR_DQ12	I/O	1.8V	DDR_DQ12	I/O							-	DDR_DQ12	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
H3	DDR_DQ13	I/O	1.8V	DDR_DQ13	I/O							-	DDR_DQ13	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
J4	DDR_DQ14	I/O	1.8V	DDR_DQ14	I/O							-	DDR_DQ14	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
H2	DDR_DQ15	I/O	1.8V	DDR_DQ15	I/O							-	DDR_DQ15	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
T1	DDR_DQ16	I/O	1.8V	DDR_DQ16	I/O							-	DDR_DQ16	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
T2	DDR_DQ17	I/O	1.8V	DDR_DQ17	I/O							-	DDR_DQ17	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
U2	DDR_DQ18	I/O	1.8V	DDR_DQ18	I/O							-	DDR_DQ18	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
T4	DDR_DQ19	I/O	1.8V	DDR_DQ19	I/O							-	DDR_DQ19	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
R4	DDR_DQ20	I/O	1.8V	DDR_DQ20	I/O							-	DDR_DQ20	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
U1	DDR_DQ21	I/O	1.8V	DDR_DQ21	I/O							-	DDR_DQ21	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
T3	DDR_DQ22	I/O	1.8V	DDR_DQ22	I/O							-	DDR_DQ22	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
U3	DDR_DQ23	I/O	1.8V	DDR_DQ23	I/O							-	DDR_DQ23	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
AA1	DDR_DQ24	I/O	1.8V	DDR_DQ24	I/O							-	DDR_DQ24	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
Y3	DDR_DQ25	I/O	1.8V	DDR_DQ25	I/O							-	DDR_DQ25	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
AA3	DDR_DQ26	I/O	1.8V	DDR_DQ26	I/O							-	DDR_DQ26	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
Y2	DDR_DQ27	I/O	1.8V	DDR_DQ27	I/O							-	DDR_DQ27	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
AA2	DDR_DQ28	I/O	1.8V	DDR_DQ28	I/O							-	DDR_DQ28	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
Y4	DDR_DQ29	I/O	1.8V	DDR_DQ29	I/O							-	DDR_DQ29	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
W4	DDR_DQ30	I/O	1.8V	DDR_DQ30	I/O							-	DDR_DQ30	-	-	-	-	I	-	-	-	-	Hi-Z	L	S
W3	DDR_DQ31	I/O	1.8V	DDR_DQ31	I/O							-	DDR_DQ31	-	-	-	-	I	-	-	-	-	Hi-Z	L	S

Note1 : This section shows bit name of CHG_PULLxx register
Note2 : This section shows bit name of CHG_DRIVExx register
Note3 : The HSI function is not available
Note4 : The on die termination function for DDR-ODT is not available

Pin I/O circuits

This section shows the types of I/O circuits used in EM/EV. The correspondence between circuits and pins is shown in the table below.

Buffer type	VDD	I/O	Low noise	Output condition (When stand by) Note1	Normal/Schmitt switch	PU/PD switch (PU50K/PD50K/none)	IOLH switch (4/6/8/12mA)	Description
A	VDD18	IO	√	Z	√	√	√	It's through at the time of Standby (without input masks).
B	VDD18	IO		PU	√	√	√	
C	VDD18	IO		PD	√	√	√	
D	VDD18	IO		Z	√	√	√	
E	VDD18	IO		L	√	√	√	
F	VDD33	IO		PU	√	√	√	
G	VDD33	IO		PD	√	√	√	
H	VDD33	IO		Z	√	√	√	
I	VDD33M	IO	√	PU	√	√	√	
J	VDD33M	IO	√	PD	√	√	√	
K	VDD33M	IO	√	Z	√	√	√	
L	VDD33M	IO		PD	√	√	√	
M	VDD18	I		–				Without for Standy signals (PONDET), Schmitt input and the PU/PD function
N	VDD18	I		PD				Anytime pull-down
O	VDD18	I		PD				Anytime pull-down
P	VDD18	I		–				Oscillator

Buffer type	VDD	I/O	CMOS/AMP switch	Termination	Impedance	Description
Q	DDR_VDDIO	IO		√	√	Address, control signals
R	DDR_VDDIO	IO		√	√	Clock
S	DDR_VDDIO	IO	√	√	√	DQ, DM
T	DDR_VDDIO	IO	√	√	√	DQS
U	DDR_VDDIO	I				Clock reset (standby)

APPENDIX E. External Bus Interface

E.1 Registers

Tables E-1, E-2 and E-3 show the external bus interface (AB0) registers.
The base address of each register is 2FFF_0000H.
The external bus interface registers can only be accessed in 32-bit (word) units.
Table E-1 shows the registers for system control.

E.1.1 System control registers

Table E-1. System Control Registers

Address	Register Name	Symbol	R/W	After Reset
0000H	Flash command start register	AB0_FLASHCOMSET	W	0000_0000H
0004H	Flash read data latch register	AB0_FLASHCOMLATCH	R	0000_0000H
0010H	Flash command (ADD0) setting register	AB0_FLASHCOMADD0	R/W	0000_0000H
0014H	Flash command (DATA0) setting register	AB0_FLASHCOMDATA0	R/W	0000_0000H
0018H	Flash command (ADD1) setting register	AB0_FLASHCOMADD1	R/W	0000_0000H
001CH	Flash command (DATA1) setting register	AB0_FLASHCOMDATA1	R/W	0000_0000H
0080H	Flash clock control register	AB0_FLASHCLKCTRL	R/W	0000_0001H
0090H	WAIT pin status register	AB0_WAIT_STATUS	R	–
0100H	CS0 base address register	AB0_CS0BASEADD	R/W	0000_0000H
0104H	CS0 bit compare register	AB0_CS0BITCOMP	R/W	F000_0000H
0110H	CS1 base address register	AB0_CS1BASEADD	R/W	3FFF_0000H
0114H	CS1 bit compare register	AB0_CS1BITCOMP	R/W	FFFF_0000H
0120H	CS2 base address register	AB0_CS2BASEADD	R/W	3FFF_0000H
0124H	CS2 bit compare register	AB0_CS2BITCOMP	R/W	FFFF_0000H
0130H	CS3 base address register	AB0_CS3BASEADD	R/W	3FFF_0000H
0134H	CS3 bit compare register	AB0_CS3BITCOMP	R/W	FFFF_0000H

Cautions 1. Writing to an internal AB0 register area outside the defined range is ignored. If this area is read, 0 is returned.

E.1.2 Parameter registers

Caution The parameter registers in Table E-2 are of dual structure and cannot be written directly. By starting each slave by using the flash command start register, the value of the parameter register is reflected in the respective internal parameter hold register.

Table E-2. Parameter Registers

Address	Register Name	Symbol	R/W	After Reset
0200H	CS0 wait control register	AB0_CS0WAITCTRL	R/W	000F_1F0FH
0204H	CS0 write wait control register	AB0_CS0WAITCTRL_W	R/W	000F_1F0FH
0208H	CS0 read mode register	AB0_CS0READCTRL	R/W	0000_0000H
020CH	CS0 wait mask register	AB0_CS0WAIT_MASK	R/W	0000_0000H
0210H	CS0 control register	AB0_CS0CONTROL	R/W	0001_0100H
0214H	CS0 read configuration register	AB0_CS0FLASHRCR	R/W	0000_D503H
0218H	Reserved	–	–	–
0220H	CS1 wait control register	AB0_CS1WAITCTRL	R/W	000F_1F0FH
0224H	CS1 write wait control register	AB0_CS1WAITCTRL_W	R/W	000F_1F0FH
0228H	CS1 read mode register	AB0_CS1READCTRL	R/W	0000_0000H
022CH	CS1 wait mask register	AB0_CS1WAIT_MASK	R/W	0000_0000H
0230H	CS1 control register	AB0_CS1CONTROL	R/W	0001_0100H
0234H	CS1 read configuration register	AB0_CS1FLASHRCR	R/W	0000_D503H
0238H	Reserved	–	–	–
0240H	CS2 wait control register	AB0_CS2WAITCTRL	R/W	000F_1F0FH
0244H	CS2 write wait control register	AB0_CS2WAITCTRL_W	R/W	000F_1F0FH
0248H	CS2 read mode register	AB0_CS2READCTRL	R/W	0000_0000H
024CH	CS2 wait mask register	AB0_CS2WAIT_MASK	R/W	0000_0000H
0250H	CS2 control register	AB0_CS2CONTROL	R/W	0001_0100H
0254H	CS2 read configuration register	AB0_CS2FLASHRCR	R/W	0000_D503H
0258H	Reserved	–	–	–
0260H	CS3 wait control register	AB0_CS3WAITCTRL	R/W	000F_1F0FH
0264H	CS3 write wait control register	AB0_CS3WAITCTRL_W	R/W	000F_1F0FH
0268H	CS3 read mode register	AB0_CS3READCTRL	R/W	0000_0000H
026CH	CS3 wait mask register	AB0_CS3WAIT_MASK	R/W	0000_0000H
0270H	CS3 control register	AB0_CS3CONTROL	R/W	0001_0100H
0274H	CS3 read configuration register	AB0_CS3FLASHRCR	R/W	0000_D503H
0278H	Reserved	–	–	–

Caution Writing to an internal AB0 register area outside the defined range is ignored. If this area is read, 0 is returned.

E.1.3 Parameter retention registers

Caution The parameter hold registers in Table E-3 are of dual structure and cannot be written directly. By starting each slave by using the flash command start register, the value of the parameter register is reflected in the respective internal parameter hold register.

Table E-3. Parameter Retention Registers

Address	Register Name	Symbol	R/W	After Reset
0300H	CS0 wait control register	AB0_CS0WAITCTRL2	R	000F_1F0FH
0304H	CS0 write wait control register	AB0_CS0WAITCTRL_W2	R	000F_1F0FH
0308H	CS0 read mode register	AB0_CS0READCTRL2	R	0000_0000H
030CH	CS0 wait mask register	AB0_CS0WAIT_MASK2	R	0000_0000H
0310H	CS0 control register	AB0_CS0CONTROL2	R	0001_0100H
0314H	CS0 read configuration register	AB0_CS0FLASHRCR2	R	0000_D503H
0318H	Reserved	–	–	–
0320H	CS1 wait control register	AB0_CS1WAITCTRL2	R	000F_1F0FH
0324H	CS1 write wait control register	AB0_CS1WAITCTRL_W2	R	000F_1F0FH
0328H	CS1 read mode register	AB0_CS1READCTRL2	R	0000_0000H
032CH	CS1 wait mask register	AB0_CS1WAIT_MASK2	R	0000_0000H
0330H	CS1 control register	AB0_CS1CONTROL2	R	0001_0100H
0334H	CS1 read configuration register	AB0_CS1FLASHRCR2	R	0000_D503H
0338H	Reserved	–	–	–
0340H	CS2 wait control register	AB0_CS2WAITCTRL2	R	000F_1F0FH
0344H	CS2 write wait control register	AB0_CS2WAITCTRL_W2	R	000F_1F0FH
0348H	CS2 read mode register	AB0_CS2READCTRL2	R	0000_0000H
034CH	CS2 wait mask register	AB0_CS2WAIT_MASK2	R	0000_0000H
0350H	CS2 control register	AB0_CS2CONTROL2	R	0001_0100H
0354H	CS2 read configuration register	AB0_CS2FLASHRCR2	R	0000_D503H
0358H	Reserved	–	–	–
0360H	CS3 wait control register	AB0_CS3WAITCTRL2	R	000F_1F0FH
0364H	CS3 write wait control register	AB0_CS3WAITCTRL_W2	R	000F_1F0FH
0368H	CS3 read mode register	AB0_CS3READCTRL2	R	0000_0000H
036CH	CS3 wait mask register	AB0_CS3WAIT_MASK2	R	0000_0000H
0370H	CS3 control register	AB0_CS3CONTROL2	R	0001_0100H
0374H	CS3 read configuration register	AB0_CS3FLASHRCR2	R	0000_D503H
0378H	Reserved	–	–	–

Caution Writing to an internal AB0 register area outside the defined range is ignored. If this area is read, 0 is returned.

E.2 Register Details

E.2.1 Flash command start register

When any of the CS0 to CS2 bits of this register (AB0_FLASHCOMSET: 2FFF_0000H) is set, the value of the parameter register specified for the CS is copied to the respective parameter hold register of AB0.
After that, a command is issued to an external device (CS) selected if the SET_MODE bit is set to 1.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	SET_MODE	Reserved		CS3	CS2	CS1	CS0

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:7	–	Reserved. If these bits are read, 0 is returned for each bit.
SET_MODE	W	6	0	Specify whether to issue a command to flash memory 0: Do not issue 1: Issue
Reserved	R	5:4	–	Reserved. If these bits are read, 0 is returned for each bit.
CS3	W	3	0	Starts CS3 (parameter copy). 0: – 1: Start
CS2	W	2	0	Starts CS2 (parameter copy). 0: – 1: Start
CS1	W	1	0	Starts CS1 (parameter copy). 0: – 1: Start
CS0	W	0	0	Starts CS0 (parameter copy). 0: – 1: Start

Cautions 1. A command can be issued to only one CS. If two or more CSs are selected, the CS with the smallest number has the highest priority.
If no CS is specified, the flash command is issued (by setting SET_MODE bit) to CS0.
Example 1) CS0 bit = 1, CS1 bit = 1, SET_MODE bit = 1
→ The parameter register is copied to the parameter hold register for CS0 and CS1.
The Flash command is issued to CS0.
Example 2) CS0 bit = 1, CS1 bit = 1, SET_MODE bit = 0
→ The parameter register is copied to the parameter hold register for CS0 and CS1.
The Flash command is not issued to CS0 and CS1.

E.2.2 Flash read data latch register

This register (AB0_FLASHCOMLATCH: 2FFF_0004H) stores the data read by using a command of the Intel StrataFlash wireless memory. Because the read command is issued only in the second bus cycle, a command that reads data in the second bus cycle is always latched.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
READ_COM							

7	6	5	4	3	2	1	0
READ_COM							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
READ_COM	R	15:0	0000H	Latch the data read by flash memory command.

E.2.3 Flash command (ADD0) setting register

This register (AB0_FLASHCOMADD0: 2FFF_0010H) sets up the command sent to the Intel StrataFlash wireless memory. This register specifies the write address of the first command cycle.

31	30	29	28	27	26	25	24
Reserved			ADD0				

23	22	21	20	19	18	17	16
ADD0							

15	14	13	12	11	10	9	8
ADD0							

7	6	5	4	3	2	1	0
ADD0							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:29	–	Reserved. If these bits are read, 0 is returned for each bit.
ADD0	R/W	28:0	0000_0000H	Specify the address of the first bus cycle.

E.2.4 Flash command (DATA0) setting register

This register (AB0_FLASHCOMDATA0: 2FFF_0014H) sets up the command sent to the Intel StrataFlash wireless memory. This register specifies the data of the first command cycle.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
DATA0							

7	6	5	4	3	2	1	0
DATA0							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
DATA0	R/W	15:0	0000H	Specify the data of the first bus cycle.

E.2.5 Flash command (ADD1) setting register

This register (AB0_FLASHCOMADD1: 2FFF_0018H) sets up the command sent to the Intel StrataFlash wireless memory. This register specifies an address in the second command cycle and reading or writing.
This register is used if the command sent to the flash memory is a two-cycle command and, when it is used, set the ValidBit bit to 1.
If a read operation is performed at this command address (second command cycle), the read data is latched to the AB0_FLASHCOMLATCH register.

31	30	29	28	27	26	25	24
ValidBit	RW	Reserved	ADD1				

23	22	21	20	19	18	17	16
ADD1							

15	14	13	12	11	10	9	8
ADD1							

7	6	5	4	3	2	1	0
ADD1							

Name	R/W	Bit No.	After Reset	Description
ValidBit	R/W	31	0	Set this bit to 1 if the second bus cycle is necessary.
RW	R/W	30	0	Specify read or write in the second bus cycle. 0: Read, 1: Write
Reserved	R	29	–	Reserved. If this bit is read, 0 is returned.
ADD1	R/W	28:0	0000_0000H	Specify the address of the second bus cycle.

E.2.6 Flash command (DATA1) setting register

This register (AB0_FLASHCOMDATA1: 2FFF_001CH) sets up the command sent to the Intel StrataFlash wireless memory. This register specifies the data in the second command cycle.
This register is used if the command sent to the flash memory is a two-cycle command and, when it is used, set the ValidBit bit of the AB0_FLASHCOMADD1 register to 1.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
DATA1							

7	6	5	4	3	2	1	0
DATA1							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
DATA1	R/W	15:0	0000H	Specify the data of the second bus cycle.

E.2.7 Flash clock control register

This register (AB0_FLASHCLKCTRL: 2FFF_0080H) specifies a frequency ratio of the AB0 clock to the flash memory clock (FLASHCLK).

- 1: AB0 clock → FLASHCLK = 2:1 (133 MHz: 66 MHz is assumed.)
- 0: AB0 clock → FLASHCLK = 1:1

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							CLK_MODE

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
CLK_MODE	R/W	0	1	Specify external memory clock mode (frequency ratio). 0: AB0 → FLASHCLK = 1:1 1: AB0 → FLASHCLK = 2:1

E.2.8 Wait pin status register

This register (AB0_WAIT_STATUS: 2FFF_0090H) indicates the AB0_WAIT pin status.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							WAIT

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
WAIT	R	0	1	Indicates the AB0_WAIT pin level. 0: Low 1: High

E.2.9 CSn base address register

AB0_CS0BASEADD: 2FFF_0100H
AB0_CS1BASEADD: 2FFF_0110H
AB0_CS2BASEADD: 2FFF_0120H
AB0_CS3BASEADD: 2FFF_0130H

31	30	29	28	27	26	25	24
Reserved		ADD					

23	22	21	20	19	18	17	16
ADD							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit No.	After Reset	Description
Reserved	R/W	31:30	–	Reserved. If these bits are read, 0 is returned for each bit.
ADD	R/W	29:16	See table below	Specify the slave base address.
Reserved	R/W	15:0	–	Reserved. If these bits are read, 0 is returned for each bit.

The initial values are as follows:

Table E-4. Initial Values (BASEADD)

CS No.	Initial Value
0	0000_0000H
1 to 3	3FFF_0000H

This register specifies the base address for each slave. However, bits 31, 30, and 15 to 0 are fixed to 0.
The specifiable range is 0000_0000H to 2FFF_0000H, except for 2FFF_0000H to 2FFF_FFFFH, because these areas are reserved for the AB0 local registers.
The base address cannot be specified extending from one bank to another.
This register must be set up together with the AB0_CS*n*BITCOMP register.

Caution If the same address range or base address is specified for separate CSs, the CS with the lower index is activated.

E.2.10 CSn bit compare register

AB0_CS0BITCOMP: 2FFF_0104H
AB0_CS1BITCOMP: 2FFF_0114H
AB0_CS2BITCOMP: 2FFF_0124H
AB0_CS3BITCOMP: 2FFF_0134H

31	30	29	28	27	26	25	24
BITCOMP							

23	22	21	20	19	18	17	16
BITCOMP							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit No.	After Reset	Description
BITCOMP	R/W	31:16	See table below	Specify the valid bit range (bits 31 and 30 are ignored because of the relationship with the base address register).
Reserved	R/W	15:0	–	Reserved. If these bits are read, 0 is returned for each bit.

The initial values are as follows:

Table E-5. Initial Values (BITCOMP)

CS No.	Initial Value
0	F000_0000H
1 to 3	FFFF_0000H

This register specifies the address range for each slave and enables the AB_CSB pin of a slave, using the following logic:

AB0_CSnBASEADD & AB0_CSnBITCOMP = (*input address*) & AB0_CSnBITCOMP

Setting example 1

When specifying 1010_0000H to 101F_FFFFH as slave 1:

AB0_CS1BASEADD = 1010_0000H, AB0_CS1BITCOMP = FFF0_0000H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CS1BITCOMP	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
CS1BASEADD	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
ADDR	ADDR[31:20] and BASEAD[31:20] are compared. If they match, this field is selected.															

Setting example 2

When specifying 0000_0000H to 0FFF_FFFFH as slave 0:

AB0_CS0BASEADD = 0000_0000H, AB0_CS0BITCOMP = F000_0000H

			29	28	27	26	25	24	23	22	21	20	19	18	17	16
CS0BITCOMP	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
CS0BASEADD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADDR	ADDR[31:28]															

E.2.11 CSn wait control register

AB0_CS0WAITCTRL: 2FFF_0200H
AB0_CS1WAITCTRL: 2FFF_0220H
AB0_CS2WAITCTRL: 2FFF_0240H
AB0_CS3WAITCTRL: 2FFF_0260H

31	30	29	28	27	26	25	24
Reserved					CSInt		

23	22	21	20	19	18	17	16
Reserved				T2			

15	14	13	12	11	10	9	8
Reserved			T1				

7	6	5	4	3	2	1	0
Reserved				T0			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:27	–	Reserved. If these bits are read, 0 is returned for each bit.
CSInt	R/W	26:24	0H	CS = H period control. CSInt + 1 cycle is set.
Reserved	R	23:20	–	Reserved. If these bits are read, 0 is returned for each bit.
T2	R/W	19:16	FH	Control T2 waits.
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
T1	R/W	12:8	1FH	Controls T1 waits. Specify 1 or larger value.
Reserved	R	7:4	–	Reserved. If these bits are read, 0 is returned for each bit.
T0	R/W	3:0	FH	Control T0 waits.

This register specifies read wait timing parameters T0, T1, T2, and CSInt for the asynchronous bus control signal.
CSInt is also used for writing.
Specify the value based on the number of AB_CLK cycles.
Therefore, the specified value is doubled in AB0 in the clock ratio 2:1 mode.
For example, a wait cycle shown in the following examples is inserted:

- CLK = 100 MHz and FLASHCLK = 50 MHz (in 2:1 clock ratio mode): 20 ns, where T1 = 1
- CLK = 100 MHz and FLASHCLK = 100 MHz (in 1:1 clock ratio mode): 10 ns, where T1 = 1

Setting range:
T0: Can be specified in a range from 0 to 15. The initial value is 15 clock cycles.
T1: Can be specified in a range from 1 to 31. The initial value is 31 clock cycles.
T2: Can be specified in a range from 0 to 15. The initial value is 15 clock cycles.
CSInt: Can be specified in a range from 0 to 7. The initial value is 0. A CSInt cycle is the specified value + 1.

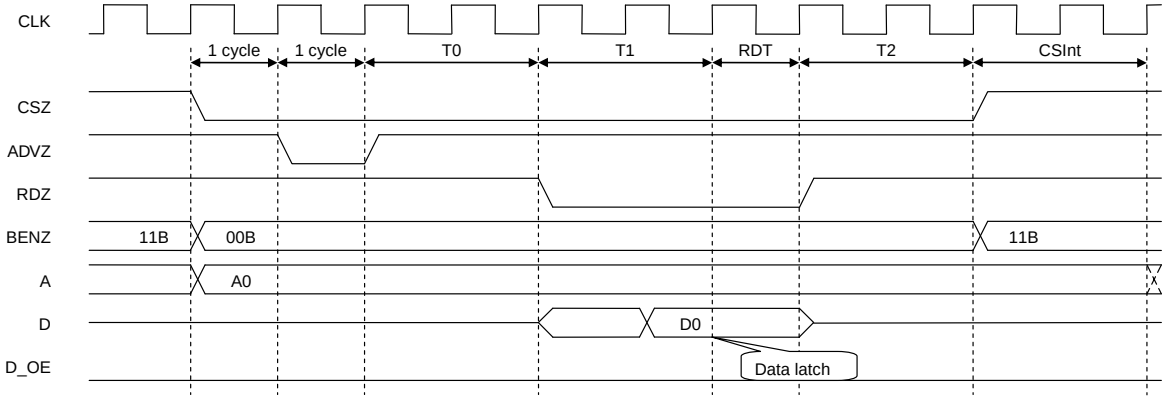
Cautions 1. In single/page read mode
In the clock ratio 2:1 mode, the sum of the values of RDT, T2, and CSInt must be 1 or more.
In the clock ratio 1:1 mode, the sum of the values of RDT, T2, and CSInt must be 2 or more.

2. The minimum value of T1 is 1. Even if 0 is specified, the operation is performed in the same manner as when 1 is specified.

3. If the value of T0 is 0 when the AD-Mux bus is used, the operation is performed in the same manner as when 1 is specified.

Figure E-1 shows the single read timing with Non Mux.

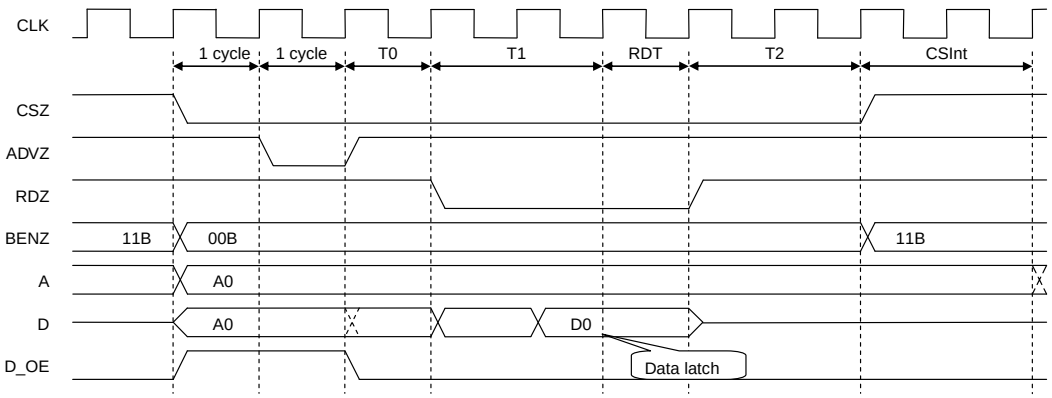
Figure E-1. Single Read Timing (Non Mux)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Figure E-2 shows the single read timing with AD-Mux.

Figure E-2. Single Read Timing (AD-Mux)

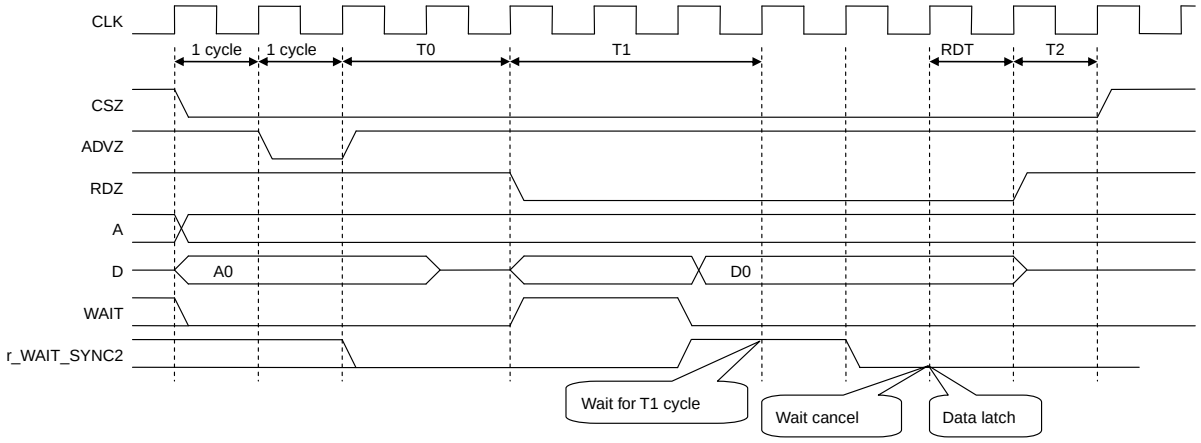


It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Caution D_OE (output enable) is deasserted at the rising edge of ADVZ, so retain the address data in the IO buffer.

Figure E-3 shows the wait timing chart in the single read mode. The WAIT signal is delayed by two clock cycles because of synchronization. The WAIT signal can be masked by using the CSn wait mask register.

Figure E-3. Wait Timing (Single Read)



Caution Specify the T1 value so that it lasts three clock cycles or longer after the delay of the WAIT signal.

E.2.12 CSn write wait control register

AB0_CS0WAITCTRL_W: 2FFF_0204H
AB0_CS1WAITCTRL_W: 2FFF_0224H
AB0_CS2WAITCTRL_W: 2FFF_0244H
AB0_CS3WAITCTRL_W: 2FFF_0264H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved				T2_W			

15	14	13	12	11	10	9	8
Reserved			T1_W				

7	6	5	4	3	2	1	0
Reserved				T0_W			

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:20	–	Reserved. If these bits are read, 0 is returned for each bit.
T2_W	R/W	19:16	FH	Control T2_W WAIT waits.
Reserved	R	15:13	–	Reserved. If these bits are read, 0 is returned for each bit.
T1_W	R/W	12:8	1FH	Controls T1_W WAIT waits. Set 1 or a larger value.
Reserved	R	7:4	–	Reserved. If these bits are read, 0 is returned for each bit.
T0_W	R/W	3:0	FH	Control T0_W waits.

This register specifies write wait timing parameters (T0_W, T1_W, and T2_W) for asynchronous bus control signal. The setting for CSInt during read is used (see **(12) CSn wait control register**).

Caution T1_W is the specified cycle + one clock cycle. CSInt during write is (specified value + 1) cycles + one clock.

Specify the value based on the number of the flash memory clock (FLASHCLK) cycles.
Therefore, the value is doubled in AB0 in the clock ratio 2:1 mode.
For example, a wait cycle shown in the following examples is inserted:

- CLK = 100 MHz and FLASHCLK = 50 MHz (2:1 clock ratio mode): 20 + 10 = 30 ns, where T1_W = 1
- CLK = 100 MHz and FLASHCLK = 100 MHz (1:1 clock ratio mode): 10 + 10 = 20 ns, where T1_W = 1

Setting range:

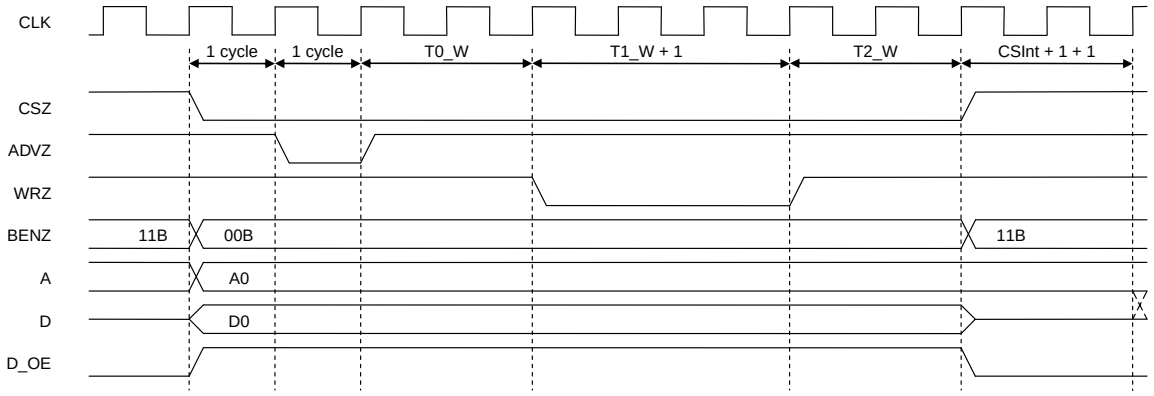
T0_W: Can be specified in a range from 0 to 15. The initial value is 15 clock cycles.
T1_W: Can be specified in a range from 1 to 31. The initial value is 31 clock cycles.
T2_W: Can be specified in a range from 0 to 15. The initial value is 15 clock cycles.
CSInt: References the value of the CSInt bit of AB0_CSnWAITCTRL for wait value during read.

Cautions

1. **In single write mode, T2_W must be set to a value of 1 or more.**
2. **The minimum value of T1 is 1. Even if 0 is specified, the operation is performed in the same manner as when 1 is specified.**
3. **Copy for a parameter holding register after register setting to make register setting reflected.**
4. **If T0_W = 0 when the AD-Mux bus is used, the address is extended by one clock cycle because it is held. Consequently, output of write data is delayed by one clock cycle. At this time, set T1_W to a value of 2 or more.**

Figure E-4 shows the single write timing with Non Mux.

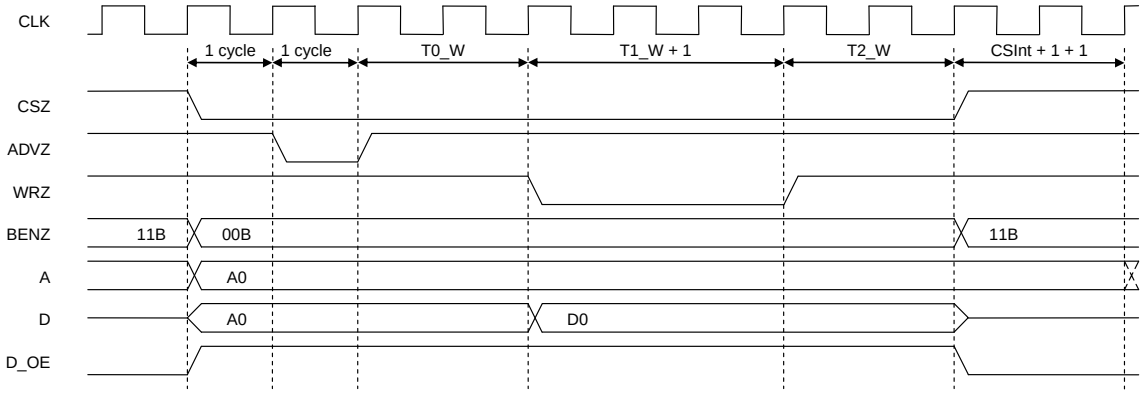
Figure E-4. Single Write Timing (Non Mux) (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Figure E-5 shows the single write timing with AD-Mux when T0 > 0.

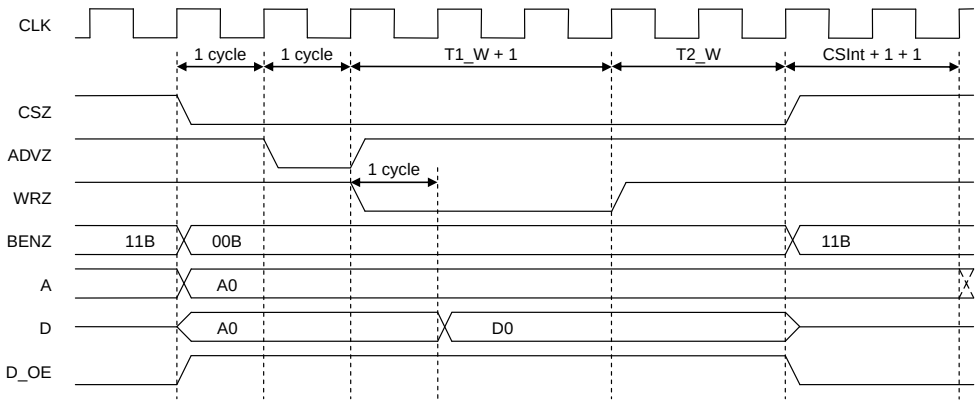
Figure E-5. Single Write Timing (AD-Mux) (T0 > 0) (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Figure E-6 shows the single write timing with AD-Mux when T0_W = 0.

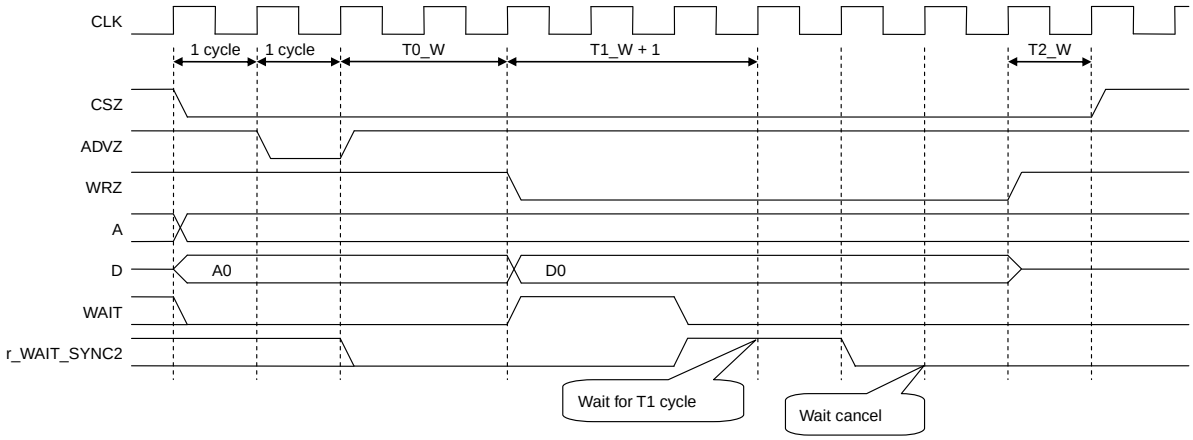
Figure E-6. Single Write Timing (AD-Mux) (T0_W = 0) (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Figure E-7 shows the wait timing chart in the single write mode. The WAIT signal is delayed by two clock cycles because of synchronization. The WAIT signal can be masked by using the CSn wait mask register.

Figure E-7. Wait Timing (Single Write) (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Caution Specify the T1_W value so that it lasts three clock cycles or longer after the delay of the WAIT signal.

E.2.13 CSn read mode register

AB0_CS0READCTRL: 2FFF_0208H
AB0_CS1READCTRL: 2FFF_0228H
AB0_CS2READCTRL: 2FFF_0248H
AB0_CS3READCTRL: 2FFF_0268H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		RDT		Reserved		READMODE	

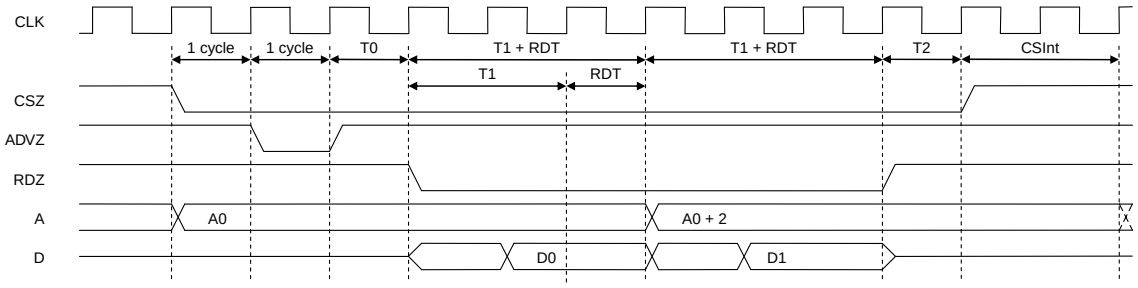
Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:6	–	Reserved. If these bits are read, 0 is returned for each bit.
RDT	R/W	5:4	0H	Specify the timing for changing read data latch. 00: Deasserts RDZ signal 1 clock cycle after latch timing. 01: Deasserts RDZ signal 2 clock cycles after latch timing. 10: Deasserts RDZ signal 3 clock cycles after latch timing. 11: Deasserts RDZ signal 4 clock cycles after latch timing.
Reserved	R	3:2	–	Reserved. If these bits are read, 0 is returned for each bit.
READMODE	R/W	1:0	0H	Specify the read mode. 00: Single read mode 01: Single read mode 10: Page read mode 11: Reserved

Specify the RDT value based on the number of AB_CLK cycles.
Therefore, the value is doubled in AB0 in the clock ratio 2:1 mode.

In the read cycle, data is captured to an internal register when a T1 period of T1 + RDT has passed and can be held during the period specified by RDT. For details about the read timing, see **Figure E-1 Single Read Timing (Non Mux)** and **Figure E-2 Single Read Timing (AD-Mux)**.

Figures E-8 show the read timing in the page read mode respectively.

Figure E-8. Page Read Timing (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

E.2.14 CSn wait mask register

This register (AB0_CSnWAIT_MASK: 2FFF_020CH + nx20H) masks the WAIT pin. (n represents the slave number)

AB0_CS0WAIT_MASK: 2FFF_020CH
AB0_CS1WAIT_MASK: 2FFF_022CH
AB0_CS2WAIT_MASK: 2FFF_024CH
AB0_CS3WAIT_MASK: 2FFF_026CH

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							WAIT_MASK

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit.
WAIT MASK	R/W	0	0	Specify whether to mask the WAIT pin. 0: Mask the WAIT pin. 1: Unmask the WAIT pin.

Cautions. The WAIT pin is masked after reset. Set up this bit together with the WP bit of the CSn read configuration register in (17).

E.2.15 CSn control register

AB0_CS0CONTROL: 2FFF_0210H
AB0_CS1CONTROL: 2FFF_0230H
AB0_CS2CONTROL: 2FFF_0250H
AB0_CS3CONTROL: 2FFF_0270H

31	30	29	28	27	26	25	24
Reserved							CS_FCLK

23	22	21	20	19	18	17	16
Reserved						CS_ADV	

15	14	13	12	11	10	9	8
Reserved							ADV_WIDTH

7	6	5	4	3	2	1	0
Reserved					AD_OE	ADDR_SEL	ADMUX_SEL

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:25	–	Reserved. If these bits are read, 0 is returned for each bit.
CS_FCLK	R/W	24	0	Specify when FLASHCLK output starts. 0: After the falling edge of CSZ 1: One clock cycle after the falling edge of CSZ
Reserved	R	23:18	–	Reserved. If these bits are read, 0 is returned for each bit.
CS_ADV	R/W	17:16	1H	Specify the timing between CSZ and ADVZ. 0: 0 clock cycles 1: 1 clock cycle 2: 2 clock cycles 3: 3 clock cycles
Reserved	R	15:9	–	Reserved. If these bits are read, 0 is returned for each bit.
ADV__WIDTH	R/W	8	1	Specify the ADV signal width. 0: 1 clock cycle 1: 2 clock cycles
Reserved	R	7:3	–	Reserved. If these bits are read, 0 is returned for each bit.
AD_OE	R/W	2	0	Control Hi-Z timing of address output to the AD bus when the AD-Mux bus is read. 0: At rising edge of ADVZ 1: One clock cycle before a falling edge of RDZ
ADDR_SEL	R/W	1	0	Select the address to output. 0: A27 to A17 1: A11 to A1
ADMUX_SEL	R/W	0	0	Select the AD-Mux device or Non Mux device. 0: AD-MUX 1: Non MUX (A-D Separate)

E.2.16 CSn read configuration register

AB0_CS0FLASHRCR: 2FFF_0214H + nx20H (n represents the slave number)
AB0_CS1FLASHRCR: 2FFF_0234H + nx20H (n represents the slave number)
AB0_CS2FLASHRCR: 2FFF_0254H + nx20H (n represents the slave number)
AB0_CS3FLASHRCR: 2FFF_0274H + nx20H (n represents the slave number)

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
RM	Reserved				WP	Reserved	WD

7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:16	–	Reserved. If these bits are read, 0 is returned for each bit.
RM	R/W	15	1	Specify the read mode. 0: Setting prohibited 1: Asynchronous page mode read (default)
Reserved	R	14:11	–	Reserved. If these bits are read, 0 is returned for each bit.
WP	R/W	10	1	Specify the polarity of the WAIT signal. 0: Active low 1: Active high (default)
Reserved	R	9	–	Reserved. If this bit is read, 0 is returned.
WD	R/W	8	1	Wait delay. 0: WAIT is deasserted with valid data (Not supported in AB0) 1: WAIT is deasserted one clock before valid data (default)
Reserved	R	7:0	–	Reserved. If these bits are read, 0 is returned for each bit.

APPENDIX F. Internal SRAM (SRC)

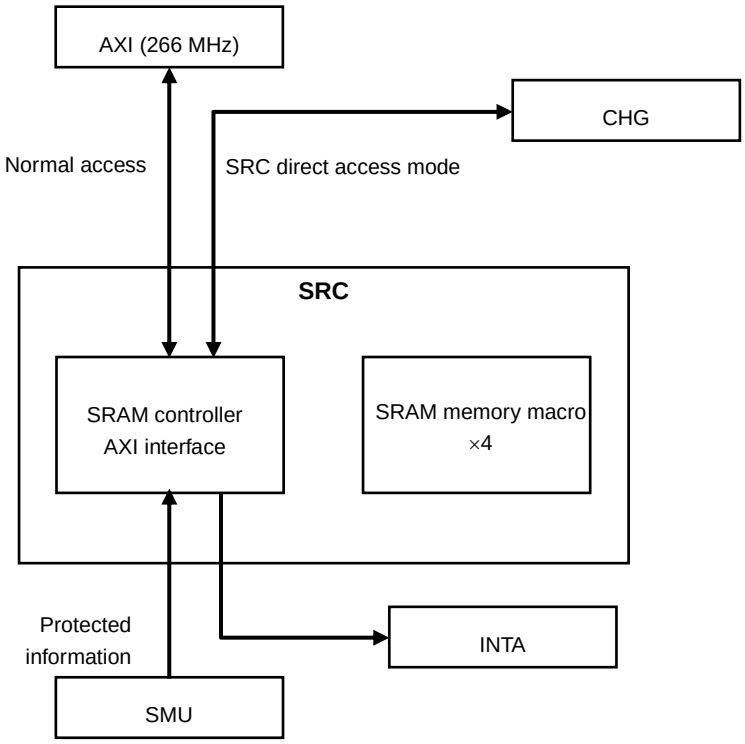
F.1 Overview

This module consists of a 128 KB on-chip single-port SRAM and an SRAM controller (SRC).
The SRC is a controller used for accessing SRAM via internal buses. Mapping frequently-accessed areas to SRAM enables high-speed (lower latency than DRAM because of 64-bit AXI connection) and low-power (lower power consumed than DRAM because I/O ports are not driven and no refresh is required) operations.

F.1.1 Function overview

- Conforms to AMBA AXI Protocol V1.0 Specification.
- The AXI bus is used to interface with the 64-bit SRAM, and runs at 266 MHz (max.).
- The AXI bus is used to interface with the SRAM to issue CPU commands.
- One input clock line
- Single, burst, and wrap transfers can be used to access the AXI bus.
- The SRC includes a 128 KB single-port SRAM.
- The SRC is not reset. It retains its values as long as the power is on.
- Configuration registers are accessed in 32-bit units.
- The SRC_CLKREQ signal is used for a clock request.
- 3 clock cycles of latency occur for a read access.

Figure F-1. Block Diagram of SRC/Internal SRAM



Remark The SRAM controller includes an AXI interface to control writing to or reading from an external device.
The SRAM memory macro includes four stages of 4,096-word 64-bit single-port SRAM.

F.2 Registers

Base address: F002_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	CPU L2 cache mode enable register	SRCEN	R/W	0000_0000H
0004H	Interrupt status register	SRC_INTSTATUS	R	0000_0000H
0008H	Interrupt raw status register	SRC_INTRAWSTATUS	R	0000_0000H
000CH	Interrupt enable/monitor register	SRC_INTENSET	R/W	0000_0000H
0010H	Interrupt enable clear register	SRC_INTENCLR	W	0000_0000H
0014H	Interrupt source clear register	SRC_INTFFCLR	W	0000_0000H

F.3 Register Details

F.3.1 CPU L2 cache mode enable register

This register (SRCEN: F002_0000H) specifies whether to use the SRC (the internal SRAM) as the L2 cache for the CPU.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SRCEN

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRCEN	R	0	0	Specify whether to use the SRC (the internal SRAM) as the L2 cache for the CPU. 0: Do not use 1: Use

F.3.2 Interrupt status register

This register (SRC_INTSTATUS: F002_0004H) indicates the status of the security error interrupt if it is enabled (unmasked).

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SRC_INT_STATUS

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRC_INT_STATUS	R	0	0	Indicates the security error interrupt status. 0: No security error interrupt 1: Security error interrupt occurred

F.3.3 Interrupt raw status register

This register (SRC_INTRAWSTATUS: F002_0008H) indicates the status of the security error interrupt source signal, regardless of whether the interrupt source is enabled or disabled.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SRC_INT_RAW_STATUS

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRC_INT_RAW_STATUS	R	0	0	Indicates the security error interrupt status. 0: No security error interrupt 1: Security error interrupt occurred

F.3.4 Interrupt enable/monitor register

This register (SRC_INTENSET: F002_000CH) enables (unmasks) interrupt sources by writing 1 to the corresponding bits. The current enable status can be read from this register.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SRC_INT_ENSET

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRC_INT_ENSET	R	0	0	Indicates whether issuance of the security error interrupt request is enabled. 0: Not enabled 1: Enabled

F.3.5 Interrupt enable clear register

This register (SRC_INTENCLR: F002_0010H) disables (masks) interrupt sources by writing 1 to the corresponding bits.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SRC_INT_ENCLR

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRC_INT_ENCLR	W	0	0	Disable issuance of the security error interrupt request. 0: Setting prohibited 1: Disable the interrupt.

F.3.6 Interrupt source clear register

This register (SRC_INTFCLR: F002_0014H) clears interrupt sources by writing 1 to the corresponding bits.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SRC_INT_FFCLR

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	0000_0000H	Reserved. If these bits are read, 0 is returned for each bit.
SRC_INT_FFCLR	W	0	0	Clear the security error interrupt source. 0: Setting prohibited 1: Clear the interrupt source.

F.4 Function overview

F.4.1 Clocks and reset

(1) Clock

Access from the AXI bus is enabled only while the BUSCLKREQ signal is high.

(2) Reset

An input asynchronous reset is synchronized in two FF stages and is used as a synchronous reset signal for the module. This reset only clears registers, and data in the SRAM is not cleared.

APPENDIX G. PMU

G.1 Overview

G.1.1 Function overview

The PMU is a module that controls turning the EM/EV on and off and switches the clock. Some control operations are performed by the SMU. The power supply is controlled by the PMU using commands to enable flexible handling of various situations related to peripheral devices or the power save mode.

○ Accessing an APB slave from an APB master can be handled while the PMU is running.

○ The number of cycles to turn PCLK on or off can be changed.
- The initial value (2 cycles for setup and 2 or 16 cycles for a hold) can be changed from 1 to 16 for the setup time and hold time.
- The setting can be specified by using a BUS0 macro register.

○ A security error occurs if a PMU command attempts to access a security area.

○ Command buffer capacity: RAM 6 KB (32 bits × 1,536 words) + FF 64 B (32 bits × 16 words)
Command buffer bit width: 32 bits

○ If the PC[13:0] bits of a command indicate an address outside the command buffer address range (1000H to 203CH), the PMU issues a command PC error interrupt and jumps to the register specified using the PMU_INT_HANDLER_PC register.

○ The conditions for status transitions are specified by using a condition detection command (TRIG_WAIT).

○ When the CPU power is on, the PMU works as an APB slave.

○ PMU registers (including the command buffer) can be accessed in 32-bit (word) units.

○ When the CPU power is off, the PMU works as an APB master and controls the power supply as follows:
- The PMU reads commands from the PMU internal command buffer and executes them.
- The PMU reads or writes to registers. It can control the following macros:
  - TIM, INTA, LCD, GIO, MEMC, AFS, STI, IIC0, PMU, SMU, CHG, USIA (SIO0), USIA (SIO1), INTT, AFS_SEC, and SMU_SEC
- SIO0 can be used to execute the power-on/-off sequences for the power IC. The SMU registers can also be used to control the power IC. The following power domain can be controlled:
  - PC domain
- The PMU controls power supply switches. The switches in the following power domains can be controlled:
  - P1, PL, and P0
  - PM (This can be controlled from both the CPU and PMU.)
  - PV, PR, PG, P2, PU, and PD (The switches in these domains can be controlled only by the CPU.)

- The PMU monitors interrupt signals for the CPU (INT_FIQ0Z, INT_IRQ0Z) and changes the mode when either of these signals is detected.
  - These signals can be detected when a command is fetched or when the TRIG_WAIT command is executed. Detection during command fetching is not executed if these signals are masked using the INT_MASK command. If an interrupt signal is detected during command fetching, execution jumps to the address specified for the POWER_ON_PC register. After that, no interrupt signal is detected during command fetching.

- The interrupt signals for the CPU (INT_FIQ0Z, INT_IRQ0Z) are input to the PMU. These signals can be masked while the PMU is running as a master. While the PMU is not running, these signals pass through the PMU and are output to the CPU. Even if the PMU is running as a master, these signals can be unmasked by using the ARMINT_MASK command.

- While the PMU is running as a master, the PMU detects an interrupt signal when a command is fetched. When an interrupt signal is detected, the power-on sequence automatically starts. However, detection during command fetching is not executed in the following cases:
  - Once an interrupt signal is detected, no interrupt signal is detected during command fetching. (Even if an interrupt signal is detected while the power-on sequence is being executed, the signal is not detected and the sequence continues running.)
  - Starting the power-on sequence can be suppressed by using the INT_MASK command. Executing the INT_MASK command does not affect the wait command operations (such as terminating the wait period).

- The PMU controls the clocks to save power consumed in the PMU. A clock request signal can be input 1 to 16 cycles before and after PSEL, which can be specified by using a BUS0 register. This setting must be specified before starting the PMU.

- To debug the PMU program, the program counter and data can be monitored by using a monitor pin while the PMU is running.

- The PMU includes a watchdog timer (WDT) (32.768 kHz, 18-bit). When the WDT times out, the PMU outputs a system reset request signal to the external power IC.

- The PMU receives a preparation ready signal (PREADY) that reports extension of an APB transfer from each slave, ANDs these signals and the signal that is driven to low level during PMU command access, and outputs the result to BUS0 as the PMU_PB1_PREADY signal.

- When the PMU is not running, signals from BUS0 are output to each slave as is.

- Accessing APB slaves by using a PMU command can be secured by specifying the security level. Accessing data by using a PMU command is handled at the same security level as that of the CPU.

- As command buffers, PMU_CMD_BUF_RAM, which consists of RAM, and PMU_CMD_BUF_FF, which consists of FFs, are incorporated. No command can be specified for addresses extending over PMU_CMD_BUF_RAM and PMU_CMD_BUF_FF.

G.1.2 WDT control and reset request

The PMU judges errors using the WDT to prevent deadlock if an error occurs. When an error occurs (that is, the WDT count reaches the specified limit value), the PMU requests the SMU to reset the EM/EV.
The WDT_COUNT_EN register setting needs to be enabled to control the WDT. Otherwise, the WDT does not run.
The WDT-based control functions only when the PMU starts running. Because the WDT count is cleared when the PMU starts or stops, counting starts after the count is cleared completely. The output of reset requests from the PMU is masked while PMU_START is disabled, or the WDT count has not been cleared completely (while a clear request is being issued).

G.1.3 Transition to power-on sequence by interrupt signal

(1) Transition to power-on sequence during normal mode

When the PMU is running, the PMU judges whether an interrupt input (INT_IRQ0Z_PMU or INT_FIQ0Z_PMU) is asserted when fetching a command from a command register. If either interrupt input is asserted, execution immediately jumps to the PC value specified by using the PMU_POWER_ON_PC register and power-on sequence is executed.

(2) Handling of interrupt signals in other modes

While the mode is changing, disable interrupts by using the INT_MASK command. After the change is complete, the system waits for an interrupt to be input according to the setting specified for the TRIG_WAIT command. Use the TRIG_WAIT command to detect interrupts input while the mode is changing and execute the appropriate processing.

G.2 Registers

The PMU registers can only be accessed in 32-bit (word) units.
These registers are accessed via the APB bus.

Base address: E010_0000H

Address	Register Name	Symbol	R/W	After Reset
0004H	Program counter (command RAM address) register	PMU_PC	R/W	0000_0000H
0008H	PMU start register	PMU_START	R/W	0000_0000H
0030H	Power-on sequence start PC register	PMU_POWER_ON_PC	R/W	0000_0000H
0060H	Watchdog timer count enable register	PMU_WDT_COUNT_EN	R/W	0000_0000H
0064H	Watchdog timer count limit register	PMU_WDT_COUNT_LMT	R/W	0003_FFFFH
0068H	Interrupt handler PC register	PMU_INT_HANDLER_PC	R/W	0000_0000H
0070H	Program status register	PMU_PSR	R	0000_0000H
0074H	TRIG_WAIT command status register	PMU_TRIG_STATUS	R	0000_0000H
0078H	General-purpose register A	PMU_REGA	R	0000_0000H
007CH	General-purpose register B	PMU_REGB	R	0000_0000H
0080H	CPU interrupt status register	PMU_INTSTATUS_A	R	0000_0000H
0084H	CPU interrupt raw status register	PMU_INTRAWSTATUS_A	R	0000_0000H
0088H	CPU interrupt enable set register	PMU_INTENSET_A	R/W	0000_0000H
008CH	CPU interrupt enable clear register	PMU_INTENCLR_A	W	0000_0000H
0090H	CPU interrupt source clear register	PMU_INTFFCLR_A	W	0000_0000H
00A8H	PC error address register	PMU_PCERR	R/W	0000_0000H
00ACH	Security error address register	PMU_SECERRADR	R/W	0000_0000H
0100H to 013CH	Command buffer FF register (16 words from 0100H to 013CH)	PMU_CMD_BUF_FF	R/W	–
1000H to 27FCH	Command buffer RAM register (1,536 words from 1000H to 27FCH)	PMU_CMD_BUF_RAM	R/W	–

G.2.1 Register details

(1) Program counter (command RAM address) register

PMU_PC: E010_0004H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		PC					

7	6	5	4	3	2	1	0
PC							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
PC	R/W	13:0	0000H	Specify the program counter value (command register address) of the command buffer. If the power-off sequence is started by using the PMU_START command, execution starts from the command stored at the address specified for this register. The command register addresses under processing are retained while the PMU is running. (It can be checked by monitoring using a debugger.

Caution Be sure to set up this register before starting the PMU by using the PMU_START command.

(2) PMU start register

PMU_START: E010_0008H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							PMU_START

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_START	R/W	0	0	0: The PMU is not running. 1: Start the PMU (running). The PMU starts by setting this bit to 1. If WDT_COUNT_EN is enabled, the watchdog timer starts counting from 0. When the PMU starts, it issues PMUCLK_REQ first (requesting starts from the write clock cycle operation). Next, the PMU confirms that STANDBYWFI has been asserted. Interrupts input during this period are handled by the CPU. Because the PMU is in the WFI (Wait for Interrupt) state while the CPU handles an interrupt, read this register via the CPU in the interrupt servicing sequence. If 1 is read, write 0 to stop the PMU. Interrupt signals INT_IRQ0Z and INT_FIQ0Z are masked in the PMU and are output to the CPU from when WFI is detected until the PMU is stopped by the PMU_END command, or until the interrupt is unmasked by using the ARMINT_MASK command. The CPU references the PMU_PC register and fetches a command from a command register, and runs according to the value. The PMU stops running only under the following conditions: 1. The PMU_END command is issued. 2. The WDT is incremented up to the upper limit and a reset request is output (forced stop by a reset)

(3) Power-on sequence start PC register

PMU_POWER_ON_PC: E010_0030H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		POWER_ON_PC					

7	6	5	4	3	2	1	0
POWER_ON_PC							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
POWER_ON_PC	R/W	13:0	0000H	Specify the command register address at which the first command when the power-on sequence starts is stored. These bits are referenced when the power-on sequence automatically starts triggered by an interrupt input.

Caution Be sure to set up this register before starting the PMU by using the PMU_START command.

(4) Watchdog timer count enable register

PMU_WDT_COUNT_EN: E010_0060H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							WDT_COUNT_EN

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
WDT_COUNT_EN	R/W	0	0	Specify whether to use the WDT while the PMU is running. 0: Do not use the WDT (default) 1: Use the WDT. If the PMU is started while this bit is set to 1, reset requests by the WDT are enabled. The WDT does not run if this bit is set to 0.

Caution Be sure to set up this register before starting the PMU by using the PMU_START command.

(5) Watchdog timer count limit register

PMU_WDT_COUNT_LMT: E010_0064H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved						WDT_COUNT_LMT	

15	14	13	12	11	10	9	8
WDT_COUNT_LMT							

7	6	5	4	3	2	1	0
WDT_COUNT_LMT							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:18	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
WDT_COUNT_LMT	R/W	17:0	3_FFFFH	Specify the WDT count limit value when the PMU is running. If the PMU_START register is set to 1 while the PMU_WDT_COUNT_EN register is 1, the WDT that runs at 32.768 kHz starts counting from 0. When the WDT count reaches the value specified by using this register, the PMU asserts a signal for requesting reset of EM/EV. (This request signal is deasserted by a reset.)

Caution **Be sure to set up this register before starting the PMU by using the PMU_START command. Clearing the WDT_COUNT_LMT bits to 0 and changing the value while the PMU is running are prohibited.**

(6) Interrupt handler PC register

PMU_INT_HANDLER_PC: E010_0068H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		PMU_INT_HANDLER_PC					

7	6	5	4	3	2	1	0
PMU_INT_HANDLER_PC							

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:14	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_INT_HANDLER_PC	R/W	13:0	0000H	Specify the address to which the program counter jumps when the PMU issues an interrupt. The PMU issues an interrupt if the PMU command PC points to an address outside the range of CMD_BUF_RAM and CMD_BUF_FF, or if a security error occurs.

Caution Be sure to set up this register before starting the PMU by using the PMU_START command.

(7) Program status register

This register (PMU_PSR: E010_0070H) stores the result of an operation command executed in the PMU. The commands subject to storage are CMP1 and CMP2. If the comparison results in match, 1 is stored; otherwise, 0 is stored. The value stored in this register is referenced upon execution of the BRANCH instruction.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							ZERO_FLAG

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:1	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
ZERO_FLAG	R	0	0	Store the result of comparison executed by CMP1 or CMP2.

(8) TRIG_WAIT command status register

This register (PMU_TRIG_STATUS: E010_0074H) is cleared in the TRIG_WAIT command decoding cycle. After that, this register retains information on triggers that occurred during execution of the TRIG_WAIT command (multiple entries possible). Specify the trigger information subject to each TRIG_WAIT command by using bits 24 to 19 of the command.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		INT	Reserved				TIMER

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:6	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
INT	R	5	0	If INT is specified for the TRIG field of the TRIG_WAIT command and the command is executed, this bit is set to 1 when occurrence of an interrupt is detected.
Reserved	R	4:1	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
TIMER	R	0	0	If TIMER is specified for the TRIG field of the TRIG_WAIT command and the command is executed, this bit is set to 1 when the PMU internal timer times out.

(9) General-purpose register A

PMU_REGA: E010_0078H

31	30	29	28	27	26	25	24
REGA							

23	22	21	20	19	18	17	16
REGA							

15	14	13	12	11	10	9	8
REGA							

7	6	5	4	3	2	1	0
REGA							

Name	R/W	Bit No.	After Reset	Description
REGA	R	31:0	0000_0000H	Used for operations in the PMU.

(10) General-purpose register B

PMU_REGB: E010_007CH

31	30	29	28	27	26	25	24
REGB							

23	22	21	20	19	18	17	16
REGB							

15	14	13	12	11	10	9	8
REGB							

7	6	5	4	3	2	1	0
REGB							

Name	R/W	Bit No.	After Reset	Description
REGB	R	31:0	0000_0000H	Used for operations in the PMU.

(11) CPU interrupt status register

This register (PMU_INTSTATUS_A: E010_0080H) indicates the status of interrupt sources enabled (unmasked). Value 0 is read from the bits corresponding to the interrupt sources disabled (masked).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_SERR_A

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	R	1	0	Indicates the status of the command PC error. 0: No command PC error interrupt 1: Command PC error interrupt occurred
PMU_SERR_A	R	0	0	Indicates the status of the CPU security error interrupt. 0: No security error interrupt 1: Security error interrupt occurred

(12) CPU interrupt raw status register

This register (PMU_INTRAWSTATUS_A: E010_0084H) indicates the status of interrupt sources, regardless of whether the interrupt source is enabled or disabled.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_RAW SERR_A

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	R	1	0	Indicates the status of the command PC error. 0: No command PC error interrupt 1: Command PC error interrupt occurred
PMU_RAWSERR_A	R	0	0	Indicates the status of the CPU security error interrupt. 0: No security error interrupt 1: Security error interrupt occurred

(13) CPU interrupt enable set register

This register (PMU_INTENSET_A: E010_0088H) enables (unmasks) interrupt sources by writing 1 to the corresponding bits.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_SERR EN_A

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	R	1	0	Indicates whether issuance of the command PC error interrupt request is enabled. 0: Not enabled 1: Enabled
	W			Enable issuance of the command PC error interrupt request. 1: Enable (unmask) the interrupt.
PMU_SERREN_A	R	0	0	Indicates whether issuance of the CPU security error request is enabled. 0: Not enabled 1: Enabled
	W			Enable issuance of the CPU security error interrupt request. 1: Enable (unmask) the interrupt.

(14) CPU interrupt enable clear register

This register (PMU_INTENCLR_A: E010_008CH) disables (masks) interrupt sources by writing 1 to the corresponding bits.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_SERR MSK_A

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	W	1	0	Disable issuance of the command PC error interrupt request. 1: Disable the interrupt.
PMU_SERRMSK_A	W	0	0	Disables issuance of the CPU security error interrupt request. 1: Disable the interrupt.

(15) CPU interrupt source clear register

This register (PMU_INTFFCLR_A: E010_0090H) clears interrupt sources by writing 1 to the corresponding bits.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_SERR CLR_A

Name	R/W	Bit No.	After Reset	Description
Reserved	R	31:2	–	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	W	1	0	Clear the command PC error interrupt source (CPU). 1: Clear the interrupt source.
PMU_SERRCLR_A	W	0	0	Clear the CPU security error interrupt source. 1: Clear the interrupt source.

(16) PC error address register

PMU_PCERR: E010_00A8H

31	30	29	28	27	26	25	24
Clear	Reserved						

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		ERRPC					

7	6	5	4	3	2	1	0
ERRPC							

Name	R/W	Bit No.	After Reset	Description
Clear	W	31	0	Writing 1 to this bit clears the value of ERRPC.
Reserved	R	30:14	0000H	Reserved. If these bits are read, 0 is returned for each bit. Writing is ignored.
ERRPC	R	13:0	0000H	Indicates the address of the command that caused a PC error.

Caution When a PC error occurs, the address of the command is stored in ERRPC and the value is retained until ERRPC is cleared.

(17) Security error address register

This register (PMU_SECERRADR: E010_00ACH) stores information about CPU security errors.
The address accessed using the REG_WRITE, REG_READ, or RMW command is determined by the values specified for the MacroSelect bit and address[15:0] bits of the command. To obtain the value, the MacroSelect value is decoded to bits 27 to 16 of SECERRADR.

Macro Select [27:16]
1FH SMU_S2 C00

The global ID of the PMU is not included in the stored error information because it is fixed.

31	30	29	28	27	26	25	24
Clear	R/W	Reserved		SECERRADR			

23	22	21	20	19	18	17	16
SECERRADR							

15	14	13	12	11	10	9	8
SECERRADR							

7	6	5	4	3	2	1	0
SECERRADR							

Name	R/W	Bit No.	After Reset	Description
Clear	W	31	0	Writing 1 to this bit clears the value of PMU_SECERRADR.
R/W	R	30	0	Indicates whether the access that caused a CPU security error was for reading or writing. 0: Read 1: Write
Reserved	R	29:28	0H	Reserved. If these bits are read, 0 is returned for each bit.
SECERRADR	R	27:0	000_0000H	Store the address at which the CPU security error occurred.

(18) Command buffer FF register

PMU_CMD_BUF_FF: E010_0100H to E010_013CH

31	30	29	28	27	26	25	24
CMD_BUF_FF							

23	22	21	20	19	18	17	16
CMD_BUF_FF							

15	14	13	12	11	10	9	8
CMD_BUF_FF							

7	6	5	4	3	2	1	0
CMD_BUF_FF							

Name	R/W	Bit No.	After Reset	Description
CMD_BUF_FF	R/W	31:0	–	Store the command to execute while the PMU is running. A command consists of 16 words. A byte enable command issued for this field is ignored. Be sure to access this field in word units.

Caution Store REG_WRITE for clearing USIA_INT following the SP0_WRITE command. If the power-on sequence starts triggered by an INT_IRQ0Z or INT_FIQ0Z input, specify the USIA_INT clear instruction for the POWER_ON_PC bit of the POWER_ON_PC register as the first command executed because REG_WRITE will not be executed.

CMD_BUF_FF can be read or written regardless of the voltage. Store the command for exiting the deep sleep or power down mode in CMD_BUF_FF. (EM/EV runs at 0.7 V.)

The same command cannot be specified for CMD_BUF_RAM and CMD_BUF_FF.

(19) Command buffer RAM register

PMU_CMD_BUF_RAM: E010_1000H to E010_27FCH

31	30	29	28	27	26	25	24
CMD_BUF_RAM							

23	22	21	20	19	18	17	16
CMD_BUF_RAM							

15	14	13	12	11	10	9	8
CMD_BUF_RAM							

7	6	5	4	3	2	1	0
CMD_BUF_RAM							

Name	R/W	Bit No.	After Reset	Description
CMD_BUF_RAM	R/W	31:0	–	Store the command to execute while the PMU is running. A command consists of 1,536 words. A byte enable command issued for this field is ignored. Be sure to access this field in word units.

Caution Store REG_WRITE for clearing USIA_INT following the SP0_WRITE command. If the power-on sequence starts triggered by an INT_IRQ0Z or INT_FIQ0Z input, specify the USIA_INT clear instruction for the POWER_ON_PC bit of the POWER_ON_PC register as the first command executed because REG_WRITE will not be executed.

Reading or writing to CMD_BUF_RAM is prohibited while EM/EV runs at 0.7 V.

Store the command for exiting the deep sleep or power down mode in CMD_BUF_FF. (EM/EV runs at 0.7 V.) The same command cannot be specified for CMD_BUF_RAM and CMD_BUF_FF.

G.3 Function Details

G.3.1 PMU commands

The REG_WRITE, REG_WRITE2, REG_READ, and RMW commands can be used to access APB slave registers. The macro is selected by using the MacroSelect bit in each command. The macro can be selected according to the following table:

Table G-1. APB Slave Macro Selection Bits

MacroSelect	Slave Name	PCLKREQ	Address
00H	TIM	TIM	E000_0000H to E000_FFFCH
01H	INTA	INTA	E002_0000H to E002_FFFCH
02H	LCD	LCD	E004_0000H to E004_FFFCH
03H	GIO	GIO	E005_0000H to E005_FFFCH
04H	MEMC	MEMC	E00A_0000H to E00A_FFFCH
05H	AFS	AFS	E00C_0000H to E00C_FFFCH
06H	–	–	–
07H	STI	STI	E018_0000H to E018_FFFCH
08H	IIC0	IIC0	E007_0000H to E007_FFFCH
09H	PMU	PMU	E010_0000H to E010_FFFCH
0AH	SMU	SMU	E011_0000H to E011_FFFCH
0BH	USIA (SIO0)	SIO0	E012_0000H to E012_FFFCH
0CH	–	–	–
0DH	–	–	–
0EH	CHG	CHG	E014_0000H to E014_FFFCH
0FH	USIA (SIO1)	SIO1	E001_0000H to E001_FFFCH
10H	AFS_SEC	AFS	E021_0000H to E021_FFFCH
11H	AB0	AB0	E00F_0000H to E00F_FFFCH
12H	INTA (INTD)	INTA	E00E_0000H to E00E_FFFCH
13H	INTA (INTT)	INTA	E003_0000H to E003_FFFCH
1FH	SMU_SEC	SMU	E020_0000H to E020_FFFCH

The 31st bit in the first word of a command is used for break processing. If this bit is set to 1, execution is kept waiting after command execution until an interrupt from GIO (GIO_INT) is input. To avoid break processing, set this bit to 0.

Set bit fields that are not assigned to any setting to 0.

Caution The command buffer area is allocated from 100H to 13CH and 1000H to 27FCH. Operation is not guaranteed if an area outside this range is specified for the program counter.

G.4 PMU Commands

This section explains the commands that are executed while the PMU is running.

G.4.1 Register access commands

Command Name	Bit width: 32 (31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Description	Execution Cycles (PMU Clock)
REG_WRITE	BK; 00h; MacroSelect; Address[15:0] Data[31:0]	Register write (2-word command) The MacroSelect bit specification is as shown in Table G-1. Byte masking is not supported. Use PWM instead.	6 + 4 **Notes 1, 2**
SP0_WRITE	BK; 01h; Address[15:0] Data[31:0]	SP0 register write (2-word command) Waits until USIA_INT occurs after write access is completed (waits for communication to end). After execution of this command, execute the REG_WRITE command to clear USIA_INT.	11 + 6 **Notes 1, 3**
REG_READ	BK; A/B; 02h; MacroSelect; Address[15:0]	Register read (1-word command) Stores the register read value to REGA or REGB according to the A/B bit field setting. The MacroSelect bit specification is as shown in Table G-1. A/B: 0: REGA 1: REGB	10 + 4 **Notes 1, 2**
RMW	BK; 03h; MacroSelect; Address[15:0] Data[31:0] Data_EN[31:0]	Register read/modify/write (3-word command) Writes data only to enabled bits (Data_EN = 1). The MacroSelect bit specification is as shown in Table G-1.	11 + 4 **Notes 1, 2**
REG_ WRITE2	BK; A/B; 09h; MacroSelect; Address[15:0]	Register write 2 (1 word command) The MacroSelect bit specification is as shown in Table G-1. Writes data in the register specified by the A/B bit field to the specified address. A/B: 0: REGA 1: REGB	5 + 4 **Notes 1, 2**

Notes 1. Processing takes extra cycles if access by the CPU occurs.

2. This depends on the number of clock cycles supplied before and after PSEL, which is specified in PB1. The value in this table shows an example when the clock is supplied for 2 cycles before PSEL (setup time) and after PSEL (hold time), respectively.

3. This depends on the number of clock cycles supplied before and after PSEL, which is specified in PB1. The value in this table shows an example when the clock is supplied for 2 cycles before PSEL (setup time) and 4 cycles after PSEL (hold time).

G.4.2 Logical operation commands

Command Name	Bit width: 32 (31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Description	Execution Cycles (PMU Clock)
MOVE	BK, A/B, 04H Data[31: 0]	General-purpose register setup command (2-word command) Stores Data[31:0] to a register according to the A/B bit field setting. A/B: 0: REGA 1: REGB	4
AND	BK, A/B, 05H Data[31: 0]	AND command (2-word command) REG(A/B) = REG (A/B) AND Data ANDs the data in the register specified by the A/B bit field and Data[31:0] and stores the result in the specified register. A/B: 0: REGA 1: REGB	4
EXOR	BK, A/B, 06H Data[31: 0]	EXOR command (2-word command) REG(A/B) = REG (A/B)EXOR Data EXORs the data in the register specified by the A/B bit field and Data[31:0] and stores the result in the specified register. A/B: 0: REGA 1: REGB	4
CMP1	BK, 07H	Compare command (1-word command) Compares the values of REGA and REGB and stores the result in bit 0 of PSR. If the values match, 1 is stored; otherwise, 0 is stored.	4
CMP2	BK, A/B, 08H Data[31: 0]	Compare command (2-word command) Compares the values of REG(A/B) and Data and stores the result in bit 0 of PSR. If the values match, 1 is stored; otherwise, 0 is stored. A/B: 0: REGA 1: REGB	4

G.4.3 Branch and jump commands

Command Name	Bit width: 32 (31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Description	Execution Cycle (PMU Clock)
BRANCH	BK, OP, 10H, JUMP value[13:0]	Conditional branch command (1-word command) References bit 0 of the PSR register and jumps to the PC for the absolute JUMP value according to op. Jumps to PC + 4 if the value of bit 0 differs. op: 0: beq 1: bne	4
JUMP	BK, 11H, JUMP value[13:0]	Relative JUMP (1-word command) (Current PC + JUMP value) Specify the jump destination in the minus direction by using the 2's complement.	4
AJUMP	BK, 12H, JUMP value[13:0]	Absolute JUMP (1-word command) Jumps to the specified PC.	4
SUBROUTINE_START	BK, 13H, JUMP value[13:0]	Jump to specified absolute JUMP value (1-word command) JUMP, AJUMP, and BRANCH within a subroutine is possible, but nesting inside another subroutine in a subroutine is not possible.	4
RFS	BK, 14H	Return From Subroutine (1-word command) Jumps to PC + 4 of the SUBROUTINE_START command that was executed immediately before this command. Only one address can be saved.	4

G.4.4 Wait commands

Command Name	Bit width: 32																																Description	Execution Cycles (PMUClock)
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
TIMERWAIT	BK	INT	20H														Count value[15:0]																32.768 kHz 16-bit timer (1-word command) Waits until timer counting ends (about 2 seconds max.). Use this command for waiting when the clock frequency is switched. Issues WDT clear when counting starts and ends. Waits first until completion of the previous TIMERWAIT end processing, if it is not complete. Set the WDT count value (WDT_COUNT_LMT) to the TIMERWAIT count value or higher to prevent the WDT timeout during normal wait period caused by this command.	**Note 2**
INTWAIT	BK		21H																														Waits until INT_IRQ0Z or INT_FIQ0Z is issued from AINT. Clears the WDT when waiting starts and ends. If the operation is to be kept waiting for a long period, store the WDT_STOP command before this command. Clears the WDT if an interrupt is active from the beginning and executes command processing.	**Note 1** **Note 3**
SMU_READY_WAIT	BK	LEVEL	23H																														Waits until the SMU operation enters the specified state. The operation is kept waiting even if INT_IRQ0Z or INT_FIQ0Z is input during the wait period. LEVEL: 0: Low level 1: High level	**Note 1**
TRIG_WAIT	BK		24H								TRG						Count value[15:0]																Trigger wait Clears the PMU_TRIG_STATUS register after a command is decoded. After that, the operation is kept waiting until the level of the trigger specified by TRIG is detected. The wait state is immediately released if the specified trigger has already occurred upon command execution. The trigger that occurred is stored in the PMU_TRIG_STATUS register and REGA. The TRIG bit field shows the following. [21]: Specifies INT as a trigger. [20]: Specifies P1WAKEUP = H as a trigger. [19]: Specifies P1WAKEUP = L as a trigger. [16]: Specifies TIMER. Multiple triggers can be specified. [20] and [19] cannot be specified at the same time. If specified, the wait period is skipped immediately after command execution. TIMER of this command specifies the use of a 32.768 kHz clock and specifies the number of countable cycles in 16-bit units. Be sure to set the count value to a value of 1 or larger, regardless of whether the TIMER is specified as a trigger. (Setting TIMER to 0 is prohibited.) If 0 is set, the subsequent TIMERWAIT command may end without a wait period being inserted. Waits until processing of the TIMERWAIT or TRIG_WAIT executed before completion of this command, if it has not been completed. Set the WDT count value to the count value of this command or larger.	**Note 1** **Note 4**
CYCLE_WAIT	BK	INT	26H																				Count value[9:0]										Wait for the specified number of clock cycles The count can be set in 10-bit units (up to 1,023). The number of cycles is counted based on PMU_CLK. The minimum count is 5 cycles. Setting a lower count is prohibited. PMU_CLK is set by the SMU. The handling of interrupt signals during the TIMERWAIT period can be changed by using the INT bit field. 0: Stop waiting when INT_IRQ0Z or INT_FIQ0Z is input during TIMERWAIT. 1: Continue waiting even if INT_IRQ0Z or INT_FIQ0Z is input.	Count value (5 min.)

Notes 1. Processing takes extra cycles before a wait condition occurs.

2. TIMERWAIT:
(Count value + (8 to 12)) × 32K clock cycles + (6 or 8) × PMU clock cycles are added according to whether clearing the WDT by the previous TRIG_WAIT or TIMERWAIT command has completed.

3. INTWAIT: 6 × PMU_CLK + 8 × PMU_32K_CLK + wait cycles (max.)

4. TRIG_WAIT:
When TIMER is not used: 5 cycles
When TIMER is used: 6 cycles (min.)
The TIMER value is calculated as (count value + 6) × 32K clock cycles.
Up to 2 × 32K clock cycles are added according to whether clearing the WDT by the previous TRIG_WAIT or TIMERWAIT command has completed.

The features of the wait commands are as follows:

Command Type	Waits for	Operation When an Interrupt Occurs	Clearing the WDT
TIMERWAIT (INT = 0)	32.768 kHz timer	Cancels waiting.	Clears the WDT before and after the wait period.
TIMERWAIT (INT = 1)	32.768 kHz timer	Ignores the interrupt.	Clears the WDT before and after the wait period.
INTWAIT	Interrupt pin level	Cancels waiting.	Clears the WDT before and after the wait period.
CYCLE_WAIT (INT = 0)	Number of PMU_CLK cycles	Cancels waiting.	–
CYCLE_WAIT (INT = 1)	Number of PMU_CLK cycles	Ignores the interrupt.	–
SMU_READY_WAIT	SMU status pin level	Ignores the interrupt.	–
TRIG_WAIT	Specified trigger pin level	Depends on the setting.	–

G.4.5 Interrupt mask commands

Command Name	Bit width: 32																																Description	Execution Cycles (PMU Clock)
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
INT_MASK	BK	MASK	30H																														Interrupt mask While interrupts are masked, the power-on sequence does not start automatically when a command is fetched by an interrupt. This setting only suppresses transition to the power-on sequence. When an interrupt occurs, the timer wait state is released. MASK: 0: Unmask interrupts 1: Mask interrupts.	4
ARMINT_MASK	BK	MASK	31H																														Masks and releases masking of interrupt signals issued to ARM. If an interrupt has already been issued upon execution of this command, the interrupt is reported to the CPU. MASK: 0: Releases interrupt masking 1: Masks interrupts	4

G.4.6 Other commands

Command Name	Bit width: 32																																Description	Execution Cycles (PMU Clock)
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
WDT_CLEAR	BK		32H																														WDT count clear	**Note 1**
WDT_STOP	BK		33H																														WDT operation suspension	5[Note 2]
WDT_ RESTART	BK		34H																														WDT count resumption	5
PMU_END	BK		35H																														PMU operation termination Clears the WDT and stops the timer. After that, clears the PMU_START register and makes PMU_CLKREQ to the SMU low level. Makes PMU_PB1_PREADY high level and ends the PMU master operation. If QR is restored, write H to the ARMNORMAL register in the SMU immediately before executing this command.	5
NOP	BK		Others																														No operation	4

Notes 1. 6 × PMU_CLK + 4 × PMU_32K_CLK (max.)

2. Execution takes five cycles because the WDT_STOP command is bufferable.

G.4.7 Other commands

A PMU command can be used to execute a break by setting the highest bit in the command's first word to 1. When a command for which a break specified is executed, the operation is kept waiting until the break state is cancelled in the next command fetch cycle.

BREAK can be cancelled by using an input from GIO, which is assigned to GPIO4.

If the pin is assigned, the break signal is asserted by an input from the GIO. In the PMU, the break is cancelled when an edge of the break signal is detected.

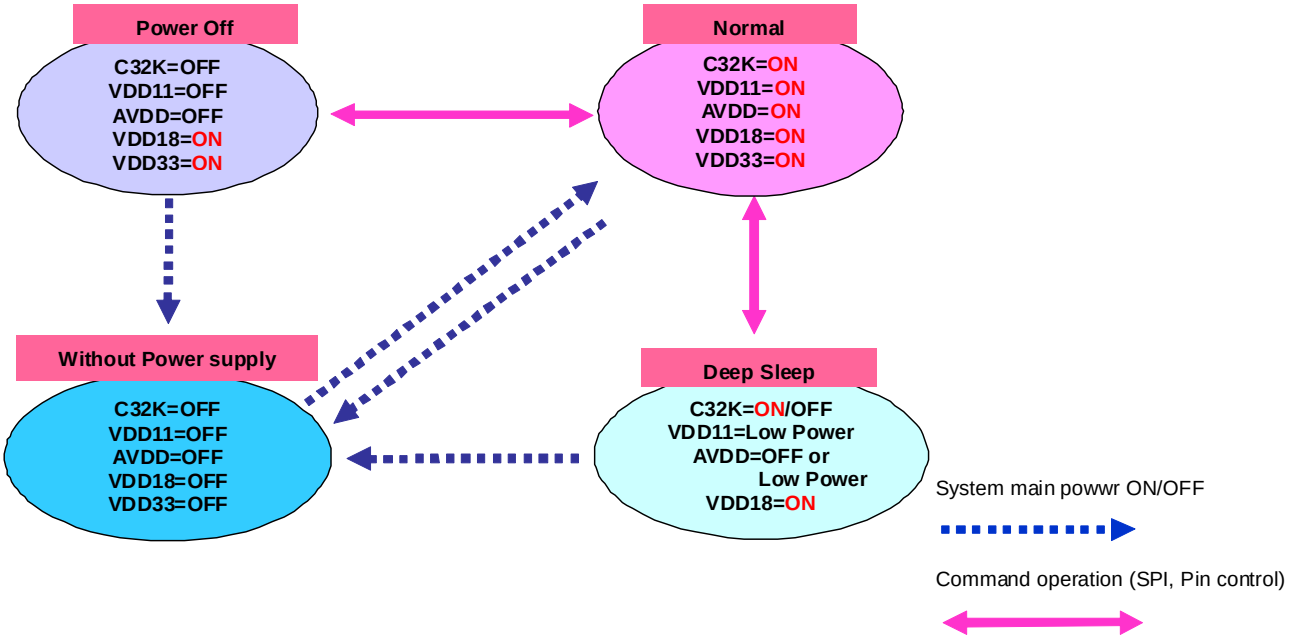
Only use the break function after stopping the WDT.

APPENDIX H. Power supply required specification

H.1 About each power supply system state

The following figure is a transition diagram of the power supply system state achieved by system power supply IC with EM/EV. There are 4 states (without power supplies, Normal, DeepSleep and PowerOff).

Figure H-1. EM/EV power supply system state transition



EM/EV power supply pins	Function
VDD11	Core power supply
AVDD	PLL power supply
VDD18	1.8V IO power supply
VDD33	3.3V power supply
VDD33D	Anti-fuse power supply (3.3V)
VDD33M	1.8V/3.3V IO power supply Note
USB_VD3311/12	Power supply for USB PHY DP/DM terminals
USB_AVDD1/2	Power supply for regurators inside USB PHY
DDR_VDDIO	DDR IO power supply
DDR_VREFH	DDR standard reference current generation
DDR_VREFL	DDR standard reference current generation

H.1.1 Normal

It's the normal condition. Power supply IC supplies a core power supply (VDD11) and a PLL power supply (AVDD) with 1.1V to EM/EV, and inputs a clock of 32.768kHz to C32K terminal. This clock is for PLLs inside EM/EV.

H.1.2 DeepSleep

It’s the low power standby conditions. Power supply IC is to set VDD11 of EM/EV as low voltage and make AVDD off or low voltage (VDD11 and the same electric potential), and a power consumption is suppressed..
Min value of VDD11 is 0.75V. Consider the output voltage error and the ripple supplied to VDD11, and decide the price of the voltage as it won't be less than 0.75 V.
There are 2 kinds, SPI control and terminal control for the transfer to DeepSleep.

H.1.3 PowerOff

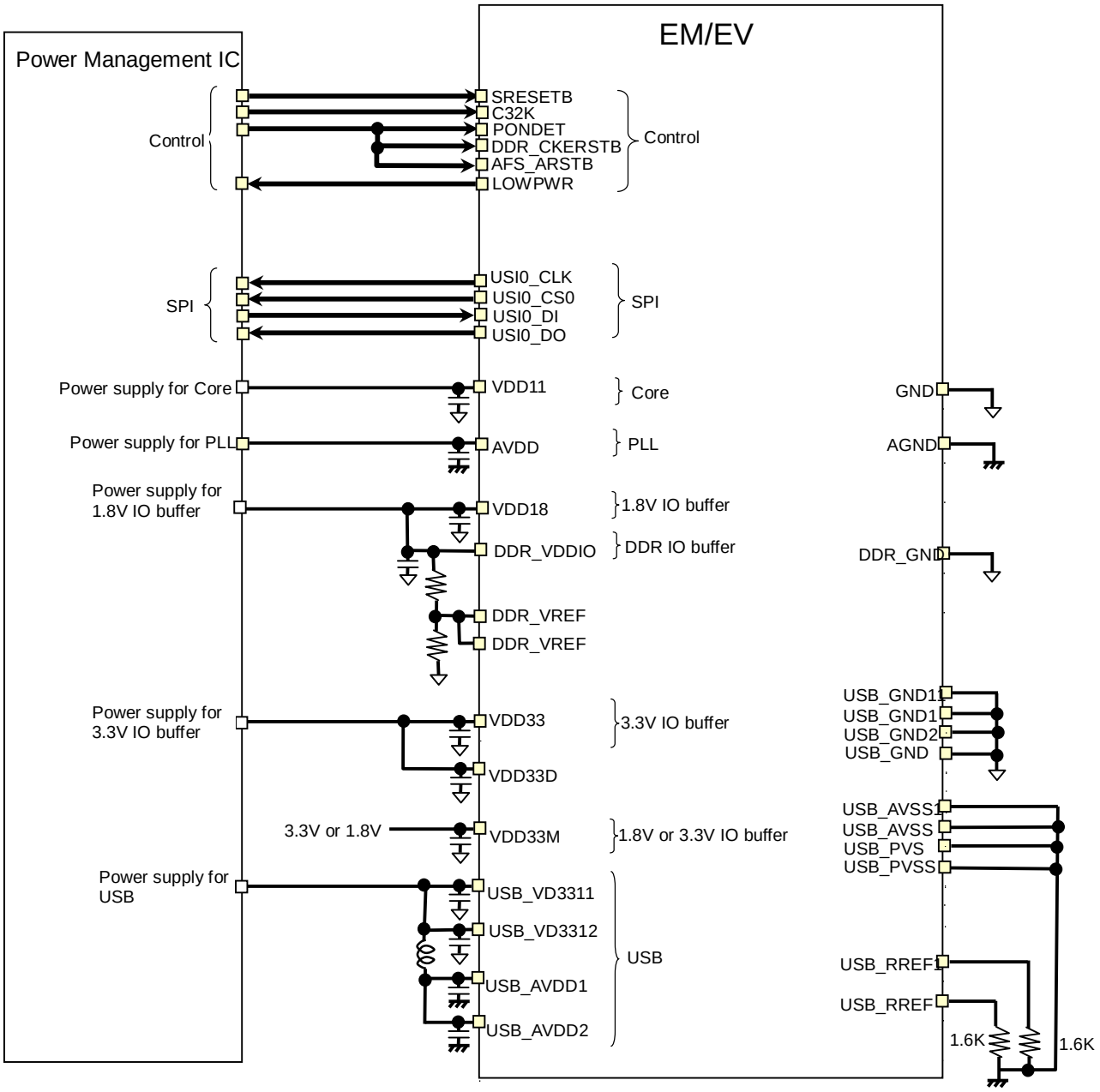
Only an IO power supply of EM/EV (VDD18,VDD33) is in the state turned on. The transfer to PowerOff is performed by only the SPI command of EM/EV.

H.1.4 Without power supply

It's in the state which has no power supplies on the system.

H.2 EM/EV power supply connection diagram (reference)

Figure H-2. EM/EV power supply connection diagram (reference)



Note

(1) When transferring by SPI control to DeepSleep, make the LOWPWR terminal Open.

(2) That VDD33M chooses 1.8V or 3.3V.

(3) Follow processing of VREF (Input Reference Voltage) in DC operating conditions in JEDEC STANDARD (DDR2 SDRAM SPECICATION) about pin handling of DDR_VREFL and DDR_VREFH.

(4) The current capacity value necessary to each power supply changes by the operate contents of EM/EV.

(5) Connect reference resistance (1.6 kΩ) with USB_RREF1/2 during analog GND (AGND,USB_AVSS,USB_PVSS).

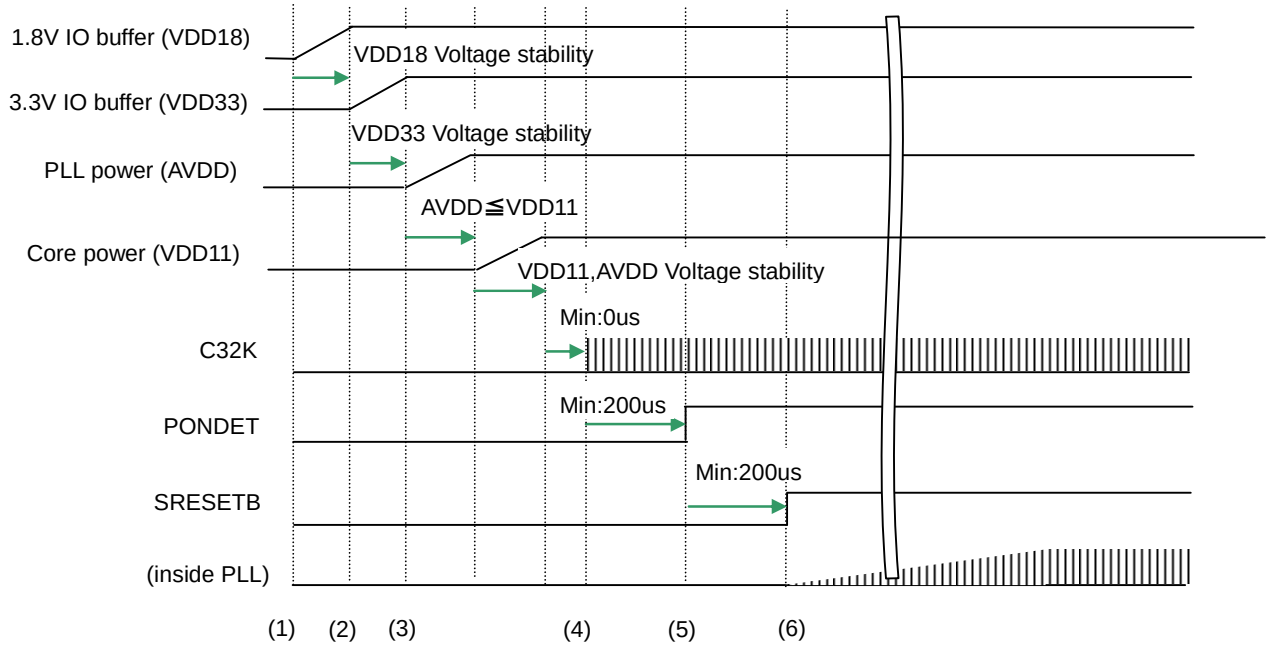
(6) Separate a digital power supply of an USB (USB_VD), an analog power supply (USB_AVDD), a digital GND (USB_GND) and an analog GND (USB_AVSS/PVSS) by an inductor or ferrite.

H.3 Power supply sequence

It's explained about transfer sequence to each power supply system state.

H.3.1 Without power supply -> Normal

Figure H-3. Without power supply -> Normal



Note : It's made power supply stability in the time when the power-supply voltage reached MIN value of the recommendation operating condition.

(1) Power supply IC supplies 1.8V IO power supply (VDD18) to EM/EV and waits for voltage stability.
(2) Power supply IC supplies 3.3V IO power supply (VDD33) to EM/EV and waits for voltage stability.
(3) Power supply IC supplies VDD11 and AVDD to EM/EV and waits for voltage stability.
(4) Power supply IC supplies C32K of EM/EV with a reference clock (32.768kHz).
(5) Power supply IC changes PONDET in EM/EV the "H" level.
(6) When power supply IC makes SRESETB in EM/EV the "H" level, the inner PLL starts to oscillate.

H.3.2 DeepSleep <-> Normal

There are SPI control and terminal control for transfer method to DeepSleep.

(1) SPI control

Figure H-4. DeepSleep <-> Normal (SPI control)

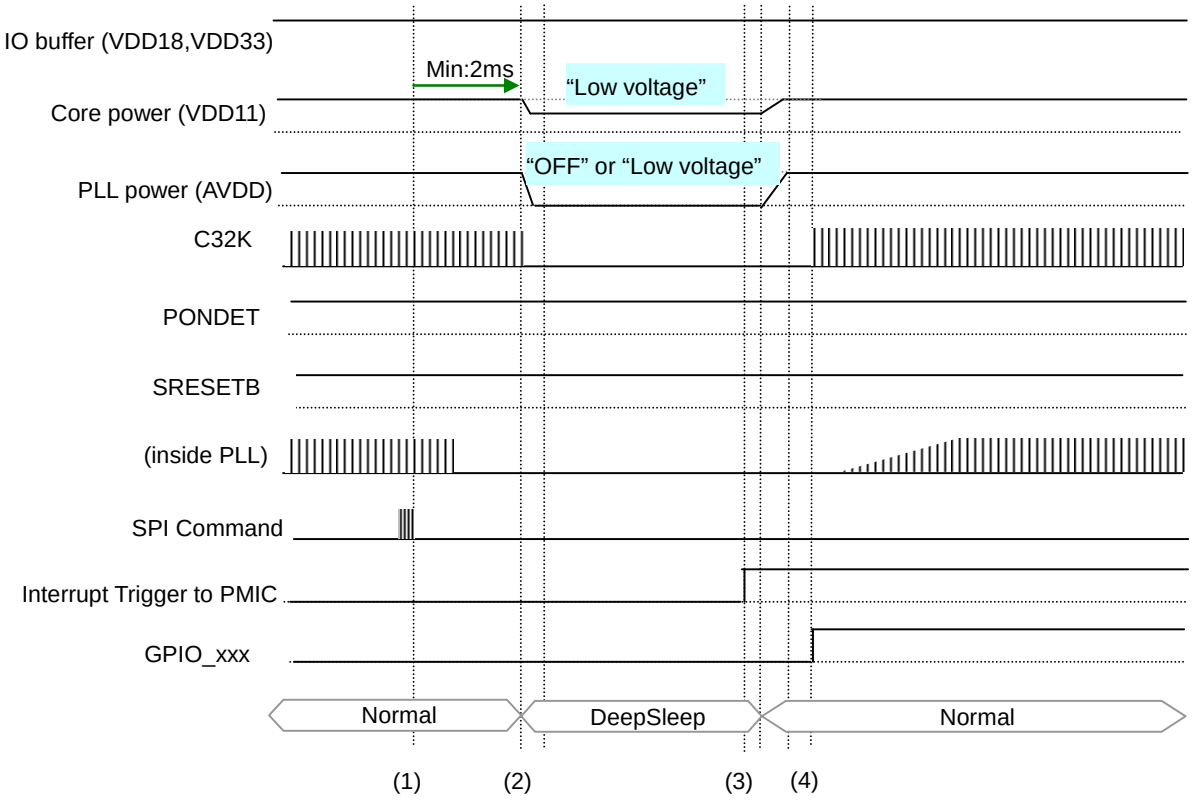
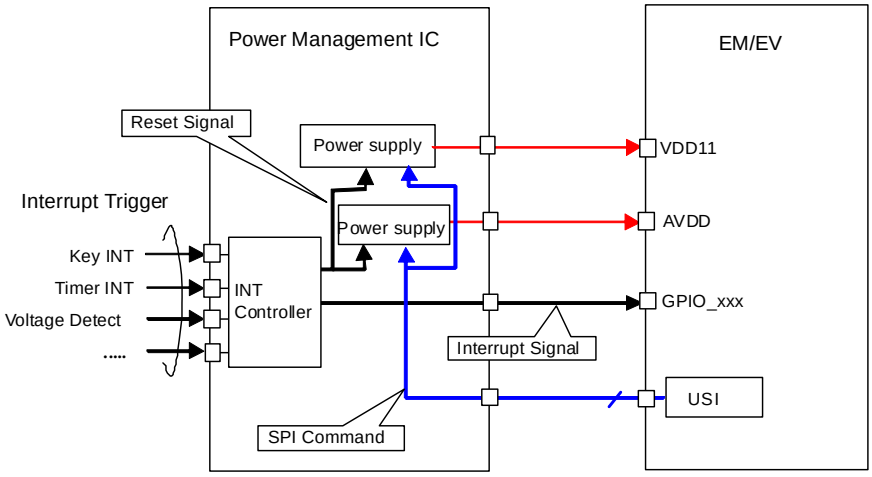


Figure H-5. Control to the DeepSleep state (SPI control Connection example)



Power supply IC and a connection example with EM/EV are indicated. Power supply IC drops the voltage of a power supply by SPI control from EM/EV and turns on a power supply by an interruption to power supply IC. A release factor of DeepSleep is interruption from outside to power supply IC.

(1) EM/EV sends the voltage change command of VDD11 to power supply IC and changes it to VDD11 and the same electric potential to AVDD or sends the off command.
(2) Power supply IC changes VDD11 to low voltage after Min:2ms passage. EM/EV does the preparations to transfer to the DeepSleep state between the 2ms. Clock input of 32.768kHz to C32K is suspended. (It may be input.)
(3) Power supply IC receives the outside return factor (Interrupt trigger), returns VDD11 of EM/EV to 1.1V from low voltage and supplies AVDD. An interrupt signal (GPIO_xxx) is transmitted to EM/EV after stability of VDD11 and AVDD.
When suspending clock input to C32K, supply is begun.
(4) When power supply IC sets GPIO in EM/EV_xxx in the Hi level, EM/EV starts the inner PLL oscillation. Restore operation to Normal is performed from DeepSleep after PLL stability.

Note : When making AVDD turn off in DeepSleep, make the power supply IC side output Hi-Z.

(2) Terminal control

Figure H-6. DeepSleep <-> Normal (Terminal control)

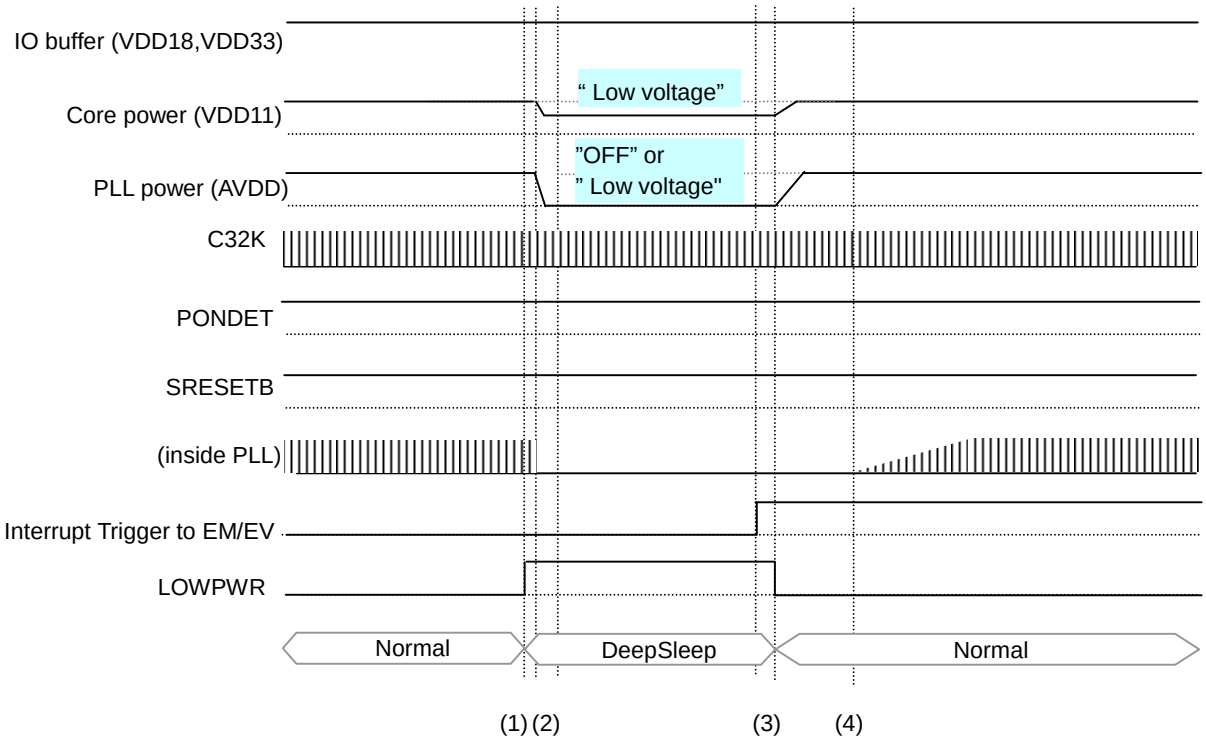
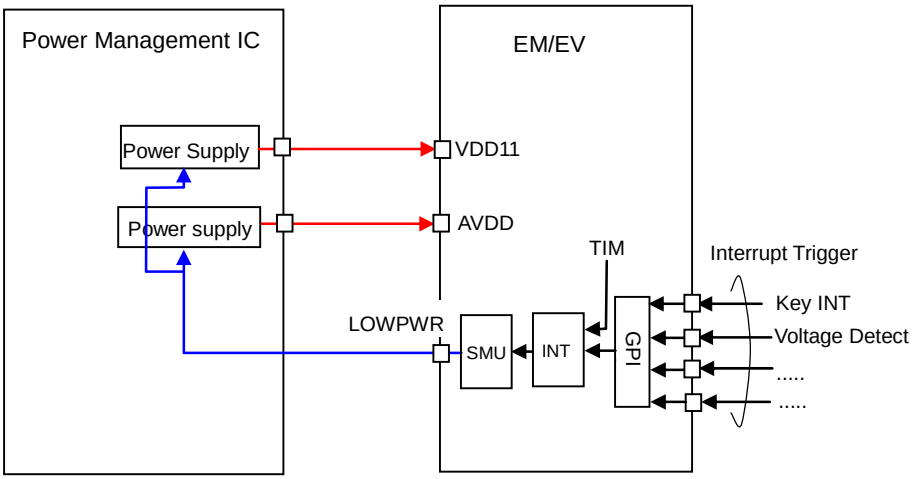


Figure H-7. Control to the DeepSleep state (Terminal control Connection example)



Power supply IC and a connection example with EM/EV. The power-supply voltage is lowered by Terminal control from EM/EV and a power supply is turned on by interruption to EM/EV. A release factor of DeepSleep is interruption to EM/EV.

(1) EM/EV transfers to DeepSleep and also rises a LOWPWR terminal.
(2) If a LOWPWR terminal for EM/EV falls, power supply IC changes VDD11 to low voltage. AVDD changes it to VDD11 and the same electric potential or establishes it off.
(3) When EM/EV receives a return factor to Normal (Interrupt Trigger by outside or internal interrupt of EM/EV), the LOWPWR terminal is falled. Power supply IC returns VDD11 to 1.1V and supplies a PLL power supply.
(4) The inner PLL oscillation is begun inside EM/EV. Restore operation to Normal is performed from DeepSleep after stability.

Note : When making AVDD turn off in DeepSleep, make the power supply IC side output Hi-Z.

H.3.3 PowerOff <-> Normal

Figure H-8. PowerOff <-> Normal

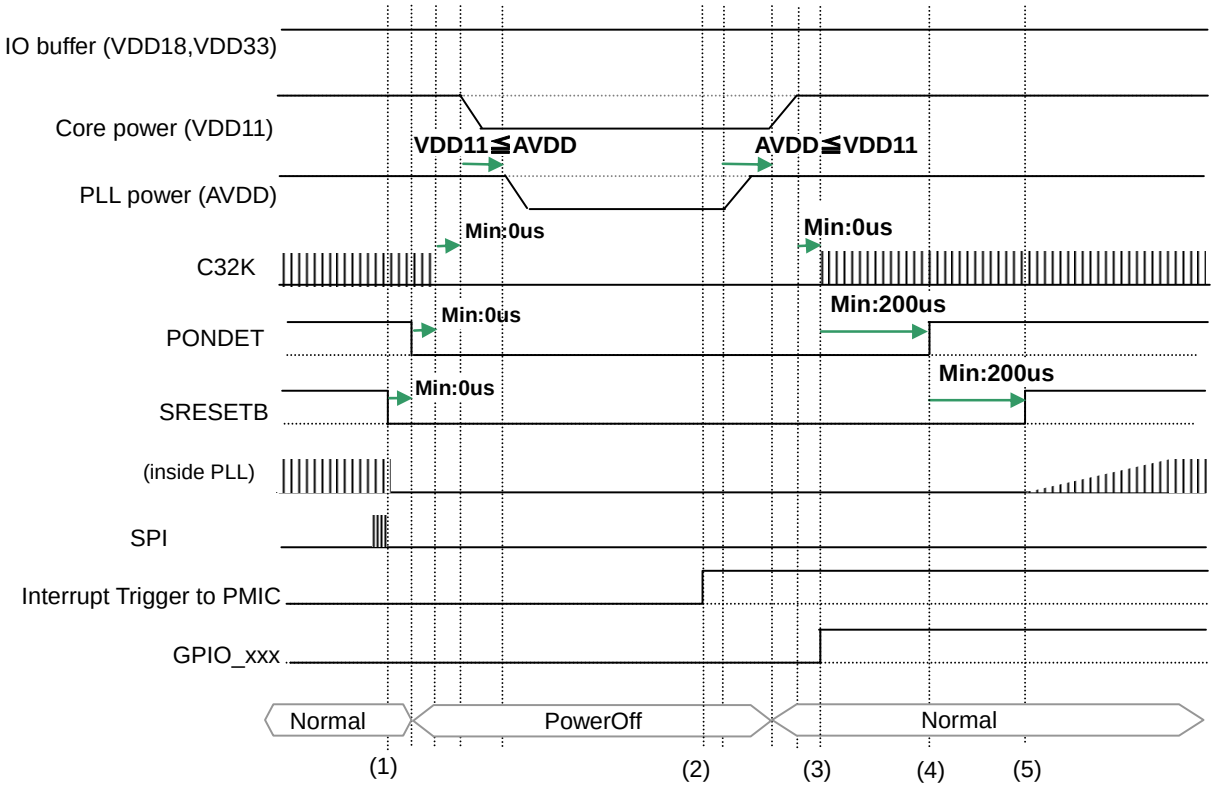
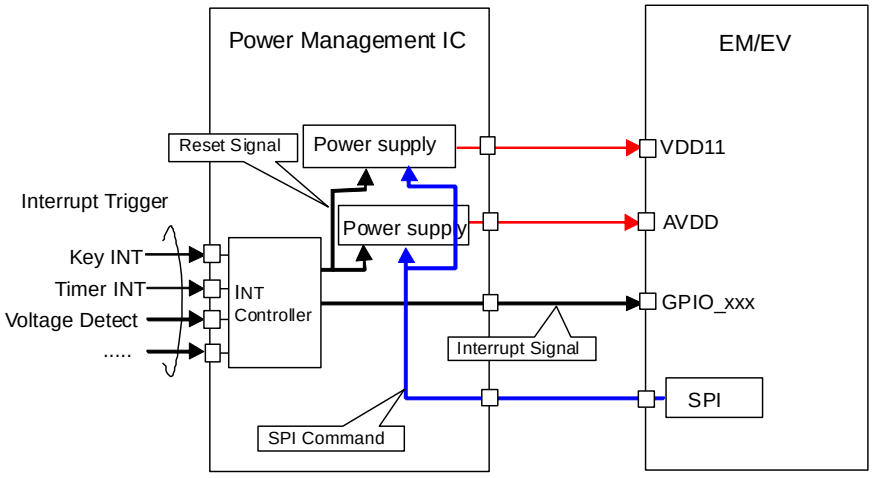


Figure H-9. Control to the PowerOff state (Connection example)



Power supply IC and a connection example with EM/EV. A power supply is turned off by SPI control from EM/EV and a power supply is turned on by interruption to power supply IC.

(1) Power supply IC rises SRESETB,PONDET in EM/EV and suspends 32.768KHz clock supply to C32K. Next supply of VDD11,AVDD is suspended.

(2) Power supply IC receives the outside return factor (Interrupt Trigger), begins supply of VDD11,AVDD to EM/EV and waits for power supply stability.

(3) After power supply stability, power supply IC inputs 32.768KHz to EM/EV.

(4) Power supply IC rises PONDET in EM/EV.

(5) When power supply IC rises SRESETB in EM/EV, a PLL inside EM/EV starts to oscillate.

REVISION HISTORY	EMMA Mobile EV2 User's Manual: 1chip

Rev.	Date	Description	
		Page	Summary
1.00	Jan 29, 2010	—	1st revision release
2.00	Mar 31, 2010	—	Incremental update from comments to the 1.0.
3.00	Jun 7, 2010	—	Incremental update from comments to the 2.0.
4.00	Jun 30, 2010	—	EM/EV1 related description addition. (The difference with EM/EV2 is mentioned.) Incremental update from comments to the 3.0. (A change part from the old revision is "★" marked in the page left end.)
5.00	Sep 30, 2010	—	Incremental update from comments to the 4.0. (A change part from the old revision is "★" marked in the page left end.)
6.00	Dec 28, 2010	—	Incremental update from comments to the 5.0. (A change part from the old revision is "★" marked in the page left end.)
7.00	Apr 15, 2011	—	Incremental update from comments to the 6.0.
8.00	May 31, 2011	—	EM/EV1 related description deletion. Incremental update from comments to the 7.0.

EMMA Mobile EV2 User's Manual: 1chip

Publication Date: Rev.1.00 Jan 29, 2010
Rev.8.00 May 31, 2011

Published by: Renesas Electronics Corporation

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

© 2011 Renesas Electronics Corporation. All rights reserved.

Colophon 1.0

1chip

EMMA Mobile EV2

Renesas Electronics Corporation

R19UH0036EJ0800