MSM6246™/MSM6290™ Chipset Training
MSM6246/MSM6290 Device

80-VF625-24 Rev. A

Qualcomm Confidential and Proprietary

QUALCOMM Incorporated
5775 Morehouse Drive
San Diego, CA 92121-1714
U.S.A.

Customer Affirmation for Technical Support*

In order to facilitate Qualcomm's compliance with a U.S. Federal Court injunction ruling dated 12/31/2007, acknowledgement of the following is required from each customer seeking technical assistance.

Customer confirms that this support request is for a wireless terminal made, sold and used solely outside the USA if it falls within the following table:

UMTS	**Qualcomm will not support for the U.S.:** MSM6275, MSM6280, MSM7200, MSM7200A, ESM6270, ESM7205, ESM7205A
1x/EV-DO	**If first sold to customer <u>after</u> 5/29/2007, Qualcomm will not support for the U.S.:** MSM6150, MSM6175, MSM6500-90, MSM6500-130, MSM6550, MSM6550A, MSM6575, MSM6800, MSM6800A, MSM7500, MSM7500A, MSM7600
	Unless used in the manner prescribed by Qualcomm for use in the U.S., Qualcomm will not support for the US: QSC6075, QSC6085, MSM7525, MSM7601, MSM7625, MDM1000, QSD8650, MSM6551, MSM6551A, MSM6801, MSM6801A, MSM6571, MSM7501, MSM7501A

The foregoing restrictions shall not apply to wireless terminals represented to Qualcomm by Verizon Wireless as being exclusively made on their behalf.

*Reference: 80-VH591-1 Revision B

The following information is licensed and proprietary material.

Revision history

Revision	Date	Description
A	February 2008	Initial release

Agenda

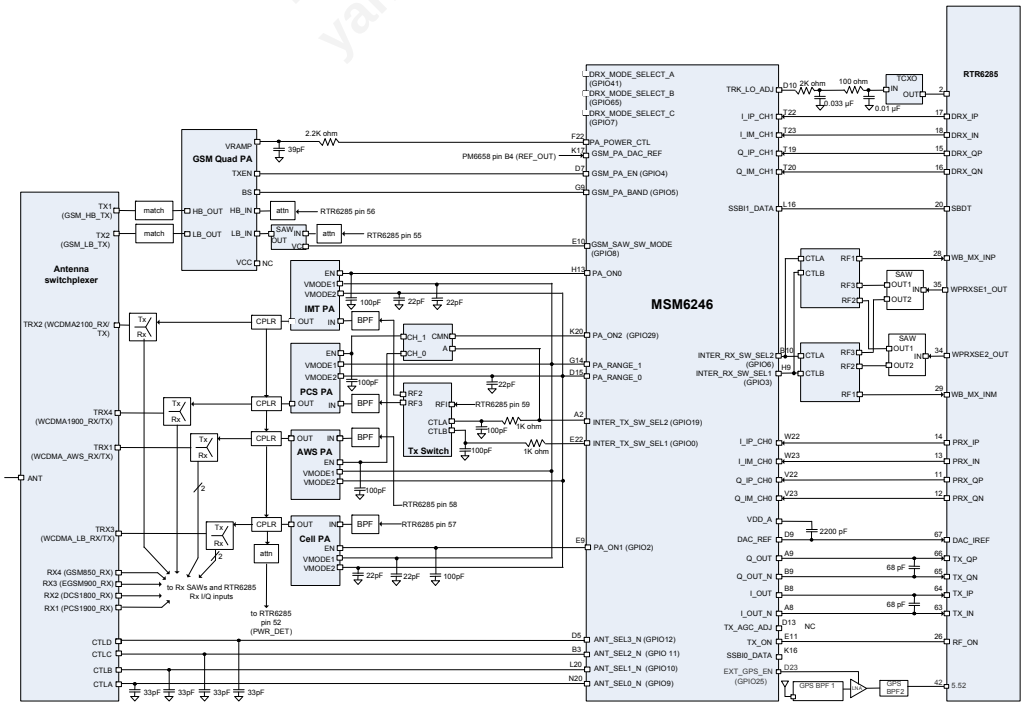
- MSM6246/MSM6290 device overview
  - Milestones, system overview, comparison of the MSM6290 device with the MSM6280™ device and the MSM6246 device with the MSM6245™ device
- New connectivity features
  - High-speed USB
  - High-capacity USB UICC interface
  - SDCC2 (SDIO)
  - Fast UART for Bluetooth® 2.0 and Bluetooth 2.1 with EDR
  - HSUPA – MSM6290 device only
  - TSIF – MSM6290 device only (update from MSM6280 device)
- Memory configurations
- MSM6246 pin removal
- MSM6246 and MSM6290 feature comparison
- MSM6246 and MSM6290 ES limitations
- SURF6246™/SURF6290™ layout and features
- Useful documents

Major Milestones

- MSM6246 milestones
  - Engineering samples: September 2007
  - Feature complete release: December 2007
  - Commercial release: March 2008

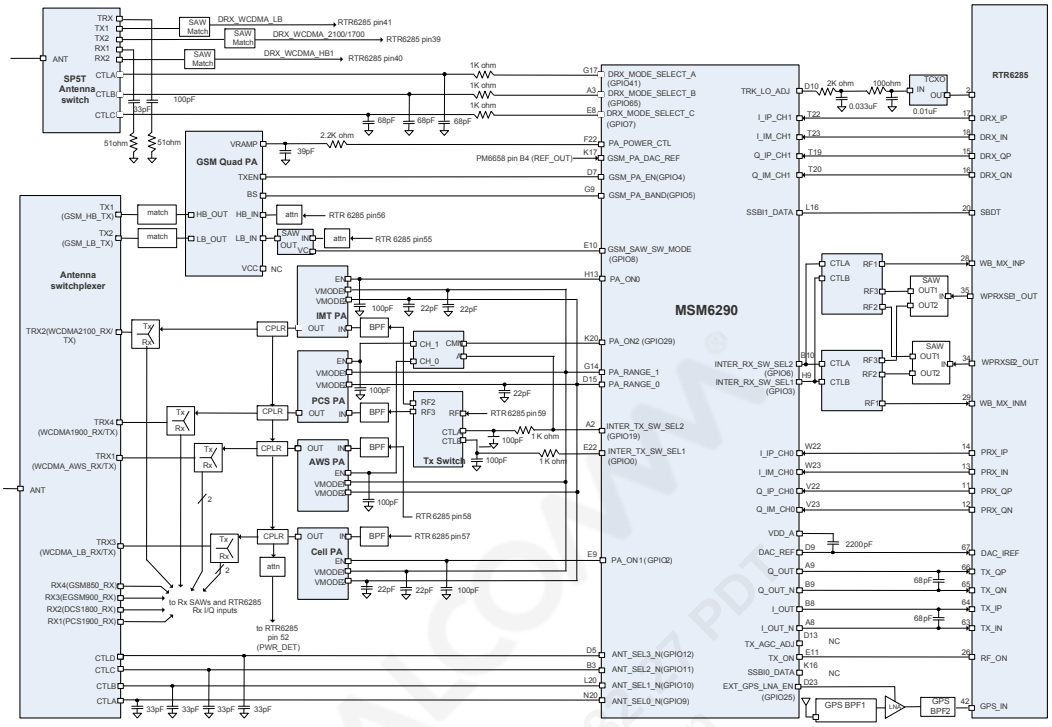
- MSM6290 milestones
  - Engineering samples: October 2007
  - Feature complete release: December 2007
  - Commercial release: March 2008
  - NOTE: HSUPA support in the March 2008 CS release will be 2.0 Mbps (10 ms TTI). Schedule for support of 2 ms TTI is TBD.

MSM6246 Block Diagram (Platform F)



Note: Platform F handsets do not support receive diversity due to GPIO limitation. Platform G (not shown) does not support receive diversity or GPS.

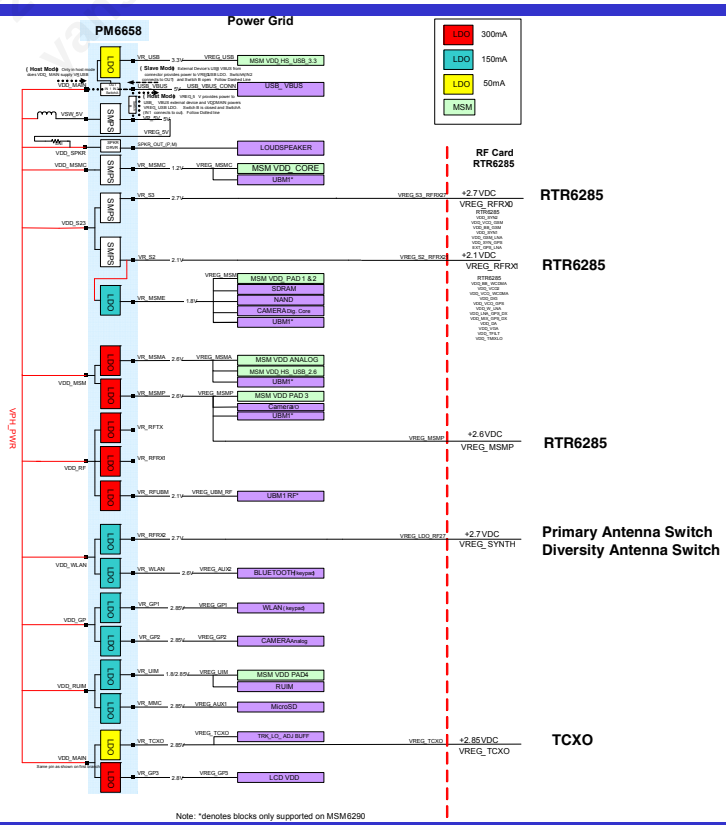
MSM6290 Block Diagram (Platform F)



Note: Platform G (not shown) does not support receive diversity or GPS.

MSM6246 and MSM6290 Power Grid

Note: MSM6246 and MSM6290 designs do not use the S3 sub-regulator for VDD_MSM. S3 does not supply enough current with the addition of HS USB and UBM (for MSM6290 device)



Feature Comparison: MSM6245 vs. MSM6246 (1 of 2)

Feature	MSM6245 device	MSM6246 device
Modem	Tri-band or quad-band WCDMA Quad-band GSM/GPRS/EDGE WEDGE DTM	Quad-band WCDMA Quad-band GSM/GPRS/EDGE HEDGE 3.6 Mbps HSDPA GPS DTM
Processor	 ARM926EJ™/AHB 225.6 MHz/75.2 MHz medium-speed /medium-power mode ARM®/AHB 122.88 MHz/61.44 MHz low-speed/ low-power mode ADSP – up to 100 MHz MDSP – up to 120 MHz	ARM926EJ/AHB 273.6 MHz/91.2 MHz high-speed/ high-power mode ARM/AHB 245.76 MHz/81.92 MHz medium-speed/ medium-power mode ARM/AHB 122.88 MHz/61.44 MHz low-speed/low-power mode ADSP – 122.88 MHz MDSP – 122.88 MHz
Package	14 x 14 mm 409 pin, 0.5 mm CSP	10 x 10 mm 384 pin, 0.4 mm NSP
Supported RF platforms	Platform B (RTR6275™ IC + RFR6275™ IC) Platform E (RTR6275 IC + RFR6275 IC) Platform G (RTR6280™ IC): no GPS	Platform F (RTR6285™ IC): receive diversity available for data cards only Platform G (RTR6280 IC): no GPS
Memory configuration	8/16-bit NAND and 32-bit SDRAM NOR + 16-bit SDRAM (both on EBI1) OneNAND™ (EBI2)	8/16-bit NAND and 32-bit SDRAM OneNAND (EBI2)
HSDPA	Not supported	3.6 Mbps
Power management IC	PM6650-2™/PM6650-3™ IC (for Platform B/E) PM6653™ IC (for Platform G)	PM6658™/PM6653 IC (for Platform F/G)
USB	3-wire USB 2.0 FS – OTG	USB 2.0 HS (peripheral and host)
High-capacity USB SIM (USB UICC)	Not supported	Supported

Feature Comparison: MSM6245 vs. MSM6246 (2 of 2)

Feature	MSM6245 device	MSM6246 device
UART	Three legacy UARTs	UART1 – high-speed UART2 (USIM) – legacy
Second SDIO	Not supported	Supported
MDDI	Supported	Not supported
GPS	Not supported	Standalone + assisted (with Platform F)
Bluetooth	BT 1.2 or BT 2.0 (no EDR) in later releases	Fast UART to I/F to BTS4020™ (BT2.0 EDR) and BTS4021™/BTS4025™ (BT2.1 EDR)
Qcamera™ (camera interface) Viewfinder frame rate	Up to 2.0 megapixel support 30 fps at QCIF 15 fps at QVGA	Up to 3.0 megapixel support 30 fps at QCIF 15 fps at QVGA
LCD HW interface	18 bpp	24 bpp
Dual microphone	Not supported	Supported*

* For dual-microphone hardware design considerations, refer to ***Application Note: Dual-Microphone Noise Cancellation Electro-Acoustical Design Guidelines*** **(80-VE797-11)**. A special license is required for the dual-microphone noise cancellation feature.

Feature Comparison: MSM6280 vs. MSM6290 (1 of 2)

Feature	MSM6280 device	MSM6290 device
Modem	Tri-band or quad-band WCDMA Quad-band GSM/GPRS/EDGE 3.6 Mbps and 7.2 Mbps HSDPA DTM GPS	Quad-band WCDMA Quad-band GSM/GPRS/EDGE 3.6 Mbps and 7.2 Mbps HSDPA DTM GPS HSUPA
Processor	ARM926EJ/AHB 273.6 MHz/91.2 MHz high-speed/high-power mode ARM/AHB 245.76 MHz/81.92 MHz medium-speed/medium-power mode ARM/AHB 122.88 MHz/61.44 MHz low-speed/low-power mode ADSP – up to 100 MHz MDSP – up to 120 MHz	ARM926EJ/AHB 297.6 MHz/99.2 MHz high-speed/high-power mode ARM/AHB 245.76 MHz/81.92 MHz medium-speed/medium-power mode ARM/AHB 122.88 MHz/61.44 MHz low-speed/low-power mode ADSP – 122.88 MHz MDSP – 122.88 MHz
Package	14 x 14 mm 409 pin, 0.5 mm CSP, 11 x 11 mm 432 pin, 0.4 mm NSP	10 x 10 mm 384 pin, 0.4 mm NSP
Supported RF platforms	Platform 3U/3U Lite Platform B/E (RTR6275 IC + RFR6275 IC) Platform D (RTR6275 IC + RFR6500™/RFR6525™ IC) Platform F (RTR6285 IC) Platform G (RTR6280 IC)	Platform F (RTR6285 IC) Platform G (RTR6280 IC)
HSDPA	3.6 Mbps for initial commercial releases 7.2 Mbps for later releases	7.2 Mbps
HSUPA	Not supported	Supported
Broadcast interface	MediaFLO™ (RBR1000™, MBD1000™) – EBI2 MBP1600™ – ISDB-T (TSIF), MediaFLO, DVB-H MBP1610™ – MediaFLO (EBI2)	MBP1600 – ISDB-T (TSIF), MediaFLO, DVB-H MBP1610 – MediaFLO (EBI2)
Power management IC	PM6650-2/PM6650-3 IC (for Platform B/E) PM6658 IC (for Platform F/G)	PM6658/PM6653 IC (for Platform F/G)

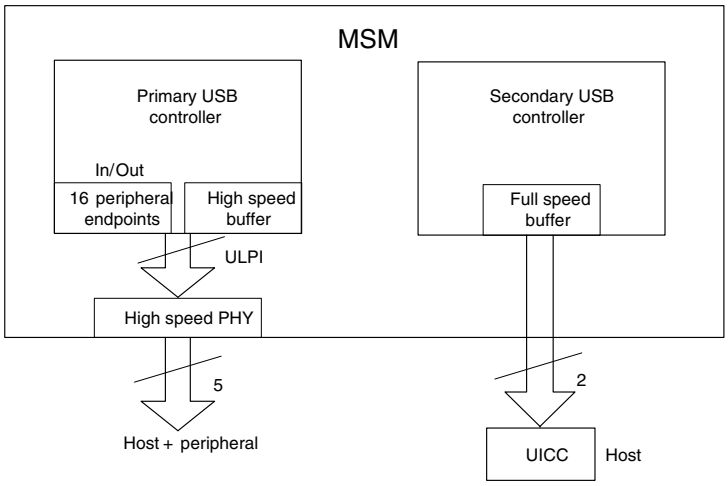
Feature Comparison: MSM6280 vs. MSM6290 (2 of 2)

Feature	MSM6280 device	MSM6290 device
USB	3-wire USB 2.0 FS -OTG	USB 2.0 HS (peripheral and host)
High-capacity USB SIM (USB UICC)	Not supported	Supported
UART	Three legacy UARTs	UART1 – high-speed; UART2 (USIM) – legacy; UART3 – legacy
2nd SDIO	Not supported	Supported
Bluetooth	BT 1.2	Fast UART to I/F to BTS4020 (BT2.0 EDR) and BTS4021/BTS4025 (BT2.1 EDR)
Digital rights management (DRM)	OMA DRM 1.0	OMA DRM 2.0
Boot mode	Trusted and normal boot	Trusted boot only
Qcamera (camera interface) Viewfinder frame rate	Up to 4.0 megapixel support 30 fps at QVGA	Up to 5.0 megapixel support 30 fps at QVGA
LCD HW interface	18 bpp	24 bpp
Display resolution	QVGA	QVGA to WQVGA scaling
2D/3D graphics acceleration	ARM/DSP based acceleration - 225 K triangles per second - 7 M pixels per second	HW accelerated - 600 K triangles per second - 90 M pixels per second

USB Features

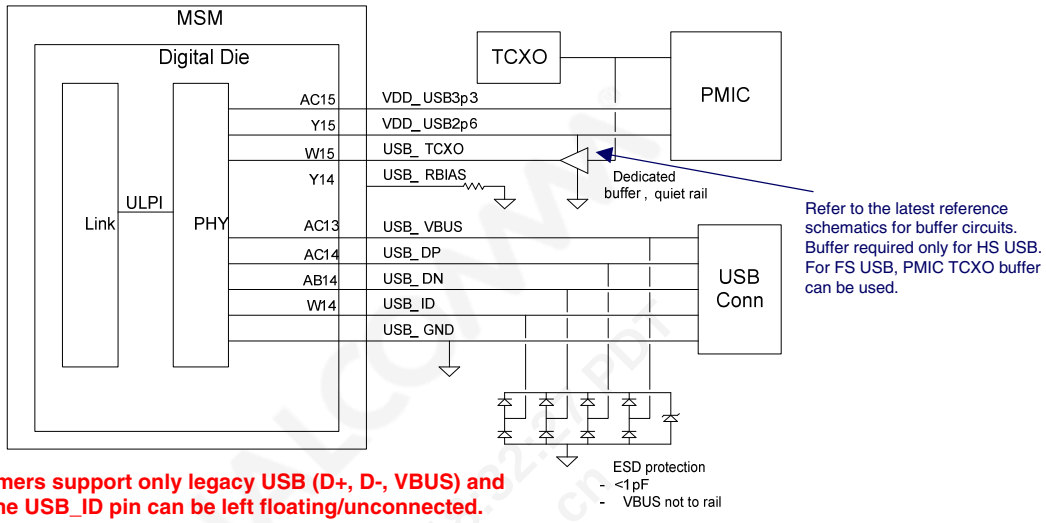
- The MSM6246 and MSM6290 devices feature a high-speed USB with an integrated physical (PHY) layer to support up to 480 Mbps (theoretical) data rates.
- The MSM6246 and MSM6290 devices support a primary and a secondary USB controller.
  - Primary USB controller features:
    - » Integrated controller
    - » Integrated high-speed PHY
    - » Operates at low-speed (1.5 Mbps), full-speed (12 Mbps) and high-speed (480 Mbps)
    - » High-speed USB controller (specification 2.0)
    - » Acts as both host and peripheral
    - » In peripheral mode, the controller has 16 IN/OUT pairs of endpoints; in host mode, the number of possible endpoints is determined by software, and can be greater than 16.
  - Secondary USB controller features:
    - » Supports USB UICC
    - » Diagnostics are not supported.

Primary and Secondary USB Controllers



Primary USB – HS USB

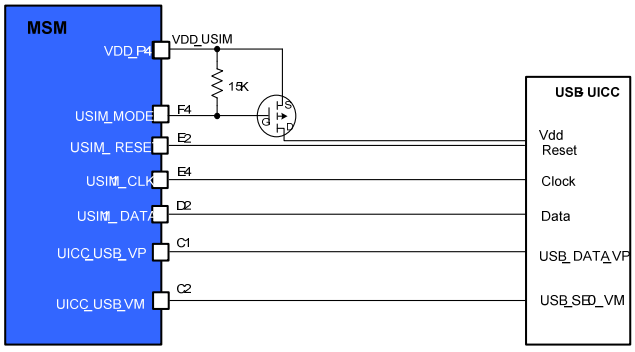
- HS or FS USB is supported on the primary USB port.
- Five USB pins are dedicated for high-speed USB interface.
- Dedicated high-speed USB VDD pads have been added to the MSM6290 and MSM6246 devices.
- Diagram of HS USB:



Note: If customers support only legacy USB (D+, D-, VBUS) and slave mode, the USB_ID pin can be left floating/unconnected.

Secondary USB – USB UICC

- The secondary USB port is used for the universal integrated circuit card (UICC). It is a SIM card with both USB and UART interfaces.
- USB UICC is supported using a FS USB 2-wire interface.
  - Two new pins have been added to the MSM6246 and MSM6290 devices.
  - The MSM6246 and MSM6290 devices contain a new pad (VDD_PAD4) for UICC. It is operated at 2.85 V (typical) or 1.8 V, depending on the card.
- Diagram of USB UICC:

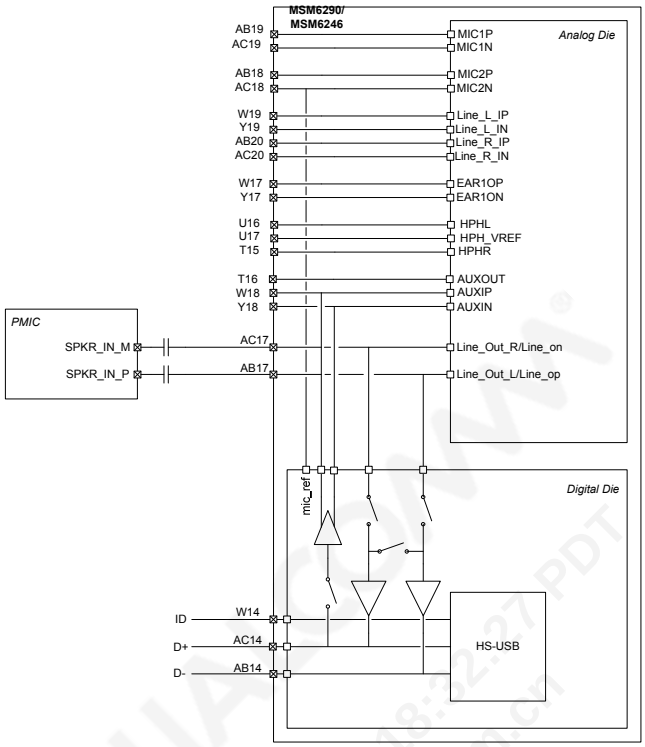


The USIM_MODE is needed to control the VDD_USIM to the connector, due to the stringent GCF timing requirements for VDD_USIM that are not satisfied by the VREG_USIM LDO on/off control.

Note: If the legacy USIM is used, the two USB UICC pins can be either connected to the USIM connector or left unconnected.

USB Audio

- The USB Audio routing scheme is shown below:



SDCC2

- A second secure digital card controller (SDCC2) port has been added to the MSM6246 and MSM6290 devices.
  - Supports SD memory card and SDIO WLAN simultaneously
- SDCC2 features are:
  - Supports the following specifications
    - » SD version 2.0
    - » SDIO version 2.0
    - » MMC version 4.2
  - Supports high-speed mode operations
  - GPIOs connected to the SDCC2 port are 3.0 V tolerant.
  - The board-level design for the SDCC2 block is the same as the primary SDCC block in the MSM6246 and MSM6290 devices.
  - 1-bit and 4-bit data modes are supported.
  - Pull-up resistors between 10 kΩ and 100 kΩ for SD, and between 50 kΩ and 100 kΩ for MMC, are required for DATA[3:0] and CMD signals. Internal pull-ups in the MSM™ device are insufficient.

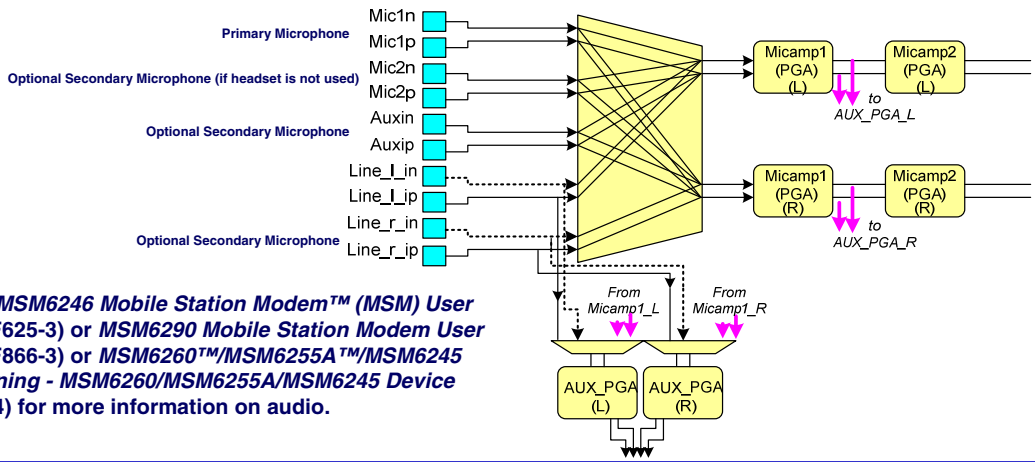
For voltage compatibility consideration and other details, refer to: *Application Note: MultiMediaCard/SD Card* (80-V7837-1).

Fast UART for BT2.0 and BT2.1 with EDR

- The UART1 data mover (UART1_DM) replaced the UART1 interface found in MSM6245 and MSM6280 devices.
- UART speeds:
  - UART1: high-speed, maximum of up to 4 Mbps using the UART1_DM data mover interface and up to 230 kbps for data services using the UART1 interface
  - UART2 maximum speed of 115 kbps – used for USB UICC or USIM
  - UART3 maximum speed of 115 kbps – MSM6290 device only
- The internal Bluetooth core that existed in the MSM6245 device and the MSM6280 device no longer exists on the MSM6246 and MSM6290 devices.
- External BT2.0/BT2.1 support is provided by the fast UART. Implementation of the data mover UART enabled the higher data rates required for BT2.0 and BT2.1.

Dual-Microphone Noise Cancellation

- Dual-microphone noise cancellation helps reduce unwanted noise and improves speech quality.
- Refer to *Application Note: Dual-Microphone Noise Cancellation Electro-Acoustical Design Guidelines* (80-VE797-11) for more details.
- The figure below shows all possible MSM audio inputs that can be used for dual-microphone noise cancellation:
  - The primary microphone and secondary microphone must be routed to separate internal ADC channels.
  - Keep in mind the differential LINE_L_IN can only be routed to the left-channel ADC and the differential LINE_R_IN can only be routed to the right-channel ADC.



Refer to the *MSM6246 Mobile Station Modem™ (MSM) User Guide* (80-VF625-3) or *MSM6290 Mobile Station Modem User Guide* (80-VF866-3) or *MSM6260™/MSM6255A™/MSM6245 Chipset Training - MSM6260/MSM6255A/MSM6245 Device* (80-VB322-24) for more information on audio.

HSUPA UE Categories (MSM6290 Device Only)

E-DCH Category	Max number of E-DPDCH channels	Minimum SF	Supported TTI	Peak rate for TTI = 10 ms*	Peak rate for TTI = 2 ms
Category 1	1	SF 4	10 ms	711 kbps	--
Category 2	2	SF 4	2 & 10 ms	1448 kbps	1448 kbps
Category 3	**2**	**SF 4**	**10 ms**	**1448 kbps**	**--**
Category 4	2	SF 2	2 & 10 ms	2000 kbps	2886 kbps
Category 5	**2**	**SF2**	**10 ms**	**2000 kbps**	**--**
Category 6	4	SF2 + SF 4	2 & 10 ms	2000 kbps	5742 kbps

Max peak data rate for 10 ms E-DCH TTI is 2 Mbps.

Max peak data rate for 2 ms E-DCH TTI is 5.742 Mbps.

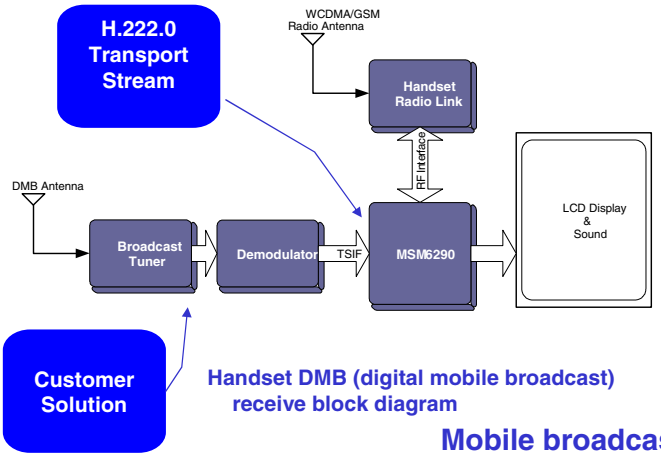
MSM6290 initial CS release only support 10 ms TTI.

2 ms TTI will be added in the later CS release, estimated max data rate for MSM6290 device is 4.5 Mbps.

TSIF Topics (MSM6290 Device Only)

- TSIF and mobile broadcast standards
- MPEG system diagram
- TSIF block diagram
- TSIF features
- Mode 1 signaling
- Mode 2 signaling
- UBM (MBP1600/MBP1610 device)

TSIF and Mobile Broadcast Standards



Handset DMB (digital mobile broadcast) receive block diagram

The handset's mobile broadcast implementation (see figure on left) that uses a separate, non-WCDMA radio link has its own antenna.

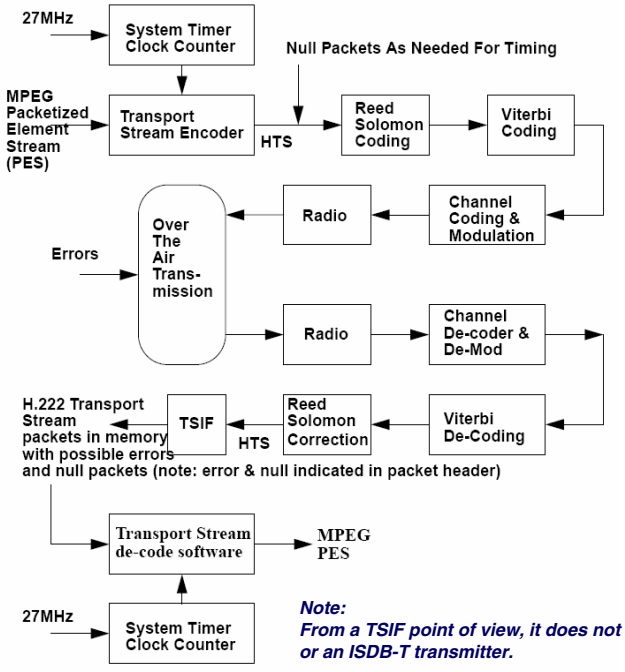
Depending on the standard used, the broadcast module may or may not output H.222.0 MPEG2 transport stream packets that the MSM6290 device supports.

TS interface in MSM6290 IC *ONLY* supports transport of TS packets from the broadcast module to the MSM device. Most DVB-H modules only support the SDIO interface, which requires the OEM to provide its own driver. QUALCOMM MBP1600 device supports DVB-H through EBI2.

Mobile broadcast standard

Standard	Region	Technology and mode	RF Bandwidth	Band	Comments
ISDB-T **Integrated Service Digital Broadcasting - Terrestrial transmission (ARIB STD-B31)**	Japan	OFDM	6 MHz or 6/13 MHz	UHF	Typical ISDB-T modules use TSIF. BTS (band segmented transmission) Only one segment is supported.
S-DMB **Satellite - Digital Mobile Broadcast (ARIB STB-B41)**	Korea	4XWCDMA	25 MHz	S-Band (2.6 GHz)	Typical S-DMB modules use TSIF.
DVB-H **Digital Video Broadcast -Handheld**	US/Europe	COFDM	5,6, 7, 8 MHz	UHF/VHF	Typical DVB-H modules do not support TSIF. DVB-H modules usually support SDIO output. The QUALCOMM MBP1600 supports DVB-H through EBI2.

MPEG System Diagram

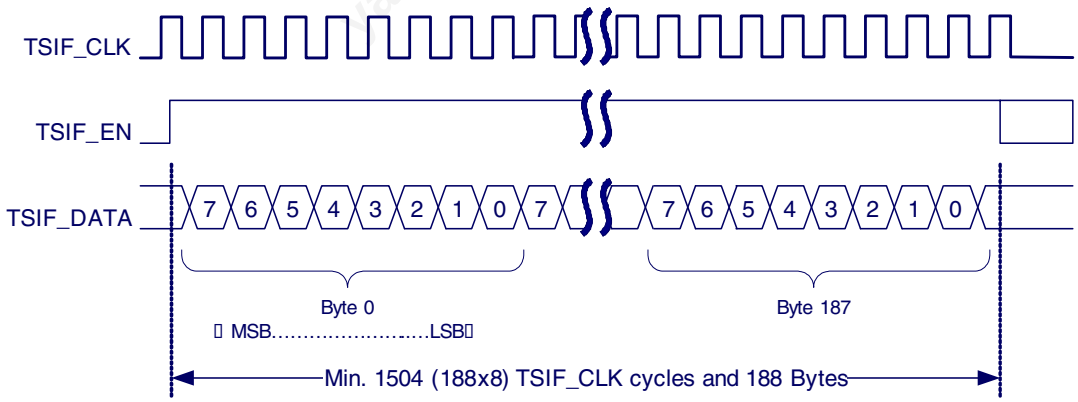


Note:
From a TSIF point of view, it does not matter if it is a DVB-H or a S-DMB or an ISDB-T transmitter.

MSM TSIF Features

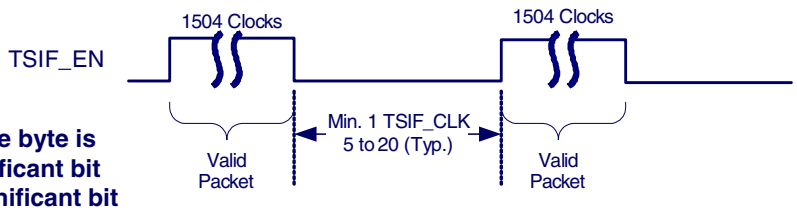
- 3 or 6-pin serial interface (3 required and 3 optional)
  - TSIF_CLK, TSIF_EN, TSIF_DATA are required.
  - TSIF_SYNC, TSIF_ERROR, TSIF_NULL are optional.
- Supports external clocks up to 4 MHz with a maximum data rate of 0.5 MB per second
- The data mover (DM) transfers *ITU-T H.222.0 Transport Stream* (HTS) packets directly from the external interface to system memory using TSIF.
- Enhanced fallback and/or debug support using a software-based copy mechanism when HTS packets are transferred directly from the external interface to system memory using TSIF
- Reports the status of each HTS packet transferred to memory via the DM or software copy
- 4 bytes of additional information (time stamp and flags) are provided with every HTS packet.
  - TSIF time stamp (TTS) is based upon a 27 MHz TSIF clock reference (TCR).
- Optional interrupts for critical events: loss-of-sync, packet available, and packet overflow

TSIF Mode 1 Signaling



Note: (1) TSIF_EN input can be programmed as "active low" or "active high" signal.
(2) TSIF_EN and TSIF_DATA are sampled on either rising or falling TSIF_CLK edge.

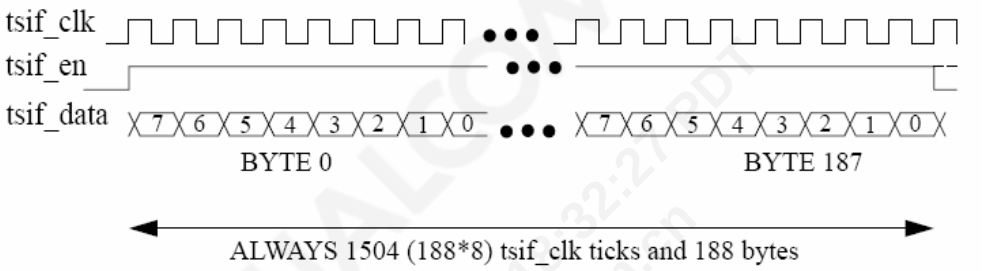
TSIF Packet Timing



Bit order within the byte is always most significant bit (MSB) to least significant bit (LSB), as illustrated.

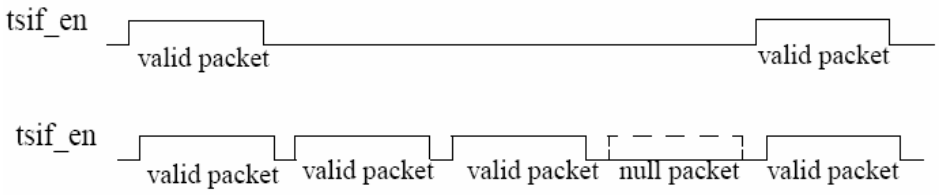
Mode 1 Details (1 of 2)

- This mode is composed of three signals – TSIF_CLK, TSIF_EN and TSIF_Data.
- The *tsif_clk* frequency depends on DMB format (ISDB-T, S-DMB, etc.).
- The “ALWAYS” statement in the figure designates one packet.
- Once asserted, as indicated by a low-to-high transition, *tsif_en* must remain asserted for at least 1504 ticks, but may extend longer.
- For most DMB applications, *tsif_en* will de-assert after 1504 ticks, but this is not required under this mode. The data captured under this 1504 tick assertion is called a *valid packet*. The low-to-high transition of *tsif_en* serves as a *new-packet-indicator*.
- After the external hardware interface (EHI) has been enabled, the receipt of the first valid packet is associated with a *first-packet-flag*. This flag tells the processing resource that the associated packet is the first of a series. Should the EHI enter an error condition of some kind which results in the loss of one or more packets, then this flag is set again to indicate the start of a new series.



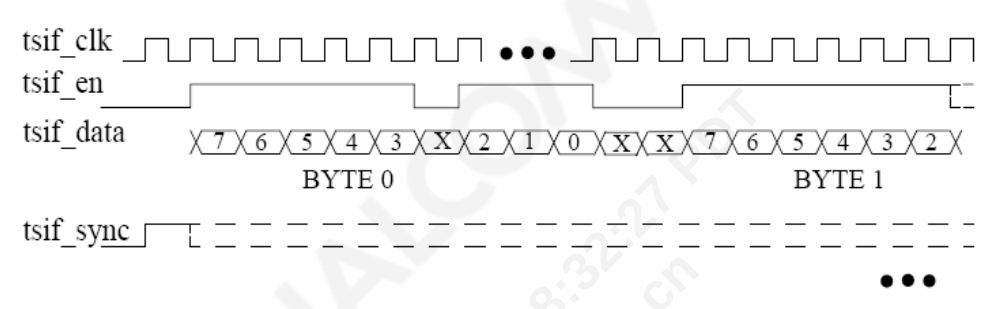
Mode 1 Details (2 of 2)

- One possible error condition is for *tsif_en* to assert and then de-assert in less than 1504 ticks. In this case, all data captured under this “short” *tsif_en* is discarded and a *loss-of-sync* error is recorded.
- An optional *time-limit* may be employed that is started each time a *valid-packet* is captured. If the *time-limit* expires before a new *valid-packet* is received, then a *timeout* error is recorded.
- Under this mode, the time between *tsif_en* assertions or *valid packets* is always at least one clock tick, but is generally on the order of 5 to 20 ticks depending on the DMB. However, it can conceptually be much longer, as illustrated. The only required behavior is that a low-to-high transition of *tsif_en* is followed by 1504 ticks of a high *tsif_en*. Furthermore, one additional tick is needed after tsif_en is de-asserted. Thus, a total of 1505 ticks is required.



TSIF Mode 2 Signaling

- This mode is composed of four signals as illustrated.
- Under this mode, the signal *tsif_sync* provides the *new-packet-indicator* function, and *tsif_en* is a free-format signal that may assert or de-assert on any clock period. Only the low-to-high transition of *tsif_sync* is needed to generate the *new-packet-indicator*. The length of time it is asserted is a “don’t care.”
- The signal *tsif_en* may be high or low at the *new-packet-indicator*. Conceptually, it could be tied high and a 1504-bit valid packet would be captured at each *new-packet-indicator*.
- The only requirement is that *tsif_en* be high, at least 1504 ticks between assertions of *tsif_sync*. If not, then a *lost-sync* error occurs. The previously presented *time-limit* and *first-packet-flag* concepts also apply.



Universal Broadcast Modem™ (UBM™)

- QUALCOMM Universal Broadcast Modem (UBM) chip provides a single-chip solution for the world's leading mobile broadcast standards. By combining digital and RF functionality into a single package, the UBM chip is a size and cost-efficient solution. The QUALCOMM UBM chipset family includes:
  - MBP1600 - supports wideband MediaFLO, DVB-H, and ISDB-T
  - MBP1610 - supports MediaFLO in US
- These chipsets are a single-chip solution that includes RF and baseband processing. They are MSM-companion ICs that provide broadcast receive-only tuning, demodulation, and decoding capabilities.
- There are two MBP/MSM interfaces: the MSM device’s EBI2 and the transport stream interface (TSIF). The MSM device’s ARM always configures the MBP via EBI2. The interface that is used for physical-layer data transport from the MBP1600 device to the MSM device depends upon the broadcast standard being supported:
  - MediaFLO uses EBI2 only.
  - ISDB-T uses TSIF for data and EBI2 for control.
  - DVB-H uses EBI2 for control and by default for data.
    - » Option of using TSIF for Program Specific Information/Service Information (PSI/SI) control packet (not implemented by QCT).
- The MediaFLO, DVB-H, and ISDB-T software protocol stacks (including video decoding and processing) are all handled within the MSM device.
- Refer to the MBP1600/MBP1610 documents for further information.

MSM6246 Device Memory Map

- The MSM6246 devices support only trusted boot.
- In trusted boot, the MSM6246 device boots from its internal boot ROM located at 0xFFFF0000.
- Memory supported on EBI1:
  - 32-bit SDRAM (low-power SDRAM)
  - CS0 and CS2 are the only chip selects available on EBI1.
- Memory supported on EBI2:
  - 8/16-bit NAND (512 byte, 2 kbyte/page)
  - Two chip selects
- A minimum of 32 MB SDRAM + 32 MB NAND for data cards is recommended.
- A minimum of 64 MB SDRAM + 64 MB NAND for handsets is recommended.

Memory block	Base address	Size (MB)
BOOT MODE=1 (NAND)		
XMEM1_CS_N[2]	0x00000000	128
RESERVED	0x08000000	N/A
XMEM1_CS_N[0]	0x10000000	128
RESERVED	0x18000000	N/A
LCD_CS_N	0x20000000	128
XMEM2_CS_N[0]	0x28000000	128
XMEM2_CS_N[1]	0x30000000	128
XMEM2_CS_N[2]	0x38000000	128
XMEM2_CS_N[3]	0x40000000	128
UART_DM	0x48000000	128
SDCC1	0x50000000	128
NAND	0x60000000	128
MOT_EST	0x68000000	128
ADSP	0x70000000	128
IMEM	0x78000000	128
MSM CORE	0x80000000	128
RESERVED	0x88000000	N/A
MODEM	0x90000000	128
HDLC (high data link control)	0x98000000	128
CRYPTO	0xA0000000	128
GRAPHICS	0xA8000000	128
RESERVED	0x88000000	N/A
SDCC2	0XB8000000	128
RESERVED	0XC0000000	N/A

MSM6290 Device Memory Map

- The MSM6290 devices support only trusted boot.
- In trusted boot, the MSM6290 device boots from its internal boot ROM located at 0xFFFF0000.
- Memory supported on EBI1:
  - 32-bit SDRAM (low-power SDRAM)
- Memory supported on EBI2:
  - 8/16-bit NAND (512 byte, 2 Kbyte/page)
  - Two chip selects
- A minimum of 32 MB SDRAM + 32 MB NAND for data cards is recommended.
- A minimum of 128 MB SDRAM + 64 MB NAND for handsets is recommended.

Memory block	Base address	Size (MB)
BOOT MODE=1 (NAND)		
XMEM1_CS_N[2]	0x00000000	128
XMEM1_CS_N [3]	0x08000000	128
XMEM1_CS_N[0]	0x10000000	128
XMEM1_CS_N[1]	0x18000000	128
LCD_CS_N	0x20000000	128
XMEM2_CS_N[0]	0x28000000	128
XMEM2_CS_N[1]	0x30000000	128
XMEM2_CS_N[2]	0x38000000	128
XMEM2_CS_N[3]	0x40000000	128
UART_DM	0x48000000	128
SDCC1	0x50000000	128
NAND	0x60000000	128
MOT_EST	0x68000000	128
ADSP	0x70000000	128
IMEM	0x78000000	128
MSM CORE	0x80000000	128
TSIF	0x88000000	128
MODEM	0x90000000	128
HDLC (high data link control)	0x98000000	128
CRYPTO	0xA0000000	128
GRAPHICS	0xA8000000	128
RESERVED	0xB0000000	128
SDCC2	0XB8000000	128
RESERVED	0XC0000000	256

Pin Removal on MSM6246 IC (from MSM6245 IC)

- A number of pins have been removed from the MSM6246 device in comparison to the MSM6245 device. The following is a list of those pins and pin functionalities. There are 105 functional GPIOs on the MSM6245 device compared to the 94 functional GPIOs on the MSM6246 device.

Removed pins	Comments
MDDIH_DATP, MDDIH_DATN, MDDIH_STBP, MDDIH_STBN	MDDI host interface has been removed from MSM6246 device.
MDDIC_DATP, MDDIC_DATN, MDDIC_STBP, MDDIC_STBN	MDDI client interface has been removed from MSM6246 device.
EBI1_CS_N[1], EBI1_CS_N[3]	GPIO77 and GPIO76 have been removed from MSM6246 device; the MSM6246 device will use only two EBI1 chip selects.
A2[20], A2[19], A2[18], A2[17]	A2[20:17] have been removed from the MSM6246 device.
GPIO84, GPIO85, GPIO86, GPIO87 (UART3/UIM2 interface)	UART3 has been removed from the MSM6246 device.
GPIO64 (UART1_RI/ETM_PIPESTAT2)	UART1_RI has been removed and ETM_PIPESTAT2 has been moved to GPIO94.
GPIO39 (UART1_DCD/KEYSENSE_IRQ_SRC)	UART1_DCD has been removed and KEYSENSE_IRQ_SRC has been moved to GPIO102.
GPIO92 (SYNTH0)	Not connected on MSM6246 device – UBM is not supported.
GPIO17	Not connected on MSM6246 device
GPIO104 (MDP_VSYNC_SECONDARY)	MDP_VSYNC_SECONDARY has been moved to GPIO19.
GPIO1	Not connected

MSM6246 IC and MSM6290 IC Differences

- The following table lists the interface feature differences and GPIO differences between the MSM6246 and MSM6290 devices. There are 107 functional GPIOs on the MSM6290 device compared to the 94 functional GPIOs on the MSM6246 device.

Feature	MSM6290	MSM6246
MDDI	Supported behind dedicated MDDI host and client pins	No support for MDDI – only parallel LCD and camera; no dedicated MDDI pins
Broadcast interface	TSIF supported behind GPIOs[87:85] UBM supported behind GPIOs[1], [17], [92], [39], or [64]	No support for TSIF/UBM. GPIOs[87:85] and GPIO[1] have been removed.
UART3	UART3 supported behind GPIOs[87:84]	No support for UART3. These GPIOs have been removed.
EBI1 chip selects	4 CS are supported on EBI1.	EBI1_CS_N[1], EBI1_CS_N[3] behind GPIO[77] and GPIO [76] are not supported – these pins are not connected.
A2[20], A2[19], A2[18], A2[17]	A2[20:0] supported. A2[20] is behind GPIO[34].	A2[20:17] pins are not connected.
GPIO[64]	UART1_RI/ETM_PIPESTAT2	UART1_RI has been removed and ETM_PIPESTAT2 has been moved to GPIO[94].
GPIO[39]	UART1_DCD/KEYSENSE_IRQ_SRC	UART1_DCD has been removed and KEYSENSE_IRQ_SRC has been moved to GPIO[102].
GPIO[104]	MDP_VSYNC_SECONDARY	MDP_VSYNC_SECONDARY has been moved to GPIO[19]; GPIO[104] has been removed.
Receive Diversity	Supported on Platform F – Rx diversity pins are behind GPIO[7] (DRX_MODE_SELECT_C), GPIO[41] (DRX_MODE_SELECT_A), and GPIO[65] (DRX_MODE_SELECT_B).	Rx diversity is not supported for handsets on Platform F for MSM6246 device. The Rx diversity GPIOs are unused GPIOs. Note that Rx diversity is available for data cards.

For a list of all MSM6290 and MSM6246 features, see slides 9-12.

MSM6246 and MSM6290 ES Limitations (1 of 3)

- **USB IN packet CRC error**
  - **Description:**
    - » In peripheral mode with the primary USB core, for all IN end points (EP), a CRC error may occur if the buffer length divided by 512 (EP buffer size) has a residue of 1 or 2 bytes (e.g. 1, 2, 513, 514, etc.).
  - **System impact:**
    - » Having a CRC error will cause a retransmission of the data, which will have an impact on performance. Another (worse) case is having three CRC errors in a row that will cause the link to drop. The failure can appear in several ways, but the most common is a simple CRC error in the short packets.
  - **Workaround:**
    - » A SW workaround for the modem and software download via QPST™ software will be included in AMSS 1.0 USB driver and PC host driver; the QUALCOMM composite driver version 2.0.4.2. The second SW release, QUALCOMM composite driver version 1.0.2.1, will include a workaround for RMNet (network), which will be available at a later date. The native window driver does not have the workaround.
    - » This issue has been identified and will be fixed in a future MSM revision.

MSM6246 and MSM6290 ES Limitations (2 of 3)

- **HS-USB leakage**
  - **Description:**
    - » There is a leakage path inside the MSM device if VDDA_USB2P6 (2.6 V) is turned off, which will cause higher-than-expected leakage current in the HS-USB core.
  - **System impact:**
    - » When VDDA_USB2P6 (2.6 V) is turned off, maximum leakage current from the VREG_MSMC domain of the PHY could be as high as ~100 µA. Since VDDA_USB2P6 is shared with VREG_MSMA, and VREG_MSMA is always on, there is no system impact.
  - **Workaround:**
    - » To prevent high leakage current, VDDA_USB2P6 (2.6 V) must be turned on at all times.
    - » This issue will be fixed in a future MSM revision.

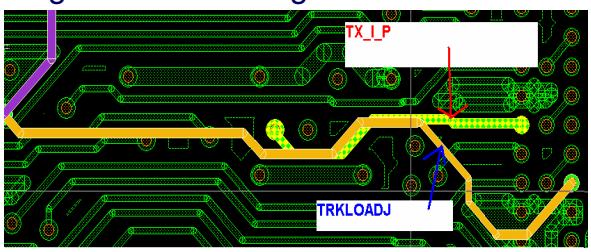
MSM6246 and MSM6290 ES Limitations (3 of 3)

- **MIC1 and MIC2 pin swap**
  - **Description:**
    - » The MIC1N and MIC1P pins were swapped with the MIC2N and MIC2P pins.
  - **System impact:**
    - » There is no system impact caused by this issue.
  - **Workaround:**
    - » A software workaround is available that corrects the pin reversal. The workaround is implemented in the current version of AMSS software.
    - » The MIC1 and MIC2 pin reversal will be fixed in a future MSM revision.

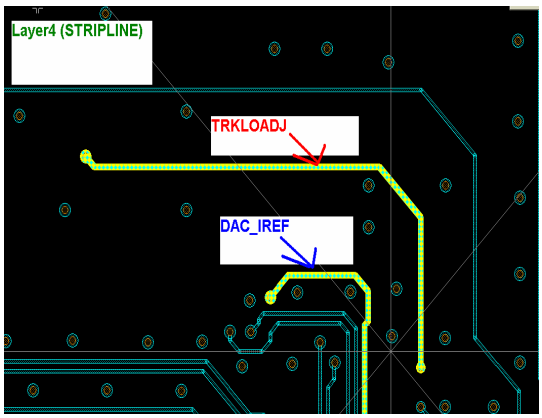
Special Board-layout Considerations

- 9.6 MHz spurs were seen on MSM6246 and MSM6290 design due to proximity of DAC_REF and Q_OUT pin. Special separation is required to minimize the spurs in order to pass the ACLR spec.
  - **Description**
    - » Digital noise coupled into the TX_I/Q or DAC_IREF line could cause the spurs seen at RF freq.
  - **Workaround**
    - » TRK_LO_ADJ, DAC_IREF, and other I/Q signals are spaced further apart and have more isolation.
  - **Result**
    - » Substantial isolation now exists between TRK_LO_ADJ, DAC_IREF, and all other I/Q signals, and spurs have been eliminated.

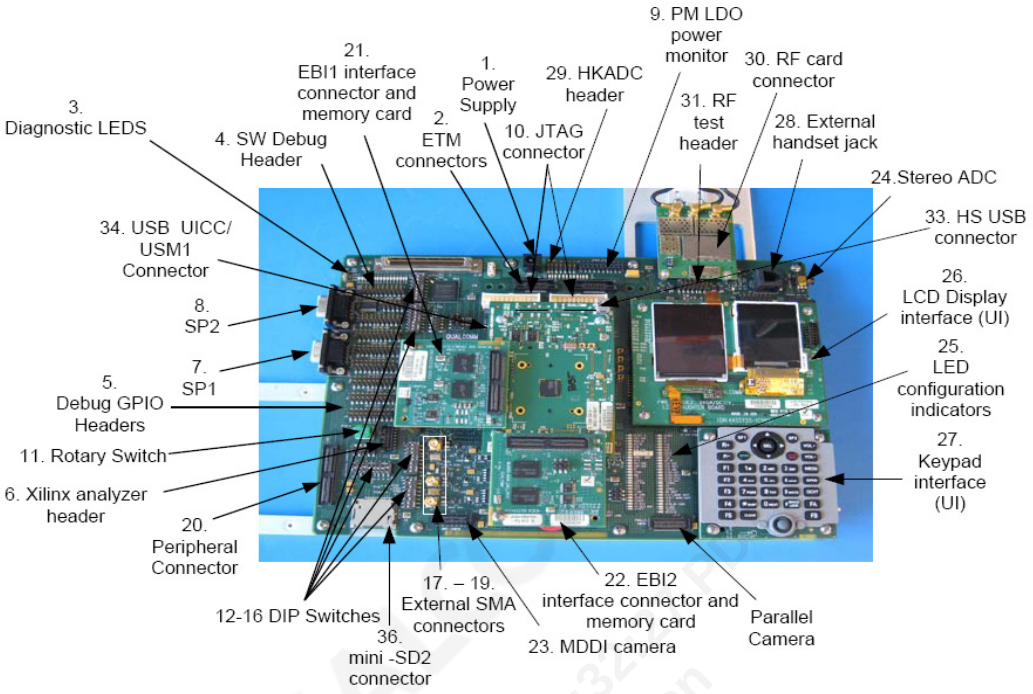
- Figure 1. Before signal isolation



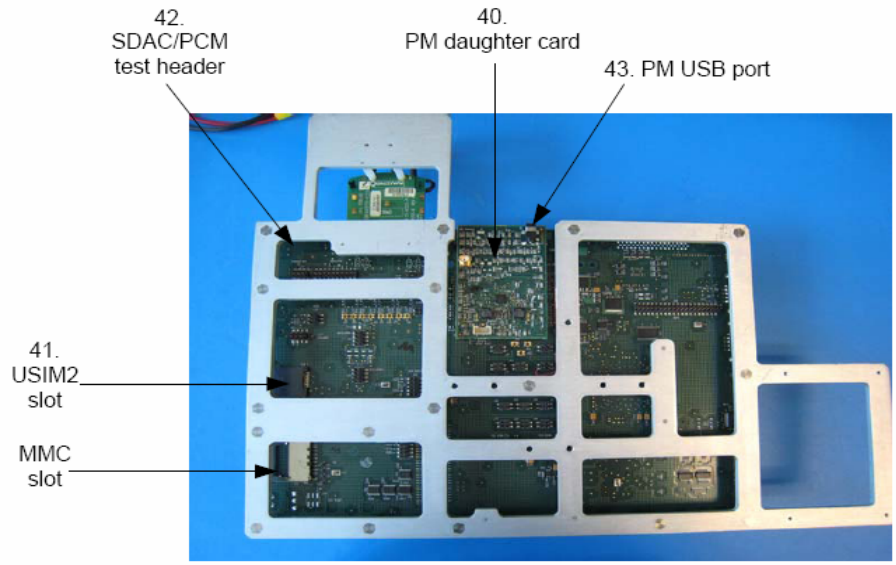
- Figure 2: After signal isolation:



SURF6246/SURF6290 Layout (Top)



SURF6246/SURF6290 Layout (Bottom)



SURF6246/SURF6290 Features

- MSM daughter card that contains the MSM6246 or MSM6290 devices
- Two external bus interfaces called EBI1 and EBI2 – memory devices are memory cards that are installed on the MSM daughter card and are connected directly to the MSM device.
- Two SURF boot modes: 8-bit or 16-bit NAND
- RFCMOS interface and RF evaluation software
- Parallel LCD for MSM6246/MSM6290 device; Serial MDDI LCD for MSM6290 device only
- Keypad
- Audio block that supports interfaces to a standard headset (RJ-11), stereo headset, and a speaker. It also supports external stereo SDAC, stereo ADC, and includes an onboard ringer.
- USIM, USB UICC, SD1, and SD2 storage devices
- HKADC block that provides monitoring and emulation of various analog signals
- Peripheral devices which include:
  - RS-232
  - Camera
  - USB
  - USB UICC
  - Bluetooth

Useful Documents

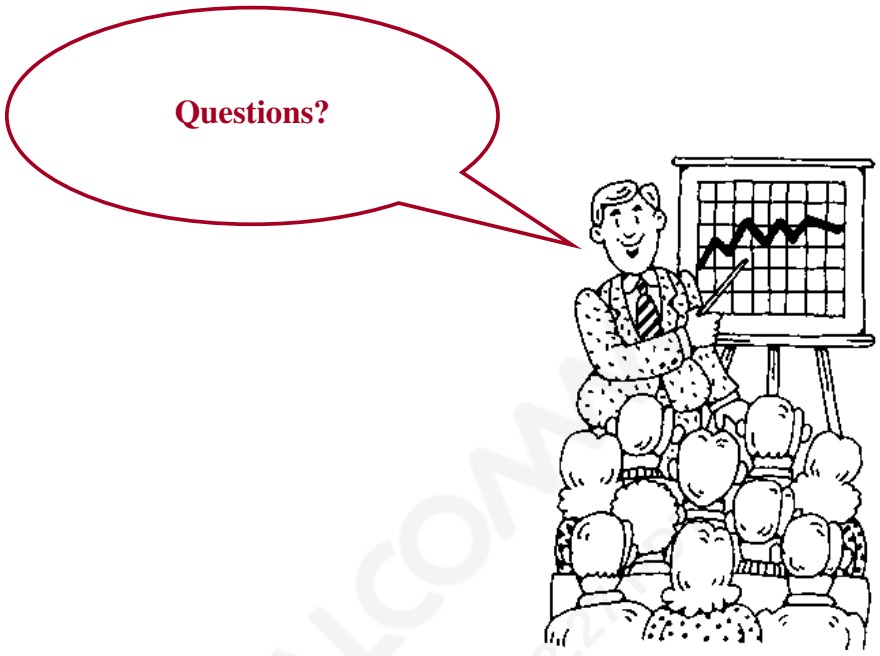
MSM6246 and MSM6290 Reference Documents

Document number	Document title
80-VF625-33	*SURF6246/SURF6290 Main Board Reference Schematic*
80-VF625-32	*SURF6246/SURF6290 Daughter Board Reference Schematic*
80-VF625-31	*SURF6246/SURF6290 Platform User Guide*
80-VF625-41	*MSM6246 Baseband for RF Platform F/G Reference Schematic*
80-VF866-41	*MSM6290 Baseband for RF Platform F/G Reference Schematic*

MSM6246 and MSM6290 Chipset Documents

Document number	Document title
80-VF625-1	*MSM6246 Mobile Station Modem Device Specification*
80-VF625-2	*MSM6246 Mobile Station Modem Software Interface*
80-VF625-3	*MSM6246 Mobile Station Modem User Guide*
80-VF866-1	*MSM6290 Mobile Station Modem Device Specification*
80-VF866-2	*MSM6290 Mobile Station Modem Software Interface*
80-VF866-3	*MSM6290 Mobile Station Modem User Guide*
80-VD203-1	*PM6658 Power Management IC Device Specification*
80-VD203-3	*PM6658 Power Management IC User Guide*
80-VD202-1	*PM6653 Power Management IC Device Specification*
80-VD202-3	*PM6653 Power Management IC User Guide*
80-VD861-1	*RTR6285/RTR6280 RF Transceiver Device Specification*
80-VD861-3	*RTR6285/RTR6280 RF Transceiver User Guide*
80-VF551-1	*Nano Scale Package FAQs*
80-VF625-12	*Application Note: MSM6290 and MSM6246 Device Comparison Guide*

Questions?



- **Service requests:**
  https://support.cdmatech.com