EMMA Mobile EV2

Multimedia Processor for Mobile Applications

R19DS0010EJ0700
Rev.7.00
May 31, 2011

DESCRIPTION

EMMA MobileTM EV (EM/EV) is an application processor for mobile multimedia handset devices. EM/EV2 utilizes two ARM® Cortex-A9 cores with two Neon extensions, an integrated audio video engine (AV engine), and a 3D graphics block to enable high-class processing in a range of applications. The processor contains a wide variety of interfaces for cameras, displays, mass storage devices, memory devices, and many other peripherals.
EM/EV achieves high-performance multimedia processing of up to HD-level decoding by means of hardware acceleration, while consuming minimal power..

FEATURES

- CPU: ARM Cortex-A9 (Frequency: 533 MHz, I-cache: 32 KB, D-cache: 32 KB, L2 cache : 256KB)
- AV engine: High-performance multimedia processor
  - Video:
    - Decoder: Multi decoder (H.264, VC-1, MPEG 1/2, H.263, MPEG-4: up to 1080p 30fps), other decoders/encoders may be implemented by software using CPU resources
  - Audio:
    - Decoder: MPEG-4 HE-AAC decoder, enhanced aacPlus decoder
- 3D Graphics accelerator (A3D)
  - 3D: 14.7 Mpix/sec
    Supporting Open-GL-ES2.0, OpenGL-ES1.x
- Image processor: Resizing, rotating, image composing with alpha blending and key color masking
- Image composer: Image composing with alpha blending and key color masking, gamma correction
  - Direct connection to LCD interface
- Security functions: Secure boot function, secure timer, secure watchdog timer, secure DMA
- Internal memories: SRAM: 128 KB, ROM: 64 KB
- DMA controller: 8 channels
- Timers: Interval timers and watchdog timers: 15 channels
- DRAM interface:
  - LPDDR-SDRAM interface: Max 200 MHz DDR (DDR400), 32 bits, up to 1.6 GB/s
  - DDR2-SDRAM interface: Max 266 MHz DDR (DDR533), 32 bits, up to 2.1 GB/s
- NOR-Flash interface: 16-bit data bus
- Peripheral interfaces:
  - Memory card interface: SD card (with CPRM × 1, SDIO × 3, CF card interface
  - Image interfaces:
    - LCD interface → Parallel interface
    - ITU-R BT.656 interface
    - Camera interface → Parallel interface
  - Other serial interfaces:
    - USB 2.0 host or peripheral × 1 and peripheral × 1 (with PHY)
    - UART × 4
    - I2C × 2
    - Unified serial interface × 6 (SPI, I2S)

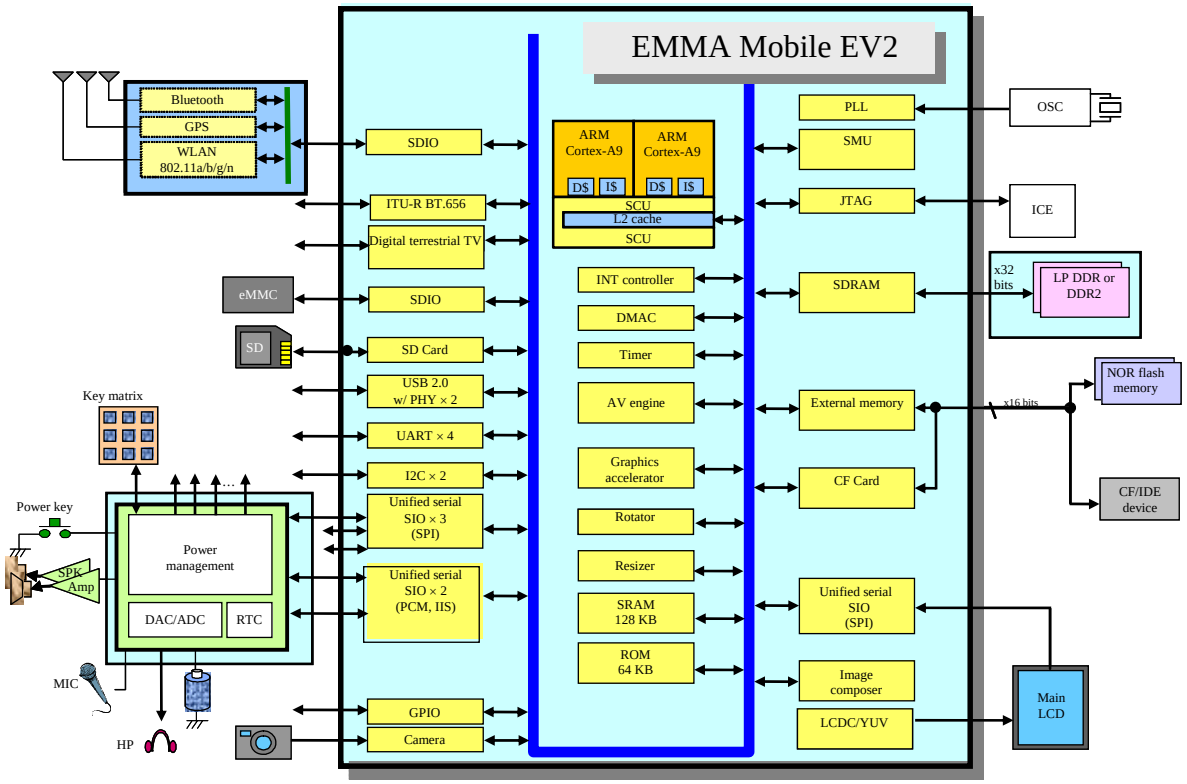
  - General-purpose I/O port interface × 159
- Testing and debugging: ARM CoreSight, JTAG

- Power supply voltage
  - Core Logic: 1.1V to 1.2 V
  - PLL: 1.1 V to 1.2V
  - IO power supply: 1.8 V, 3.3 V
- Power management
  Several power saving operation modes are supported.
- Package
  393-pin FPBGA package (16 × 16 mm), ball pitch: 0.65 mm

Order Information

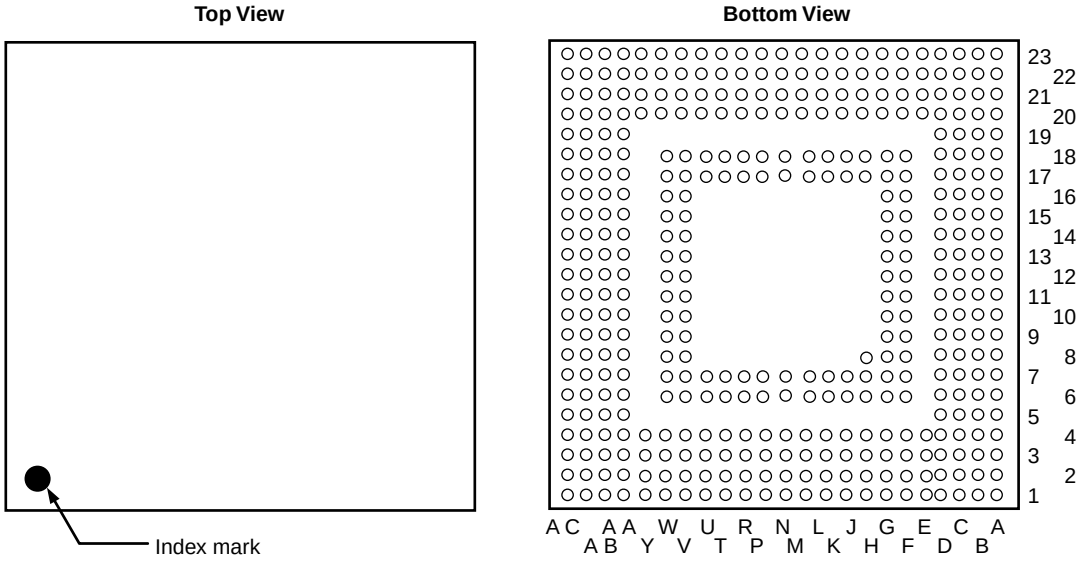
Part No.	Package Type
μPD77642BF1-GA9-A	393pin FPBGA (16mm×16mm, 0.65mm pitch)

BLOCK DIAGRAM



PIN LAYOUT

393-pin FPBGA (16×16mm, 0.65mm pitch)



PIN ASSIGNMENT

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Pin No.	Pin Name
A1	GND
A2	GND
A3	VDD33D
A4	AVDD
A5	C32K
A6	GND
A7	GND
A8	OSC0_XT2
A9	OSC0_XT1
A10	GND
A11	JT_TCK
A12	LOWPWR
A13	PONDET
A14	GND
A15	LCD3_B1
A16	LCD3_B0
A17	LCD3_G1
A18	LCD3_G0
A19	LCD3_R2
A20	LCD3_R0
A21	LCD3_CLK_I
A22	GND
A23	GND
B1	GND
B2	GND
B3	AFS_ARSTB
B4	AVDD
B5	GND
B6	USI0_CLK
B7	USI0_CS0
B8	USI0_CS1
B9	USI0_CS2
B10	USI0_DI
B11	USI0_DO
B12	SRESETB
B13	VDD18
B14	LCD3_B5
B15	LCD3_B2
B16	LCD3_G5

Pin No.	Pin Name
B17	LCD3_G2
B18	LCD3_R5
B19	LCD3_R3
B20	LCD3_R1
B21	LCD3_HS
B22	LCD3_PXCLK
B23	GND
C1	DDR_DQ7
C2	DDR_DQ0
C3	DDR_DQ2
C4	AGND
C5	NECTESTIO
C6	UTEST (When being unused, ”L” is fixed.)
C7	GND
C8	GND
C9	USI1_CLK
C10	USI1_DI
C11	JT_TRSTB
C12	NC (leave open)
C13	JT_TDI
C14	LCD3_B6
C15	LCD3_B3
C16	LCD3_G6
C17	LCD3_G3
C18	LCD3_R6
C19	LCD3_R4
C20	LCD3_VS
C21	GPIO_019
C22	AB_AD1
C23	AB_AD0
D1	DDR_DM0
D2	DDR_DQ4
D3	DDR_DQ6
D4	DDR_DQ1
D5	AGND
D6	TE1
D7	TE2
D8	GND
D9	GND

Pin No.	Pin Name
D10	USI1_DO
D11	USI1_CS0
D12	JT_DBG_EN
D13	JT_TDO
D14	LCD3_B7
D15	LCD3_B4
D16	LCD3_G7
D17	LCD3_G4
D18	LCD3_R7
D19	LCD3_DE
D20	GPIO_024
D21	AB_CSB0
D22	AB_AD3
D23	AB_AD2
E1	DDR_DQS0
E2	DDR_DQS0B
E3	DDR_DQ3
E4	DDR_DQ5
E20	GPIO_025
E21	AB_CSB1
E22	AB_AD5
E23	AB_AD4
F1	DDR_DQS1
F2	DDR_DQS1B
F3	DDR_GND
F4	DDR_VREFL
F6	DDR_VDDIO
F7	VDD33
F8	TRSTB
F9	VDD11
F10	VDD11
F11	BOOTSEL2
F12	BOOTSEL0
F13	JT_TDOEN
F14	JT_TMS
F15	VDD18
F16	GPIO_026
F17	GPIO_027
F18	GPIO_028

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
F20	AB_CSB2	H20	AB_WRB	L17	AB_A27
F21	AB_AD8	H21	AB_AD14	L18	AB_A24
F22	AB_AD7	H22	AB_AD13	L20	AB_WAIT
F23	AB_AD6	H23	AB_AD12	L21	AB_A19
G1	DDR_DQ11	J1	DDR_A0	L22	HSI_ACREADY Note1
G2	DDR_DQ8	J2	DDR_A2	L23	HSI_CAFLAG Note1
G3	DDR_DM1	J3	DDR_GND	M1	DDR_CK
G4	DDR_DQ9	J4	DDR_DQ14	M2	DDR_CKB
G6	VDD11	J6	DDR_CS1B	M3	DDR_GND
G7	GND	J7	VDD11	M4	DDR_WEB
G8	VDD18	J17	VDD11	M6	DDR_ODT Note2
G9	GND	J18	GPIO_031	M7	GND
G10	GND	J20	AB_RDB	M17	AB_A28
G11	BOOTSEL1	J21	AB_A17	M18	AB_A25
G12	VDD33M	J22	AB_AD15	M20	AB_A22
G13	VDD11	J23	AB_CLK	M21	AB_A20
G14	GND	K1	DDR_BA2	M22	HSI_CAREADY Note1
G15	VDD33	K2	DDR_BA0	M23	HSI_ACFLAG Note1
G16	VDD11	K3	DDR_A3	N1	DDR_CKE1
G17	GND	K4	DDR_A10	N2	DDR_GND
G18	GPIO_029	K6	DDR_CASB	N3	DDR_A11
G20	AB_CSB3	K7	DDR_VDDIO	N4	DDR_A13
G21	AB_AD11	K17	VDD33	N6	DDR_CKERSTB
G22	AB_AD10	K18	VDD11	N7	DDR_VDDIO
G23	AB_AD9	K20	AB_ADV	N17	VDD18
H1	DDR_DQ12	K21	AB_A18	N18	AB_A26
H2	DDR_DQ15	K22	HSI_CAWAKE Note1	N20	AB_A23
H3	DDR_DQ13	K23	HSI_CADATA Note1	N21	AB_A21
H4	DDR_DQ10	L1	DDR_CKE0	N22	HSI_ACWAKE Note1
H6	DDR_VDDIO	L2	DDR_A14	N23	HSI_ACDATA Note1
H7	GND	L3	DDR_A1	P1	DDR_A12
H8	GND	L4	DDR_BA1	P2	DDR_A7
H17	VDD33	L6	DDR_RASB	P3	DDR_A8
H18	GPIO_030	L7	DDR_CS0B	P4	DDR_A6

Note1 The HSI function is not available.

Note2 The on die termination function for DDR-ODT is not available.

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
P6	VDD11	U11	GND	Y1	DDR_DM3
P7	GND	U12	GND	Y2	DDR_DQ27
P17	VDD11	U13	VDD11	Y3	DDR_DQ25
P18	NTSC_DATA1	U14	VDD33	Y4	DDR_DQ29
P20	NTSC_DATA0	U15	VDD33	Y5	PWM1
P21	GND	U16	GND	Y6	USI2_CS2
P22	IC	U17	VDD18	Y7	USI2_CS0
P23	IC	U18	NTSC_DATA7	Y8	IIC1_SDA
R1	DDR_A9	U20	NTSC_DATA6	Y9	IIC1_SCL
R2	DDR_A5	U21	CAM_YUV3	Y10	UART1_TX
R3	DDR_A4	U22	CAM_YUV4	Y11	UART1_RX
R4	DDR_DQ20	U23	CAM_YUV5	Y12	SDI0_CMD
R6	DDR_VDDIO	V1	DDR_DQS2	Y13	SDI0_DATA1
R7	GND	V2	DDR_DQS2B	Y14	SDI0_DATA3
R17	VDD33	V3	DDR_GND	Y15	SDI0_DATA5
R18	NTSC_DATA3	V4	DDR_VREFH	Y16	SDI0_DATA7
R20	NTSC_DATA2	V6	VDD18	Y17	SD_DATA2
R21	GND	V7	VDD33M	Y18	SD_DATA0
R22	IC	V8	GPIO_004	Y19	GPIO_015
R23	IC	V9	GPIO_002	Y20	GPIO_014
T1	DDR_DQ16	V10	GPIO_000	Y21	GPIO_013
T2	DDR_DQ17	V11	VDD18	Y22	GND
T3	DDR_DQ22	V12	UART0_TX	Y23	CAM_CLKI
T4	DDR_DQ19	V13	UART0_RX	AA1	DDR_DQ24
T6	DDR_VDDIO	V14	VDD11	AA2	DDR_DQ28
T7	GND	V15	GPIO_009	AA3	DDR_DQ26
T17	VDD11	V16	GPIO_008	AA4	PWM0
T18	NTSC_DATA5	V17	GPIO_007	AA5	USI2_DO
T20	NTSC_DATA4	V18	GPIO_006	AA6	USI2_DI
T21	CAM_YUV0	V20	NTSC_CLK	AA7	USI2_CS1
T22	CAM_YUV1	V21	CAM_HS	AA8	IIC0_SDA
T23	CAM_YUV2	V22	CAM_YUV6	AA9	IIC0_SCL
U1	DDR_DQ21	V23	CAM_YUV7	AA10	UART1_CTSB
U2	DDR_DQ18	W1	DDR_DQS3	AA11	USB_GND11
U3	DDR_DQ23	W2	DDR_DQS3B	AA12	USB_VBUS
U4	DDR_DM2	W3	DDR_DQ31	AA13	SDI0_DATA0
U6	VDD11	W4	DDR_DQ30	AA14	SDI0_DATA2
U7	GND	W20	GPIO_017	AA15	SDI0_DATA4
U8	GPIO_005	W21	GPIO_016	AA16	SDI0_DATA6
U9	GPIO_003	W22	CAM_VS	AA17	SD_DATA3
U10	GPIO_001	W23	CAM_CLKO	AA18	SD_DATA1

Remark IC : Internally-connected pins (pull it down)

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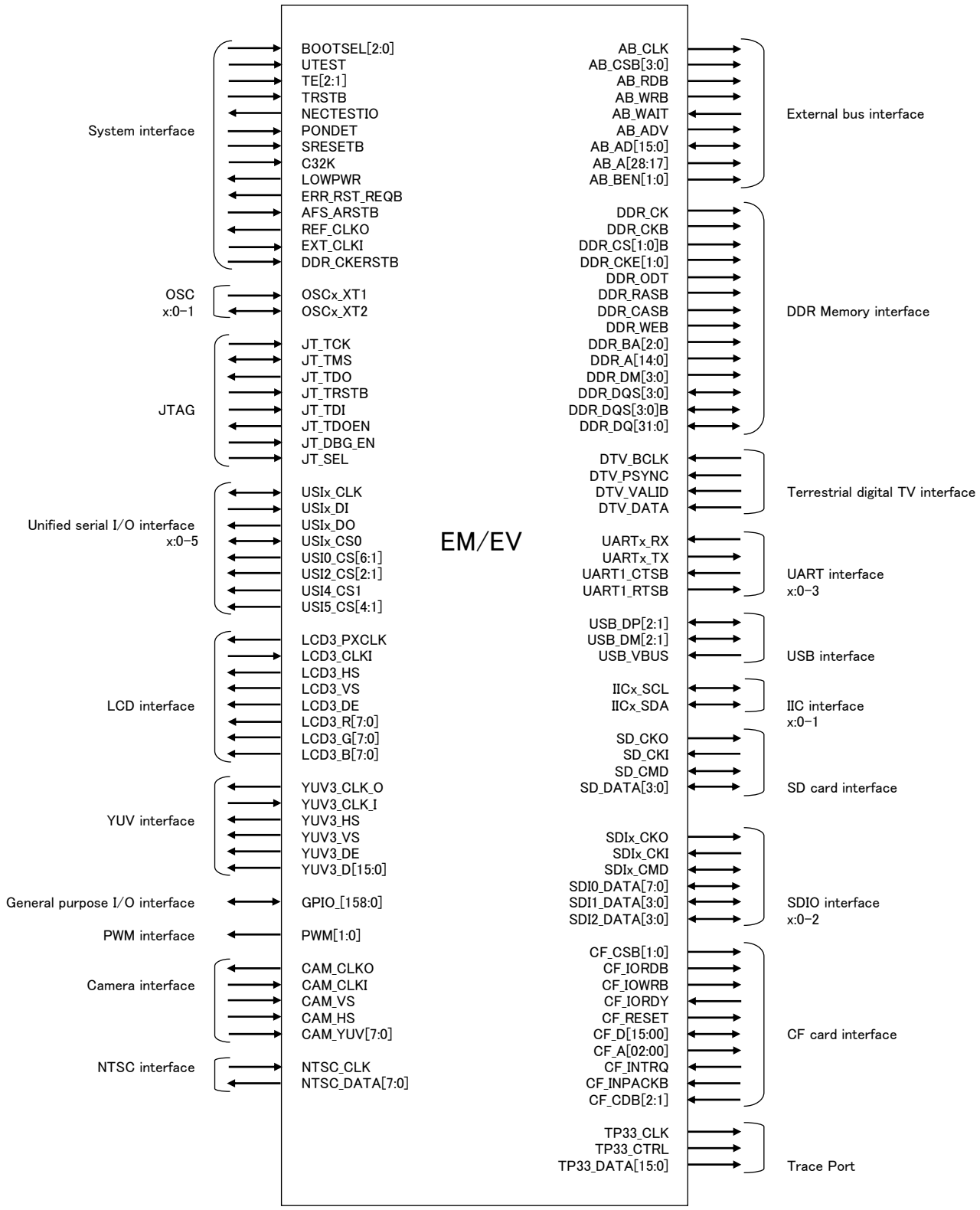
Pin No.	Pin Name
AA19	SDI1_DATA3
AA20	GPIO_012
AA21	GPIO_011
AA22	GPIO_010
AA23	SDI1_CKI
AB1	GND
AB2	GND
AB3	GPIO_119
AB4	USI3_CS0
AB5	USI2_CLK
AB6	USB_AVSS2
AB7	USB_PVSS2
AB8	USB_VD3312
AB9	USB_DP2
AB10	UART1_RTSB
AB11	USB_AVDD1
AB12	USB_AVSS1
AB13	USB_DP1
AB14	USB_VD3311
AB15	GND
AB16	GPIO_049
AB17	SD_CMD
AB18	SDI0_CKO
AB19	SDI1_DATA2
AB20	SDI1_DATA1
AB21	SDI1_DATA0
AB22	SDI1_CKO
AB23	GND
AC1	GND
AC2	GND
AC3	USI3_DO
AC4	USI3_DI
AC5	USI3_CLK
AC6	USB_AVDD2
AC7	USB_RREF2
AC8	USB_GND12
AC9	USB_DM2

Pin No.	Pin Name
AC10	USB_GND22
AC11	USB_RREF1
AC12	USB_PVSS1
AC13	USB_DM1
AC14	USB_GND21
AC15	OSC1_XT1
AC16	OSC1_XT2
AC17	GND
AC18	SDI0_CKI
AC19	SD_CKI
AC20	SD_CKO
AC21	SDI1_CMD
AC22	GND
AC23	GND

CONTENTS

1. PIN FUNCTIONS

1.1 Pin Configuration



1.2 Pin Functions

1.2.1 Boot select signals (VDD18)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
BOOTSEL2	F11	Input	Boot mode selection 2	–	A
BOOTSEL1	G11	Input	Boot mode selection 1	–	A
BOOTSEL0	F12	Input	Boot mode selection 0	–	A

1.2.2 System control signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
UTEST Note4	C6	Input	Test	–	A
TE1	D6	Input	Test	–	N
TE2	D7	Input	Test	–	O
TRSTB	F8	Input	Test	–	C
NECTESTIO Note1	C5	Output	Test	–	–
PONDET	A13	Input	Power-on reset	–	M
SRESETB	B12	Input	System reset	–	D
C32K Note3	A5	Input	32.768 kHz clock	–	A
ERR_RST_REQB	U9	Output	Error reset request	*GPIO_003*	L
LOWPWR	A12	Output	Low power control signal	GPIO_154	E
AFS_ARSTB	B3	Input	Antifuse asynchronous reset	–	A
REF_CLKO Note2	V8	Output	Reference clock input	*GPIO_004*	L
EXT_CLKI NOTE2	U8	Input	Reference clock output	*GPIO_005*	L
DDR_CKERSTB	N6	Input	Clock reset input	–	U.

Note1 VDD33

Note2 VDD18/VDD33

Note3 input : schmitt

Note4 When being unused, ”L” is fixed.

1.2.3 OSC signals (VDD18)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
OSC0_XT1	A9	Input	OSC input	–	P
OSC0_XT2	A8	I/O	OSC output	–	P
OSC1_XT1	AC15	Input	OSC input	–	P
OSC1_XT2	AC16	I/O	OSC output	–	P

1.2.4 JTAG signals (VDD18, VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
JT_TCK	A11	Input	JTAG clock input	–	C
JT_TRSTB	C11	Input	JTAG reset input	–	C
JT_TMS	F14	I/O	JTAG test mode	–	B
JT_TDI	C13	Input	JTAG data input	–	B
JT_TDO	D13	Output	JTAG data output	GPIO_151	E
JT_TDOEN	F13	Output	JTAG data output enable	GPIO_152	E
JT_DBG_EN	D12	Input	JTAG debug enable	–	C
JT_SEL NOTE	V9	Input	JTAG select	GPIO_002	L

Note1 VDD18/VDD33

1.2.5 External memory interface signals (VDD33)

(1/2)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
AB_AD15	J22	I/O	Address/data bus bit 15	SDI2_DATA3, CF_D15, *GPIO_092*	G
AB_AD14	H21	I/O	Address/data bus bit 14	SDI2_DATA2, CF_D14, *GPIO_091*	G
AB_AD13	H22	I/O	Address/data bus bit 13	SDI2_DATA1, CF_D13, USI5_CS2, *GPIO_090*	G
AB_AD12	H23	I/O	Address/data bus bit 12	SDI2_DATA0, CF_D12, USI5_CS1, *GPIO_089*	G
AB_AD11	G21	I/O	Address/data bus bit 11	DTV_DATA, CF_D11, USI5_CS0, *GPIO_088*	G
AB_AD10	G22	I/O	Address/data bus bit 10	DTV_VALID, CF_D10, USI5_DO, *GPIO_087*	G
AB_AD9	G23	I/O	Address/data bus bit 9	DTV_PSYNC, CF_D09, USI5_DI, *GPIO_086*	G
AB_AD8	F21	I/O	Address/data bus bit 8	DTV_BCLK, CF_D08, USI5_CLK, *GPIO_085*	G
AB_AD7	F22	I/O	Address/data bus bit 7	CF_D07, *GPIO_084*	G
AB_AD6	F23	I/O	Address/data bus bit 6	CF_D06, *GPIO_083*	G
AB_AD5	E22	I/O	Address/data bus bit 5	CF_D05, *GPIO_082*	G
AB_AD4	E23	I/O	Address/data bus bit 4	CF_D04, *GPIO_081*	G
AB_AD3	D22	I/O	Address/data bus bit 3	CF_D03, *GPIO_080*	G
AB_AD2	D23	I/O	Address/data bus bit 2	CF_D02, *GPIO_079*	G
AB_AD1	C22	I/O	Address/data bus bit 1	CF_D01, *GPIO_078*	G
AB_AD0	C23	I/O	Address/data bus bit 0	CF_D00, *GPIO_077*	G
AB_A28	M17	Output	Address bus bit 26	AB_BEN1, *GPIO_104*	H
AB_A27	L17	Output	Address bus bit 26	AB_BEN0, *GPIO_103*	H
AB_A26	N18	Output	Address bus bit 26	CF_CDB2, *GPIO_102*	H
AB_A25	M18	Output	Address bus bit 25	CF_CDB1, *GPIO_101*	H
AB_A24	L18	Output	Address bus bit 24	CF_INPACKB, *GPIO_100*	H

(2/2)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
AB_A23	N20	Output	Address bus bit 23	SDI2_CMD, *GPIO_099*	H
AB_A22	M20	Output	Address bus bit 22	SDI2_CKI, *GPIO_098*	H
AB_A21	N21	Output	Address bus bit 21	SDI2_CKO, CF_INTRQ, *GPIO_097*	H
AB_A20	M21	Output	Address bus bit 20	*GPIO_096*	H
AB_A19	L21	Output	Address bus bit 19	CF_A02, *GPIO_095*	G
AB_A18	K21	Output	Address bus bit 18	CF_A01, *GPIO_094*	G
AB_A17	J21	Output	Address bus bit 17	CF_A00, *GPIO_093*	G
AB_RDB	J20	Output	Read strobe	CF_IORDB, *GPIO_073*	H
AB_WRB	H20	Output	Write strobe	CF_IOWRB, *GPIO_074*	H
AB_ADV	K20	Output	Address valid	CF_RESET, *GPIO_076*	H
AB_WAIT	L20	Input	Wait	CF_IORDY, *GPIO_075*	H
AB_CSB3	G20	Output	Chip select 3	CF_CSB1, *GPIO_072*	H
AB_CSB2	F20	Output	Chip select 2	CF_CSB0, *GPIO_071*	H
AB_CSB1	E21	Output	Chip select 1	*GPIO_070*	F
AB_CSB0	D21	Output	Chip select 0	*GPIO_069*	F
AB_CLK	J23	Output	Bus clock output	*GPIO_068*	G
AB_BEN1	M17	Output	Byte enable	*GPIO_104*	H
AB_BEN0	L17	Output	Byte enable	*GPIO_103*	H

1.2.6 SDRAM interface signals (VDD18)

(1/3)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
DDR_A14	L2	Output	Command/address bit 14	–	Q
DDR_A13	N4	Output	Command/address bit 13	–	Q
DDR_A12	P1	Output	Command/address bit 12	–	Q
DDR_A11	N3	Output	Command/address bit 11	–	Q
DDR_A10	K4	Output	Command/address bit 10	–	Q
DDR_A9	R1	Output	Command/address bit 9	–	Q
DDR_A8	P3	Output	Command/address bit 8	–	Q
DDR_A7	P2	Output	Command/address bit 7	–	Q
DDR_A6	P4	Output	Command/address bit 6	–	Q
DDR_A5	R2	Output	Command/address bit 5	–	Q
DDR_A4	R3	Output	Command/address bit 4	–	Q
DDR_A3	K3	Output	Command/address bit 3	–	Q
DDR_A2	J2	Output	Command/address bit 2	–	Q
DDR_A1	L3	Output	Command/address bit 1	–	Q
DDR_A0	J1	Output	Command/address bit 0	–	Q
DDR_CS0B	L7	Output	Chip select 0	–	Q
DDR_CS1B	J6	Output	Chip select 1	–	Q

(2/3)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
DDR_CK	M1	Output	Clock +	–	R
DDR_CKB	M2	Output	Clock –	–	R
DDR_CKE0	L1	Output	Clock enable 0	–	Q
DDR_CKE1	N1	Output	Clock enable 1	–	Q
DDR_DM3	Y1	I/O	Data mask bit 3	–	S
DDR_DM2	U4	I/O	Data mask bit 2	–	S
DDR_DM1	G3	I/O	Data mask bit 1	–	S
DDR_DM0	D1	I/O	Data mask bit 0	–	S
DDR_DQ31	W3	I/O	Data bit 31	–	S
DDR_DQ30	W4	I/O	Data bit 30	–	S
DDR_DQ29	Y4	I/O	Data bit 29	–	S
DDR_DQ28	AA2	I/O	Data bit 28	–	S
DDR_DQ27	Y2	I/O	Data bit 27	–	S
DDR_DQ26	AA3	I/O	Data bit 26	–	S
DDR_DQ25	Y3	I/O	Data bit 25	–	S
DDR_DQ24	AA1	I/O	Data bit 24	–	S
DDR_DQ23	U3	I/O	Data bit 23	–	S
DDR_DQ22	T3	I/O	Data bit 22	–	S
DDR_DQ21	U1	I/O	Data bit 21	–	S
DDR_DQ20	R4	I/O	Data bit 20	–	S
DDR_DQ19	T4	I/O	Data bit 19	–	S
DDR_DQ18	U2	I/O	Data bit 18	–	S
DDR_DQ17	T2	I/O	Data bit 17	–	S
DDR_DQ16	T1	I/O	Data bit 16	–	S
DDR_DQ15	H2	I/O	Data bit 15	–	S
DDR_DQ14	J4	I/O	Data bit 14	–	S
DDR_DQ13	H3	I/O	Data bit 13	–	S
DDR_DQ12	H1	I/O	Data bit 12	–	S
DDR_DQ11	G1	I/O	Data bit 11	–	S
DDR_DQ10	H4	I/O	Data bit 10	–	S
DDR_DQ9	G4	I/O	Data bit 9	–	S
DDR_DQ8	G2	I/O	Data bit 8	–	S
DDR_DQ7	C1	I/O	Data bit 7	–	S
DDR_DQ6	D3	I/O	Data bit 6	–	S
DDR_DQ5	E4	I/O	Data bit 5	–	S
DDR_DQ4	D2	I/O	Data bit 4	–	S
DDR_DQ3	E3	I/O	Data bit 3	–	S
DDR_DQ2	C3	I/O	Data bit 2	–	S
DDR_DQS3	W1	I/O	Data strobe bit 3 +	–	T
DDR_DQS3B	W2	I/O	Data strobe bit 3 –	–	T
DDR_DQS2	V1	I/O	Data strobe bit 2 +	–	T

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Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
DDR_DQS2B	V2	I/O	Data strobe bit 2 –	–	T
DDR_DQS1	F1	I/O	Data strobe bit 1 +	–	T
DDR_DQS1B	F2	I/O	Data strobe bit 1 –	–	T
DDR_DQS0	E1	I/O	Data strobe bit 0 +	–	T
DDR_DQS0B	E2	I/O	Data strobe bit 0 –	–	T
DDR_RASB	L6	Output	RAS	–	Q
DDR_CASB	K6	Output	CAS	–	Q
DDR_WEB	M4	Output	Write enable	–	Q
DDR_BA2	K1	Output	Bank address bit 2	–	Q
DDR_BA1	L4	Output	Bank address bit 1	–	Q
DDR_BA0	K2	Output	Bank address bit 0	–	Q
DDR_ODT Note	M6	Output	On-die termination	–	Q

Note : The on die termination function for DDR-ODT is not available.

1.2.7 Unified serial interface port 0 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
USI0_DI	B10	Input	Port 0 data input	–	L
USI0_DO	B11	Output	Port 0 data output	–	L
USI0_CLK	B6	I/O	Port 0 clock input/output	–	L
USI0_CS6	AB4	Output	Port 0 CS6	USI3_CS0, *GPIO_118*	L
USI0_CS5	AC3	Output	Port 0 CS5	USI3_DO, *GPIO_117*	L
USI0_CS4	AC4	Output	Port 0 CS4	USI3_DI, *GPIO_116*	L
USI0_CS3	AC5	Output	Port 0 CS3	USI3_CLK, *GPIO_115*	L
USI0_CS2	B9	Output	Port 0 CS2	*GPIO_106*	L
USI0_CS1	B8	Output	Port 0 CS1	*GPIO_105*	L
USI0_CS0	B7	I/O	Port 0 CS0	–	L

1.2.8 Unified serial interface port 1 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
USI1_DI	C10	Input	Port 1 data input	GPIO_107	J
USI1_DO	D10	Output	Port 1 data output	GPIO_108	J
USI1_CLK	C9	I/O	Port 1 clock input/output	–	J
USI1_CS0	D11	I/O	Port 1 CS0	–	J

1.2.9 Unified serial interface port 2 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
USI2_DI	AA6	Input	Port 2 data input	DTV_PSYNC, *GPIO_110*	L
USI2_DO	AA5	Output	Port 2 data output	DTV_VALID, *GPIO_111*	L
USI2_CLK	AB5	I/O	Port 2 clock input/output	DTV_BCLK, *GPIO_109*	L
USI2_CS2	Y6	Output	Port 2 CS2	USI4_CS1, *GPIO_114*	L
USI2_CS1	AA7	Output	Port 2 CS1	USI4_CS0, *GPIO_113*	L
USI2_CS0	Y7	I/O	Port 2 CS0	DTV_DATA, *GPIO_112*	L
USI2_DI	AA6	Input	Port 2 data input	DTV_PSYNC, *GPIO_110*	L

1.2.10 Unified serial interface port 3 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
USI3_DI	AC4	Input	Port 3 data input	USI0_CS4, *GPIO_116*	L
USI3_DO	AC3	Output	Port 3 data output	USI0_CS5, *GPIO_117*	L
USI3_CLK	AC5	I/O	Port 3 clock input/output	USI0_CS3, *GPIO_115*	L
USI3_CS0	AB4	I/O	Port 3 CS0	USI0_CS6, *GPIO_118*	L

1.2.11 Unified serial interface port 4 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
USI4_DI	AA4	Input	Port 4 data input	PWM0, *GPIO_120*	L
USI4_DO	Y5	Output	Port 4 data output	PWM1, *GPIO_121*	L
USI4_CLK	AB3	I/O	Port 4 clock input/output	*GPIO_119*	L
USI4_CS1	Y6	Output	Port 4 CS1	USI2_CS2, *GPIO_114*	L
USI4_CS0	AA7	I/O	Port 4 CS0	USI2_CS1, *GPIO_113*	L

1.2.12 Unified serial interface port 5 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
USI5_DI	G23 Note1	Input	Port 5 data input	AB_AD9, DTV_PSYNC, CF_D09, *GPIO_086*	G
	M22 Note2			*GPIO_150*	C
USI5_DO	G22 Note1	Output	Port 5 data output	AB_AD10, DTV_VALID, CF_D10, *GPIO_087*	G
	K23 Note2			*GPIO_144*	C
USI5_CLK	F21 Note1	I/O	Port 5 clock input/output	AB_AD8, DTV_BCLK, CF_D08, *GPIO_085*	G
	K22 Note2			*GPIO_143*	C
USI5_CS4	M23 Note2	Output	Port 5 CS4	*GPIO_149*	C
USI5_CS3	N23 Note2	Output	Port 5 CS3	*GPIO_148*	C
USI5_CS2	H22 Note1	Output	Port 5 CS2	AB_AD13, SDI2_DATA1, CF_D13, *GPIO_090*	G
	N22 Note2			*GPIO_147*	C
USI5_CS1	H23 Note1	Output	Port 5 CS1	AB_AD12, SDI2_DATA0, CF_D12, *GPIO_089*	G
	L22 Note2			*GPIO_146*	C
USI5_CS0	G21 Note1	I/O	Port 5 CS0	AB_AD11, DTV_DATA, CF_D11, *GPIO_088*	G
	L23 Note2			*GPIO_145*	C

Note1 VDD33

Note2 VDD18

1.2.13 Digital terrestrial TV interface signals (VDD33, VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
DTV_BCLK	F21 Note1	Input	DTV clock input	AB_AD8, CF_D08, USI5_CLK, *GPIO_085*	G
	AB5 Note2			*USI2_CLK*, GPIO_109	L
DTV_PSYNC	G23 Note1	Input	DTV sync.	AB_AD9, CF_D09, USI5_DI, *GPIO_086*	G
	AA6 Note2			*USI2_DI*, GPIO_110	L
DTV_VALID	G22 Note1	Input	DTV valid	AB_AD10, CF_D10, USI5_DO, *GPIO_087*	G
	AA5 Note2			*USI2_DO*, GPIO_111	L
DTV_DATA	G21 Note1	Input	DTV data input	AB_AD11, CF_D11, USI5_CS0, *GPIO_088*	G
	Y7 Note2			*USI2_CS0*, GPIO_112	L

1.2.14 UART interface port 0 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
UART0_RX	V13	Input	Port 0 SIN	–	J
UART0_TX	V12	Output	Port 0 SOUT	–	I

1.2.15 UART interface port 1 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
UART1_RX	Y11	Input	Port 1 SIN	*GPIO_155*	J
UART1_TX	Y10	Output	Port 1 SOUT	*GPIO_156*	K
UART1_RTSB	AB10	Output	Port 1 RTS	UART2_TX,*GPIO_158*	K
UART1_CTSB	AA10	Input	Port 1 CTS	UART2_RX,*GPIO_157*	J

1.2.16 UART interface port 2 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
UART2_RX	AA10	Input	Port 2 SIN	UART1_CTSB, *GPIO_157*	J
UART2_TX	AB10	Output	Port 2 SOUT	UART1_RTSB, *GPIO_158*	K

1.2.17 UART interface port 3 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
UART3_RX	Y9	Input	Port 3 SIN	*IIC1_SCL*, GPIO_046	K
UART3_TX	Y8	Output	Port 3 SOUT	*IIC1_SDA*, GPIO_047	K

1.2.18 USB interface port1 signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
USB_DP1	AB13	I/O	USB port1 data input/output	–	Note
USB_DM1	AC13	I/O	USB port 1data input/output	–	Note

Note : Refer to USB Specification Revision 2.0.

1.2.19 USB interface port2 signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
USB_DP2	AB9	I/O	USB port2 data input/output	–	Note
USB_DM2	AC9	I/O	USB port 2data input/output	–	Note
USB_VBUS	AA12	Input	USB VBUS	GPIO_153	H

Note : Refer to USB Specification Revision 2.0.

1.2.20 I2C interface port 0 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
IIC0_SCL	AA9	OT	IIC0 clock	GPIO_044	K
IIC0_SDA	AA8	OT	IIC0 data	GPIO_045	K

Remark OT: 3-state output

1.2.21 I2C interface port 1 signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
IIC1_SCL	Y9	OT	IIC0 clock	UART3_RX, GPIO_046	K
IIC1_SDA	Y8	OT	IIC0 data	UART3_TX, GPIO_047	K

Remark OT: 3-state output

1.2.22 LCD interface signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
LCD3_PXCLK	B22	Output	Pixel clock	YUV3_CLK_O, *GPIO_018*	G
LCD3_CLK_I	A21	Input	Clock input	YUV3_CLK_I, *GPIO_020*	G
LCD3_HS	B21	Output	H sync	YUV3_HS, *GPIO_021*	G
LCD3_VS	C20	Output	V sync	YUV3_VS, *GPIO_022*	G
LCD3_DE	D19	Output	Enable	YUV3_DE, *GPIO_023*	G
LCD3_R7	D18	Output	Red 7	TP33_CTRL, *GPIO_039*	G
LCD3_R6	C18	Output	Red 6	TP33_CLK, *GPIO_038*	G
LCD3_R5	B18	Output	Red 5	*GPIO_037*	G
LCD3_R4	C19	Output	Red 4	*GPIO_036*	G
LCD3_R3	B19	Output	Red 3	*GPIO_035*	G
LCD3_R2	A19	Output	Red 2	*GPIO_034*	G
LCD3_R1	B20	Output	Red 1	*GPIO_033*	G
LCD3_R0	A20	Output	Red 0	*GPIO_032*	G
LCD3_G7	D16	Output	Green 7	YUV3_D7, TP33_DATA7	G
LCD3_G6	C16	Output	Green 6	YUV3_D6, TP33_DATA6	G
LCD3_G5	B16	Output	Green 5	YUV3_D5, TP33_DATA5	G
LCD3_G4	D17	Output	Green 4	YUV3_D4, TP33_DATA4	G
LCD3_G3	C17	Output	Green 3	YUV3_D3, TP33_DATA3	G
LCD3_G2	B17	Output	Green 2	YUV3_D2, TP33_DATA2	G
LCD3_G1	A17	Output	Green 1	YUV3_D1, TP33_DATA1, *GPIO_041*	G
LCD3_G0	A18	Output	Green 0	YUV3_D0, TP33_DATA0, *GPIO_040*	G
LCD3_B7	D14	Output	Blue 7	YUV3_D15, TP33_DATA15	G
LCD3_B6	C14	Output	Blue 6	YUV3_D14, TP33_DATA14	G
LCD3_B5	B14	Output	Blue 5	YUV3_D13, TP33_DATA13	G
LCD3_B4	D15	Output	Blue 4	YUV3_D12, TP33_DATA12	G
LCD3_B3	C15	Output	Blue 3	YUV3_D11, TP33_DATA11	G
LCD3_B2	B15	Output	Blue 2	YUV3_D10, TP33_DATA10	G
LCD3_B1	A15	Output	Blue 1	YUV3_D9, TP33_DATA9, *GPIO_043*	G
LCD3_B0	A16	Output	Blue 0	YUV3_D8, TP33_DATA8, *GPIO_042*	G

1.2.23 YUV interface signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
YUV3_D15	D14	Output	Data bit 15	*LCD3_B7*, TP33_DATA15	G
YUV3_D14	C14	Output	Data bit 14	*LCD3_B6*, TP33_DATA14	G
YUV3_D13	B14	Output	Data bit 13	*LCD3_B5*, TP33_DATA13	G
YUV3_D12	D15	Output	Data bit 12	*LCD3_B4*, TP33_DATA12	G
YUV3_D11	C15	Output	Data bit 11	*LCD3_B3*, TP33_DATA11	G
YUV3_D10	B15	Output	Data bit 10	*LCD3_B2*, TP33_DATA10	G
YUV3_D9	A15	Output	Data bit 9	LCD3_B1, TP33_DATA9, *GPIO_043*	G
YUV3_D8	A16	Output	Data bit 8	LCD3_B0, TP33_DATA8, *GPIO_042*	G
YUV3_D7	D16	Output	Data bit 7	*LCD3_G7*, TP33_DATA7	G
YUV3_D6	C16	Output	Data bit 6	*LCD3_G6*, TP33_DATA6	G
YUV3_D5	B16	Output	Data bit 5	*LCD3_G5*, TP33_DATA5	G
YUV3_D4	D17	Output	Data bit 4	*LCD3_G4*, TP33_DATA4	G
YUV3_D3	C17	Output	Data bit 3	*LCD3_G3*, TP33_DATA3	G
YUV3_D2	B17	Output	Data bit 2	*LCD3_G2*, TP33_DATA2	G
YUV3_D1	A17	Output	Data bit 1	LCD3_G1, TP33_DATA1, *GPIO_041*	G
YUV3_D0	A18	Output	Data bit 0	LCD3_G0, TP33_DATA0, *GPIO_040*	G
YUV3_CLK_O	B22	Output	Clock	LCD3_PXCLK, *GPIO_018*	G
YUV3_CLK_I	A21	Input	Clock	LCD3_CLK_I, *GPIO_020*	G
YUV3_HS	B21	Output	Hsync	LCD3_HS, *GPIO_021*	G
YUV3_VS	C20	Output	Vsync	LCD3_VS, *GPIO_022*	G
YUV3_DE	D19	Output	Enable	LCD3_DE, *GPIO_023*	G

1.2.24 SD card interface signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
SD_CKO	AC20	Output	SD card clock output	–	G
SD_CKI	AC19	Input	SD card clock input	GPIO_048	G
SD_CMD	AB17	I/O	SD card command	–	G
SD_DATA3	AA17	I/O	SD card data bit 3	–	G
SD_DATA2	Y17	I/O	SD card data bit 2	–	G
SD_DATA1	AA18	I/O	SD card data bit 1	–	G
SD_DATA0	Y18	I/O	SD card data bit 0	–	G

1.2.25 SDIO interface port 0 signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
SDI0_CMD	Y12	I/O	SDIO0 command	GPIO_052	G
SDI0_DATA7	Y16	I/O	SDIO0 data bit 7	*GPIO_060*	G
SDI0_DATA6	AA16	I/O	SDIO0 data bit 6	*GPIO_059*	G
SDI0_DATA5	Y15	I/O	SDIO0 data bit 5	*GPIO_058*	G
SDI0_DATA4	AA15	I/O	SDIO0 data bit 4	*GPIO_057*	G
SDI0_DATA3	Y14	I/O	SDIO0 data bit 3	GPIO_056	G
SDI0_DATA2	AA14	I/O	SDIO0 data bit 2	GPIO_055	G
SDI0_DATA1	Y13	I/O	SDIO0 data bit 1	GPIO_054	G
SDI0_DATA0	AA13	I/O	SDIO0 data bit 0	GPIO_053	G
SDI0_CKO	AB18	Output	SDIO0 clock output	*GPIO_050*	G
SDI0_CKI	AC18	Input	SDIO0 clock input	GPIO_051	G

1.2.26 SDIO interface port 1 signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
SDI1_CMD	AC21	I/O	SDIO1 CMD	GPIO_063	G
SDI1_DATA3	AA19	I/O	SDIO1 data bit 3	GPIO_067	G
SDI1_DATA2	AB19	I/O	SDIO1 data bit 2	GPIO_066	G
SDI1_DATA1	AB20	I/O	SDIO1 data bit 1	GPIO_065	G
SDI1_DATA0	AB21	I/O	SDIO1 data bit 0	GPIO_064	G
SDI1_CKO	AB22	Output	SDIO1 clock output	*GPIO_061*	G
SDI1_CKI	AA23	Input	SDIO1 clock input	GPIO_062	G

1.2.27 SDIO interface port 2 signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
SDI2_CMD	N20	I/O	SDIO2 command	AB_A23, *GPIO_099*	H
SDI2_DATA3	J22	I/O	SDIO2 data bit 3	AB_AD15, SDI2_DATA3, CF_D15, *GPIO_092*	G
SDI2_DATA2	H21	I/O	SDIO2 data bit 2	AB_AD14, SDI2_DATA2, CF_D14, *GPIO_091*	G
SDI2_DATA1	H22	I/O	SDIO2 data bit 1	AB_AD13, SDI2_DATA1, CF_D13, USI5_CS2, *GPIO_090*	G
SDI2_DATA0	H23	I/O	SDIO2 data bit 0	AB_AD12, SDI2_DATA0, CF_D12, USI5_CS1, *GPIO_089*	G
SDI2_CKO	N21	Output	SDIO2 clock output	AB_A21, CF_INTRQ, *GPIO_097*	H
SDI2_CKI	M20	Input	SDIO2 clock input	AB_A22, *GPIO_098*	H

1.2.28 CF card interface signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
CF_D15	J22	I/O	CF data bit 15	AB_AD15, SDI2_DATA3, *GPIO_092*	G
CF_D14	H21	I/O	CF data bit 14	AB_AD14, SDI2_DATA2, *GPIO_091*	G
CF_D13	H22	I/O	CF data bit 13	AB_AD13, SDI2_DATA1, USI5_CS2, *GPIO_090*	G
CF_D12	H23	I/O	CF data bit 12	AB_AD12, SDI2_DATA0, USI5_CS1, *GPIO_089*	G
CF_D11	G21	I/O	CF data bit 11	AB_AD11, DTV_DATA, USI5_CS0, *GPIO_088*	G
CF_D10	G22	I/O	CF data bit 10	AB_AD10, DTV_VALID, USI5_DO, *GPIO_087*	G
CF_D09	G23	I/O	CF data bit 9	AB_AD9, DTV_PSYNC, USI5_DI, *GPIO_086*	G
CF_D08	F21	I/O	CF data bit 8	AB_AD8, DTV_BCLK, USI5_CLK, *GPIO_085*	G
CF_D07	F22	I/O	CF data bit 7	AB_AD7, *GPIO_084*	G
CF_D06	F23	I/O	CF data bit 6	AB_AD6, *GPIO_083*	G
CF_D05	E22	I/O	CF data bit 5	AB_AD5, *GPIO_082*	G
CF_D04	E23	I/O	CF data bit 4	AB_AD4, *GPIO_081*	G
CF_D03	D22	I/O	CF data bit 3	AB_AD3, *GPIO_080*	G
CF_D02	D23	I/O	CF data bit 2	AB_AD2, *GPIO_079*	G
CF_D01	C22	I/O	CF data bit 1	AB_AD1, *GPIO_078*	G
CF_D00	C23	I/O	CF data bit 0	AB_AD0, *GPIO_077*	G
CF_CSB1	G20	Output	CF chip select 1	AB_CSB3, *GPIO_072*	H
CF_CSB0	F20	Output	CF chip select 0	AB_CSB2, *GPIO_071*	H
CF_RESET	K20	Output	CF reset output	AB_ADV, *GPIO_076*	H
CF_A02	L21	Output	CF address bit 2	AB_A19, *GPIO_095*	G
CF_A01	K21	Output	CF address bit 1	AB_A18, *GPIO_094*	G
CF_A00	J21	Output	CF address bit 0	AB_A17, *GPIO_093*	G
CF_IOWRB	H20	Output	CF write strobe	AB_WRB, *GPIO_074*	H
CF_IORDB	J20	Output	CF read strobe	AB_RDB, *GPIO_073*	H
CF_IORDY	L20	Input	CF I/O ready	AB_WAIT, *GPIO_075*	H
CF_INTRQ	N21	Input	CF INT request	AB_A21, SDI2_CKO, *GPIO_097*	H
CF_INPACKB	L18	Input		AB_A24, *GPIO_100*	H
CF_CDB1	M18	Input	CF card detection 1	AB_A25, *GPIO_101*	H
CF_CDB2	N18	Input	CF card detection 2	AB_A26, *GPIO_102*	H

1.2.29 GPIO interface signals (VDD18 / VDD33)

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Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
GPIO_158	AB10	I/O	General-purpose I/O	UART1_RTSB, UART2_TX	K
GPIO_157	AA10	I/O	General-purpose I/O	UART1_CTSB, UART2_RX	J
GPIO_156	Y10	I/O	General-purpose I/O	UART1_TX	K
GPIO_155	Y11	I/O	General-purpose I/O	UART1_RX	J
GPIO_154 NOTE1	A12	I/O	General-purpose I/O	*LOWPWR*	E
GPIO_153 NOTE2	AA12	I/O	General-purpose I/O	*USB_VBUS*	H
GPIO_152 NOTE1	F13	I/O	General-purpose I/O	*JT_TDOEN*	E
GPIO_151 NOTE1	D13	I/O	General-purpose I/O	*JT_TDO*	E
GPIO_150 NOTE1	M22	I/O	General-purpose I/O	USI5_DI	C
GPIO_149 NOTE1	M23	I/O	General-purpose I/O	USI5_CS4	C
GPIO_148 NOTE1	N23	I/O	General-purpose I/O	USI5_CS3	C
GPIO_147 NOTE1	N22	I/O	General-purpose I/O	USI5_CS2	C
GPIO_146 NOTE1	L22	I/O	General-purpose I/O	USI5_CS1	C
GPIO_145 NOTE1	L23	I/O	General-purpose I/O	USI5_CS0	C
GPIO_144 NOTE1	K23	I/O	General-purpose I/O	USI5_DO	C
GPIO_143 NOTE1	K22	I/O	General-purpose I/O	USI5_CLK	C
GPIO_142 NOTE2	V23	I/O	General-purpose I/O	CAM_YUV7	G
GPIO_141 NOTE2	V22	I/O	General-purpose I/O	CAM_YUV6	G
GPIO_140 NOTE2	U23	I/O	General-purpose I/O	CAM_YUV5	G
GPIO_139 NOTE2	U22	I/O	General-purpose I/O	CAM_YUV4	G
GPIO_138 NOTE2	U21	I/O	General-purpose I/O	CAM_YUV3	G
GPIO_137 NOTE2	T23	I/O	General-purpose I/O	CAM_YUV2	G
GPIO_136 NOTE2	T22	I/O	General-purpose I/O	CAM_YUV1	G
GPIO_135 NOTE2	T21	I/O	General-purpose I/O	CAM_YUV0	G
GPIO_134 NOTE2	V21	I/O	General-purpose I/O	CAM_HS	G
GPIO_133 NOTE2	W22	I/O	General-purpose I/O	CAM_VS	H
GPIO_132 NOTE2	Y23	I/O	General-purpose I/O	CAM_CLKI	H
GPIO_131 NOTE2	W23	I/O	General-purpose I/O	CAM_CLKO	G
GPIO_130 NOTE2	U18	I/O	General-purpose I/O	NTSC_DATA7	H
GPIO_129 NOTE2	U20	I/O	General-purpose I/O	NTSC_DATA6	H
GPIO_128 NOTE2	T18	I/O	General-purpose I/O	NTSC_DATA5	G
GPIO_127 NOTE2	T20	I/O	General-purpose I/O	NTSC_DATA4	G
GPIO_126 NOTE2	R18	I/O	General-purpose I/O	NTSC_DATA3	G
GPIO_125 NOTE2	R20	I/O	General-purpose I/O	NTSC_DATA2	G
GPIO_124 NOTE2	P18	I/O	General-purpose I/O	NTSC_DATA1	G
GPIO_123 NOTE2	P20	I/O	General-purpose I/O	NTSC_DATA0	G
GPIO_122 NOTE2	V20	I/O	General-purpose I/O	NTSC_CLK	G
GPIO_121	Y5	I/O	General-purpose I/O	PWM1, USI4_DO	L
GPIO_120	AA4	I/O	General-purpose I/O	PWM0, USI4_DI	L

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Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
GPIO_119	AB3	I/O	General-purpose I/O	USI4_CLK	L
GPIO_118	AB4	I/O	General-purpose I/O	USI3_CS0, USI0_CS6	L
GPIO_117	AC3	I/O	General-purpose I/O	USI3_DO, USI0_CS5	L
GPIO_116	AC4	I/O	General-purpose I/O	USI3_DI, USI0_CS4	L
GPIO_115	AC5	I/O	General-purpose I/O	USI3_CLK, USI0_CS3	L
GPIO_114	Y6	I/O	General-purpose I/O	USI2_CS2, USI4_CS1	L
GPIO_113	AA7	I/O	General-purpose I/O	USI2_CS1, USI4_CS0	L
GPIO_112	Y7	I/O	General-purpose I/O	*USI2_CS0*, DTV_DATA	L
GPIO_111	AA5	I/O	General-purpose I/O	*USI2_DO*, DTV_VALID	L
GPIO_110	AA6	I/O	General-purpose I/O	*USI2_DI*, DTV_PSYNC	L
GPIO_109	AB5	I/O	General-purpose I/O	*USI2_CLK*, DTV_BCLK	L
GPIO_108	D10	I/O	General-purpose I/O	*USI1_DO*	J
GPIO_107	C10	I/O	General-purpose I/O	*USI1_DI*	J
GPIO_106	B9	I/O	General-purpose I/O	USI0_CS2	L
GPIO_105	B8	I/O	General-purpose I/O	USI0_CS1	L
GPIO_104 NOTE2	M17	I/O	General-purpose I/O	AB_A28, AB_BEN1	H
GPIO_103 NOTE2	L17	I/O	General-purpose I/O	AB_A27, AB_BEN0	H
GPIO_102 NOTE2	N18	I/O	General-purpose I/O	AB_A26, CF_CDB2	H
GPIO_101 NOTE2	M18	I/O	General-purpose I/O	AB_A25, CF_CDB1	H
GPIO_100 NOTE2	L18	I/O	General-purpose I/O	AB_A24, CF_INPACKB	H
GPIO_099 NOTE2	N20	I/O	General-purpose I/O	AB_A23, SDI2_CMD	H
GPIO_098 NOTE2	M20	I/O	General-purpose I/O	AB_A22, SDI2_CKI	H
GPIO_097 NOTE2	N21	I/O	General-purpose I/O	AB_A21, SDI2_CKO, CF_INTRQ	H
GPIO_096 NOTE2	M21	I/O	General-purpose I/O	AB_A20	H
GPIO_095 NOTE2	L21	I/O	General-purpose I/O	AB_A19, CF_A02	G
GPIO_094 NOTE2	K21	I/O	General-purpose I/O	AB_A18, CF_A01	G
GPIO_093 NOTE2	J21	I/O	General-purpose I/O	AB_A17, CF_A00	G
GPIO_092 NOTE2	J22	I/O	General-purpose I/O	AB_AD15, SDI2_DATA3, CF_D15	G
GPIO_091 NOTE2	H21	I/O	General-purpose I/O	AB_AD14, SDI2_DATA2, CF_D14	G
GPIO_090 NOTE2	H22	I/O	General-purpose I/O	AB_AD13, SDI2_DATA1, CF_D13, USI5_CS2	G
GPIO_089 NOTE2	H23	I/O	General-purpose I/O	AB_AD12, SDI2_DATA0, CF_D12, USI5_CS1	G
GPIO_088 NOTE2	G21	I/O	General-purpose I/O	AB_AD11, DTV_DATA, CF_D11, USI5_CS0	G
GPIO_087 NOTE2	G22	I/O	General-purpose I/O	AB_AD10, DTV_VALID, CF_D10, USI5_DO	G
GPIO_086 NOTE2	G23	I/O	General-purpose I/O	AB_AD9, DTV_PSYNC, CF_D09, USI5_DI	G
GPIO_085 NOTE2	F21	I/O	General-purpose I/O	AB_AD8, DTV_BCLK, CF_D08, USI5_CLK	G
GPIO_084 NOTE2	F22	I/O	General-purpose I/O	AB_AD7, CF_D07	G

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Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
GPIO_083 NOTE2	F23	I/O	General-purpose I/O	AB_AD6, CF_D06	G
GPIO_082 NOTE2	E22	I/O	General-purpose I/O	AB_AD5, CF_D05	G
GPIO_081 NOTE2	E23	I/O	General-purpose I/O	AB_AD4, CF_D04	G
GPIO_080 NOTE2	D22	I/O	General-purpose I/O	AB_AD3, CF_D03	G
GPIO_079 NOTE2	D23	I/O	General-purpose I/O	AB_AD2, CF_D02	G
GPIO_078 NOTE2	C22	I/O	General-purpose I/O	AB_AD1, CF_D01	G
GPIO_077 NOTE2	C23	I/O	General-purpose I/O	AB_AD0, CF_D00	G
GPIO_076 NOTE2	K20	I/O	General-purpose I/O	AB_ADV, CF_RESET	H
GPIO_075 NOTE2	L20	I/O	General-purpose I/O	AB_WAIT, CF_IORDY	H
GPIO_074 NOTE2	H20	I/O	General-purpose I/O	AB_WRB, CF_IOWRB	H
GPIO_073 NOTE2	J20	I/O	General-purpose I/O	AB_RDB, CF_IORDB	H
GPIO_072 NOTE2	G20	I/O	General-purpose I/O	AB_CSB3, CF_CSB1	H
GPIO_071 NOTE2	F20	I/O	General-purpose I/O	AB_CSB2, CF_CSB0	H
GPIO_070 NOTE2	E21	I/O	General-purpose I/O	AB_CSB1	F
GPIO_069 NOTE2	D21	I/O	General-purpose I/O	AB_CSB0	F
GPIO_068 NOTE2	J23	I/O	General-purpose I/O	AB_CLK	G
GPIO_067 NOTE2	AA19	I/O	General-purpose I/O	*SDI1_DATA3*	G
GPIO_066 NOTE2	AB19	I/O	General-purpose I/O	*SDI1_DATA2*	G
GPIO_065 NOTE2	AB20	I/O	General-purpose I/O	*SDI1_DATA1*	G
GPIO_064 NOTE2	AB21	I/O	General-purpose I/O	*SDI1_DATA0*	G
GPIO_063 NOTE2	AC21	I/O	General-purpose I/O	*SDI1_CMD*	G
GPIO_062 NOTE2	AA23	I/O	General-purpose I/O	*SDI1_CKI*	G
GPIO_061 NOTE2	AB22	I/O	General-purpose I/O	SDI1_CKO	G
GPIO_060 NOTE2	Y16	I/O	General-purpose I/O	SDI0_DATA7	G
GPIO_059 NOTE2	AA16	I/O	General-purpose I/O	SDI0_DATA6	G
GPIO_058 NOTE2	Y15	I/O	General-purpose I/O	SDI0_DATA5	G
GPIO_057 NOTE2	AA15	I/O	General-purpose I/O	SDI0_DATA4	G
GPIO_056 NOTE2	Y14	I/O	General-purpose I/O	*SDI0_DATA3*	G
GPIO_055 NOTE2	AA14	I/O	General-purpose I/O	*SDI0_DATA2*	G
GPIO_054 NOTE2	Y13	I/O	General-purpose I/O	*SDI0_DATA1*	G
GPIO_053 NOTE2	AA13	I/O	General-purpose I/O	*SDI0_DATA0*	G
GPIO_052 NOTE2	Y12	I/O	General-purpose I/O	*SDI0_CMD*	G
GPIO_051 NOTE2	AC18	I/O	General-purpose I/O	*SDI0_CKI*	G
GPIO_050 NOTE2	AB18	I/O	General-purpose I/O	*SDI0_CKO*	G
GPIO_049 NOTE2	AB16	I/O	General-purpose I/O	–	G
GPIO_048 NOTE2	AC19	I/O	General-purpose I/O	*SD_CKI*	G
GPIO_047	Y8	I/O	General-purpose I/O	*IIC1_SDA*, UART3_TX	K
GPIO_046	Y9	I/O	General-purpose I/O	*IIC1_SCL*, UART3_RX	K
GPIO_045	AA8	I/O	General-purpose I/O	*IIC0_SDA*	K

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Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
GPIO_044	AA9	I/O	General-purpose I/O	*IIC0_SCL*	K
GPIO_043 NOTE2	A15	I/O	General-purpose I/O	LCD3_B1, YUV3_D9, TP33_DATA9	G
GPIO_042 NOTE2	A16	I/O	General-purpose I/O	LCD3_B0, YUV3_D8, TP33_DATA8	G
GPIO_041 NOTE2	A17	I/O	General-purpose I/O	LCD3_G1, YUV3_D1, TP33_DATA1	G
GPIO_040 NOTE2	A18	I/O	General-purpose I/O	LCD3_G0, YUV3_D0, TP33_DATA0	G
GPIO_039 NOTE2	D18	I/O	General-purpose I/O	LCD3_R7, TP33_CTRL	G
GPIO_038 NOTE2	C18	I/O	General-purpose I/O	LCD3_R6, TP33_CLK	G
GPIO_037 NOTE2	B18	I/O	General-purpose I/O	LCD_R5	G
GPIO_036 NOTE2	C19	I/O	General-purpose I/O	LCD_R4	G
GPIO_035 NOTE2	B19	I/O	General-purpose I/O	LCD_R3	G
GPIO_034 NOTE2	A19	I/O	General-purpose I/O	LCD_R2	G
GPIO_033 NOTE2	B20	I/O	General-purpose I/O	LCD_R1	G
GPIO_032 NOTE2	A20	I/O	General-purpose I/O	LCD_R0	G
GPIO_031 NOTE2	J18	I/O	General-purpose I/O	–	H
GPIO_030 NOTE2	H18	I/O	General-purpose I/O	–	H
GPIO_029 NOTE2	G18	I/O	General-purpose I/O	–	H
GPIO_028 NOTE2	F18	I/O	General-purpose I/O	–	H
GPIO_027 NOTE2	F17	I/O	General-purpose I/O	–	H
GPIO_026 NOTE2	F16	I/O	General-purpose I/O	–	G
GPIO_025 NOTE2	E20	I/O	General-purpose I/O	–	G
GPIO_024 NOTE2	D20	I/O	General-purpose I/O	–	G
GPIO_023 NOTE2	D19	I/O	General-purpose I/O	LCD3_DE, YUV3_DE	G
GPIO_022 NOTE2	C20	I/O	General-purpose I/O	LCD3_VS, YUV3_VS	G
GPIO_021 NOTE2	B21	I/O	General-purpose I/O	LCD3_HS, YUV3_HS	G
GPIO_020 NOTE2	A21	I/O	General-purpose I/O	LCD3_CLK_I, YUV3_CLK_I	G
GPIO_019 NOTE2	C21	I/O	General-purpose I/O	–	G
GPIO_018 NOTE2	B22	I/O	General-purpose I/O	LCD3_PXCLK, YUV3_CLK_O	G
GPIO_017 NOTE2	W20	I/O	General-purpose I/O	–	G
GPIO_016 NOTE2	W21	I/O	General-purpose I/O	–	G
GPIO_015 NOTE2	Y19	I/O	General-purpose I/O	–	G
GPIO_014 NOTE2	Y20	I/O	General-purpose I/O	–	G
GPIO_013 NOTE2	Y21	I/O	General-purpose I/O	–	G
GPIO_012 NOTE2	AA20	I/O	General-purpose I/O	–	H
GPIO_011 NOTE2	AA21	I/O	General-purpose I/O	–	H
GPIO_010 NOTE2	AA22	I/O	General-purpose I/O	–	G
GPIO_009 NOTE2	V15	I/O	General-purpose I/O	–	G
GPIO_008 NOTE2	V16	I/O	General-purpose I/O	–	H
GPIO_007 NOTE2	V17	I/O	General-purpose I/O	–	H

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Pin Name	Pin No.	IO Type	Function	Alternate Pin Function	Buffer Type
GPIO_006 NOTE2	V18	I/O	General-purpose I/O	–	G
GPIO_005	U8	I/O	General-purpose I/O	EXT_CLKI	L
GPIO_004	V8	I/O	General-purpose I/O	REF_CLKO	L
GPIO_003	U9	I/O	General-purpose I/O	–	L
GPIO_002	V9	I/O	General-purpose I/O	JT_SEL	L
GPIO_001	U10	I/O	General-purpose I/O	–	L
GPIO_000	V10	I/O	General-purpose I/O	–	L

Note1 VDD18

Note2 VDD33

1.2.30 PWM interface signals (VDD18 / VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
PWM0	AA4	Output	PWM output channel 0	USI4_DI, *GPIO_120*	L
PWM1	Y5	Output	PWM output channel 1	USI4_DO, *GPIO_121*	L

1.2.31 Camera interface signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
CAM_YUV7	V23	Input	Data bit 7	*GPIO_142*	G
CAM_YUV6	V22	Input	Data bit 6	*GPIO_141*	G
CAM_YUV5	U23	Input	Data bit 5	*GPIO_140*	G
CAM_YUV4	U22	Input	Data bit 4	*GPIO_139*	G
CAM_YUV3	U21	Input	Data bit 3	*GPIO_138*	G
CAM_YUV2	T23	Input	Data bit 2	*GPIO_137*	G
CAM_YUV1	T22	Input	Data bit 1	*GPIO_136*	G
CAM_YUV0	T21	Input	Data bit 0	*GPIO_135*	G
CAM_VS	W22	Input	Vertical sync.	*GPIO_133*	H
CAM_HS	V21	Input	Horizontal sync.	*GPIO_134*	G
CAM_CLKI	Y23	Input	Clock input	*GPIO_132*	H
CAM_CLKO	W23	Output	Clock output	*GPIO_131*	G

1.2.32 ITU-R BT.656 interface signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
NTSC_DATA7	U18	Output	Data bit 7	*GPIO_130*	H
NTSC_DATA6	U20	Output	Data bit 6	*GPIO_129*	H
NTSC_DATA5	T18	Output	Data bit 5	*GPIO_128*	G
NTSC_DATA4	T20	Output	Data bit 4	*GPIO_127*	G
NTSC_DATA3	R18	Output	Data bit 3	*GPIO_126*	G
NTSC_DATA2	R20	Output	Data bit 2	*GPIO_125*	G
NTSC_DATA1	P18	Output	Data bit 1	*GPIO_124*	G
NTSC_DATA0	P20	Output	Data bit 0	*GPIO_123*	G
NTSC_CLK	V20	Input	NTSC clock input	*GPIO_122*	G

1.2.33 Trace port interface signals (VDD33)

Pin Name	Pin No.	IO Type	Function	Alternate Pin Function *(Italic notation is a default pin.)*	Buffer Type
TP33_DATA15	D14	Output	Trace data bit 15	*LCD3_B7*, YUV3_D15	G
TP33_DATA14	C14	Output	Trace data bit 14	*LCD3_B6*, YUV3_D14	G
TP33_DATA13	B14	Output	Trace data bit 13	*LCD3_B5*, YUV3_D13	G
TP33_DATA12	D15	Output	Trace data bit 12	*LCD3_B4*, YUV3_D12	G
TP33_DATA11	C15	Output	Trace data bit 11	*LCD3_B3*, YUV3_D11	G
TP33_DATA10	B15	Output	Trace data bit 10	*LCD3_B2*, YUV3_D10	G
TP33_DATA9	A15	Output	Trace data bit 9	LCD3_B1, YUV3_D9, *GPIO_043*	G
TP33_DATA8	A16	Output	Trace data bit 8	LCD3_B0, YUV3_D8, *GPIO_042*	G
TP33_DATA7	D16	Output	Trace data bit 7	*LCD3_G7*, YUV3_D7	G
TP33_DATA6	C16	Output	Trace data bit 6	*LCD3_G6*, YUV3_D6	G
TP33_DATA5	B16	Output	Trace data bit 5	*LCD3_G5*, YUV3_D5	G
TP33_DATA4	D17	Output	Trace data bit 4	*LCD3_G4*, YUV3_D4	G
TP33_DATA3	C17	Output	Trace data bit 3	*LCD3_G3*, YUV3_D3	G
TP33_DATA2	B17	Output	Trace data bit 2	*LCD3_G2*, YUV3_D2	G
TP33_DATA1	A17	Output	Trace data bit 1	LCD3_G1, YUV3_D1, *GPIO_041*	G
TP33_DATA0	A18	Output	Trace data bit 0	LCD3_G0, YUV3_D0, *GPIO_040*	G
TP33_CLK	C18	Output	Trace clock output	LCD3_R6, *GPIO_038*	G
TP33_CTRL	D18	Output	Trace control	LCD3_R7, *GPIO_039*	G

1.2.34 Power supply pins

Pin Name	Pin No.	Function
AVDD	A4, B4	PLL power supply
AGND	C4, D5	PLL GND
DDR_VDDIO	F6, H6, K7, N7, R6, T6	DDR IO power supply
DDR_GND	F3, J3, M3, N2, V3	DDR GND
DDR_VREFH	V4	DDR standard reference current generation
DDR_VREFL	F4	DDR standard reference current generation
USB_AVDD1	AB11	Power supply for regulators inside USB PHY 1
USB_AVDD2	AC6	Power supply for regulators inside USB PHY 2
USB_VD3311	AB14	Power supply for USB PHY 1 DP/DM terminals
USB_VD3312	AB8	Power supply for USBPHY 2 DP/DM terminals
USB_GND11	AA11	USB PHY 1 IO GND
USB_GND12	AC8	USB PHY 2 IO GND
USB_GND21	AC14	USB PHY 1 IO GND
USB_GND22	AC10	USB PHY 2 IO GND
USB_AVSS1	AB12	USB PHY 1 regulators GND
USB_AVSS2	AB6	USB PHY 2 regulators GND
USB_PVSS1	AC12	USB PHY 1 PLL GND
USB_PVSS2	AB7	USB PHY 2 PLL GND
USB_RREF1	AC11	USB PHY 1 standard reference current generation
USB_RREF2	AC7	USB PHY 2 standard reference current generation
VDD33D	A3	Anti-fuse power supply (3.3 V)
VDD33	F7, G15, H17, K17, R17, U14, U15	3.3 V IO power supply
VDD33M	G12, V7	1.8V/3.3 V IO power supply Note
VDD18	B13, F15, G8, N17, U17, V6, V11	1.8 V IO power supply
VDD11	F9, F10, G6, G13, G16, J7, J17, K18, P6, P17, T17, U6, U13, V14	Core power supply
GND	A1,A2, A6, A7, A10, A14, A22, A23, B1, B2, B5, B23, C7, C8, D8, D9, G7, G9, G10, G14, G17, H7, H8, M7, P7, P21, R7, R21, T7, U7, U11, U12, U16, Y22, AB1, AB2, AB15, AB23, AC1, AC2, AC17, AC22, AC23	GND

Note One of 1.8V and 3.3V can be chosen and used. It's chosen by setting the voltage supplied to VDD33M to 1.8V or 3.3V.

1.3 Pin I/O Circuits

This section shows the types of I/O circuits used in EM/EV. The correspondence between circuits and pins is shown in the table below.

Buffer type	VDD	I/O	Low noise	Output condition (When stand by)	Normal/Schmitt switch	PU/PD switch (PU50K/PD50K/none)	IOLH switch (4/6/8/12mA)	Description
A	VDD18	IO	√	Z	√	√	√	It's through at the time of Standby (without input masks).
B	VDD18	IO		PU	√	√	√	
C	VDD18	IO		PD	√	√	√	
D	VDD18	IO		Z	√	√	√	
E	VDD18	IO		L	√	√	√	
F	VDD33M	IO		PU	√	√	√	
G	VDD33	IO		PD	√	√	√	
H	VDD33M	IO		Z	√	√	√	
J	VDD33M	IO	√	PD	√	√	√	
K	VDD33M	IO	√	Z	√	√	√	
L	VDD33M	IO		PD	√	√	√	
M	VDD18	I		–				Without for Standy signals (PONDET), Schmitt input and the PU/PD function
N	VDD18	I		PD				Anytime pull-down
O	VDD18	I		PD				Anytime pull-down
P	VDD18	I		–				Oscillator

Buffer type	VDD	I/O	CMOS/AMP switch	Termination	Impedance	Description
Q	DDR_VDDIO	IO		√	√	Address, control signals
R	DDR_VDDIO	IO		√	√	Clock
S	DDR_VDDIO	IO	√	√	√	DQ, DM
T	DDR_VDDIO	IO	√	√	√	DQS
U	DDR_VDDIO	I				Clock reset (standby)

2. ELECTRICAL SPECIFICATIONS

2.1 Absolute Maximum Ratings

Parameter	Symbol	Function	Rating	Unit
Power supply voltage	VDD11	Core power supply	−0.45 to +1.8	V
	AVDD	PLL power supply	−0.45 to +1.8	V
	VDD18	1.8 V IO power supply	−0.5 to +2.5	V
	VDD33	3.3 V IO power supply	−0.5 to +4.6	V
	VDD33M	1.8V/3.3 V IO power supply Note	−0.5 to +4.6	V
	VDD33D	Anti-fuse power supply	−0.5 to +4.6	V
	USB_AVDD1	Power supply for regulators inside USB PHY 1	−0.5 to +4.6	V
	USB_AVDD2	Power supply for regulators inside USB PHY 2	−0.5 to +4.6	V
	USB_VDD3311	Power supply for USB PHY 1 DP/DM terminals	−0.5 to +4.6	V
	USB_VDD3312	Power supply for USBPHY 2 DP/DM terminals	−0.5 to +4.6	V
	DDR_VDDIO	DDR IO power supply	−0.5 to +2.5	V
Input voltage	V_{I_18}	1.8 V IO power supply	−0.5 to VDD18 + 0.5	V
	V_{I_33}	3.3 V IO power supply	−0.5 to VDD33 + 0.5	V
	V_{I_33M}	1.8V/3.3 V IO power supply Note	−0.5 to VDD33M + 0.5	V
Output voltage	V_{O_18}	1.8 V IO power supply	−0.5 to VDD18 + 0.5	V
	V_{O_33}	3.3 V IO power supply	−0.5 to VDD33 + 0.5	V
	V_{O_33M}	1.8V/3.3 V IO power supply Note	−0.5 to VDD33M + 0.5	V
Storage temperature	T_{stg}	—	−65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Note One of 1.8V and 3.3V can be chosen and used. It's chosen by setting the voltage supplied to VDD33M to 1.8V or 3.3V.

2.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	VDD11	Normal operation	1.10	1.15	1.20	V
		Power saving mode Note1	0.75	—	—	V
	AVDD	—	1.10	1.15	1.20	V
	VDD18	—	1.65	1.80	1.95	V
	VDD33	—	3.0	3.3	3.6	V
	VDD33M	1.8V supply	1.65	1.80	1.95	V
		3.3V supply	3.0	3.3	3.6	V
	VDD33D	—	3.0	3.3	3.6	V
	USB_AVDD1	Note2	3.0	3.3	3.6	V
	USB_AVDD2	Note2	3.0	3.3	3.6	V
	USB_VDD3311	Note2	3.0	3.3	3.6	V
	USB_VDD3312	Note2	3.0	3.3	3.6	V
	DDR_VDDIO	Note3	1.7	1.8	1.9	V
OSC oscillation voltage Note4	VOSC	—	1.65	—	—	V
Operating ambient temperature	TA	—	−10	—	+70	°C

Notes **1.** The voltage which can guarantee a data-hold of an SRAM at the time of a power-saving mode.

. **2.** Refer to USB Specification Revision 2.0 about DC characteristics of USB port I/F.

3. Refer to JEDEC standards about DC characteristics of DDR2 I/F.

. **4.**The voltage which can guarantee continuation after oscillation starting after turning on the power and oscillation starting.

2.3 Capacitance

(TA = +25°C, f = 1 MHz, unmeasured pins returned to 0 V)

Parameter	Symbol	Buffer type	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	1.8 V IO	1	—	5	pF
		3.3 V IO	2	—	6	pF
		1.8V/3.3V IO	2		6	pF
Output capacitance	C_O	1.8 V	1	—	5	pF
		2.8 V	2	—	6	pF
		1.8V/3.3V IO	2		6	pF
I/O capacitance	C_{IO}	1.8 V	1	—	5	pF
		2.8 V	2	—	6	pF
		1.8V/3.3V IO	2		6	pF

※DDR terminal is non-applicable.

2.4 DC Characteristics

2.4.1 VDD18

(Unless it's designated in particular by the item after this, it'll be the standard under 2.2 recommendation operating condition.)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load Note 1		V_{DD18} – 0.1	—	—	V
Output voltage, low	V_{OL}	No DC load Note 1		—	—	0.1	V
Input voltage, high	V_{IH}	CMOS input		0.65 × V_{DD18}	—	V_{DD18} + 0.3	V
Input voltage, low	V_{IL}	CMOS input		–0.3	—	0.35 × V_{DD18}	V
Output current, high	I_{OH1}	V_{OH}=V_{DD18} -0.45V Note 2	4 mA setting Note 3	3.2	—	—	mA
	I_{OH2}		6 mA setting Note 3	4.8	—	—	mA
	I_{OH3}		8 mA setting Note 3	6.3	—	—	mA
	I_{OH4}		12 mA setting Note 3	7.7	—	—	mA
Output current, low	I_{OL1}	V_{OL}=0.45V Note 2	4 mA setting Note 3	3.2	—	—	mA
	I_{OL2}		6 mA setting Note 3	4.8	—	—	mA
	I_{OL3}		8 mA setting Note 3	6.3	—	—	mA
	I_{OL4}		12 mA setting Note 3	7.7	—	—	mA
Hysteresis voltage	V_H	Schmitt input		0.1 × V_{DD18}	—	0.4 × V_{DD18}	V
Negative trigger voltage	V_N	Schmitt input		0.3 × V_{DD18}	—	0.6 × V_{DD18}	V
Positive trigger voltage	V_P	Schmitt input		0.4 × V_{DD18}	—	0.7 × V_{DD18}	V
Input leakage current, high	I_{LH}	V_I = V_{DD18}		—	—	10	μA
Input leakage current, low	I_{LL}	V_I = GND		—	—	10	μA
Pull-up resistance	R_{PU}	—		37	50	80	kΩ
Pull-down resistance	R_{PD}	—		37	50	80	kΩ

Notes **1.** The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the I/O buffer output current drive switch register. It's established at CHG_DRIVE0-5 register of a CHG module.

2.4.2 VDD33

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load Note 1		V_{DD33} – 0.1	–	–	V
Output voltage, low	V_{OL}	No DC load Note 1		–	–	0.1	V
Input voltage, high	V_{IH}	CMOS input		2.0	–	V_{DD33} + 0.3	V
Input voltage, low	V_{IL}	CMOS input		–0.3	–	0.8	V
Output current, high	I_{OH1}	$V_{OH} = V_{DD33(min)}$ – 0.6 V Note 2	4 mA setting Note 3	4	–	–	mA
	I_{OH2}		6 mA setting Note 3	6	–	–	mA
	I_{OH3}		8 mA setting Note 3	7.8	–	–	mA
	I_{OH4}		12 mA setting Note 3	9.5	–	–	mA
Output current, low	I_{OL1}	V_{OL} = 0.4 V Note 2	4 mA setting Note 3	4	–	–	mA
	I_{OL2}		6 mA setting Note 3	6	–	–	mA
	I_{OL3}		8 mA setting Note 3	7.8	–	–	mA
	I_{OL4}		12 mA setting Note 3	9.5	–	–	mA
Hysteresis voltage	V_H	Schmitt input		0.11 × V_{DD33}	–	0.41 × V_{DD33}	V
Negative trigger voltage	V_N	Schmitt input		0.17 × V_{DD33}	–	0.38 × V_{DD33}	V
Positive trigger voltage	V_P	Schmitt input		0.54 × V_{DD33}	–	0.65 × V_{DD33}	V
Input leakage current, high	I_{L_H}	$V_I = V_{DD33}$		–	–	10	μA
Input leakage current, low	I_{L_L}	V_I = GND		–	–	10	μA
Pull-up resistance	R_{PU}	50 kΩ resistor		37	50	80	kΩ
Pull-down resistance	R_{PD}	50 kΩ resistor		37	50	80	kΩ

Notes **1.** The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the output current drive switch register. It's established at CHG_DRIVE0-5 register of a CHG module.

2.4.3 VDD33M (1.8V supply)

The power-supply voltage when supplying VDD33M with 1.8V, is shown with VDD18M.

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load Note 1		V_{DD18M} – 0.1	–	–	V
Output voltage, low	V_{OL}	No DC load Note 1		–	–	0.1	V
Input voltage, high	V_{IH}	CMOS input		0.65 × V_{DD18M}	–	V_{DD18M} + 0.3	V
Input voltage, low	V_{IL}	CMOS input		–0.3	–	0.35 × V_{DD18M}	V
Output current, high	I_{OH1}	V_{OH} = V_{DD18M} – 0.6 V Note 2	4 mA setting Note 3	2.2	–	–	mA
	I_{OH2}		6 mA setting Note 3	3.3	–	–	mA
	I_{OH3}		8 mA setting Note 3	4.3	–	–	mA
	I_{OH4}		12 mA setting Note 3	5.4	–	–	mA
Output current, low	I_{OL1}	V_{OL} = 0.4 V Note 2	4 mA setting Note 3	2.8	–	–	mA
	I_{OL2}		6 mA setting Note 3	4.1	–	–	mA
	I_{OL3}		8 mA setting Note 3	5.4	–	–	mA
	I_{OL4}		12 mA setting Note 3	6.7	–	–	mA
Hysteresis voltage	V_H	Schmitt input		0.1 × V_{DD18M}	–	0.4 × V_{DD18M}	V
Negative trigger voltage	V_N	Schmitt input		0.2 × V_{DD18M}	–	0.6 × V_{DD18M}	V
Positive trigger voltage	V_P	Schmitt input		0.4 × V_{DD18M}	–	0.7 × V_{DD18M}	V
Input leakage current, high	I_{L_H}	V_I = V_{DD18M}		–	–	10	μA
Input leakage current, low	I_{L_L}	V_I = GND		–	–	10	μA
Pull-up resistance	R_{PU}	50 kΩ resistor		37	50	80	kΩ
Pull-down resistance	R_{PD}	50 kΩ resistor		37	50	80	kΩ

Notes **1.** The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the output current drive switch register. It's established at CHG_DRIVE0-5 register of a CHG module.

2.4.4 VDD33M (3.3V supply)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	No DC load Note 1		V_{DD33M} – 0.1	–	–	V
Output voltage, low	V_{OL}	No DC load Note 1		–	–	0.1	V
Input voltage, high	V_{IH}	CMOS input		2.0	–	V_{DD33M} + 0.5	V
Input voltage, low	V_{IL}	CMOS input		–0.3	–	0.8	V
Output current, high	I_{OH1}	V_{OH} = $V_{DD33M(min)}$ – 0.6 V Note 2	4 mA setting Note 3	4	–	–	mA
	I_{OH2}		6 mA setting Note 3	6	–	–	mA
	I_{OH3}		8 mA setting Note 3	7.8	–	–	mA
	I_{OH4}		12 mA setting Note 3	9.5	–	–	mA
Output current, low	I_{OL1}	V_{OL} = 0.4 V Note 2	4 mA setting Note 3	4	–	–	mA
	I_{OL2}		6 mA setting Note 3	6	–	–	mA
	I_{OL3}		8 mA setting Note 3	7.8	–	–	mA
	I_{OL4}		12 mA setting Note 3	9.5	–	–	mA
Hysteresis voltage	V_H	Schmitt input		0.11 × V_{DD33M}	–	0.41 × V_{DD33M}	V
Negative trigger voltage	V_N	Schmitt input		0.17 × V_{DD33M}	–	0.38 × V_{DD33M}	V
Positive trigger voltage	V_P	Schmitt input		0.54 × V_{DD33M}	–	0.65 × V_{DD33M}	V
Input leakage current, high	I_{L_H}	V_I = V_{DD33M}		–	–	10	μA
Input leakage current, low	I_{L_L}	V_I = GND		–	–	10	μA
Pull-up resistance	R_{PU}	50 kΩ resistor		37	50	80	kΩ
Pull-down resistance	R_{PD}	50 kΩ resistor		37	50	80	kΩ

Notes **1.** The parameters V_{OH} and V_{OL} here are the values guaranteed when there is no load when applying the DC current.

2. The parameters V_{OH} and V_{OL} here define the output current.

3. This is the value set to the output current drive switch register. It's established at CHG_DRIVE0-5 register of a CHG module.

2.4.5 Standby state current

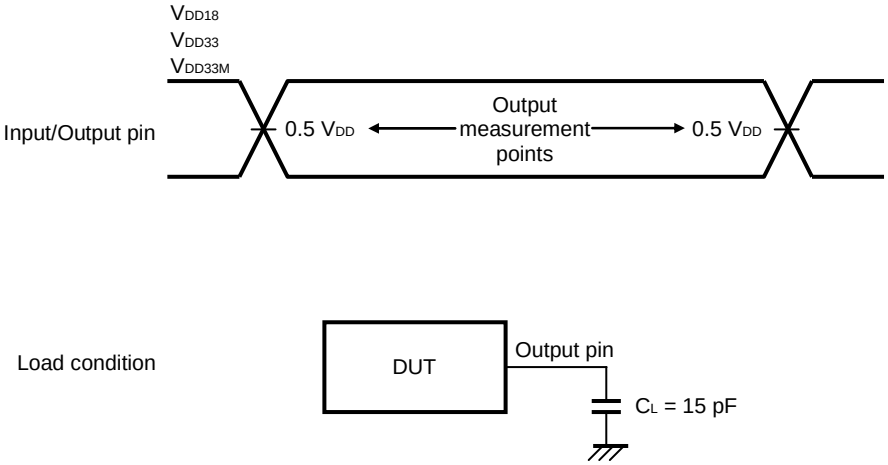
(T_A = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Standby current	I_{DD_PA}	Logic power supply PA, f = 0 Hz, V_{DD11} = 0.75 V	—	0.6	—	μA
	I_{DD_IO18}	IO power supply f = 0 Hz, V_{IO18} = 1.8 V	—	5	—	μA
	I_{DD_IO33}	IO power supply f = 0 Hz, V_{IO3} = 3.3 V	—	5	—	μA
	I_{DD_IO33M}	IO power supply f = 0 Hz, V_{IO3} = 3.3 V	—	5	—	μA

2.5 AC Characteristics

2.5.1 AC test I/O measurement points

Figure 2-1. AC Test I/O Measurement Points



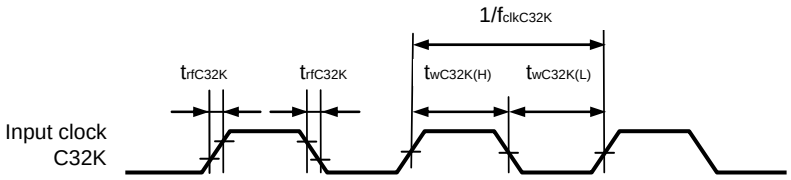
Remark Excluding the OSC pin. Unless specified otherwise, the load of C_L is assumed to be 15 pF.
Unless it's designated in particular by the item after this, it'll be the standard under 2.2 recommendation operating condition

2.5.2 System control

(1) Clock (input timing requirements)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
C32K frequency	$f_{clkC32K}$	–	–	32.768	–	kHz
C32K rise/fall time	t_{rfC32K}	0 to 90%	–	–	1	μs
32 kHz input clock duty ratio	$I_{dutyC32K}$	–	30	–	70	%
32 kHz input clock jitter	$I_{jitterC32K}$	–	–20	–	20	ns

Figure 2-2. Clock Timing



(2) PLL

PLL1 lock up time : 200 μ s max
PLL2 lock up time : 2000 μ s max
PLL3 lock up time : 800 μ s max
PLL4 lock up time : 2000 μ s max

(3) OSC

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
OSC oscillation frequency range	$f_{C(OSC)}$	Internal oscillator OSCx Note1,Note2, Note3 (OSCx_XT1, OSCx_XT2)		1	–	27	MHz
		AMP ability setting Note4	C1=1 / C0=1	20	–	27	MHz
			C1=1 / C0=0	10	–	20	MHz
			C1=0 / C0=1	4	–	10	MHz
			C1=0 / C0=0	1	–	4	MHz

OSC lock up time : 2000 μ s max Note5

Notes **1.** x=1 or 2

2. Use by 10-27MHz is recommended. If you have any question (When using by 1-10MHz), please contact us through

"http://japan.renesas.com/contact/contact_tech.html " (Japanese) or

"http://america2.renesas.com/support/index.html " (English).

3. It's subject to the next restrictions.

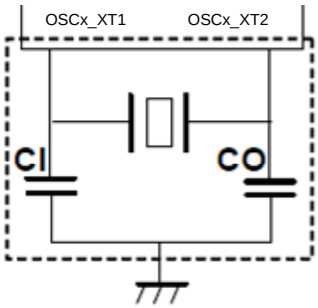
Oscillation frequency ≦ 20MHz : Capacitance is 8pF.

Oscillation frequency > 20MHz : Capacitance is 7pF.

4. It's possible to choose a correspondence frequency by changing the AMP ability. Setting is a OSC_CX register of a SMU module.

5. For lock up time to change by quartz crystal units, estimate by actual environment.

Figure 2-3. Recommended Oscillator



Cautions 1. Keep the wiring length between the oscillator and the OSCx_XT1 and OSCx_XT2 pins as short as possible.

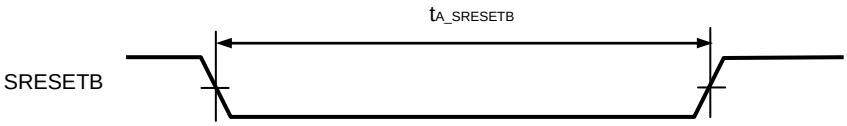
2. Do not cross the wiring with the other signal lines in the area enclosed by the broken lines.

3. Thoroughly evaluate matching of the resonator.

(3) Reset

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SRESETB low-level width	$t_{A\_SRESETB}$	—	6	—	—	ms

Figure 2-4. Reset Timing



2.5.3 Asynchronous bus (AB) interface

（VDD33＝3.3±0.3 V, input pin : Normal , Drive=8mA)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
AB_CSB[3:0] fall to AB_ADV fall	t_{200}	－	CS_ADV×Tf-5	CS_ADV×Tf+5	ns	
AB_CSB[3:0] active width (at read)	t_{201}	－	(CS_ADV+ADV_WIDTH+1+T0+T1+RDT+1+T2) × Tf-5	(CS_ADV+ADV_WIDTH+1+T0+T1+RDT+1+T2) ×Tf+5	ns	1, 2, 4, 5
AB_CSB[3:0] fall to AB_ADV rise	t_{202}	－	(CS_ADV+ADV_WIDTH+1)×Tf-5	(CS_ADV+ADV_WIDTH+1)×Tf+5	ns	
AB_ADV active width	t_{203}	AB_ADV=Low	(ADV_WIDTH+1)×Tf-5	(ADV_WIDTH+1)×Tf+5	ns	
Lower ADD hold time (at AD-Mux read)	t_{204}	－	See Note6	See Note6	ns	1, 6
AB_ADV rise to AB_RDB fall	t_{205}	Falling edge of AB_RDB	T0×Tf-5	T0×Tf+5	ns	1
AB_RDB active width	t_{206}	AB_RDB=Low	(T1+RDT+1)×Tf-5	(T1+RDT+1)×Tf+5	ns	4, 5
AB_RDB rise to AB_CSB[3:0] rise	t_{207}	Rising edge of AB_RDB	T2×Tf-5	T2×Tf+5	ns	4, 5
AB_CSB[3:0] assert interval time (at read)	t_{208}	－	(CSint+1)×Tf-5	－	ns	4, 5
Read data setup time	t_{209}	Rising edge of AB_RDB	(RDT+1)×Tf + 8	－	ns	4, 5
Read data hold time	t_{210}	Rising edge of AB_RDB	0	－	ns	
Address determination to AB_RDB fall	t_{211}	Falling edge of AB_RDB	(CS_ADV+ADV_WIDTH+1+T0)×Tf-5	(CS_ADV+ADV_WIDTH+1+T0)×Tf-5	ns	1
AB_CSB[3:0] fall to AB_RDB fall	t_{212}	Falling edge of AB_RDB	(CS_ADV+ADV_WIDTH+1+T0)×Tf-5	(CS_ADV+ADV_WIDTH+1+T0)×Tf+5	ns	1
AB_CSB[3:0] fall to lower ADD output delay (at AD-MUX)	t_{213}	－	-5	5	ns	
AB_RDB rise to ADD output transition time	t_{214}	－	(T2+CSint+1)×Tf-5	－	ns	4, 5
AB_CSB[3:0] active width (at write)	t_{220}	－	(CLK_MODE=1 setting) (CS_ADV+ADV_WIDTH+1+T0_W+T1_W+0.5+T2_W)×Tf – 5 (CLK_MODE=0 setting) (CS_ADV+ADV_WIDTH+1+T0_W+T1_W+1+T2_W)×Tf – 5	(CLK_MODE=1 setting) (CS_ADV+ADV_WIDTH+1+T0_W+T1_W+0.5+T2_W)×Tf + 5 (CLK_MODE=0 setting) (CS_ADV+ADV_WIDTH+1+T0_W+T1_W+1+T2_W)×Tf + 5	ns	3, 7

(2/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
AB_ADV rise to AB_WRB fall	t_{221}	Falling edge of AB_WRB	T0_W×Tf-5	T0_W×Tf+5	ns	
AB_WRB active width	t_{222}	AB_WRB=Low	(CLK_MODE=1 setting) (T1_W+0.5)×Tf - 5 (CLK_MODE=0 setting) (T1_W+1)×Tf – 5	(CLK_MODE=1 setting) (T1_W+0.5)×Tf + 5 (CLK_MODE=0 setting) (T1_W+1)×Tf + 5	ns	3, 7
AB_WRB rise to AB_CSB[3:0] rise	t_{223}	Rising edge of AB_WRB	T2_W×Tf-5	T2_W×Tf+5	ns	
AB_WRB rise to AB_AD[15:0] Hi-z transition	t_{224}	Rising edge of AB_WRB	T2_W×Tf-5	T2_W×Tf+5	ns	
Address determination to AB_WRB fall	t_{225}	Falling edge of AB_WRB	(CS_ADV+ADV_WIDTH+1+T0_W)×Tf-5	(CS_ADV+ADV_WIDTH+1+T0_W)×Tf+5	ns	
AB_CSB[3:0] fall to AB_WRB fall	t_{226}	Falling edge of AB_WRB	(CS_ADV+ADV_WIDTH+1+T0_W)×Tf-5	(CS_ADV+ADV_WIDTH+1+T0_W)×Tf+5	ns	
AB_CSB[3:0] assert interval time (at write)	t_{227}	–	(CLK_MODE=1 setting) (CSint+1+0.5)×Tf - 5 (CLK_MODE=0 setting) (CSint+1+1)×Tf – 5	–	ns	4, 5, 7
AB_WRB to Data output start time (at AD non Mux)	t_{228}	–	-5	5	ns	
AB_ADV rise to AB_AD[15:0] ADD-Data transition (at AD-Mux write)	t_{229}	–	T0_W×Tf-5	T0_W×Tf+5	ns	8
AB_WRB rise to ADD transition time	t_{230}	–	(CLK_MODE=1 setting) (T2_W+CSint+1+0.5)×Tf - 5 (CLK_MODE=0 setting) (T2_W+CSint+1+1)×Tf – 5	–	ns	7
AB_WAIT rise to T1 section end	t_{240}	–	(CLK_MODE=1 setting) 1×Tf+8 (CLK_MODE=0 setting) 2×Tf+8	–	ns	7,9
AB_WAIT fall to AB_RDB rise	t_{241}	–	–	(CLK_MODE=1 setting) (2+RDT+1)×Tf+12 (CLK_MODE=0 setting) (3+RDT+1)×Tf+12	ns	7

(3/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
AB_WAIT rise to T1_W+1 section end or (AB_WAIT rise to T1_W+0.5 section end)	t_{242}	−	(CLK_MODE=1 setting) 1×Tf+8 (CLK_MODE=0 setting) 2×Tf+8	−	ns	7, 10
AB_WAIT fall to AB_WRB rise	t_{243}	−	−	(CLK_MODE=1 setting) 2×Tf+12 (CLK_MODE=0 setting) 3×Tf+12	ns	7

Remark Tf = AB0_CLK 2clocks (CLK_MODE=1 setting)
AB0_CLK 1 clock (CLK_MODE=0 setting) AB0_CLK is HFB domain clock.
Refer to SMU User's manual (S20082EJ) for a setting method of AB0_CLK frequency.
ex) In case of PLL2=500MHz, a frequency of AB0_CLK can be set as 125MHz by the following setting.
DMSRC_PLLSEL_NRM = 4 (CKMODE_PLLSEL register)
HFBDOMAIN_DIV_NRA = 3 (NORMALA_DIV register)
MODE_SEL = 1 (CLK_MODE_SEL register)

T0, T1, T2, CSInt : AB0_CSxWAITCTRL setting value
T0_W, T1_W, T2_W : AB0_CSxWAITCTRL_W setting value
RDT : AB0_CSxREADCTRL setting value
CS_ADV, ADV_WIDTH : AB0_CSxCONTROL setting value
x : 0-5

Note 1 Setting of T0 operates as setting of "1" in case of "0" at the time of AD-MUX.
2 Setting of T1 operates as setting of "1" in case of "0".
3 Setting of T1_W operates as setting of "1" in case of "0".
4 It's necessary to make the total of the set value of RDT,T2,CSINT more than 1 at the time of CLK_MODE=1 setting.
5 It's necessary to make the total of the set value of RDT,T2,CSINT more than 2 at the time of CLK_MODE=0 setting.
6 t204 is in combination of AD_OE bit (AB0_CSxCONTROL) and CLK_MODE, and 4 ways of timing can be established. (the following).

Lower ADD hold time (min)

	CLK_MODE=0	CLK_MODE=1
AD_OE=0	-5	-5
AD_OE=1	(T0-1)×Tf-5	(T0-0.5)×Tf-5

Lower ADD hold time (max)

	CLK_MODE=0	CLK_MODE=1
AD_OE=0	5	5
AD_OE=1	(T0-1)×Tf+5	(T0-0.5)×Tf+5

When it's CLK_MODE=0, T0=1 setting it changes into Hi-Z by the same timing as a fall of AB_RDB.

7 It's possible to set CLK_MODE at the AB_FLASHCLKCTRL register.
8 Only when setting of T0_W is 0 at the time of AD-Mux, refer to following Min,Max.
t229 = Min : 0.5×Tf-5, Max : 0.5×Tf+5 (CLK_MODE=1 setting, AD-Mux, T0_W=0)
t229 = Min : 1×Tf-5, Max : 1×Tf+5 (CLK_MODE=0 setting, AD-Mux, T0_W=0)

9 Condition to use WAIT function

Active AB_WAIT signal by the minimum time before the end of T1 section. Data latch will stop till inactivating AB_WAIT.

In case of inactivating AB_WAIT signal by the minimum time before the end of T1 section, Wait function will not work.

10 Condition to use WAIT function

Active AB_WAIT signal by the minimum time before the end of T1 section. Data latch will stop till inactivating AB_WAIT.

In case of inactivating AB_WAIT signal by the minimum time before the end of T1 section, Wait function will not work.

(At the time of CLK_MODE=1 is “T1_W+0.5”)

Figure 2-5. Single Read Timing (AD-Mux)

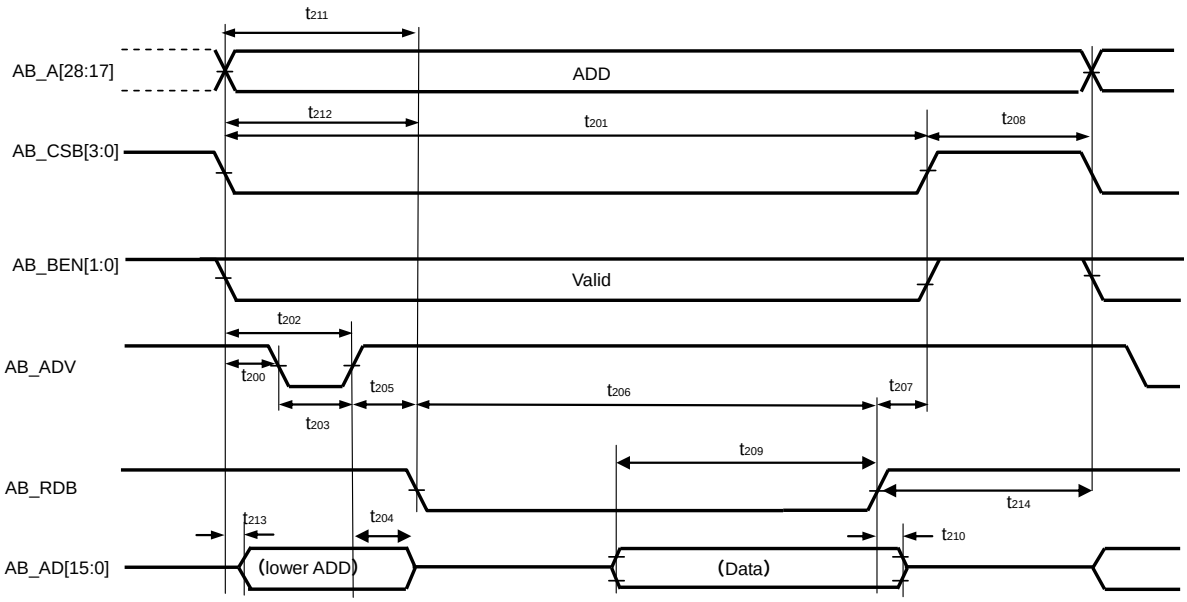


Figure 2-6. Single Write Timing (AD-Mux)

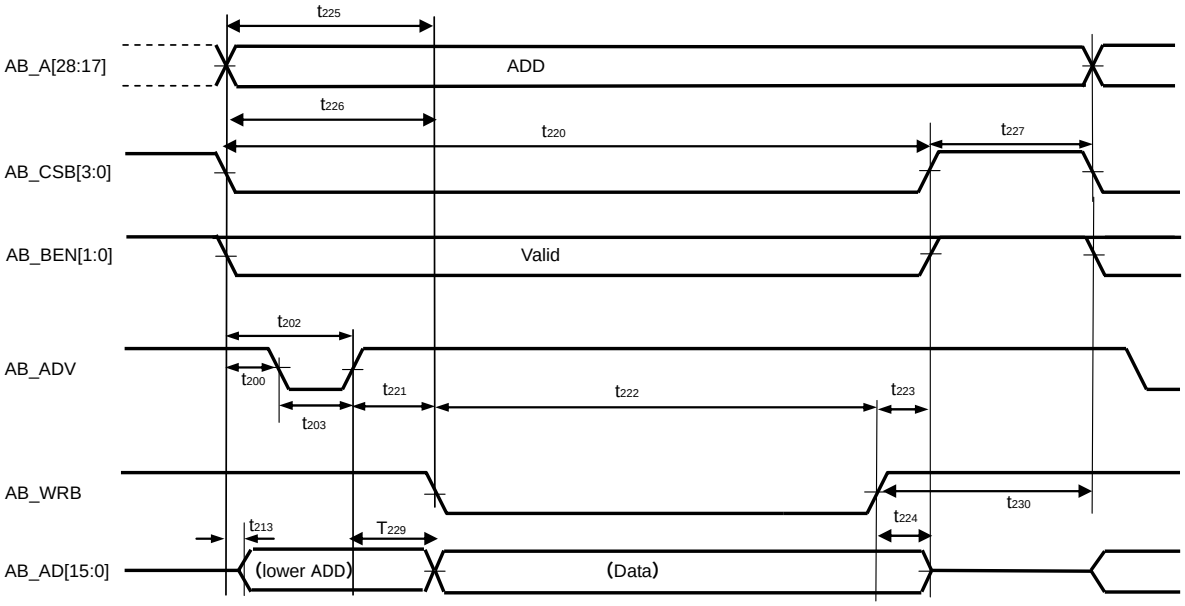


Figure 2-7. Single Read Timing (AD non Mux)

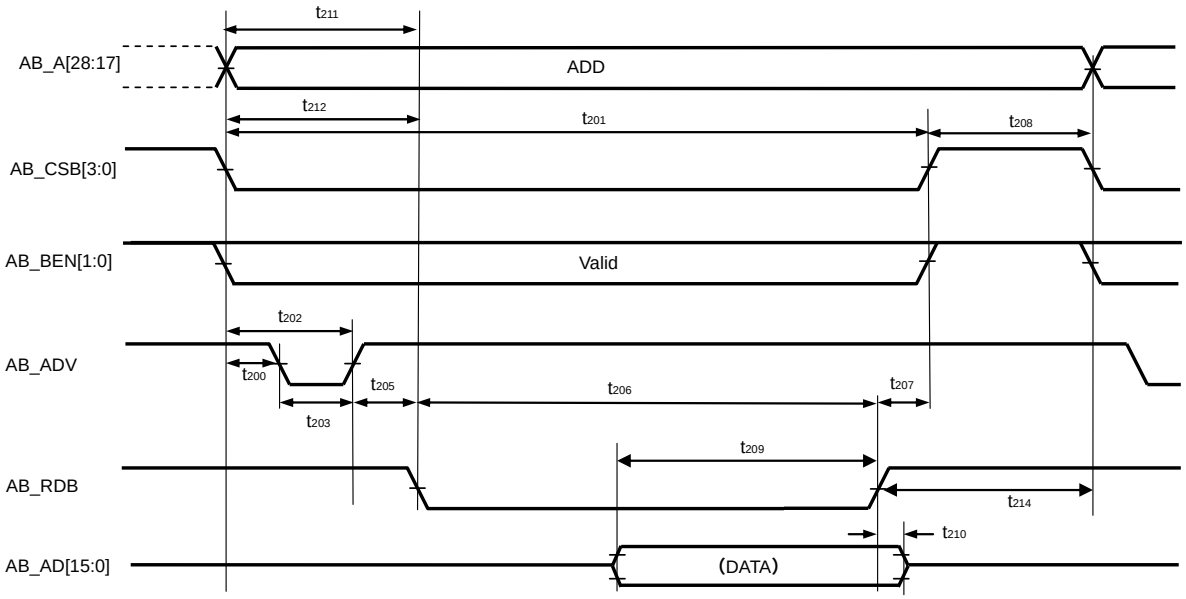


Figure 2-8. Single Write Timing (AD non Mux)

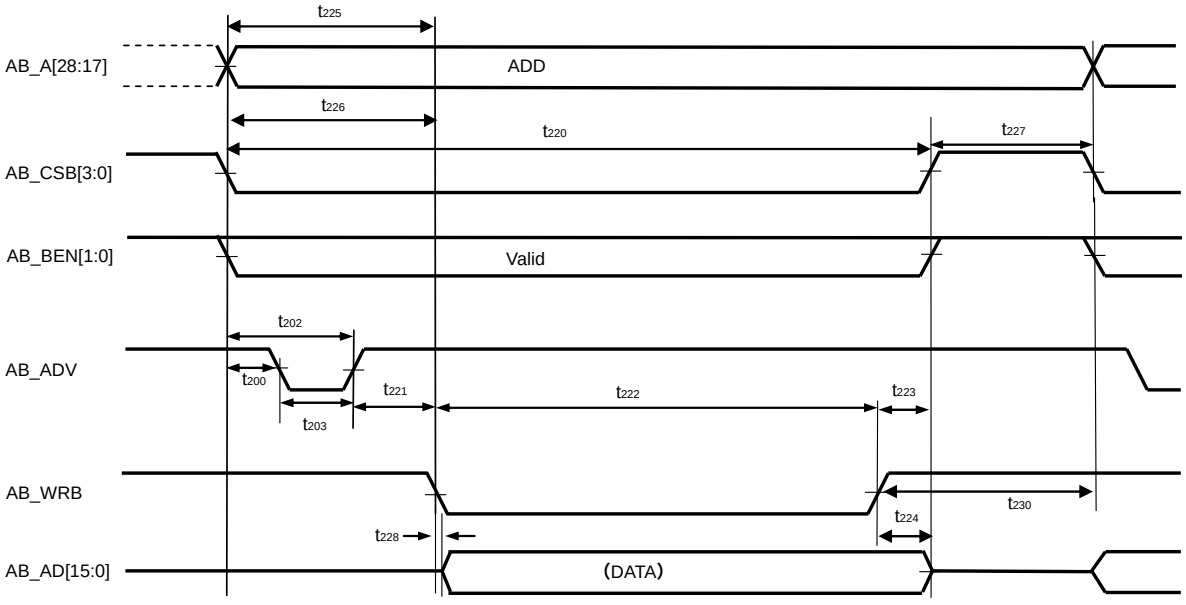


Figure 2-9. Single Read Timing (Wait)

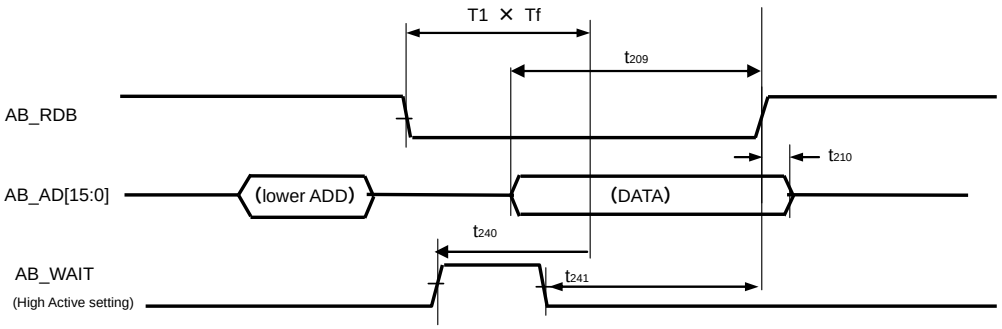
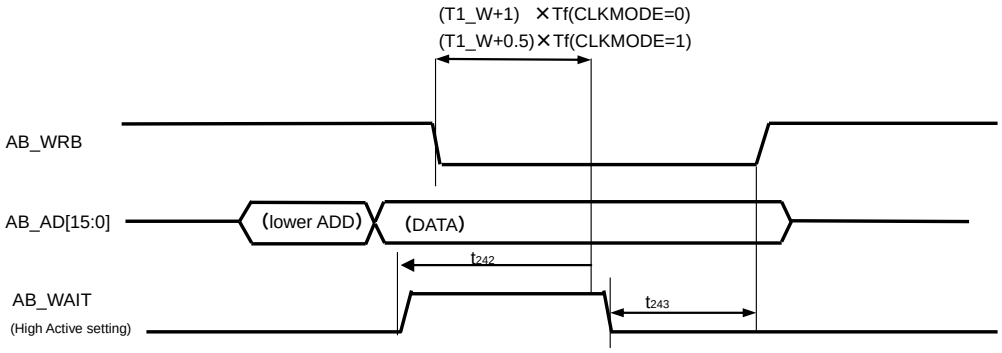


Figure 2-10. Single Write Timing (Wait)



2.5.4 IIC interface

Parameter	Symbol	Conditions	Standard Mode[Note 1]		High-Speed Mode[Note 1]		Unit
			MIN.	MAX.	MIN.	MAX.	
IIC_SCL clock frequency	f_C	—	0	100	0	400	kHz
IIC bus free time	t_{BF}	Interval between stop and start conditions	4.7	–	1.3	–	μs
IIC hold time[Note 2]	t_{H1}	—	4.0	–	0.6	–	μs
IIC hold time (SCL clock)	t_{WL}	"Low" state	4.7	–	1.3	–	μs
	t_{WH}	"Hi" state	4.0	–	0.6	–	μs
IIC setup time	t_{SU1}	Start condition Restart condition	4.7	–	0.6	–	μs
IIC data setup time	t_{SU2}	—	250	–	100[Note 3]	–	ns
IIC rise time	t_R	SDA and SCL signals	–	–	–	300[Note 4]	ns
IIC fall time	t_F	SDA and SCL signals	–	–	–	300[Note 4]	ns
IIC setup time	t_{SU3}	Stop condition	4.0	–	0.6	–	μs
IIC data hold time	t_{H2}	Clock fall output	5.0	–	—	–	μs
		Clock fall input	0	3.45	0[Note 5]	0.9[Note 6]	μs
Capacitance load of each IIC bus line	C_b	—	–	400	–	400	pF

Notes 1. Select the standard mode or high-speed mode by using the SMC0 bit of the IIC0 clock select register (IICCL0).

2. At the start condition, the first clock pulse is generated after the hold time.

3. The high-speed mode I^2C bus can be used in the standard-mode I^2C bus system. In this case, set the high-speed mode I^2C bus so that it meets the following conditions.

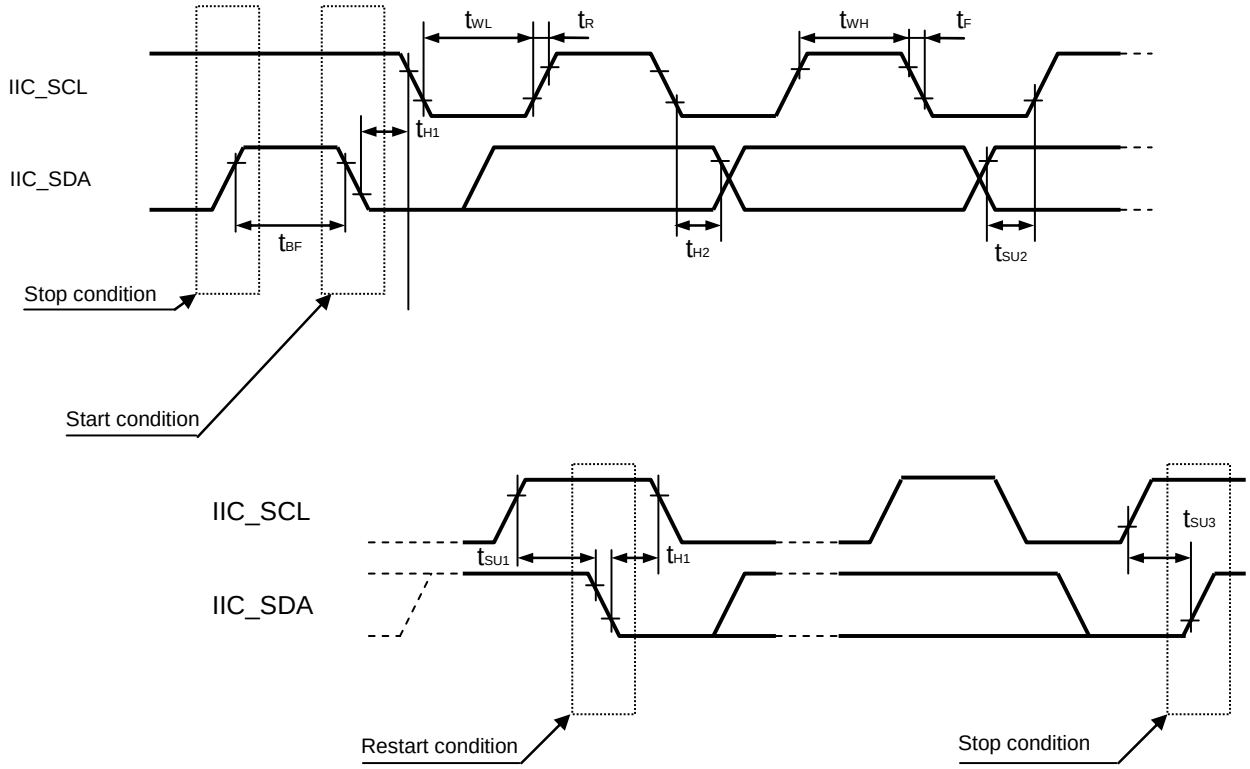
- If the system does not extend the IIC_SCL signal's low state hold time: $t_{SU2} \geq 250$ ns

4. Do not input noise exceeding the hysteresis width of the 1.8 V system IO Schmitt buffer during a rise or fall time.

5. The system requires a minimum of 300 ns hold time internally for the SDA signal (at V_{IH} (MIN.) [0.7 V_{DD2}] of IIC_SCL signal) in order to occupy the undefined area at the falling edge of IIC_SCL.

6. If the system does not extend the IIC_SCL signal low hold time (t_{WL}), only the maximum data hold time (t_{H2}) needs to be satisfied.

Figure 2-11. IIC Bus Interface Timing



2.5.5 Unified Serial Interface

(1) Audio/Voice interface

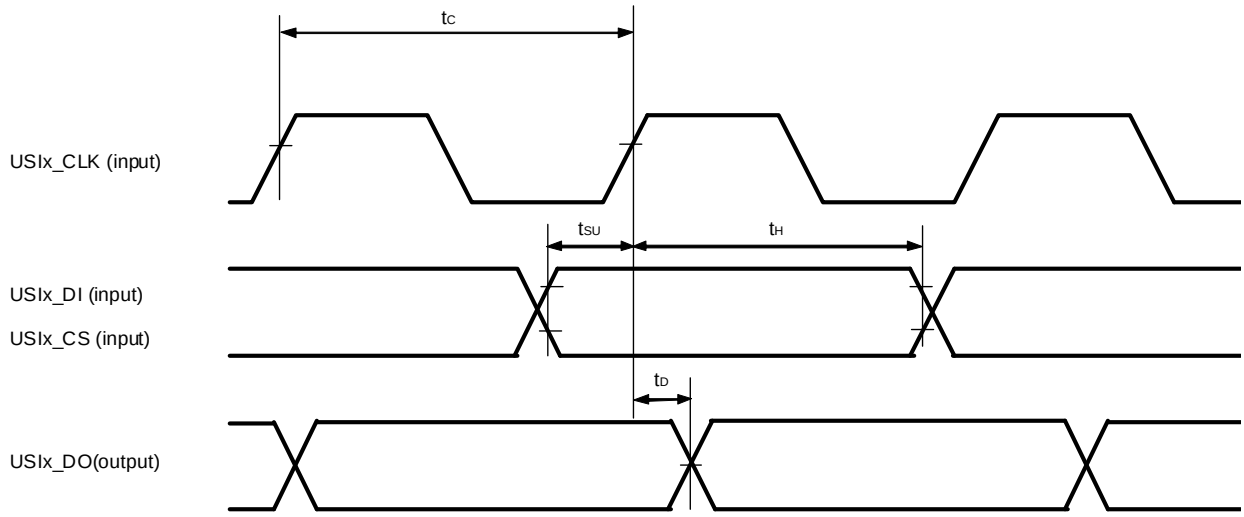
(a) Slave mode

（VDD33＝3.3±0.3 V, input pin : schmitt , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USIx_CLK cycle time	t_C	–	50	–	–	ns
USIx_DI, USIx_CS setup time	t_{SU}	Rise or fall of USI_xCLK	20	–	–	ns
USIx_DI, USIx_CS hold time	t_H	Rise or fall of USI_xCLK	20	–	–	ns
USIx_DO output delay time	t_D	Rise or fall of USI_xCLK	0	–	20	ns

Remark Time from the valid edge
x = 0-5

Figure 2-12. Audio/Voice Interface Timing (Slave Mode)



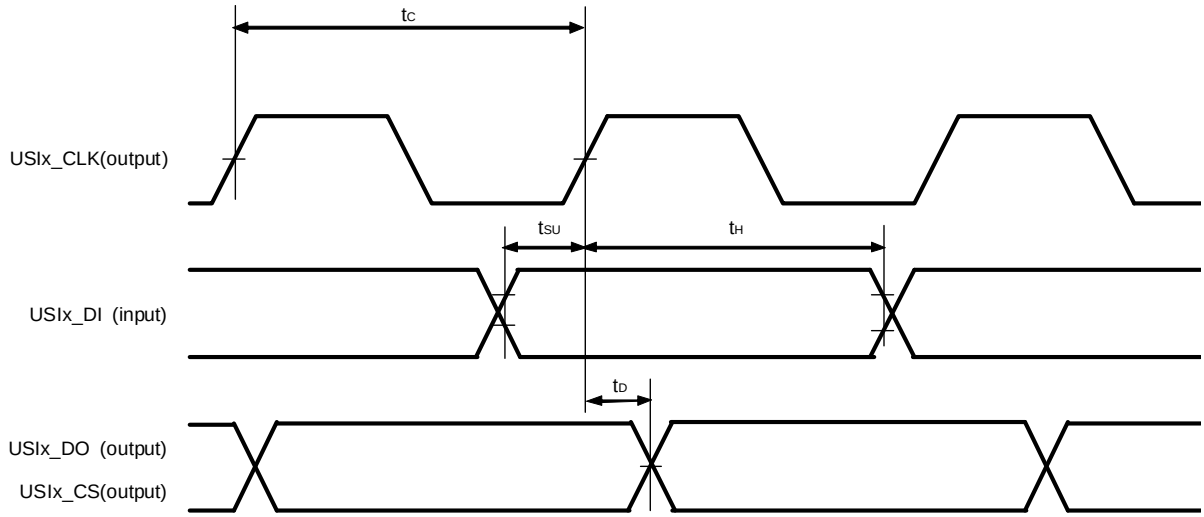
(b) Master mode

（VDD33＝3.3±0.3 V, input pin : schmitt , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USIx_CLK cycle time	t_C	–	50	—	—	ns
USIx_DI setup time	t_{SU}	–	20	—	—	ns
USIx_DI hold time	t_H	–	20	—	—	ns
USIx_DO, USIx_CS output delay time	t_D	–	–5	—	20	ns

Remark Time from the valid edge
x = 0-3

Figure 2-13. Audio/Voice Interface Timing (Master Mode)



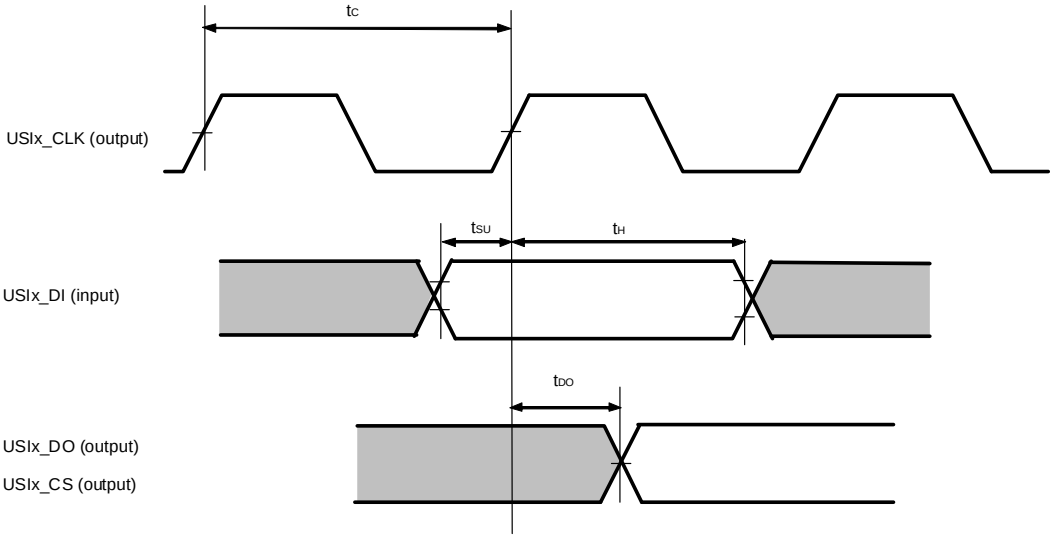
(2) SPI interface

(a) Master mode

（VDD33＝3.3±0.3 V, input pin : Normal , Drive=4mA (USI0, USI1) 6mA (USI2))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
<USI0-1, 3-5> x=0-1, 3-5						
USIx_CLK output cycle	t_C	—	33	—	—	ns
USIx_DI setup time	t_{SU0}	Rise or fall of USI_xCLK	12	—	—	ns
USIx_DI hold time	t_{H0}	Rise or fall of USI_xCLK	0	—	—	ns
USIx_DO, USIx_CS output delay time	t_{DO}	Rise or fall of USI_xCLK	0	—	12	ns
<USI2> x=2						
USIx_CLK output cycle	t_C	—	16.6	—	—	ns
USIx_DI setup time	t_{SU0}	Rise or fall of USI_xCLK	8	—	—	ns
USIx_DI hold time	t_{H0}	Rise or fall of USI_xCLK	0	—	—	ns
USIx_DO, USIx_CS output delay time	t_{DO}	Rise or fall of USI_xCLK	0	—	6	ns

Figure 2-14. SPI Interface Timing (Master Mode)



Notes 1. USIx_CLK can output reverse by register setting.
2. USIx_CLK doesn't output USIx_CLK inactive period (It'll be inactive level fixing.)
3. When the read latency of the connection device is long, it's an input/output phase switch function of DI/DO (rising/falling of SCLK) and is applicable.

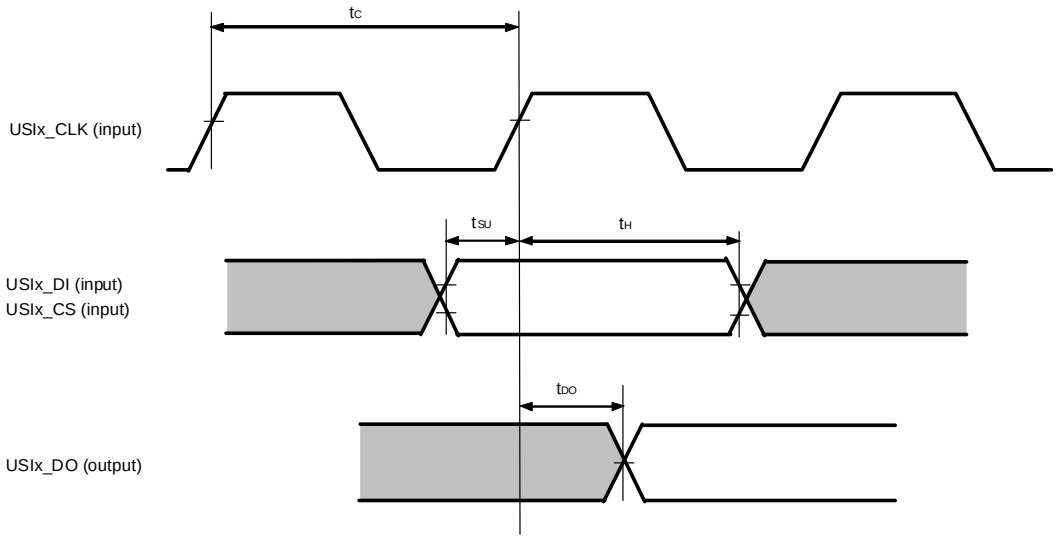
(b) Slave mode

（VDD33＝3.3±0.3 V, input pin : Normal , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USIx_CLK input cycle	t_C	–	50	—	—	ns
USIx_DI, USIx_CS setup time	t_{SU}	Rise or fall of USI_xCLK	5	—	—	ns
USIx_DI, USIx_CS hold time	t_H	Rise or fall of USI_xCLK	15	—	—	ns
USIx_DO delay time	t_{DO}	Rise or fall of USI_xCLK	3	—	20	ns

Remark Time from the valid edge
x = 0-5

Figure 2-15. SPI Interface Timing (Slave Mode)



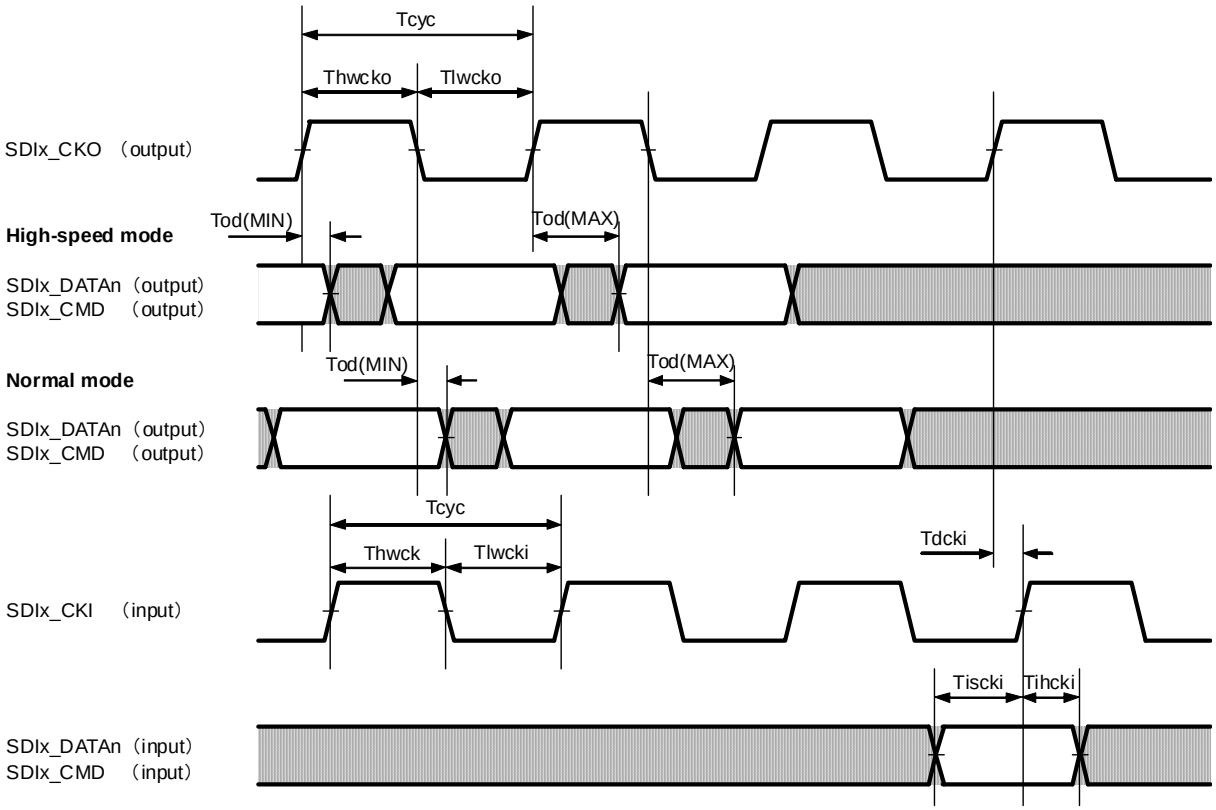
2.5.6 SDIO interface

SDIO1, 2 is MMC non-correspondence.

(VDD33＝3.3±0.3 V, input pin : schmitt, Drive=8mA, outside loop, CMD and Data is pull-up)

Parameter	Symbol	Conditions	SD0 (SDIA), SD1 (SDIB), SD2 (SDIC)			
			MIN.	TYP.	MAX.	Unit
Clock cycle	T_{cyc}	—	19.2	—	—	ns
Output clock high-level width	T_{hwcko}	@52MHz	8.1	9.6	11.1	ns
Output clock low-level width	T_{lwcko}	@52MHz	8.1	9.6	11.1	ns
Output delay	T_{od}	SDIO	3	—	14	ns
Output delay	T_{od}	SDI1, SDI2	2	—	14	ns
Input clock high-level width	T_{hwcki}	—	7.6	9.6	11.6	ns
Input clock low-level width	T_{lwcki}	—	7.6	9.6	11.6	ns
Input clock delay time	T_{dcki}	—	0	—	10	ns
Setup time	T_{iscki}	—	2	—	—	ns
Hold time	T_{ihcki}	—	1	—	—	ns

Figure 2-16. SDIO Interface Timing



Remark x = 0 to 2

n = 0 to 7 (SDI0)

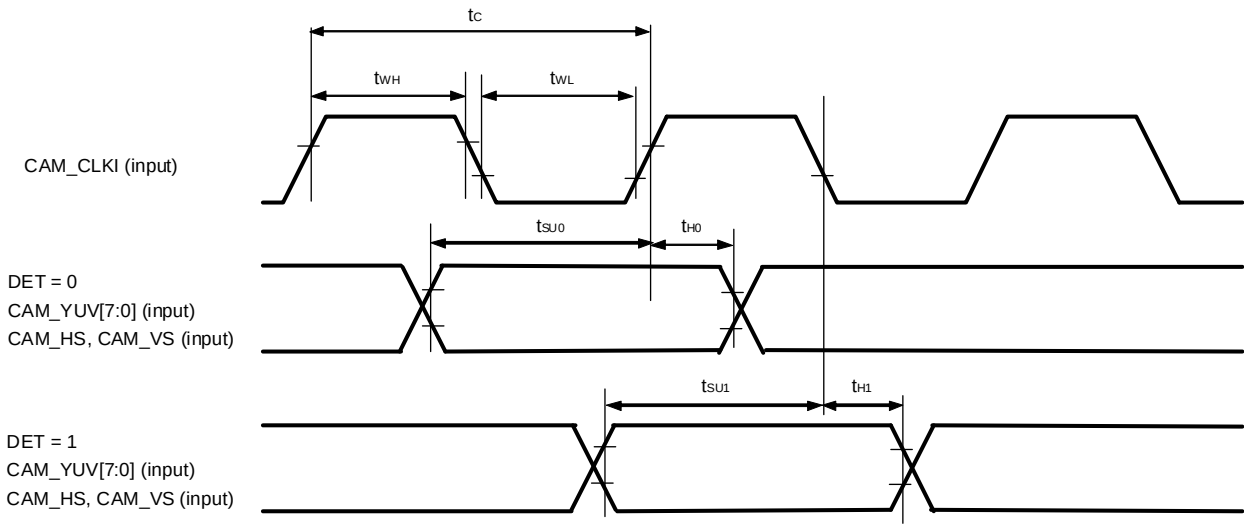
0 to 3 (SDI1, SDI2)

2.5.7 Camera interface

（VDD33＝3.3±0.3 V, input pin : Normal)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CAM_CLKI input cycle	t_C	—	10	—	—	ns
CAM_CLKI high-level width	t_{WH}	—	4	—	—	ns
CAM_CLKI low-level width	t_{WL}	—	4	—	—	ns
CAM_YUV[7:0], CAM_HS, CAM_VS setup time	t_{SU0}	DET = 0	5	—	—	ns
CAM_YUV[7:0], CAM_HS, CAM_VS hold time	t_{H0}	DET = 0	0	—	—	ns
CAM_YUV[7:0], CAM_HS, CAM_VS setup time	t_{SU1}	DET = 1	5	—	—	ns
CAM_YUV[7:0], CAM_HS, CAM_VS hold time	t_{H1}	DET = 1	0	—	—	ns

Figure 2-17. Camera Interface Timing



2.5.8 LCD interface

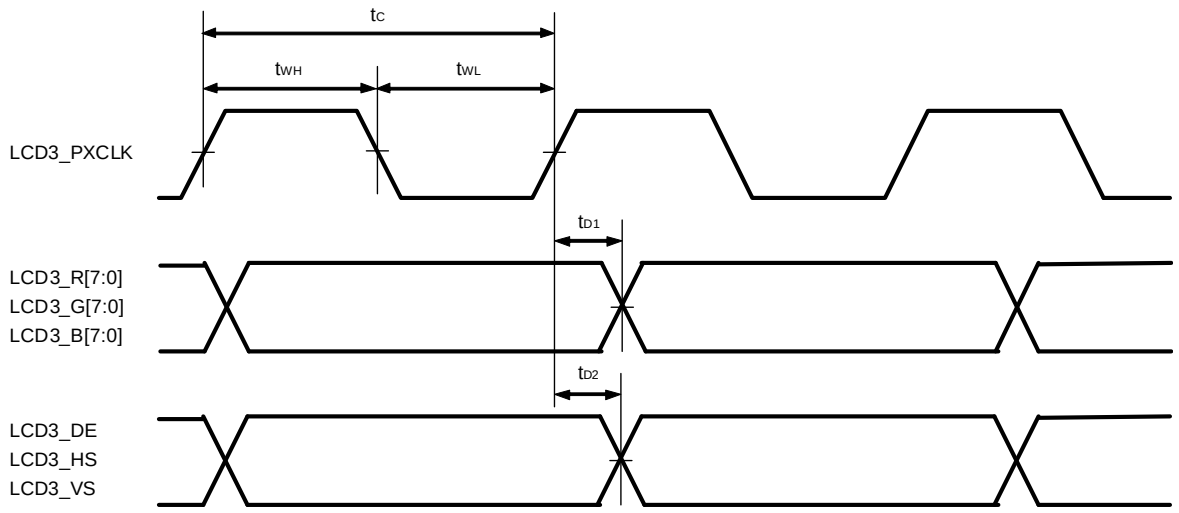
(1) LCD interface

（VDD33＝3.3±0.3 V, input pin : Normal , Drive=8mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD3_PXCLK output cycle	t_C	—	10	—	—	ns
LCD3_PXCLK high-level width	t_{WH}	—	4	—	—	ns
LCD3_PXCLK low-level width	t_{WL}	—	4	—	—	ns
LCD3_R/G/B[7:0], LCD3_HS, LCD3_VS and LCD3_DE data delay time	t_{D1}	LCD3_R/G/B[7:0]	1	—	6	ns
	t_{D2}	LCD3_HS, LCD3_VS, LCD3_DE	1	—	6	ns

Remark The setting of the rise and fall timing for LCD3_PXCLK is based on the valid edge set by the CLKPOL value in the LCD control register (rising: CLKPOL = 0, falling: CLKPOL = 1).

Figure 2-18. LCD Interface Timing



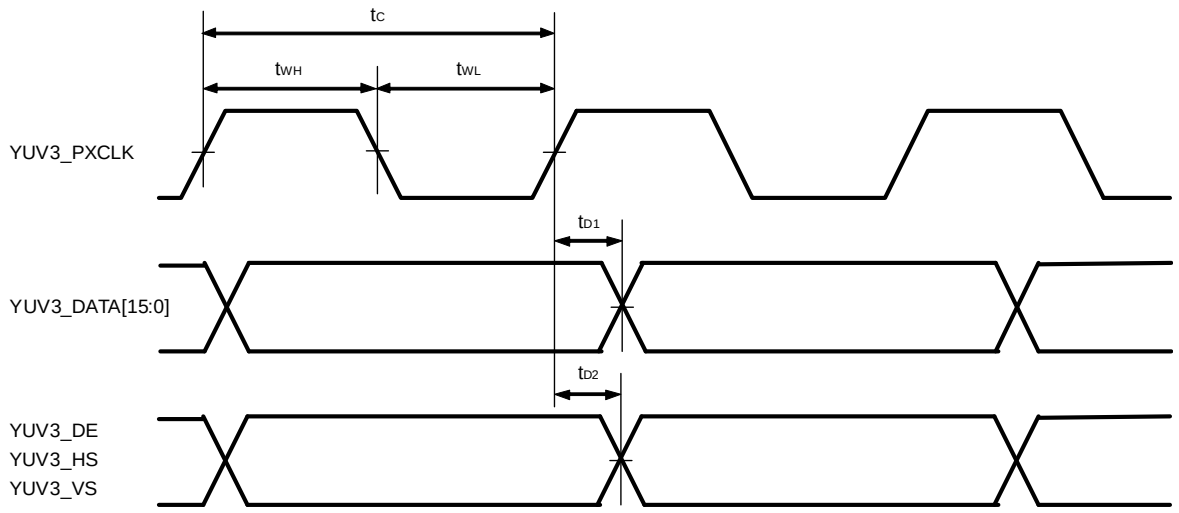
(2) YUV interface

（VDD33＝3.3±0.3 V, input pin : Normal , Drive=8mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
YUV3_PXCLK output cycle	t_C	—	10	—	—	ns
YUV3_PXCLK high-level width	t_{WH}	—	4	—	—	ns
YUV3_PXCLK low-level width	t_{WL}	—	4	—	—	ns
YUV3_DATA[15:0], YUV3_HS, YUV3_VS, YUV3_DE data delay time	t_{D1}	YUV3_DATA[15:0]	1	—	6	ns
	t_{D2}	YUV3_HS, YUV3_VS, YUV3_DE	1	—	6	ns

Remark The setting of the rise and fall timing for YUV3_PXCLK is based on the valid edge set by the CLKPOL value in the LCD control register (rising: CLKPOL = 0, falling: CLKPOL = 1).

Figure 2-19. YUV Interface Timing



2.5.9 USB interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB_CLK cycle (24MHz)	$T_{cycUCLK24}$	—	—	24	—	MHz

Note ±500 ppm (± 100ppm recommendation)

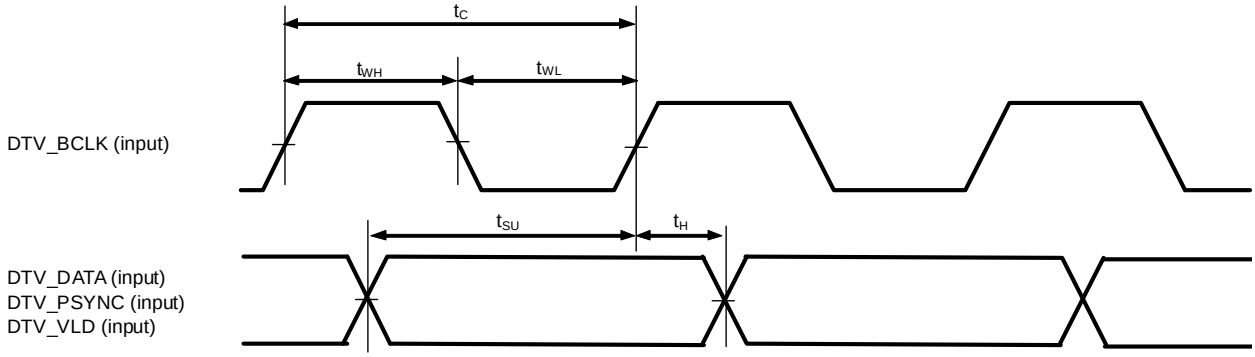
Refer to USB Specification Revision2.0 about AC and DC characteristics in a USB port.

2.5.10 Digital terrestrial TV interface

（VDD33＝3.3±0.3 V, input pin : schmitt , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DTV_BCLK input cycle	t_C	－	25	－	－	ns
DTV_BCLK high-level width	t_{WH}	－	10	－	－	ns
DTV_BCLK low-level width	t_{WL}	－	10	－	－	ns
DTV_DATA, DTV_PSYNC, DTV_VLD setup time	t_{SU}	－	6	－	－	ns
DTV_DATA, DTV_PSYNC, DTV_VLD hold time	t_H	－	0	－	－	ns

Figure 2-20. DTV Interface Timing



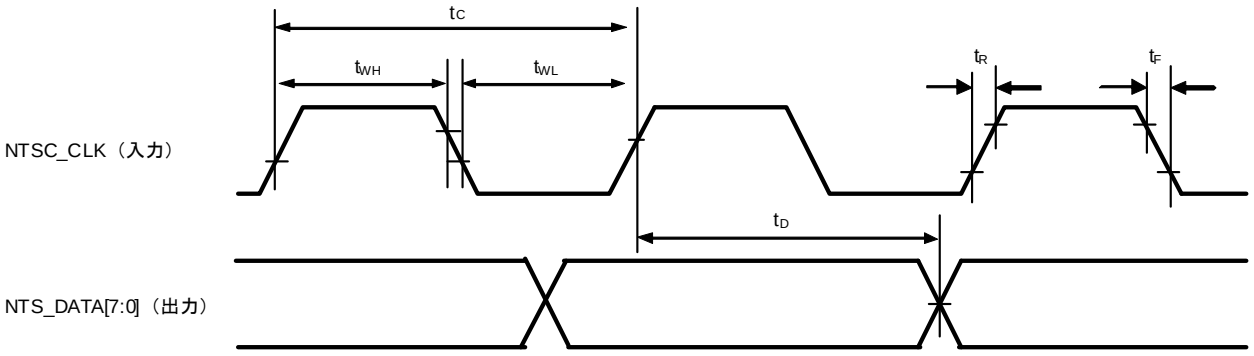
2.5.11 ITU-R BT.656 interface

（VDD33＝3.3±0.3 V, input pin : Normal (only clock is Schmitt) , Drive=8mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NTSC_CLK input cycle	t_C	—	—	37[Note]	—	ns
NTSC_CLK high-level width	t_{WH}	—	13	—	—	ns
NTSC_CLK low-level width	t_{WL}	—	13	—	—	ns
NTSC_CLK rise time	t_R	—		—	5	ns
NTSC_CLK fall time	t_F	—		—	5	ns
NTSC_DATA output delay time	t_D	Rising edge of NTSC_CLK	4	_	18	ns

Note NTSC_CLK = 27 MHz

Figure 2-21. NTSC Interface Timing

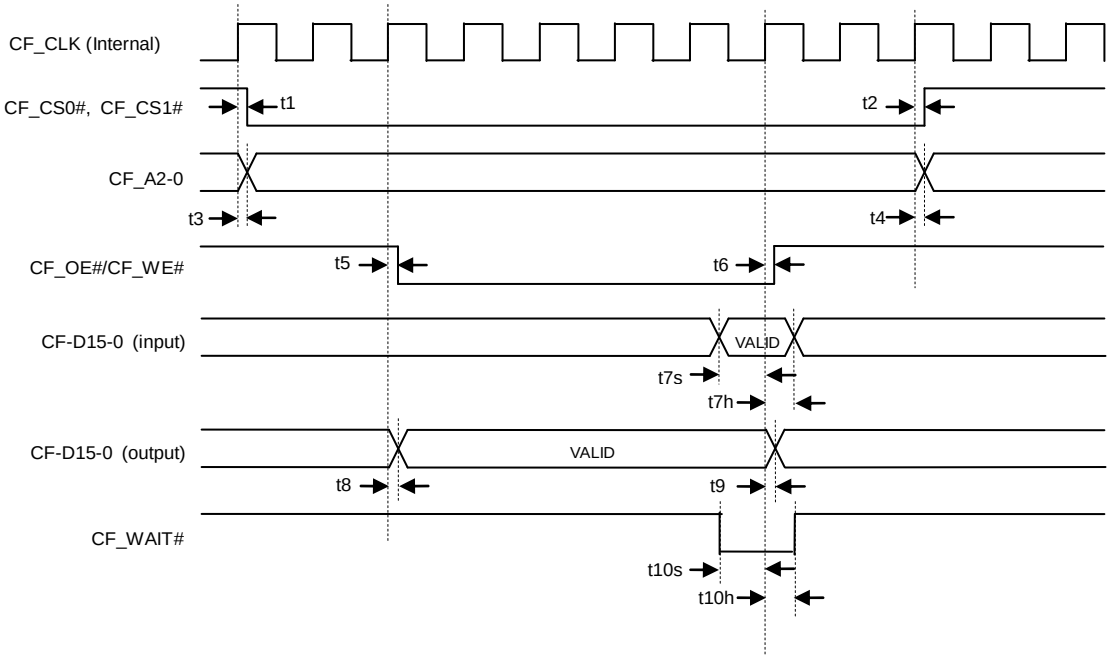


2.5.12 CF card interface (PIO mode)

（VDD33＝3.3±0.3 V, input pin : schmitt , Drive=4mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CF_CLK frequency	–	–	–	–	100	MHz
CF CLK cycle	–	–	10	–	–	ns
Until CF_CS0#, CF_CS1# becomes active	t1	–	–	–	11	ns
Until CF_CS0#, CF_CS1# becomes inactive.	t2	–	–	–	11	ns
The delay until CF_A2-0 becomes effective	t3	–	–	–	12	ns
The delay until CF_A2-0 becomes invalid	t4	–	–	–	12	ns
Until CF_OE#, CF_WE# becomes active	t5	–	–	–	12	ns
Until CF_OE#, CF_WE# becomes inactive.	t6	–	–	–	12	ns
Data setup time	t7s	–	8	–	–	ns
Data hold time	t7h	–	0	–	–	ns
The delay until data becomes effective	t8	–	–	–	11	ns
The delay until data becomes invalid	t9	–	–	–	11	ns
CF_WAIT# setup time	t10s	–	9	–	–	ns
CF_WAIT# hold time	t10h	–	0	–	–	ns

Figure 2-22. CF card Interface Timing (PIO mode)

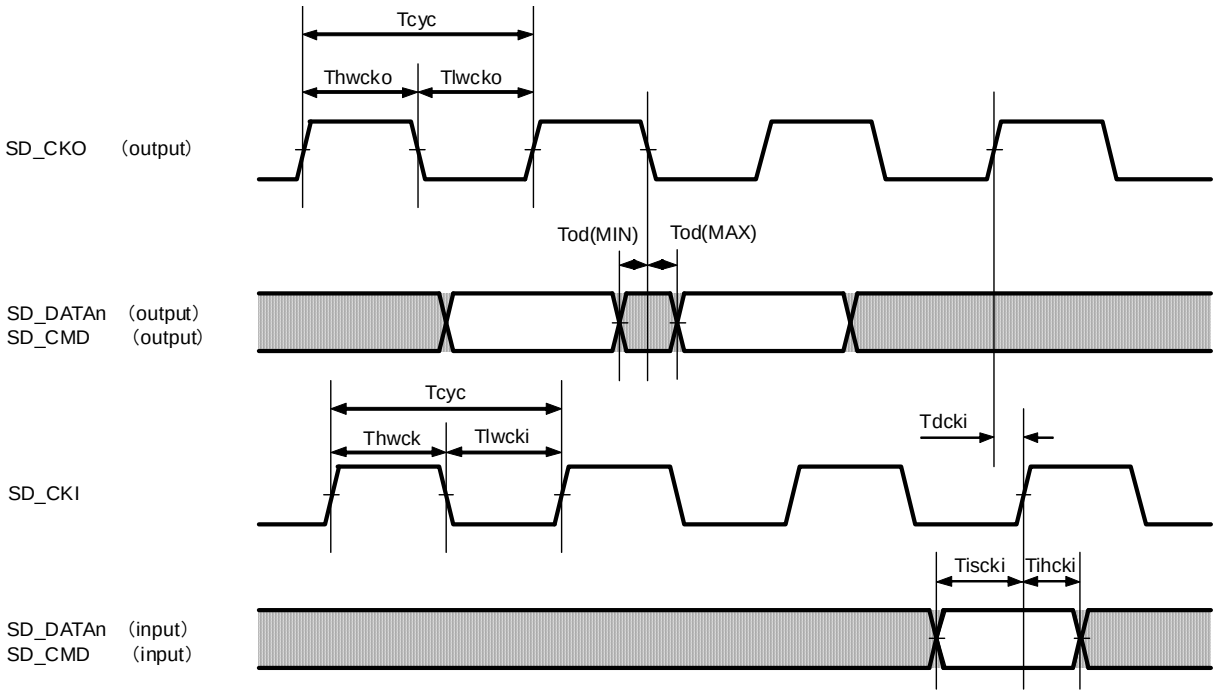


2.5.13 SD card interface

（VDD33＝3.3±0.3 V, input pin : schmitt, Drive=8mA, outside loop, CMD and Data is pull-up ）

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock cycle	T_{cyc}	—	20	—	—	ns
Output clock high-level width	T_{hwcko}	@50MHz	8.5	10	11.5	ns
Output clock low-level width	T_{lwcko}	@50MHz	8.5	10	11.5	ns
Output delay	T_{od}	—	-3	—	2	ns
Input clock high-level width	T_{hwcki}	@50MHz	8	—	11	ns
Input clock low-level width	T_{lwcki}	@50MHz	8	—	11	ns
Input clock delay time	T_{dcki}	—	0	—	6	ns
Setup time	T_{iscki}	—	2	—	—	ns
Hold time	T_{ihcki}	—	1	—	—	ns

Figure 2-23. SD card Interface Timing



Remark n = 0 to 3

2.5.14 SDRAM Interface

(1) DDR2-533

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DDR_CK, DDR_CKB cycle time	t_{CK}	—	3.75	—	8	ns
DDR_CK, DDR_CKB high level width	t_{CKH}	—	0.45	—	0.55	t_{CK}
DDR_CK, DDR_CKB low level width	t_{CKL}	—	0.45	—	0.55	t_{CK}
Address/Command terminal delay time	t_{CKSQ}	Note1	-1	—	1	ns
DDR_DQx, DDR_DMy output valid time Note2	t_{DQSDQ}	From DDR_DQSy	—	—	$0.25t_{ck}$-0.5	ns
DDR_DQx, DDR_DMy output skew time Note2	t_{DQSQO}	—	—	—	0.35	ns
DDR_DQSy output delay time	t_{DQSS}	—	-0.20	—	0.20	t_{CK}
DDR_DQx hold time Note2	T_{QH}	—	1.27	—	—	ns
DDR_DQx input skew time	t_{DQSQI}	From DDR_DQSy	—	—	0.32	ns
DDR_DQSy input access time	t_{DQSCK}	From CK	—	—	1	ns

Remark x = 0 to 31 y = 0 to 3

Register setting can adjust the delay time to DDR_CK/DDR_CKB, DQ/DM output, DQS output and DQS input.

Note **1** : DDR_A[14:0], DDR_BA[2:0], DDR_CSB[1:0], DDR_CKE[1:0], DDR_RASB, DDR_CASB, DDR_WEB

2 : The specification during a signal in the following each group.

1) DDR_DM[0], DDR_DQ[7:0]
2) DDR_DM[1], DDR_DQ[15:8]
3) DDR_DM[2], DDR_DQ[23:16]
4) DDR_DM[3], DDR_DQ[31:24]

Figure 2-24. DDR2 Output Timing

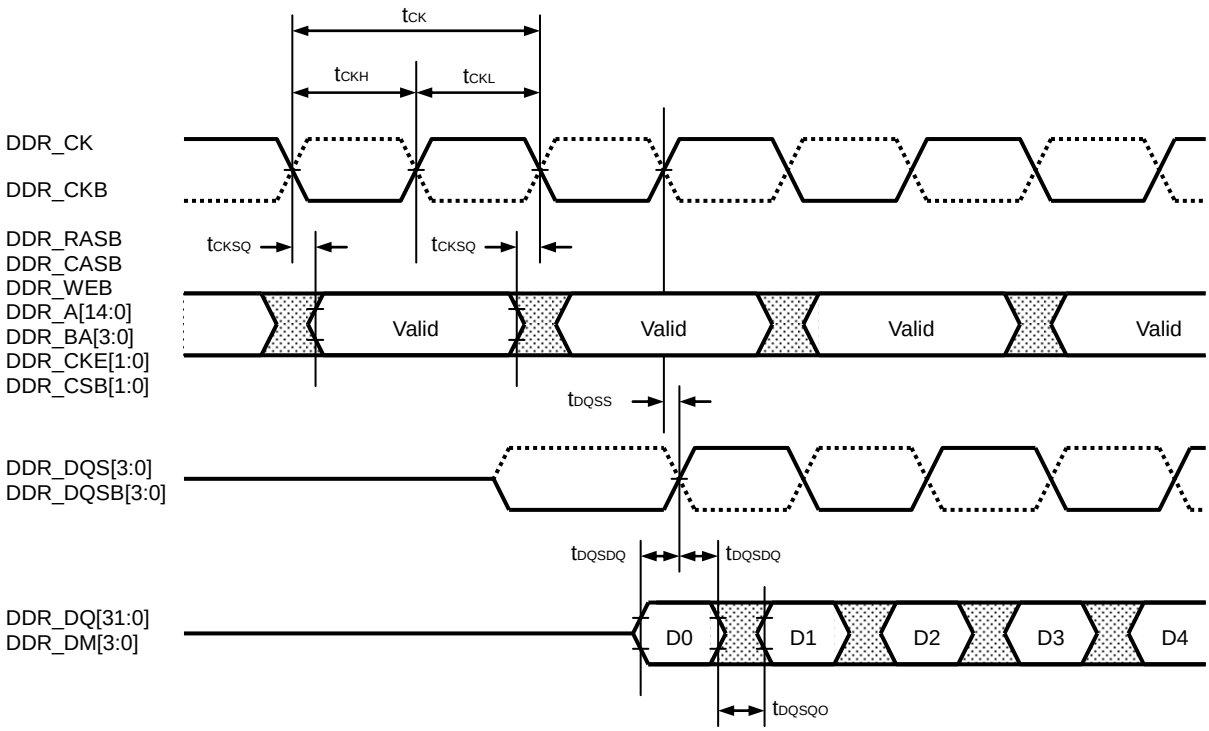
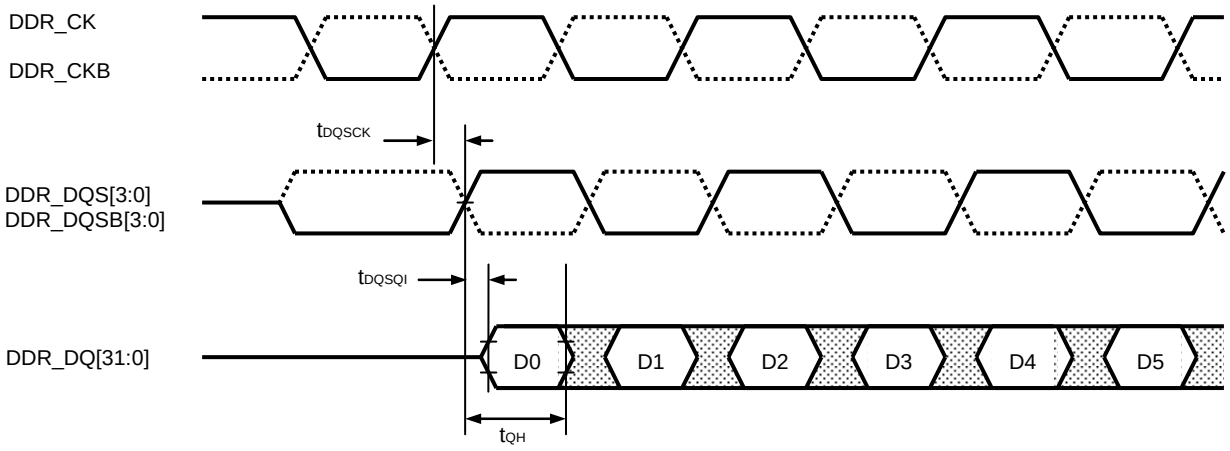


Figure 2-25. DDR2 Input Timing



(2) LPDDR-400

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
DDR_CK, DDR_CKB cycle time	t_{CK}	—	5	—	100	ns
DDR_CK, DDR_CKB high level width	t_{CKH}	—	0.45	—	0.55	t_{CK}
DDR_CK, DDR_CKB low level width	t_{CKL}	—	0.45	—	0.55	t_{CK}
Address/command terminal delay time Note1	t_{CKSQ}	From DDR_CK	-0.8	—	0.8	ns
DDR_DQx, DDR_DMy output valid time Note2	t_{DQSDQ}	From DDR_DQSy	$0.25t_{ck}$-0.6	—	—	ns
DDR_DQx, DDR_DMy output skew time Note2	t_{DQSQO}	—	—	—	0.8	ns
DDR_DQSy output delay time	t_{DQSS}	—	0.8	—	1.2	t_{CK}
DDR_DQSy input delay time	t_{DQSCK}	From DDR_CK	2.0	—	5.2	ns
DDR_DQx input skew time	t_{DQSQI}	From DDR_DQSy	—	—	0.5	ns
DDR_DQx hold time Note2	t_{QH}	From DDR_DQSy	1.7	—	—	ns

Remark x = 0 to 31 y = 0 to 3

Register setting can adjust the delay time to DDR_CK/DDR_CKB, DQ/DM output, DQS output and DQS input. The specification after a delayed adjustment is prescribed.

Note **1** : DDR_A[14:0], DDR_BA[2:0], DDR_CSB[1:0], DDR_CKE[1:0], DDR_RASB, DDR_CASB, DDR_WEB

2 : The specification during a signal in the following each group.

1) DDR_DM[0], DDR_DQ[7:0]
2) DDR_DM[1], DDR_DQ[15:8]
3) DDR_DM[2], DDR_DQ[23:16]
4) DDR_DM[3], DDR_DQ[31:24]

Figure 2-26. LP-DDR Output Timing

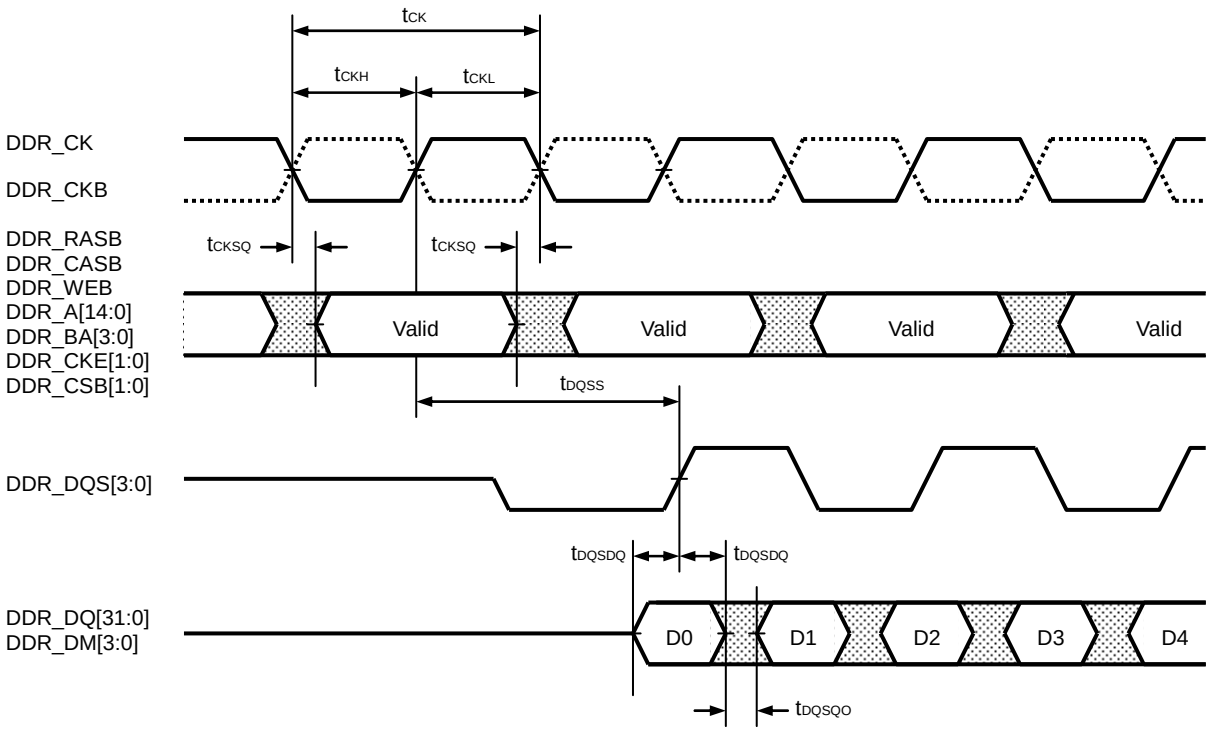
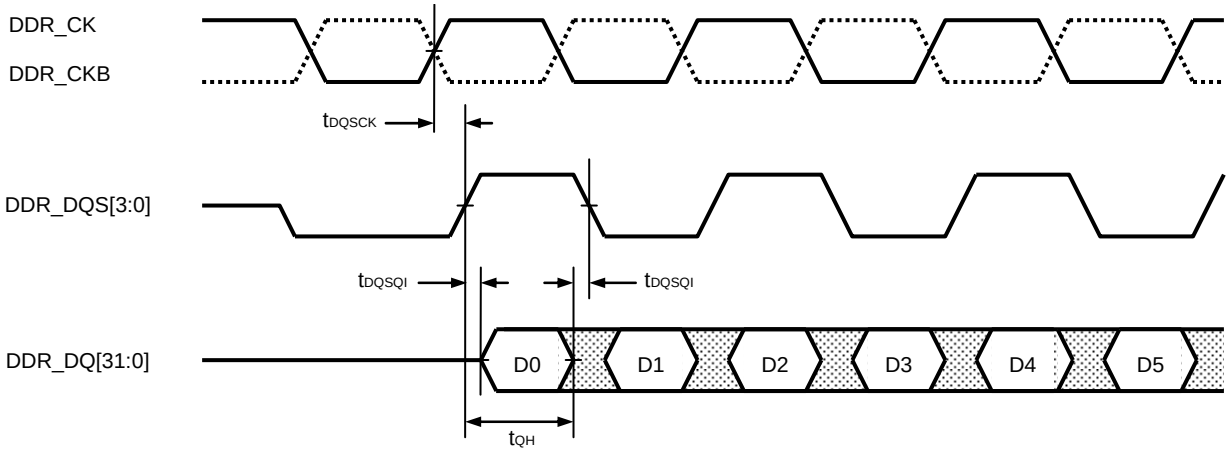


Figure 2-27. LP-DDR Input Timing

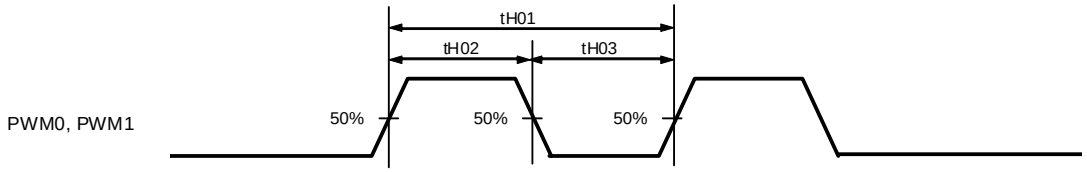


2.5.15 PWM Interface

（VDD33＝3.3±0.3 V,input pin : normal, Drive=4mA)

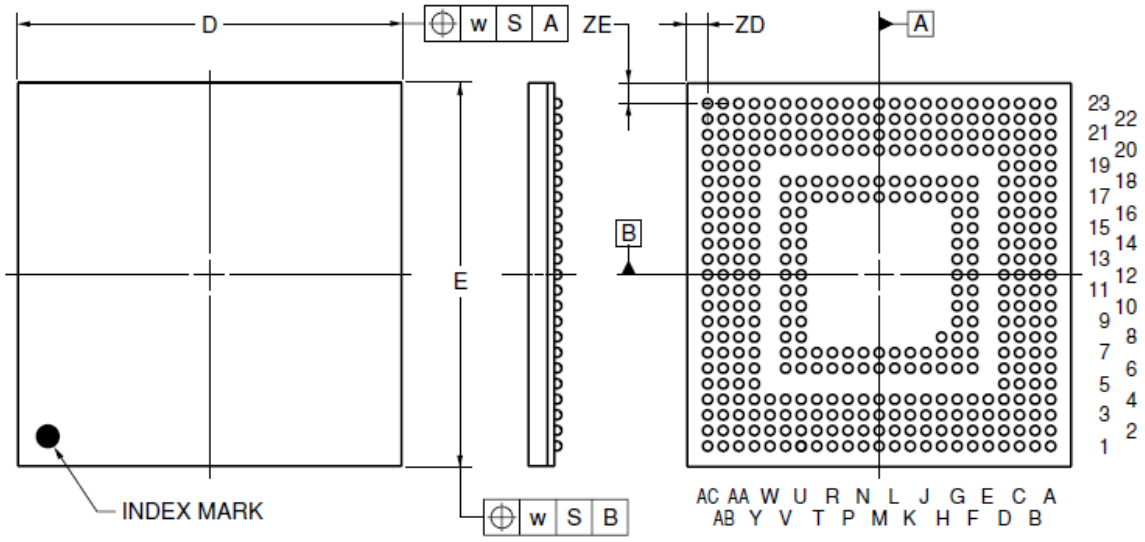
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output cycle	tH01	—	50	—	1000	ns
High level width	tH02	—	25	—	500	ns
Low level width	tH03	—	25	—	500	ns

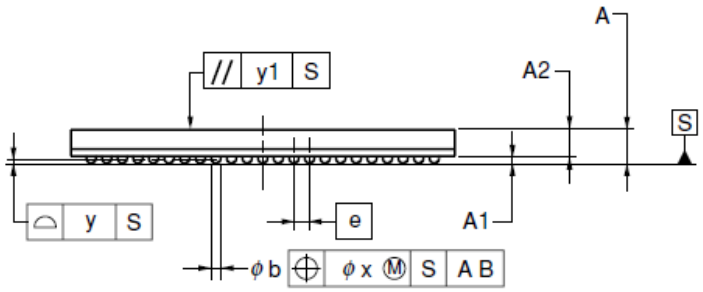
Figure 2-28. PWM Interface Timing (Transmission)



3. PACKAGE DRAWING

393-PIN PLASTIC FBGA (16x16)





(UNIT:mm)

ITEM	DIMENSIONS
D	16.00±0.10
E	16.00±0.10
w	0.20
A	1.41±0.10
A1	0.30±0.05
A2	1.11
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.85
ZE	0.85

P393F1-65-GA9

REVISION HISTORY	EMMA Mobile EV2 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.0	February 8, 2010	—	—
2.0	February 18, 2010	—	2.5.6 SDIO interface specification modified. 2.5.14 SD card interface specification modified. 2.5.15 DDR2 SDRAM interface specification is added.
Provisional 3rd	February 26, 2010	—	1.2 Pin functions Buffer type added. 1.3 Pin I/O circuits added.
Provisional 4th	March 19, 2010	—	2.1 Absolute Maximum Ratings added. 2.2 Recommended Operating Conditions added. 2.3 Capacitance added. 2.4 DC Characteristics added. 2.5.1 AC test I/O measurement points added. 2.5.2 System control added. Incremental update from comments to the provisional 3rd.
Provisional 5th	July 23, 2010	—	2.5.13 Memory stick interface deleted. EM/EV1 is added. (The difference with EM/EV2 is mentioned.) Incremental update from comments to the provisional 4th. (A change part from the old revision is "★" marked in the page left end.)
Provisional 6th	August 4, 2010	—	Order Information added. 2.5.14(2) LP-DDR SDRAM Interface specification added. Incremental update from comments to the provisional 5th. (A change part from the old revision is "★" marked in the page left end.)
Provisional 7th	August 6, 2010	—	2.5.15 PWM Interface Specification added. Incremental update from comments to the provisional 6th. (A change part from provisional 4th is "★" marked in the page left end.)
3.0	August 23, 2010	—	Regular version issue
4.0	September 30, 2010	—	ARM logo added. (Face page) Incremental update from comments to the provisional 3.0. (A change part from 3.0 is "★" marked in the page left end.)
5.0	February 10, 2011	—	Order Information changed. AC Characteristics changed. (IIC, SDIO, SDC, SDRAM) Incremental update from comments to the provisional 4.0. (A change part from 4.0 is "★" marked in the page left end.)
6.0	April 15, 2011	—	AC Characteristics changed. (Asynchronous bus, SDRAM Interface) Incremental update from comments to the provisional 5.0. (A change part from 5.0 is "★" marked in the page left end.)

Rev.	Date	Description	
		Page	Summary
7.0	May 31, 2010	—	Incremental update from comments to the provisional 6.0. (A change part from 6.0 is “★” marked in the page left end.)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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