Document Reference Code

CN-01

Low Side Synchronous Buck

Overall sizing V0.9

Document summary :

This document justify the sizing of the elements used for the one phase solid state transformer that will be the first version of the OwnTech hardware. A methodology is presented to determine an optimal transformer ratio that minimize the loss for the dual active bridge, and takes into account the input boost converter constraints.

Diffusion : External, Internal, or Confidential

Date	Revision	Creator	Reviewer	Approver	Status
	D				
	C				
	B				
	A				
25/06/2020	-	ALINEI	VILLA	VILLA	PREL

Preliminary PREL, Good For Execution GFE, As Built ASB

Table of Content

1. Introduction

The studied power topology is composed of three standard power converters. A low voltage high current synchronous buck, a dual active bridge and a second high voltage low current synchronous buck. This power architecture enables bidirectional power conversions, with high gain capabilities to switch from standard grid AC voltage levels to virtually any electrical appliances requiring lower voltages to operate. An important application of this bidirectional operation mode is to inject power to a grid from low voltage sources such as batteries.

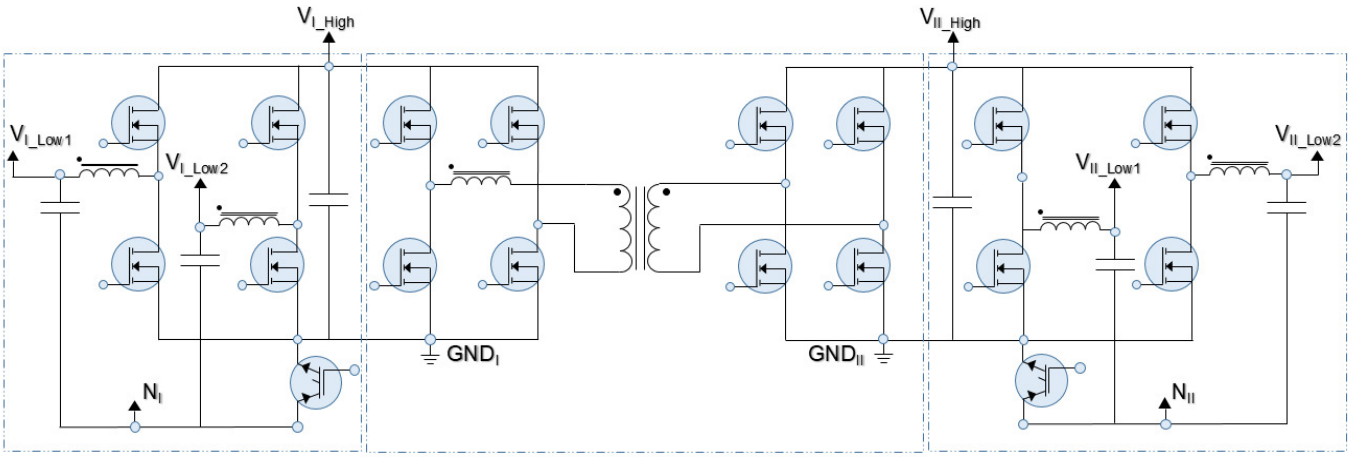


Figure 1 One phase SST power topology

From a design perspective, the objective is to obtain maximal efficiency on the broadest number of power applications while minimizing costs.
To tackle this challenge, the problem is broken down in representative case studies :

	Function	Input	Output
Low to high voltage power flow	Battery inverter	12V	$230V_{Ac}$
	Battery inverter	24V	$230V_{Ac}$
	Battery inverter	48V	$230V_{Ac}$
	Battery inverter	72V	$230V_{Ac}$
High to low voltage power flow	Battery charger	$230V_{Ac}$	12V
	Battery charger	$230V_{Ac}$	24V
	Battery charger	$230V_{Ac}$	48V
	Battery charger	$230V_{Ac}$	72V

Table 1 Case studies taken into account for the global sizing of the power architecture

These cases are representative of the SST power architecture wide operating range. They allow the operation for the system on the target low voltage DC bus levels while imposing constraints on the high voltage DC bus levels which guarntee the 230VAc operation.

From this case studies specification we can derive the intermediate voltage level both on the V_{I_High} and V_{II_High} DC links. The V_{II_High} link minimal voltage is imposed by the output voltage of the inverter stage.

$$V_{II\_Hi\_min} = \sqrt{2}\ \text{x}\ 230\text{V} + 25\text{V} = 350\text{V}$$

The 25V margin allows an increase in efficiency of the inverter and prevents its saturation at high or low duty cycles. For safety, we have chosen a minimal V_{II_High} voltage of 400V.

The maximal V_{II_High} level is constrained by the high side switching device technology. In order to lower cost, state of the art 650V Si MOSFET will be used. In this context we define a maximal V_{II_High} link voltage of 450V.

$$400V < V_{II\_High} < 450V$$

This V_{II_High} constraint will be used to design the high side synchronous buck.

frequency dual active bridge topology. This is due to the fact that the voltage gain needed at the low side synchronous buck while it operates in boost mode depends indirectly on the transformer turn ratio to match the V_{II_High} link voltage constraints.

From a gain persepective we must ensure that :

$$G_{Boost} \times G_{DAB} \times V_{I\_Low} = V_{II\_High}$$

In practice we have some constraint on G_{Boost}

High gain are limitated by the effective series resistor (ESR) of the boost topology, coming from the practical copper losses of the boost inductor.

The voltage converting ratio of the boost converter accounting for the ESR is given by the equation below

$$\frac{Vout}{Vin} = \frac{1}{1-D} \times \frac{1}{\left(1+\frac{R_L}{(1-D)^2 R}\right)}$$

Where RL is the inductor parasitic resistance
R is the load resistance
D is the duty cycle

Source : https://www.onsemi.com/pub/Collateral/AN-5081.pdf.pdf

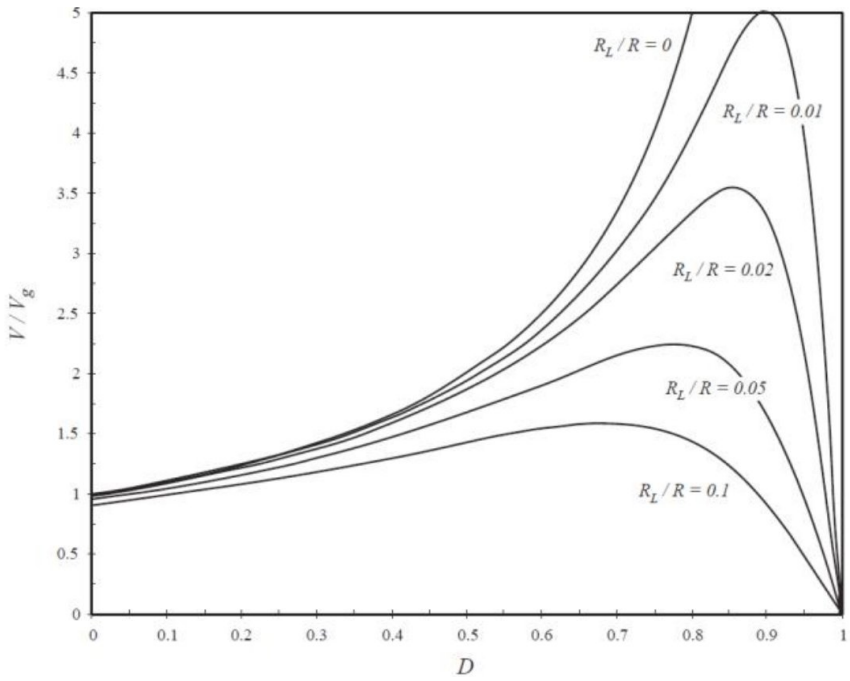


Figure 2 : Boost converter Gain evolution for different R_L/R ratios

The boost converter will be design in such a way that RL/R < 0.002
In practice we make sure that the duty cycle doesn't exceed 0.8

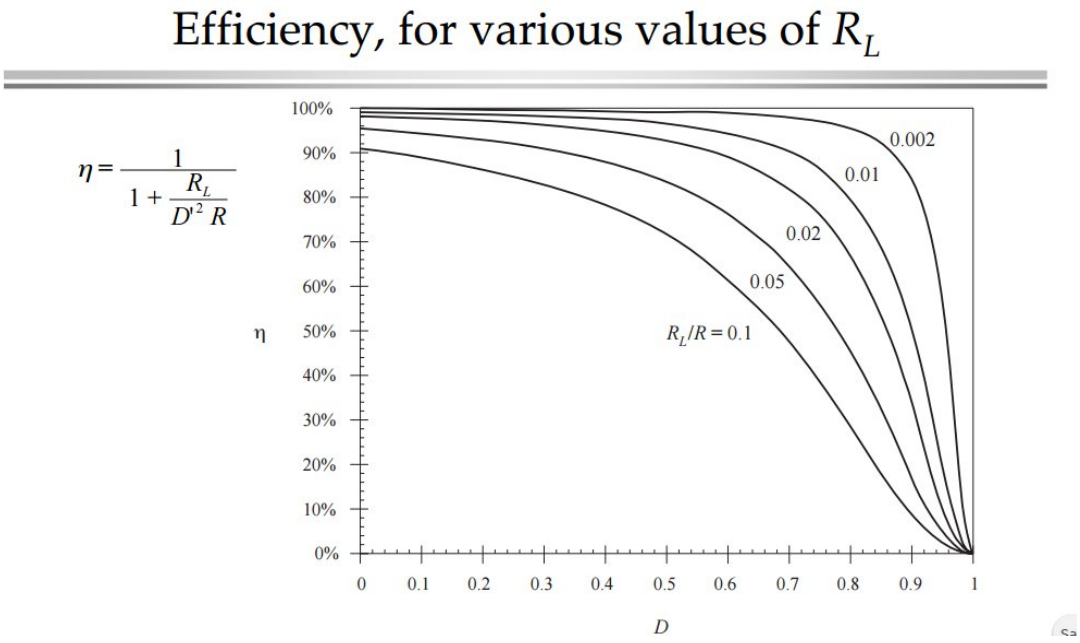


Figure 3 : Boost converter efficiency evolution for different R_L/R ratios

The sycnhronous buck maximal boost constraint can be derived from these two hypothesis

$$G_{Boost} < 5$$

From this possible gain we can derive voltage range of V_{I_High} for the cases studies defined in page 1.
Here, rough calculation are made without considering the R_L/R loss ratio, in practice, duty cycles are to be greater to take it into account.

$V_{I\_Low\_min}$	$V_{I\_Low\_max}$		G_{Boost}	D	$V_{I\_High\_min}$	$V_{I\_High\_max}$	
12	15	V_{DC}	5	0,8	60	75	V_{DC}
24	28	V_{DC}	2,86	0,65	69	80	V_{DC}
48	55	V_{DC}	1,43	0,3	69	79	V_{DC}
72	80	V_{DC}	1,11	0,1	80	89	V_{DC}

The voltage level at V_{I_High} is

$$60V_{DC} < V_{I\_High} < 90V_{DC}$$

If we recall the voltage constraint on V_{II_High}

$$400V < V_{II\_High} < 450V$$

We can derive the turn ratio necessary to obtain the required G_{DAB}

$$G_{DAB} = \eta_{turn} \times M(D_{DAB})$$

Where $M(D_{DAB})$ is the gain controled by the duty cycle of the DAB. This gain can not be over than 1 when using single phase shift modulation to control the DAB.

In a first approach it is planned to operate the DAB with a single phase shift modulation, which is the easiest control technic.

The gain of the Dual Active Bridge (DAB) is constrained by its Zero Voltage Switching locus. The highest efficiency are obtained when the gain is equal to the transforming turn ratio.

The efficiency falls drastically when the converter is put away from its ZVS operating range, either when the gain is far from 1 or when operating at light loads.

This means that the turn ratio will directly impact the $M(D_{DAB})$ required to respect the V_{II_High} voltage range specified earlier, and as a consequence will have a direct impact on the overall efficiency.

A good n_{turn} choice will provide enough gain to rise the lowest V_{I_High} to the lowest V_{II_High}, while maintaining a $M(D_{DAB})$ close to one when V_{I_High} is maximal, without tresspassing the maximal V_{II_High} voltage level.

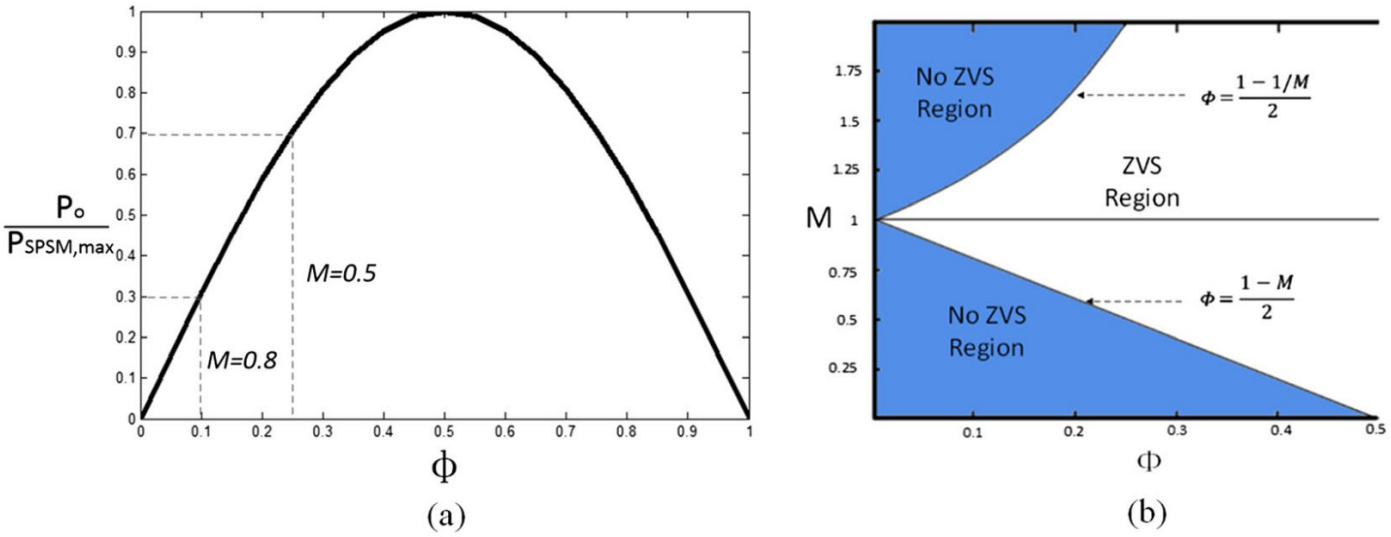


Figure 4 (a) Normalized output power characteristic of single phase-shift modulation (b) zero voltage switching characteristic (ZVS) of single phase-shift modulation when M varies from 0 to 2 and the phase shift is from 0 to 0.5

$V_{I\_Low\_min}$	$V_{I\_Low\_max}$	$V_{I\_High\_min}$	$V_{I\_High\_max}$	n_{turn}	$M(D_{DAB})$	$M(D_{DAB})$	$V_{II\_High\_min}$	$V_{II\_High\_max}$
12	15	60	75	6	1	1	360	450
24	28	69	80	6	1	0,93	411	446
48	55	69	79	6	1	0,95	411	448
72	80	80	89	6	0,93	0,84	446	448

For a turn ratio of 6 we see that we can not obtain the minimal 400V when VI_Low_min is 12V.

$V_{I\_Low\_min}$	$V_{I\_Low\_max}$	$V_{I\_High\_min}$	$V_{I\_High\_max}$	n_{turn}	$M(D_{DAB})$	$M(D_{DAB})$	$V_{II\_High\_min}$	$V_{II\_High\_max}$
12	15	60	75	7	1	0,85	420	446
24	28	69	80	7	0,92	0,8	442	448
48	55	69	79	7	0,9	0,8	432	440
72	80	80	89	7	0,8	0,72	448	448

For a turn ratio of 7 we see that we obtain an output compatible with the desired output range, but the $M(D_{DAB})$ is far from 1 leading to lower efficiencies.

When n_{turn} is higher than 6, the DAB can output 400V even at 12V, but at the cost of having lower efficiency for the rest of the operative range. In order not to penalize most cases, $n_{turn} = 6$ is retained as the transformer turn ratio.

$$n_{turn} = 6$$

Inductor sizing according to boost converter constraints

Design constraints

In order to determine the inductor value, it is necessary to introduce the power rating of the converter
From the power rating, the I_{I_Low} current level can be estimated.
From a general overview of the off the shelf component available, one could see that it is hard to find magnetics rated for more than 10amps for tens of uH inductance range
For the transformer, it is hard to find of the shelf references rated for more than 300W.
Hence, the vision is to design a unity block of 300W and to parrallel it to reach the application power ratings.

It is foreseen that the OwnTech converter prototype will be based on three 300W blocks, to be able to generate 900W of 1 phase AC or 900W of 3 phase AC.
Two currents will size the magnetics, the low side current will determine the size of the inductor, and the high side current will size the transformer.
For a given power rating, the current level will rise as VI_Low drop, and for the 12V case the current value will be limited to 8 amps, in order to pick an inductor rated for 10 amps.

Critical inductance value

To keep the boost converter to operate in discontinuous current mode (DCM), The inductor value must satisfy the following inequality

$$L > K(D) \times \frac{RT_s}{2} \qquad K(D) = D(1-D)^2$$

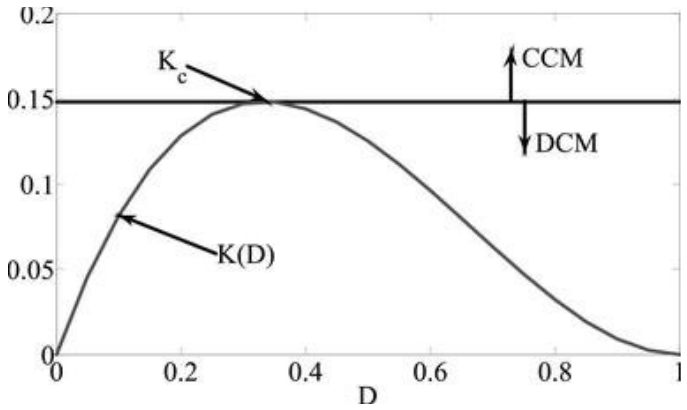


Figure 5 Evolution of K depending on the duty cycle

In our case the converter must be able to operate at any duty cycle to adapt the gain to any situation
Hence Kc = 0.15 is taken to derive the minimal L value called Lcrit in the following

V_{I_low}	I_{I_low}	n_legs	Pper_leg	Ptot	$I_{I\_High\_max}$	DCM boundary power	DCM boundary per leg	fsw
12	8	2	96	192	5	120	60	200000
24	7	2	168	336	5	120	60	200000
48	3,5	2	168	336	5	120	60	200000
72	2,7	2	194	389	5	120	60	200000

$V_{I\_High\_min}$	$V_{I\_High\_max}$	$R_{eq(min)}$ per phase	$R_{eq(max)}$ per phase	$R_{eq(min)}$	$R_{eq(max)}$	inductor value	inductor value
60	75	38	59	60	94	2,3E-05	3,5E-05
69	80	28	38	78	107	2,9E-05	4,0E-05
69	79	28	37	78	103	2,9E-05	3,9E-05
80	89	33	41	107	132	4,0E-05	4,9E-05

We choose the closest inductor value available, that cover most of the cases

L_chosen	0,000047	uH

Gain	$I_{transfo}$	D	I_{ripple}	I_{peak}
5	3,2	0,8	1,02	9,0
2,86	4,9	0,65	1,66	8,7
1,43	4,9	0,3	1,53	5,0
1,11	4,9	0,1	0,77	3,5

$$I_{\text{ripple}} = \frac{Vin * D}{L * fsw} \qquad REQ_{min} = \frac{Vmin^2}{P} \qquad REQ_{max} = \frac{Vmax^2}{P}$$

The current ripple gives the peak current flowing through the inductor for each considered case. The peak current sizes the saturation current of the inductor this saturation depend on the magnetic circuit of the core. The load current sizes the IL of the inductor, which depends on the omhic losses, and results in a +40°C temperature rise.

$$\frac{R_{inductor}}{R_{eq\_min}} \leq 0{,}002$$

Inductor parasitic resistance must be kept below	56	mΩ

Inductor sizing according to buck converter constraints

V_{I_High}	I_{I_Low}	nb_leg	V_{I_Low}	D	Il_high	Req	Lcrit	Fsw
60	8	2	12	0,20	1,6	1,5	3,00E-06	200000
70	7	2	24	0,34	2,4	3,43	5,63E-06	200000
70	3,5	2	48	0,69	2,4	13,7	1,08E-05	200000
90	2,7	2	72	0,80	2,16	26,7	1,33E-05	200000

DCM Boundary power (W)	DCM boundary per leg	$I_{I\_low\_boundary}$	Req_max	L
120	60	5,0	2,4	4,80E-06
120	60	2,5	9,6	1,58E-05
120	60	1,3	38,4	3,02E-05
120	60	0,8	86,4	4,32E-05

L choosen	47	uH

Foreseen inductor **Wurth 7443634700**

The choosen inductor value permits to stay above the DCM boundary for the defined power level.

Capacitor current stress calculation

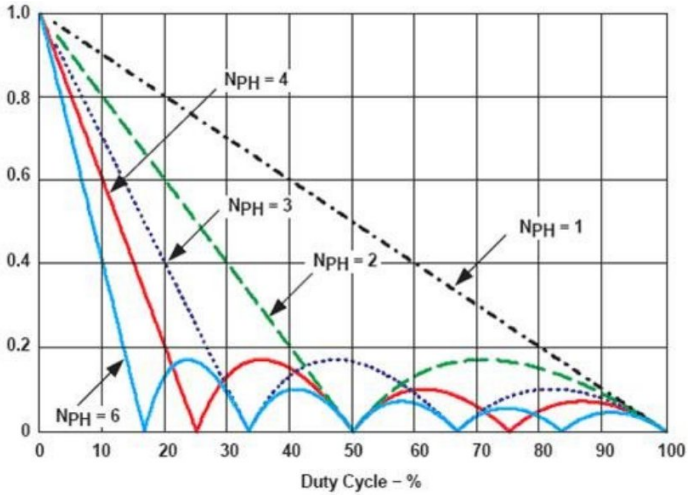


Figure 6 Buck output caps - Boost input caps normalized current stress

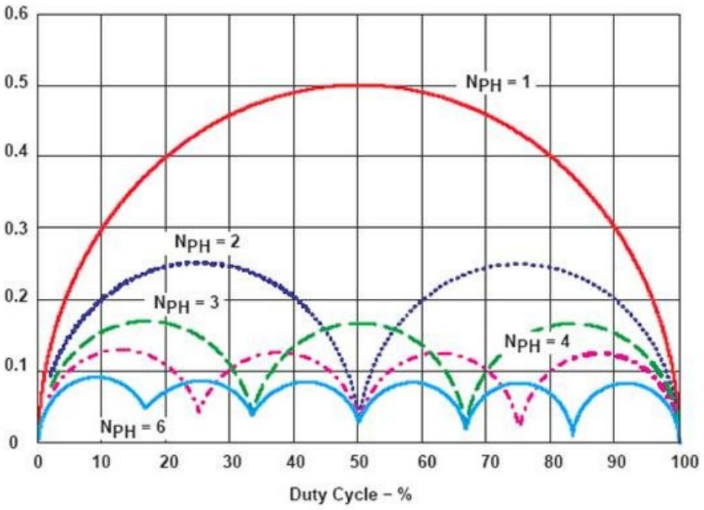


Figure 7 Buck input caps - Boost output caps normalized current stress

For sizing the capacitors we use two application notes, one giving equation for interleaved buck and one giving equations for interleaved boost.

Boost equations

Worst case for caps current stress is in High gain situation, for a duty cycle of arount 0.85.
Input current ripple is given for duty cycle > 0.5
Ico max is for max duty cycle which is 0.85

$$\Delta I_{in} = k_{in}(\delta - \frac{1}{2})T = \left(\delta - \frac{1}{2}\right)(2 - 2\delta)\frac{V_{out}T}{L_{in}}$$

Output current ripple is given for duty cycle > 0.5
Ico max is for max duty cycle which is 0.85

$$I_{CoRMS} = \frac{I_{out}}{2(1-\delta)}\sqrt{\frac{1}{2}(2\delta - 1)(2 - 2\delta)}$$

Buck equations

Worst case for caps current stress is in Low gain situation, for a duty cycle of arount 0.2

$$I_{CIN_{norm}(RMS)} = \sqrt{\left(D - \frac{m}{n}\right) \times \left(\frac{1+m}{n} - D\right)}$$

where

- $D = V_{OUT} / V_{IN}$
- n = # of phases
- m = floor $(n \times D)$

$$I_{COUT_{ripple,norm}} = \frac{n}{D \times (1 - D)} \times \left(D - \frac{m}{n}\right) \times \left(\frac{1+m}{n} - D\right)$$

m	1	
nb	2	
Vout	70	Vout
Fsw	200000	Hz
T	0,000005	s
L	0,000047	H
Dmax	0,85	
$I_{I\_High\_max}$	5	Arms
$I_{C\_I\_High}$	5,4	Arms
$\Delta I_{C\_I\_Low}$	0,8	A
$I_{C\_I\_Low\_RMS}$	0,5	Arms

VI_Low	12	27	53
VI_High	60	70	70
I_{I_High}	5,0	5,0	5,0
I_{I_Low}	25,0	13,0	6,6
m	0,00	0,00	1,00
D	0,20	0,39	0,76
$I_{C\_I\_High\_RMS}/I$	0,24	0,21	0,25
$I_{C\_I\_Low\_pp}/I_{C\_}$	0,75	0,37	0,68
$I_{C\_I\_High\_RMS}$	1,22	1,05	1,25
$I_{C\_I\_Low\_pp}$	18,75	4,82	4,49
$I_{C\_I\_Low\_RMS}$	9,38	2,41	2,24

The current ratings of the low side and high side caps are derived from the equation given page X.
As such, the spreadsheet above give us a current stress of :

$I_{C\_I\_low}$	9,4	A_{RMS}
$I_{C\_I\_high}$	5,4	A_{RMS}

In the following capacitors sizing will take these value as minimal current requirement.
High side and low side capacitors must be sized properly to withstand the current stress calculated.

Capacitor bank design - General design considerations

Both capacitor banks will be composed of film capacitors and MLCC capacitors.
The MLCC capacitors will be supplying the current while the film capacitor will provide the bulk capacitance to reach the desired voltage ripple.
MLCC caps will be class 2 caps, X7R type
Two MLCC values will be choosen with different capacitance to mix their frequency response

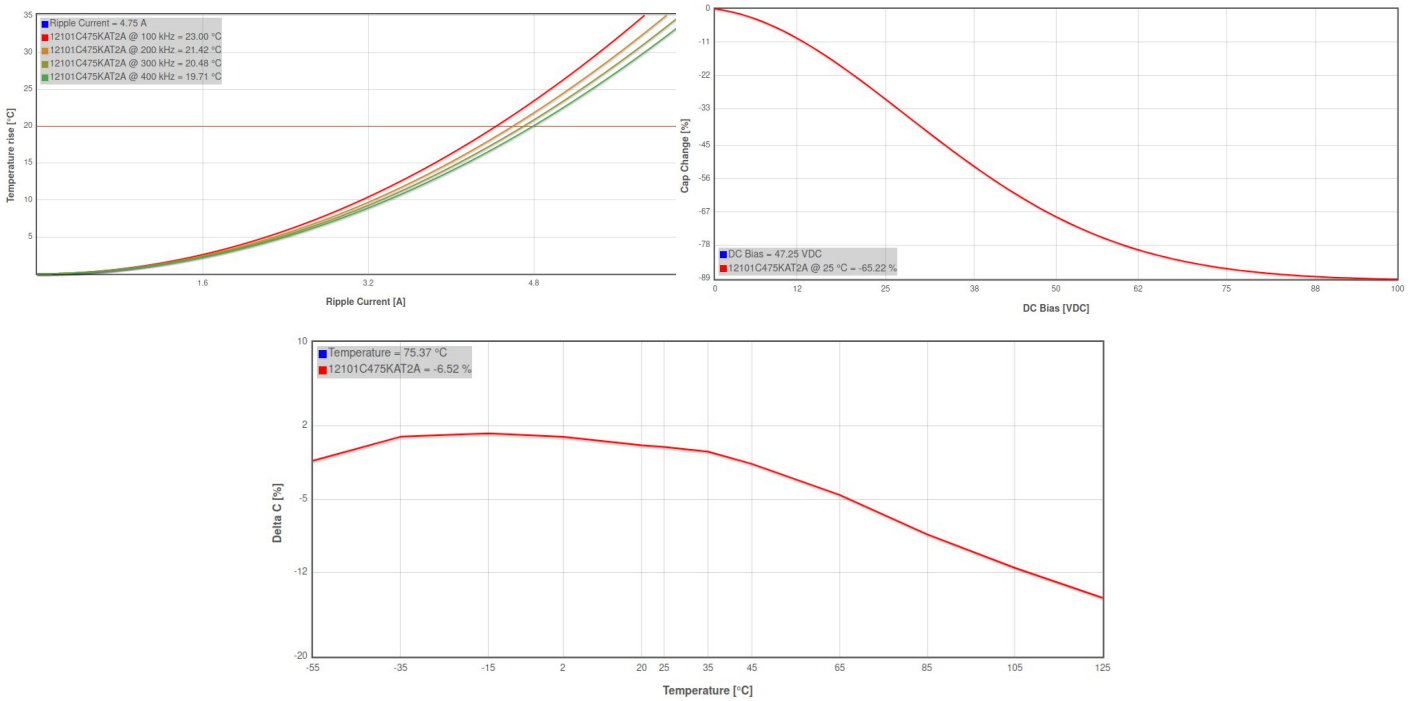


Figure 8 Ripple current of a 4,7uF 100V X7R 1210 capacitor - DC bias of the same cap - Temp bias of the same cap.

The low side capacitance must be sized for a voltage ripple of 1% of the DC voltage supplied to the application
The worst case scenario is when supplying 12VDC - the voltage ripple must be below 120mV

The high side capacitance must be sized for the DC bus voltage, between 60V and 90V. The voltage ripple depends on the input requirement of the DAB topology. This voltage is an internal DC bus, not meant to be delivered for the customer application. 3% of voltage ripple is considered good enough.

For sake of conservatism, two 100V MLCC will be placed in serie to withstand any voltage spike that might occur.
On the high side, the large DC bias lower drastically the capacitance of the MLCC. A 70% capacitance derating must be taken into account according to the supplier datasheets.

Derating 12101C475KAT2A		15V	27V	53V
Normal temp +20°C rise	40°C	-14%	-34%	-73%
Temperature when in hot environment +20°C rise	80°C	-15%	-37%	-78%

Source https://spicat.avx.com/product/mlcc/chartview/12101C475KAT2A

Voltage ripple

Buck mode, low side voltage ripple

Low side capacitance is derived from the table below.

V_{I_Low}	12	27	53	V
ΔV_{I_Low}	2,5%	1,0%	0,5%	%
ΔV_{I_low}	0,3	0,27	0,265	V
nb	2	2	2	-
Fsw	400000	400000	400000	Hz
Ipp	18,8	4,8	4,5	A
C_{I_Low}	2,0E-05	5,6E-06	5,3E-06	F

Here Fsw is nb*fsw as the cap current switching frequency is depending on the leg number

$$C_{OUT,Ripple} = \frac{I_{PP}}{8 \times f_{sw} \times \Delta V_{OUT(DC)}}$$

Nominal current ripple current per capacitor (+20°C T rise)				4,5	A_{RMS}
Nominal capacitance per capacitor				4,7	uF
Capacitor cost (1000units)				0,6	€
ESR @200kHz				0,0062	Ω
	15V	27V	53V		
40°C	3,9	3,0	1,2	A_{RMS}	
80°C	3,8	2,8	1,0	A_{RMS}	
40°C	4,0	3,1	1,3	uF	
80°C	4,0	3,0	1,0	uF	

Table 2 Corrected current capabilities and capacitance per capacitor depending on voltage and temperature

	15V	27V	53V
40°C	3	1	2
80°C	3	1	3

Minimal capacitor to withstand the I_{I_low} current ripple			3	
An extra capacitor is added for sake of conservatism			4	
Cost of the required MLCC caps			2,4	€

40°C	16,1	12,3	5,1	uF
80°C	15,9	11,9	4,1	uF

Polypropylene film capacitor is selected to provide the bulk capacitance to reach the desired voltage ripple
This technology has a good frequency stability, really low parasitic ESR and ESL.
Although, it has a lower capacitance density compared with PET or PEN
This film technology has really good durability in humid conditions and has good resistance to fungus.

The main drawback of PP is it poor maximal operating temperature. In our case, temperature is not the main concern as the converter is designed to operate in temperature not exceeeding 60°C

A 160VDC 10uF PP wound type capacitor is presented for the task. R75GR51004000J

		Capacitance		10	uF	
		Cost (per 500units)		1,9	€	
		15V	27V	53V	Cost	
Missing capacitance	80°C	4	-6,3	1,2		uF
Number of film capacitor	80°C	1	0	1	4,3	€
Number of equivalent MLCC	80°C	1	-2	2	3,6	€
Total capacitance (MLCC case)	80°C	23,91	17,78	6,13		uF
Total ESR @200kHz (MLCC case)		0,00103	0,00103	0,00103		Ω

Full MLCC option seem cheaper for low voltages. And more compact
Film capacitor source :
generaltechnicalinformation.pdf

Boost mode, high side voltage ripple

Conservative case is when the boost converter operate at high gain, with light load.

$$C_{I\_High} = \frac{V_{I\_High} \times D}{f_{sw} \times R \times \Delta_{VI\_High}}$$

In this case, we choose a DeltaVout below 0,5V

Conservative formula for 1 phase boost converters

DeltaV$_{I_High}$	0,5%	0,5%
DeltaV$_{I_High}$	0,3	0,45
V$_{I_High}$	60	90
Dmax	0,85	0,85
Fsw	200000	200000
Rmax	132	132
C$_{I_High}$	6,5E-06	6,5E-06

Current stress seen by the capacitor is given in page X, we recall :

I$_{C_I_high}$	5,4	**A$_{RMS}$**
Voltage ripple capacitance	6,45	uF

The voltage level on the high side require to place two 100V capacitors in series.
We recall the characteristics and derating table of 1210 X7R 100V class 2 MLCC capacitor below

Nominal current ripple current per capacitor (+20°C T rise)	4,5	**A$_{RMS}$**
Nominal capacitance per capacitor	4,7	**uF**
Capacitor cost (1000units)	0,6	**€**

Below we estimate the capacity derating of this MLCC capacitor with the elevation of DV voltage and temperature rise

Derating 12101C475KAT2A		15V	27V	45V	53V
Normal temp +20°C rise	40°C	-14%	-34%	-45%	-73%
Temperature when in hot environment +20°C rise	80°C	-15%	-37%	-49%	-78%

The derating to be considered is for VI_High between 60 and 90VDC. So between 30 and 45VDC per capacitor (2 in series)
As such, we consider a conservative -49% for the following calculations.

As such, a pair of series capacitor in worst operating conditions will have following characteristics

Maximal voltage	200	**V**
Current ripple (°20C)	1,10	**A_{RMS}**
Capacitance	1,15	**uF**
ESR @200kHz	0,0124	Ω

Hence, the required number of MLCC caps to supply the ripple current is :

Minimal capacitor to withstand the II_High current ripple	5	**pairs**
An extra capacitor is added for sake of conservatism	6	**pairs**

The minimal number of MLCC caps to reach the Voltage ripple specification is

Minimal capacitance to reach voltage ripple specification	6	**pairs**
Approximative high side capacitor cost :	7,2	**€**
ESR of the equivalent capacitor	0,0021	Ω
Total capacitance	6,90	**uF**

Transistors

The transistor choice has not been optimised yet. First prototypes will use IRFR4615 which is a 150V N channel DPAK mosfet from Infineon. A rough estimation of the losses is done below.
Transistors loss are evaluated in buck mode in conservative conditions where the duty cycle is about 0.8.

VILow	60	V
Fsw	200000	hz
Dmax	0,8	
Dmin	0,2	
Io	8	A
I_{RMS_LS}	7,16	A
I_{RMS_HS}	3,58	A

The foreseen mosfet is the IRFR4615 which as the following characteristics

IRFR4615			**IPD200N12N3 G**		
V_{DS}	150	V	**V_{DS}**	150	V
R_{DSon}	0,034	Ohm	**R_{DSon}**	0,016	Ohm
R_{DSon}@100°C	0,0544	Ohm	**R_{DSon}@100°C**	0,0256	Ohm
Gate charge	26	nC	**Gate charge**	31	nC
Rise time	3,5E-08	s	**Rise time**	1,7E-08	s
Fall time	2,00E-08	s	**Fall time**	9,00E-09	s
tsw	4,5E-08	ns	**tsw**	2,15E-08	ns

IRFR4615

P_{cond_LS}	2,8	W	**P_{cond_HS}**	0,7	W
P_{sw_LS}	1,0	W	**P_{sw_HS}**	1,0	W
P_{LS}	3,8	W	**P_{HS}**	1,7	W
P_{total}	11	W			
%loss	4%	W			

The loss share is quite high for this mosfet. It is mainly due to its average R_{DSOn} characteristic leading to high conduction losses

IPD200N12N3 G

P_{cond_LS}	1,3	W	**P_{cond_HS}**	0,3	W
P_{sw_LS}	0,5	W	**P_{sw_HS}**	0,0	W
P_{LS}	1,8	W	**P_{HS}**	0,3	W
P_{total}	4	W			
%loss	1%	W			

To keep the transistor at an acceptable junction temperature, we've to dissipate their losses through an heatsink.

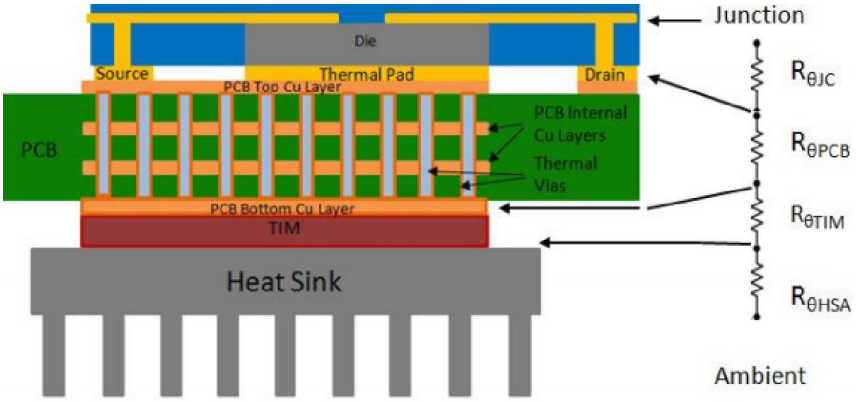


Figure 9 Schematic showing the transistor thermal path.

The choosen PCB is a standard 1.6mm thick FR4 PCB
In our case we have around 16, 0.4mm wide thermal via per DPAK footprint. According to the chart, the equivalent RTH is about 14°C/W
We estimate the RTH of a silicon based thermal interface material of 3°C/W

For a lab ambient temp of 25°C

Tamb	25	°C
Rthvias	14	°C/W
RTIM	3	°C/W
Rheatsink	5	°C/W
Rth sum	22	°C/W
Ploss	3	W
T junction	91	°C

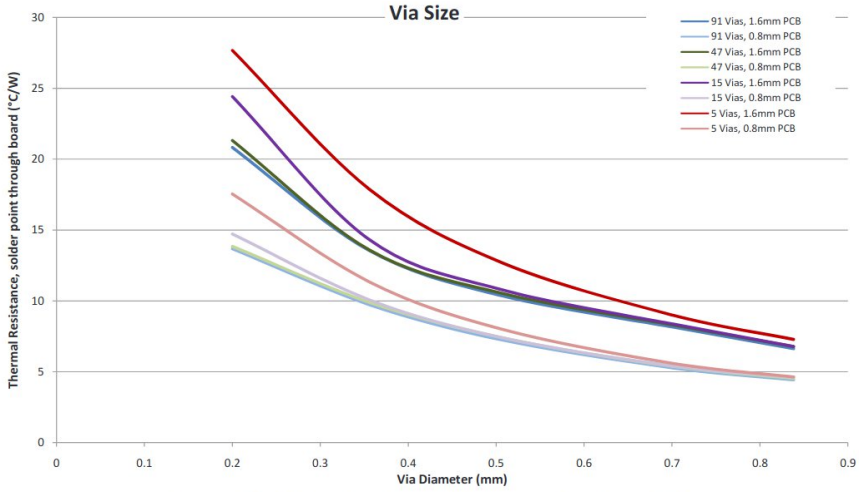


Chart 4: FR-4 PCB with various via diameters and numbers of vias

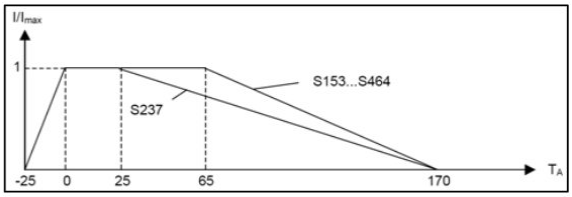
Figure 10 Thermal resistance of a given set of vias.

This conservative estimation stays below 100°C so we don't have to fear a thermal runaway issue.

Boost mode inrush current protection

During start up, the high side DC link capacitance is discharged and a large current can flow. To limit this transient effect, it is foreseen to use a NTC thermistor (negative thermal coefficient). When the converter start up, the cold thermistor act as a serie resistor preventing the inrush current to flow freely.

This initial current will progressively heat up the NTC as it slowly charge the high side DC link capacitor, and thus reduce the serie resistance, permitting the nominal current to flow freely.



NTC resistance at continuous current

The effective resistance for the usual current change can be approximated as follows:

$R_{NTC} = k \times I^{n}$ [Ω] $0.3 \times I_{max} < I \leq I_{max}$

R_{NTC} Resistance value to be determined at a current I

k, n Fit parameter, see individual data sheet of inrush current limiter

I Continuous current flowing through the NTC

The continuous current I in the application should be between 30% and 100% of the specified maximum continuous current I_{max}.

The calculated values only serve as an estimate for operation in still air at an ambient temperature of 25 °C. This equation yields sufficiently accurate results for the limited current range stated above.

Figure 11 Thermal evolution of NTC current handling capacity

I is choosen as 0.5xI_{nom}				
	0,5	**I_{nom}**	17	A
		I	8,5	A

R25 of the thermistor depends on the VI_Low, which won't exceed 28V at Inom

V_{I_Low} range @ I_{nom}	15	28	V
R_{25}	1,76	3,29	Ω

Electrical specification and ordering codes

R_{25} Ω	I_{max} (0...65 °C) A	C_{test} [1] 230 V AC ∝F	C_{test} [1] 110 V AC ∝F	R_{min} (@ I_{max}, 25 °C) Ω	Ordering code
1	16	1000	4000	0.021	B57364S0109M0**
2	12	1000	4000	0.036	B57364S0209M0**
2.5	11	1000	4000	0.044	B57364S0259M0**
4	9.5	1000	4000	0.059	B57364S0409M0**
5	8.5	1000	4000	0.073	B57364S0509M0**
10	7.5	1000	4000	0.098	B57364S0100M0**

Calculated R25 value would lead us to choose 2 or 2.5 ohms NTC but effective Imax limitations constrain us to choose 1ohm NTC.

EPCOS **B57364S0109M0**** is choosen as Inrush current limiter

During component placement, the inrush current limiter will be placed away from the PTC that should be placed away from the NTC heat.

Overcurrent protection

It is necessary to protect the converter from current that exceed the maximal inductor rating.
Resetable PTC (positive thermal coefficient thermistor) are foreseen for this application. These device are sensitive to temperature, so when ambiant temperature rise, there hold current and trip current characteristics decrease. For prototyping purpose, the protection will be design for room temperature, to correctly protect the device in these thermal conditions.

The PTC fuse will be placed close to the inductor, so that when the inductor runs hot, it lower the tripping threshold of the PTC, and get protected.

Foreseen inductor Wurth 7443634700	I_R	12	A
	I_{SAT}	8,5	A
Max operating voltage at hold current	V_{Hold}	28	V

Table R3 — Electrical Characteristics (Cont'd)

Part Number	I_H (A)	I_T (A)	V_{MAX} (V_{DC})	V_{MAX} ($V_{AC\ RMS}$)	I_{MAX} (DC_{ADC})	I_{MAX} (AC_{ARMS})	$P_{D\,Typ}$ (W)	Max Time-to-trip (A)	Max Time-to-trip (s)	R_{MIN} (Ω)	R_{MAX} (Ω)	R_{1MAX} (Ω)	Lead Size [mm² (AWG)]
RKEF; 60V													
RKEF050	0.50	1.00	60	—	40	—	1.00	8.00	0.8	0.320	0.529	0.900	[0.205mm² (24)]
RKEF065	0.65	1.30	60	—	40	—	1.25	8.00	1.0	0.250	0.450	0.720	[0.205mm² (24)]
RKEF075	0.75	1.50	60	—	40	—	1.40	8.00	1.5	0.200	0.390	0.640	[0.205mm² (24)]
RKEF090	0.90	1.80	60	—	40	—	1.50	8.00	2.0	0.190	0.320	0.520	[0.205mm² (24)]
RKEF110	1.10	2.20	60	—	40	—	2.20	8.00	3.0	0.170	0.280	0.470	[0.520mm² (20)]
RKEF135	1.35	2.70	60	—	40	—	2.30	8.00	4.5	0.110	0.220	0.370	[0.520mm² (20)]
RKEF160	1.60	3.20	60	—	40	—	2.40	8.20	9.0	0.100	0.200	0.320	[0.520mm² (20)]
RKEF185	1.85	3.70	60	—	40	—	2.60	9.25	12.6	0.060	0.152	0.250	[0.520mm² (20)]
RKEF250	2.50	5.00	60	—	40	—	2.80	12.50	15.6	0.040	0.085	0.140	[0.520mm² (20)]
RKEF300	3.00	6.00	60	—	40	—	3.20	15.00	19.8	0.030	0.050	0.080	[0.520mm² (20)]
RKEF375	3.75	7.50	60	—	40	—	3.40	18.75	22.0	0.017	0.040	0.060	[0.520mm² (20)]
RKEF400	4.00	8.00	60	—	40	—	3.70	20.00	24.0	0.014	0.038	0.060	[0.520mm² (20)]
RKEF500	5.00	10.00	60	—	40	—	5.00	25.00	28.0	0.012	0.030	0.050	[0.520mm² (20)]

RKEF500 is the PTC reference that has the highest hold current. One can see that the rated current of the converter exceed the max holding current of the available PTC. To cope with this issue, two RKEF500 will be placed in parallel.

In this case, only PTC resettable fuses of the same part number and rating should be used. Just as with two of the same resistors in parallel halves the effective resistance in the circuit per Ohm's law, an application with two parallel PTC fuses will experience the same resistance change (50% lower). However, the hold/trip current does not double. A general rule of thumb is that this hold and trip current increase is 1.6 to 1.8 * Ihold of a single PTC resettable fuse. The maximum current, IMAX remains the same as a single PTC resettable fuse.

2 parrallel RKEF500	I_{Hold}	8,5	A
	I_{Trip}	17	A
	R	0,015	Ω

Driver IC

In order to drive the MOSFET transistors, we've choosen an isolated driver IC. 3kV isolation class suffice
Choosing an isolated driver greatly simplify the integration
We've choosen an IC that drives one power leg, both the high side and low side transistors.
We've choosen an IC that is not generating the complementary PWM. The microcontroller has to generate both the low side and high side PWM signal.
The choosen transistor driver must provide a selectable hardware deadtime to ensure redundancy with the software deadtime.
Choosen transistor must have a SOIC16 footprint
4A current drive capacity is required to take profit of the choosen IRFU4615 transtors.
Transistors are driven with a 0V to 15V V_{GS} signal.
In this case a simple bootstrap circuit suffice to supply the high side supply.

From these criteria the choosen reference is TI UCC21222
Passives surounding the IC are choosen mostly according to the UCC21222 datasheet application exemple.

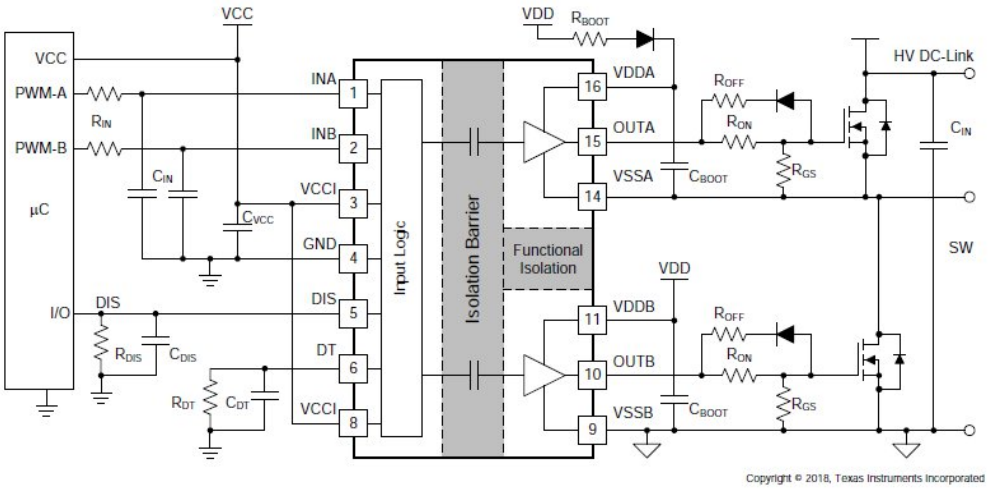


Figure 11 Typical UCC21222 driver application

Name	Values	Unit	Comments
VGS	15	V	Driving voltage level choosen
R_G	2,7	Ohm	From IRFR4615 Datasheet
R_{ON}	2,2	Ohm	IMax = VGS/(RG+RON) = 3A > 4A from UCC21222
R_{OFF}	0	Ohm	ISink = VGS / (RG+ROFF) = 5.5A > 6A from UCC21222
R_{GS}	1000	Ohm	"1 kΩ, 10 kΩ, or 100 kΩ ought to work."

Driver IC

Passives surounding the IC are choosen mostly according to the UCC21222 datasheet application exemple.

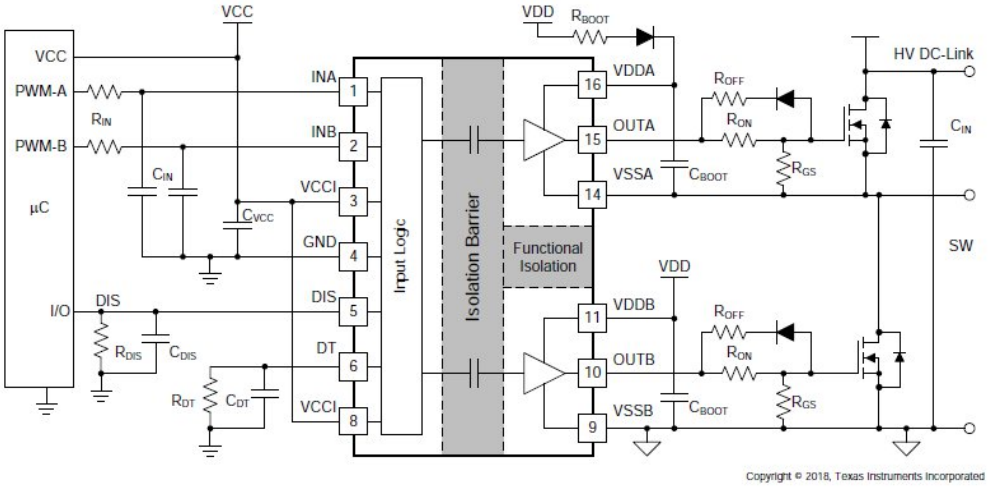


Figure 12 Typical UCC21222 driver application

Mostly as per datasheet page 26 to 31 we choose :

Name	Values	Unit	Comments
R_{IN}	51	Ohm	As per datasheet
C_{IN}	33	pF	As per datasheet
C_{VCC}	100	nF	As per datasheet - one per 5V input
C_{VCChf}	10	nF	Extra 10nF cap added - might not be necessary
D_{Boot}	200	V	Choosen to support max VDC
	4	A	As per datasheet
	16	ns	Same magnitude order than datasheet diode
	STTH4R02U	ref	
R_{DT}	20	kOhm	200ns hardware deadtime - as per datasheet
C_{DT}	10	nF	Not 2.2nF as in datasheet but should be ok
R_{Boot}	2,2	Ohm	As per datasheet but 0805 instead of 1210 might heat to much in this case will be changed for 12Ohm
C_{Boot}	1	uF	As per datasheet
C_{Boot2}	100	nF	As per datasheet
C_{VDD}	10	uF	As per datasheet
C_{VDD2}	100	nF	Not 220nF as in datasheet but should be ok

Measurment stage purpose

In order to control the power flow, the measurment stage measures and adapts the physical signals to voltage signals suitable for the MCU ADC module.
In our case the foreseen microcontroller is the NUCLEOF334R8.

The requirement for the ADC signals are to be between 0V and 3.3V referenced to DGNG, the isolated digital ground.

The physical signals to be measured on board are :

Physical name	Label name	Max physical amplitude	Signal dynamic	Required aquisition speed	Sensor technology
AC voltage	Vl_Low1	±80V	~kHz		Voltage divider and ±250mV 60kHz isolated amplifier
	Vl_Low2	±80V	~kHz		Voltage divider and ±250mV 60kHz isolated amplifier
AC currents	Il_Low1	±10A	200kHz		1MHz ±20A Isolated Hall effect sensor
	Il_Low2	±10A	200kHz		1MHz ±20A Isolated Hall effect sensor
DC current	Il_High	20A	~kHz		120kHz ±20A Isolated Hall effect sensor
DC voltage	Vl_High	120V	~kHz		Voltage divider and +2V 100kHz isolated amplifier
Temperature	Tp	-40 to 110°C	Hz	1 per minute	-40 to 110°C Temperature sensor

Table 3 Signals and sensors characteristics

Voltage measurments are isolated via isolated operational amplifiers. Two type of opamp are selected for this purpose. The AMC1311 is choosen for the DC bus measurment while the AMC1100 is choosen for the AC measures. In both case their output is a differential signal that goes through a diffenrial filter before heading to the MCU ADC.

Current measurments are isolated via contactless hall effect based measurment. We use 1MHz bandwith ACS730 for measuring the inductors current, because of the signal dynamic requirment. For the DC current the ACS724 suffice. The ACS724 and ACS730 footprints are compatible, with minimal care of selecting suitable capacitor on pin7.

For the temperature measurment we use a TO-92 LM35, which is bended and contact the VOUT copper plane close to the transistors. It is important to ass thermal grease to maximise thermal conduction to the sensor.

Neutral to ground digital connexion

A particularity of this converter is it's possibility to contact the neutral point to ground. This feature permit to use the converter

- As a DC/DC converter, with two independant low side inputs/outputs referenced to GND.
- As an interleaved DC/DC converter with one input and one output both in buck mode or boost mode. with the input and the output referenced to GND
- As a single phase inverter with an output referenced to a floating neutral point.

This last mode is the one requiring to implement this digital neutral to ground connexion.

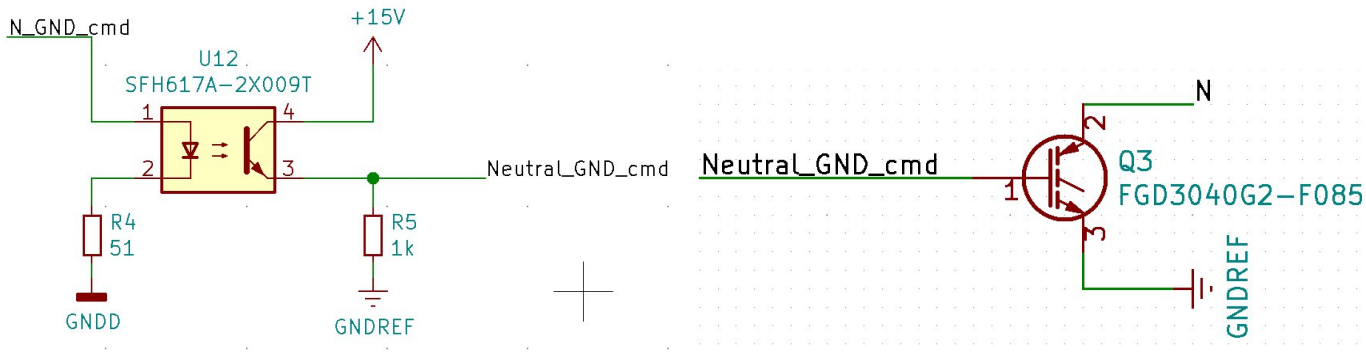


Figure 13 Neutral to ground IGBT and its command circuit

The configuration of the ground to neutral switch state is done offline, without power. Here this connexion is though as a solid state relay.
Therefore no dynamic behaviour is expected from the IGBT selected to perform the task.
A 400V, 40A IGBT DPAK based IGBT is selected for the switch.
IGBT is suitable for the task as it can handle consequent current flow, and has no body diode which is a mandatory feature for this application.

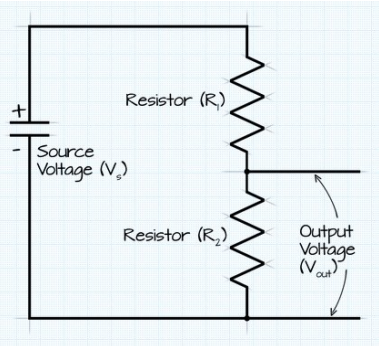
Optocoupler passives

Name	Values	Unit	Comments
R4	51	Ohm	As per datasheet page 4
R5	1000	Ohm	As per datasheet page 4

AC voltage sensing

Low side Voltage Dividers

VIn	80	V
VOut	0,25	V
R1	150000	Ohm
R2	470,2	Ohm
I1	5,32E-04	A
I2	5,32E-04	A
P1	4,24E-02	W
P2	1,33E-04	W



$$V_{out} = \frac{V_s \times R_2}{(R_1 + R_2)}$$

VI_Low1 and VI_Low2 voltage dividers are calculated in order to give a +250mV signal for the input voltage of 80V. This +250mV output voltage correspond to the max input voltage of the AMC1100. The AMC 1100 is an isolated fully differential operational amplifier that as a fixed gain of 8. The voltage divider is using standard 0.5% or 0.1% thin film resistors and dissipate less than the 125mW maximal limit of the 0805 package.

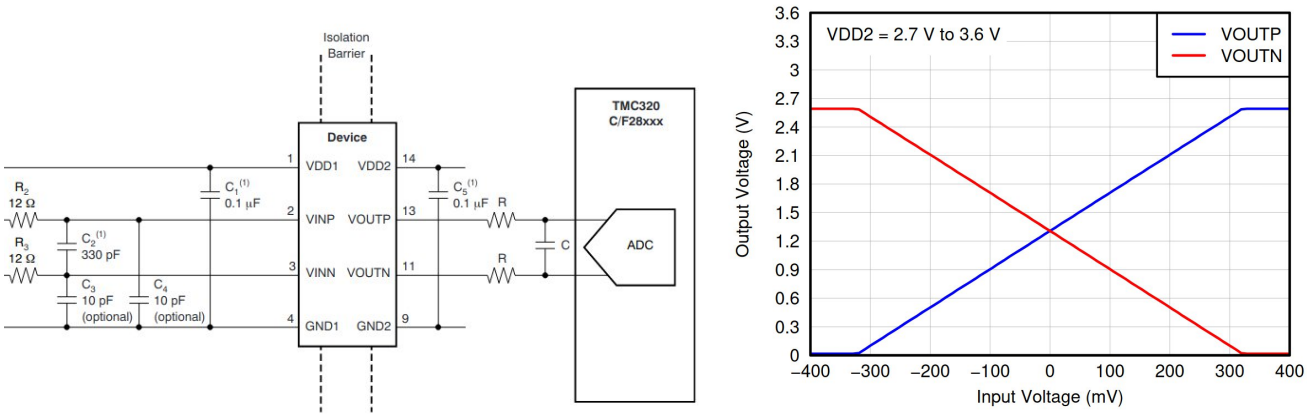
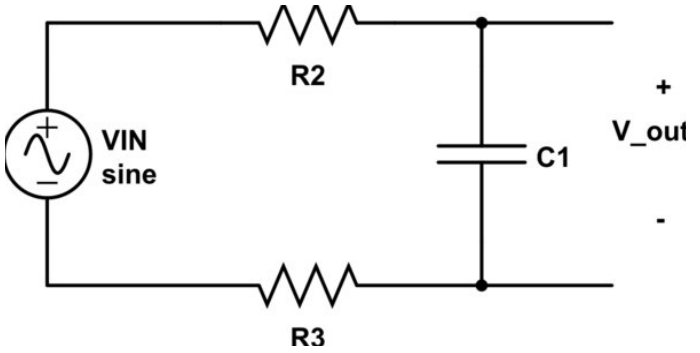


Figure 14 AMC1100 Typical application schematic and differential output evolution

In our case VDD1 is supplied with 5V referenced to the neutral. VDD2 is supplied with 3.3V referenced to the DGND. AMC1100 has a fixed gain of 8. The differiental output is centered at around 1.3V when the input signal is 0V. Decoupling caps are choosen as per datasheet. Input RC filter suggested by the manufacturer is selected as per datasheet. Output filter is choosen egual to input filter per default. Might be necessary to tune these filters.

Differential analog signal filtering

The AMC1100 also has an input differential filter. TI, the chip manufacturer gives default value of 12ohm and 330pF.



$$f = \frac{1}{2\pi[R1+R2]C}$$

The cutoff frequency of a differential RC filter is given above.

Analog input filter for AMC1100

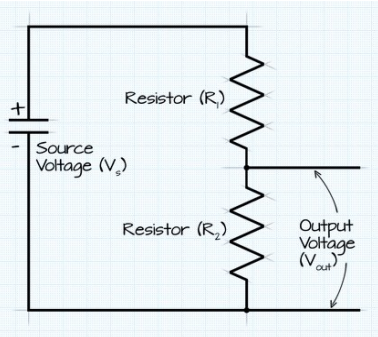
R	12	Ohm
C	3,3E-10	F
F	2,01E+07	Hz

As a preliminary test, these values will be implemented for the opamp output as well.

DC voltage sensing

High side Voltage Divider

VIn	120	V
VOut	2	V
R1	330000	Ohm
R2	5593,2	Ohm
I1	3,58E-04	A
I2	3,58E-04	A
P1	4,22E-02	W
P2	7,15E-04	W



$$V_{out} = \frac{V_s \times R_2}{(R_1 + R_2)}$$

VI_High voltage divider is calculated in order to give a +2V signal for an input voltage of 120V. This +2V output voltage correspond to the max input voltage of the AMC1311. The AMC 1311 is an isolated operational amplifier that as a fixed gain of 1. The voltage divider is using standard 0.5% or 0.1% thin film resistors and dissipate less than the 125mW maximal limit of the 0805 package.

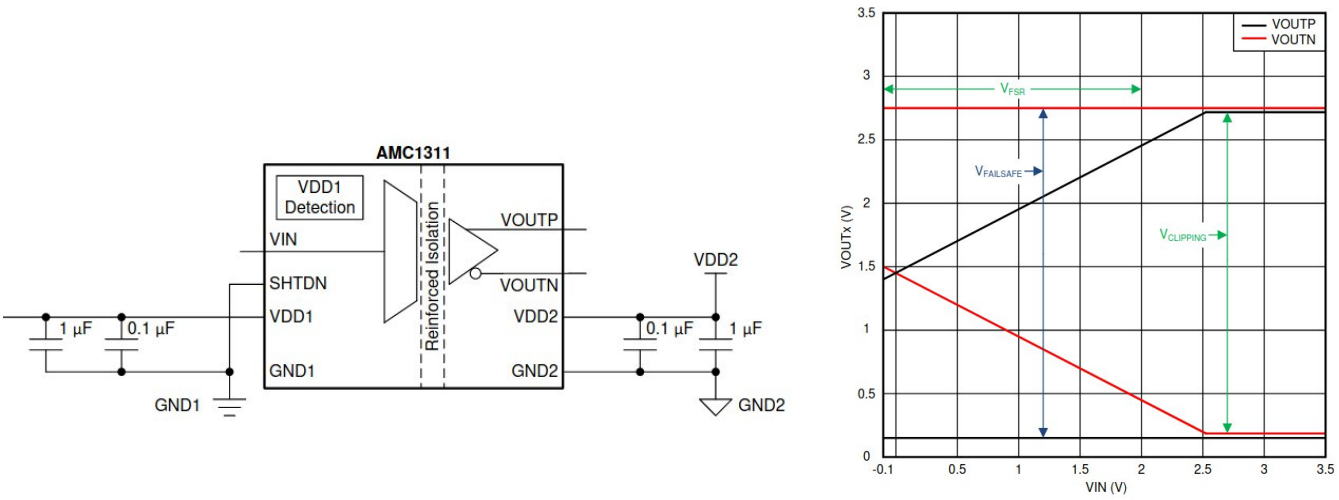


Figure 15 AMC1311 Typical application schematic and differential output evolution

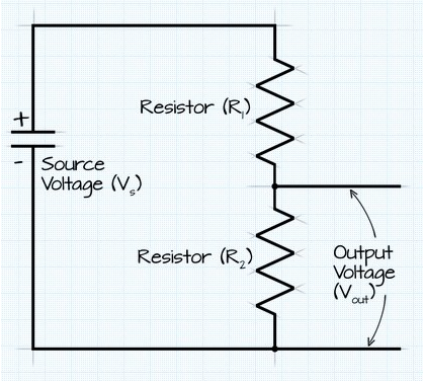
In our case VDD1 is supplied with 5V referenced to the neutral. VDD2 is supplied with 3.3V referenced to the DGND. AMC1100 has a fixed gain of 8. The differiental output has a 1.44V common mode. Decoupling caps are choosen as per datasheet. Output RC filter suggested by the manufacturer is selected by default egual to the AC measurment. Might be necessary to tune the filter.

Signal Voltage Dividers

The sensors signals coming from the current sensors and thermistance are based on 5V. They need to be lowered to a 3.3V scale to be measured by the MCU ADC.

VIn	5	V
VOut	3,3	V
R1	20000	Ohm
R2	38824	Ohm
I1	8,50E-05	A
I2	8,50E-05	A
P1	1,45E-04	W
P2	2,81E-04	W

$$V_{out} = \frac{V_s \times R_2}{(R_1 + R_2)}$$



20K and 39K are selected as resistors values for the voltage divider. They will be 0.5% or 0.1% thin film resistor to limit ESL as much as possible while maintaining suitable accuracy.

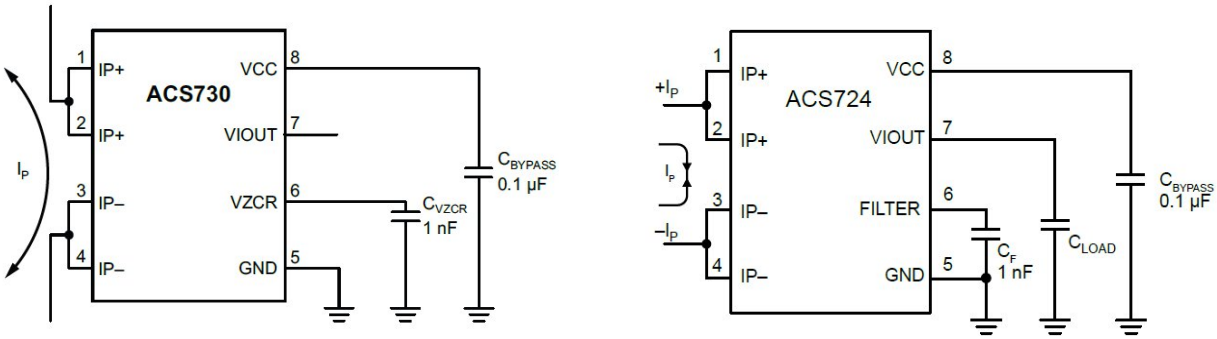


Figure 16 ACS730 and ACS724 typical application shcematic

Current sensors are supplied with 5V referenced to DGND. A 100nF decoupling capacitor is placed closest to VCC pin as per datasheet.

For the ACS730 it is mandatory to place a 1nF capacitor on pin 7

For the ACS724, the 1nF on pin 7 provide a bandwith of 170kHz Filter can be changed according to the chart below.

C_F (nF)	t_r (µs)
Open	3.5
1	5.8
4.7	17.5
22	73.5
47	88.2
100	291.3
220	623
470	1120