Experiment 2-1 NOR Gate Circuit

OBJECTIVE

1. To understand how to construct other logic gates using NOR gates.
2. To construct NOT and OR gates using NOR gates.

DISCUSSION

The symbol of a NOR gate is shown in Fig. 2-1-1. The Boolean expression for the NOR gate is $F=\overline{A+B}$; in De Morgan's theorem, $F=\overline{A+B}=\overline{A}\,\overline{B}$.

When A=B, $F=\overline{A+B}=\overline{A}\,\overline{A}=\overline{A}$. When B=0, $F=\overline{A+B}=\overline{A+0}=\overline{A}$. Therefore, the NOR gate can be used to construct NOT; OR; AND; NAND; and XOR gates. However we will not attempt to construct various logic gates in this experiment by connecting NOR gates in different ways.

Fig. 2-1-1 Symbol of NOR gate

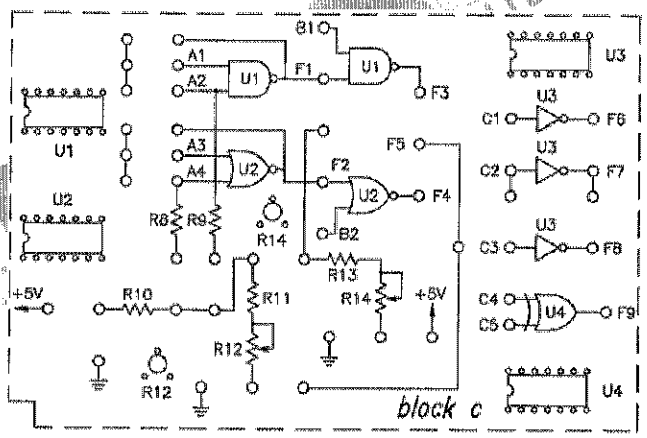
EQUIPMENT REQUIRED

1. KL-22001 Basic Electrical/Electronic Circuit Lab
2. KL-26001 Combinational Logic Circuit Experiment Module (1)

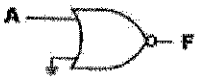
PROCEDURE

1. Set the KL-26001 Module on the KL-22001 Basic Electrical/Electronic Circuit Lab, and locate block c. U2 of Fig. 2-1-2(a) will be used to construct a NOT gate as

shown in Fig. 2-1-2(b). Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26001 Module.



(a) KL-26001 block c

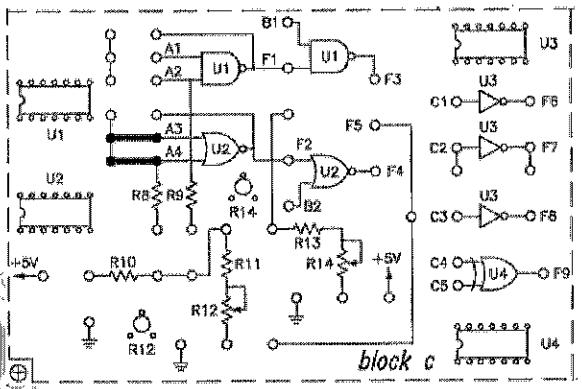


(b) Equivalent to a NOT gate

Fig. 2-1-2 NOR gate used as NOT gate

2. Connect inputs A3, A4 to Data Switches SW0, SW1 and the output F2 to Logic Indicator L1. Set SW0 to "0" and observe states of F1 at SW1="0" and SW1="1".
   When SW1="0", F2= _____
   When SW1="1", F2= _____
   Does the circuit operate as a NOT gate? _____

3. Complete the connections by referring to the wiring diagram in Fig. 2-1-3(a) and the circuit in Fig. 2-1-3(b). This connects A3 and A4 together (A3=A4). Connect A3 to Data Switch SW0 and the output F2 to Logic Indicator L1.
   When SW0="0", F2= _____
   When SW0="1", F2= _____
   Does the circuit operate as a NOT gate? _____



(a) Wiring diagram (KL-26001 block c)

(b) Equivalent to a NOT gate

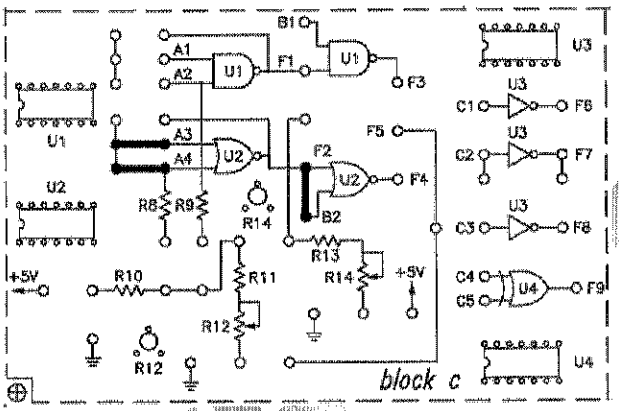
Fig. 2-1-3 NOR gate used as NOT gate

4. Complete the connections by referring to the wiring diagram in Fig. 2-1-4(a) and the circuit in Fig. 2-1-4(b). Connect A3 to Data Switch SW0 and the output F4 to Logic Indicator L1.

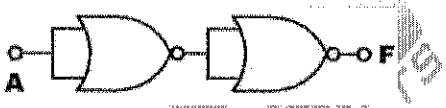
   When SW0="0", F4= _____

   When SW0="1", F4= _____

   Does the circuit operate as a buffer? _____



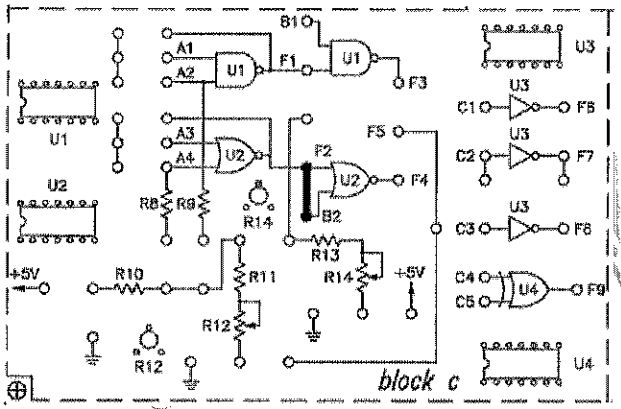
(a) Wiring diagram (KL-26001 block c)



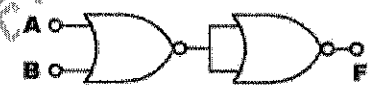
(b) Equivalent to a buffer

Fig. 2-1-4 NOR gate used as a buffer

5. Complete the connections by referring to the wiring diagram in Fig. 2-1-5(a) and the circuit in Fig. 2-1-5(b). Connect inputs A3 to SW0, A4 to SW1; and output F4 to Logic Indicator L1.



(a) Wiring diagram (KL-26001 block c)



(b) Equivalent to an OR gate

Fig. 2-1-5 NOR gate used as an OR gate

6. Follow the input sequences and record the output states in Table 2-1-1.

SW0(A3)	SW1(A4)	F4
0	0	
0	1	
1	0	
1	1	

Table 2-1-1

Experiment 2-2 NAND Gate Circuit

OBJECTIVE

1. To understand how to construct various logic gates with NAND gates.
2. To construct NOT, AND and OR gates using NAND gates.

DISCUSSION

The symbol of a NAND gate is shown in Fig. 2-4. The Boolean expression for a NAND gate is $F=\overline{AB}$; in De Morgan's theorem, $\overline{AB}=\overline{A}+\overline{B}$.

When A=B, $F=\overline{AB}=\overline{A}$. When B=1, $F=\overline{AB}=\overline{A\cdot 1}=\overline{A}$. Like the NOR gates, NAND gates can be used to construct just about any basic logic gates. We will attempt to construct various basic gates in this experiment by connecting NAND gates in different ways.

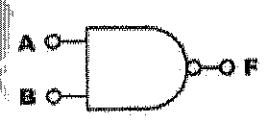


Fig. 2-2-1 Symbol of NAND gate

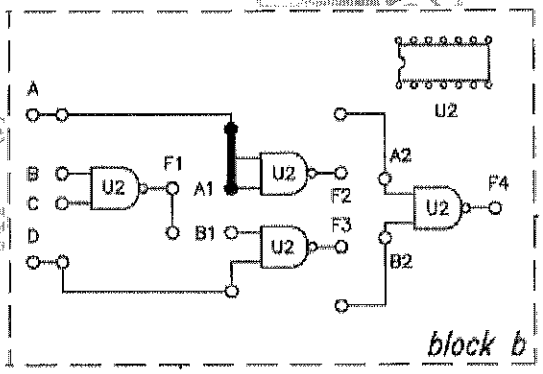
EQUIPMENT REQUIRED

1. KL-22001 Basic Electrical/Electronic Circuit Lab
2. KL-26001 Combinational Logic Circuit Experiment Module (1)

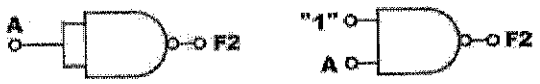
PROCEDURE

1. Set the KL-26001 Module on the KL-22001 Basic Electrical/Electronic Circuit Lab, and locate block b. Insert the bridging plug shown in Fig. 2-2-2(a), using U2 to

construct the NOT gate shown in the left-hand side of Fig. 2-2-2(b). Apply +5VDC from the Fixed Power on KL-22001 Lab to KL-26001 Module.



(a) Wiring diagram (KL-26001 block b)



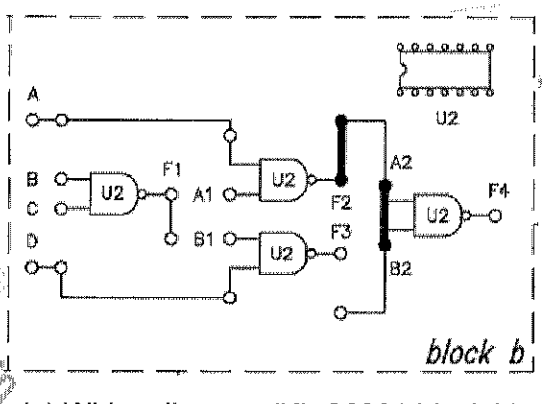
(b) NOT gate constructed with NAND gate

Fig. 2-2-2 NOT gate constructed with NAND gate

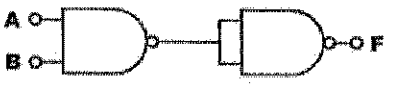
2. Connect input A to Data Switch SW1 and output F2 to Logic Indicator L1. Observe and record the output states.
   When SW1="0", F2=_____
   When SW1="1", F2=_____
   Does the circuit act as a NOT gate? _____

3. Remove the bridging plug between A and A1. Connect input A1 to +5V ("1") to create the NOT gate shown in the right-hand side of Fig. 2-2-2(b). Remain other connections unchanged. Observe the output states.
   When SW1="0", F2=_____
   When SW1="1", F2=_____
   Does the circuit act as a NOT gate? _____

4. Complete the connections by referring to the wiring diagram in Fig. 2-2-3(a) and the circuit in Fig. 2-2-3(b). Connect A to SW1, A1 to SW2 and F4 to L1.



(a) Wiring diagram (KL-26001 block b)



(b) Equivalent to an AND gate

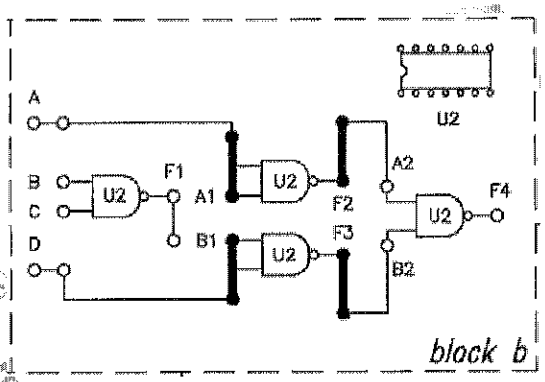
Fig. 2-2-3 AND gate constructed with NAND gates

5. Follow the input sequences and record the outputs in Table 2-2-1. Does the circuit act as an AND gate? _____

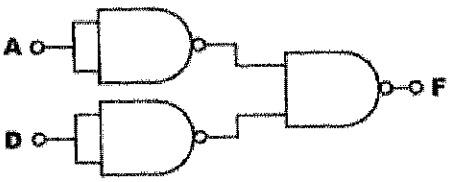
SW2(A1)	SW1(A)	F4
0	0	
0	1	
1	0	
1	1	

Table 2-2-1

6. Complete the connections by referring to the wiring diagram in Fig. 2-2-4(a) and the circuit in Fig. 2-2-4(b). Connect A to SW1; D to SW2, and F4 to L1.



(a) Wiring diagram (KL-26001 block b)



(b) Equivalent to an OR gate

Fig 2-2-4 OR gate constructed with NAND gates

7. Follow the input sequences in Table 2-2-2 and record the outputs.

   Does the circuit act as an OR gate (F=A+B)? _____

SW2(D)	SW1(A)	F4
0	0	
0	1	
1	0	
1	1	

Table 2-2-2