Digital VLSI Circuits and HDL

Mazad S. Zaveri, PhD

What can we implements using the three modeling methods?

- For Combinational Circuits
  - We can use:
    - Gate level modeling
    - Data flow modeling
    - Behavioral modeling
- For Sequencing Elements
  - We can use only:
    - Behavioral modeling
    - (We may have some readymade modules for sequencing elements; But if we use that, then it becomes more like “structural” modeling (similar to gate level modeling)

Writing Comments

```
a = b && c; // This is a one-line comment

/* This is a multiple line
   comment */

/* This is /* an illegal */ comment */
```

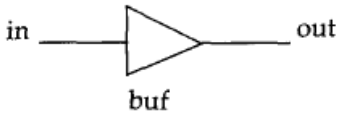
Signal Values

Table 3-1 Value Levels

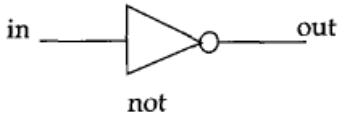
Value Level	Condition in Hardware Circuits
0	Logic zero, false condition
1	Logic one, true condition
x	Unknown value
z	High impedance, floating state

Gate Primitives in Verilog

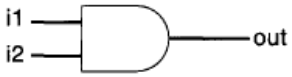
```
wire OUT, IN1, IN2;

// basic gate instantiations.
and a1(OUT, IN1, IN2);
nand na1(OUT, IN1, IN2);
or or1(OUT, IN1, IN2);
nor nor1(OUT, IN1, IN2);
xor x1(OUT, IN1, IN2);
xnor nx1(OUT, IN1, IN2);

// More than two inputs; 3 input nand gate
nand na1_3inp(OUT, IN1, IN2, IN3);

// gate instantiation without instance name
and (OUT, IN1, IN2); // legal gate instantiation
```



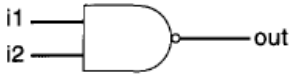
buf



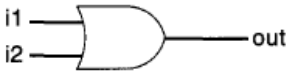
not



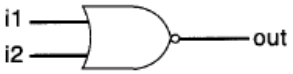
and



nand

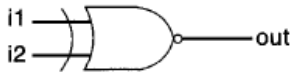


or



nor

xor



xnor

```
 // basic gate instantiations
 buf b1(OUT1, IN);
 not n1(OUT1, IN);
```

- **Truth-tables for the gate primitives**
  - z means floating
  - x means undefined

and	i1: 0	1	x	z
i2: 0	0	0	0	0
1	0	1	x	x
x	0	x	x	x
z	0	x	x	x

nand	i1: 0	1	x	z
i2: 0	1	1	1	1
1	1	0	x	x
x	1	x	x	x
z	1	x	x	x

or	i1: 0	1	x	z
i2: 0	0	1	x	x
1	1	1	1	1
x	x	1	x	x
z	x	1	x	x

nor	i1: 0	1	x	z
i2: 0	1	0	x	x
1	0	0	0	0
x	x	0	x	x
z	x	0	x	x

buf	in	out
	0	0
	1	1
	x	x
	z	x

not	in	out
	0	1
	1	0
	x	x
	z	x

xor	i1: 0	1	x	z
i2: 0	0	1	x	x
1	1	0	x	x
x	x	x	x	x
z	x	x	x	x

xnor	i1: 0	1	x	z
i2: 0	1	0	x	x
1	0	1	x	x
x	x	x	x	x
z	x	x	x	x