B.Tech 4th Sem (ICT)

(IC202T) Analog Circuit Design

UNIT- I

- Bias Stabilization Techniques f or BJT, Thermal Stability. Small signal Analysis of BJT and FET amplifiers. High frequency model of BJT.

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DIFFERENCE BETWEEN A TEACHER AND A PROFESSOR

A Professor of Philosophy at the University of Houston has explained the difference between high school teachers and university professors.

He said, "I am your professor, not your teacher." He stressed that, "Teachers are evaluated on the basis of learning outcomes, generally as measured by standardized tests. If you don't learn, then your teacher is blamed."

He added, "It is not part of my job to make you learn. At university, learning is your job—and yours alone. My job is to lead you to the fountain of knowledge. Whether you drink deeply or only gargle is entirely up to you."

INTRODUCTION

- The BJT as a circuit element operates various circuits with many major and minor modifications.
- For the analysis of such circuits, we obtain the various conditions for proper operation of the device, and also determine the projected range of operation of the device.
- A detailed study of the device in a two-port mode simplifies the circuit analysis of the device to a large extent.
- Thus, we calculate the various parameters of the devices' performance, namely voltage gain, current gain, input impedance, and output impedance.
- The frequency response of the device is dealt with in detail, and a study of the various regions of operation in the frequency scale is also explained.
- Finally, we will discuss the various configurations of the device and take a look into the high-frequency operation of the device and its performance in those regions.

Transistor Biasing

The basic function of transistor is amplification. The process of raising the strength of weak signal without any change in its general shape is referred as faithful amplification. For faithful amplification it is essential that:-

1. Emitter-Base junction is forward biased
2. Collector- Base junction is reversed biased
3. Proper zero signal collector current

The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is called transistor biasing.

WHY BIASING?

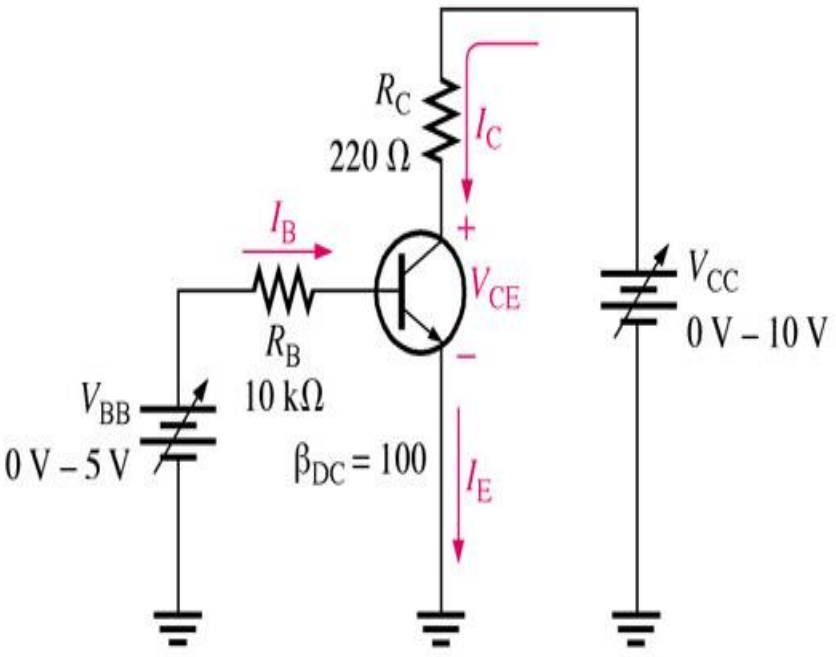
If the transistor is not biased properly, it would work inefficiently and produce distortion in output signal.

HOW A TRANSISTOR CAN BE BIASED?

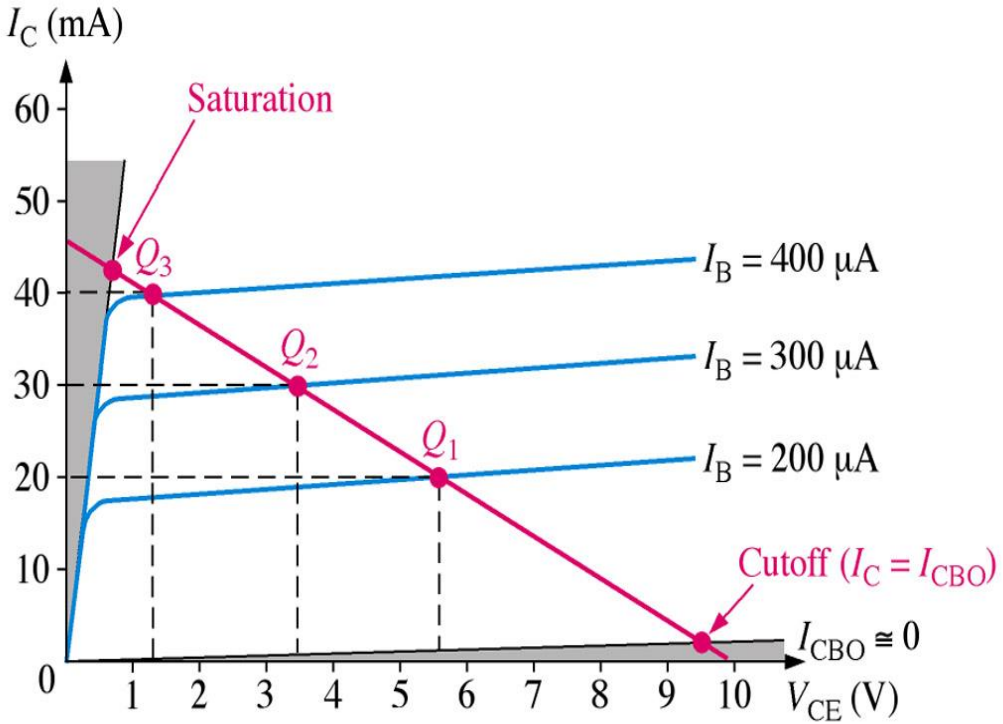
A transistor is biased either with the help of battery or associating a circuit with the transistor. The later method is more efficient and is frequently used. The circuit used for transistor biasing is called the biasing circuit.

The DC Operating Point

For a transistor circuit to amplify it must be properly biased with dc voltages. The dc operating point between saturation and cutoff is called the **Q-point.** The goal is to set the Q-point such that it does not go into saturation or cutoff when an a ac signal is applied.



(a) DC biased circuit



BIAS STABILITY

❖ Through proper biasing, a desired quiescent operating point of the transistor amplifier in the active region (linear region) of the characteristics is obtained. It is desired that once selected the operating point should remain stable. The maintenance of operating point stable is called Stabilisation.

❖ The selection of a proper quiescent point generally depends on the following factors:

(a) The amplitude of the signal to be handled by the amplifier and distortion level in signal

(b) The load to which the amplifier is to work for a corresponding supply voltage

❖ The operating point of a transistor amplifier shifts mainly with changes in temperature, since the transistor parameters — *β, I_{CO} and V_{BE} (where the symbols carry their usual meaning)—are functions of* temperature.

The Thermal Stability of Operating Point (S)

❖**Stability Factor *S*:-** The stability factor *S, as the change of collector current with respect to the reverse saturation* current (Ico), keeping β *and VBE constant. This can be written as:*

The Thermal Stability Factor : S_{Ico}

$$S = \left.\frac{\partial I_c}{\partial I_{co}}\right|_{V_{be},\,\beta}$$

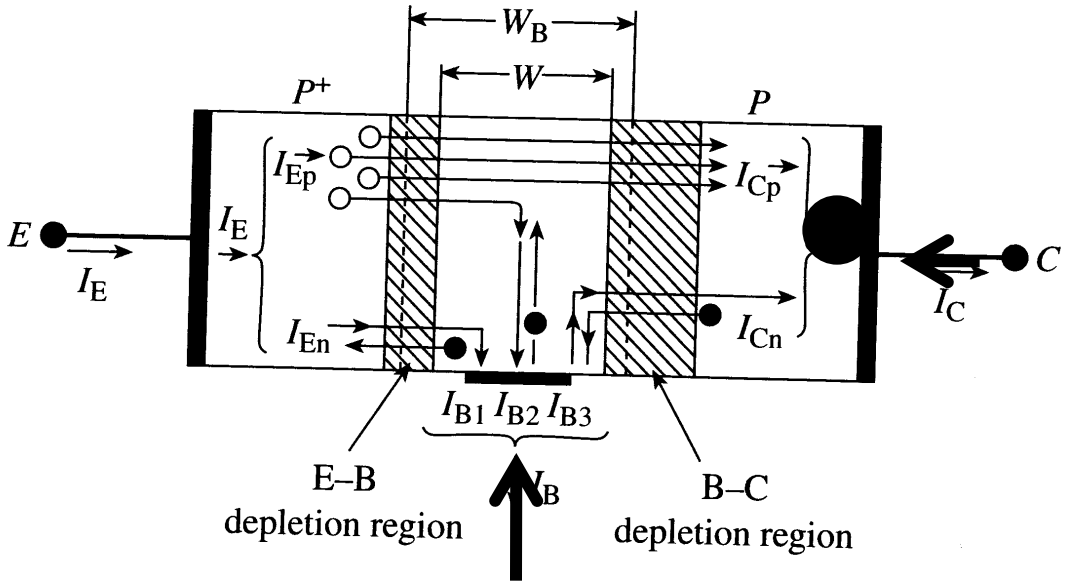
This equation signifies that I_c Changes S times as fast as I_{co}

Derivation of I_C

Differentiating the equation of Collector Current $I_C = (1+\beta)Ico + \beta I_b$ & rearranging the terms we can write

$$S = \frac{1+\beta}{1-\beta\,(\partial I_b/\partial I_C)}$$

It may be noted that Lower is the value of S better is the stability



$I_C+I_B+I_E=0$ all current going into device are taken +ve

$I_C=--\alpha I_E+I_{CO}$;from BJT current components diagram

$=-\alpha(-I_C-I_B)+I_{CO}$;from above equation

$I_C(1-\alpha)= \alpha I_B+I_{CO}$

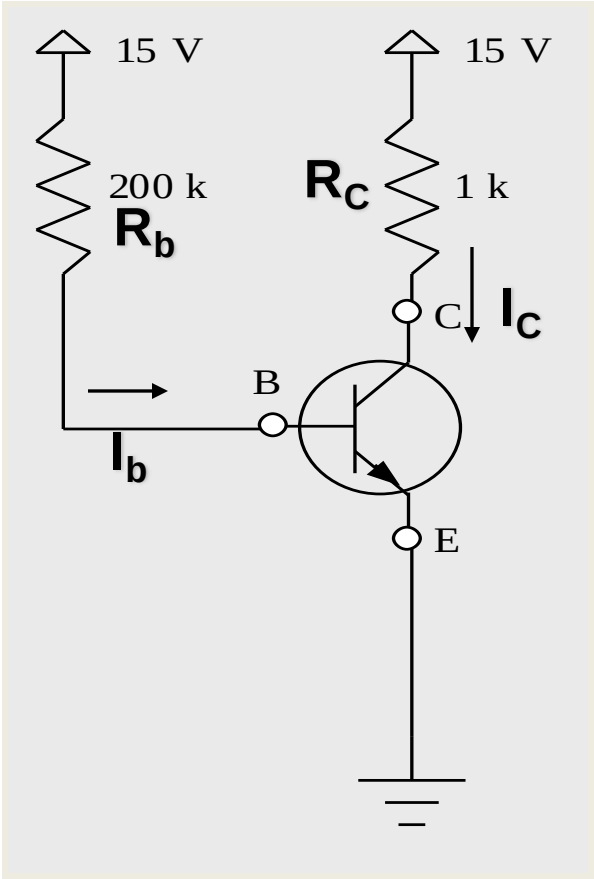
$I_C=(\alpha/(1- \alpha))I_B+I_{CO}/(1- \alpha)$

$=\beta I_B+(1+ \beta)I_{CO}$

Various Biasing Circuits

- **Fixed Bias Circuit**
- **Fixed Bias with Emitter Resistor**
- **Collector to Base Bias Circuit**
- **Potential Divider Bias Circuit**

The Fixed Bias Circuit



The Thermal Stability Factor : S

$$S = \frac{\partial I_c}{\partial I_{co}}\Bigg|_{V_{be},\,\beta}$$

General Equation of S Comes out to be

$$S = \frac{1+\beta}{1-\beta\,(\partial I_b/\partial I_C)}$$

Applying KVL through Base Circuit we can write, $I_b R_b + V_{be} = V_{cc}$

Diff w. r. t. I_C, we get $(\partial I_b / \partial I_c) = 0$

$S_{Ico} = (1+\beta)$ is very large

Indicating high un-stability

Merits:

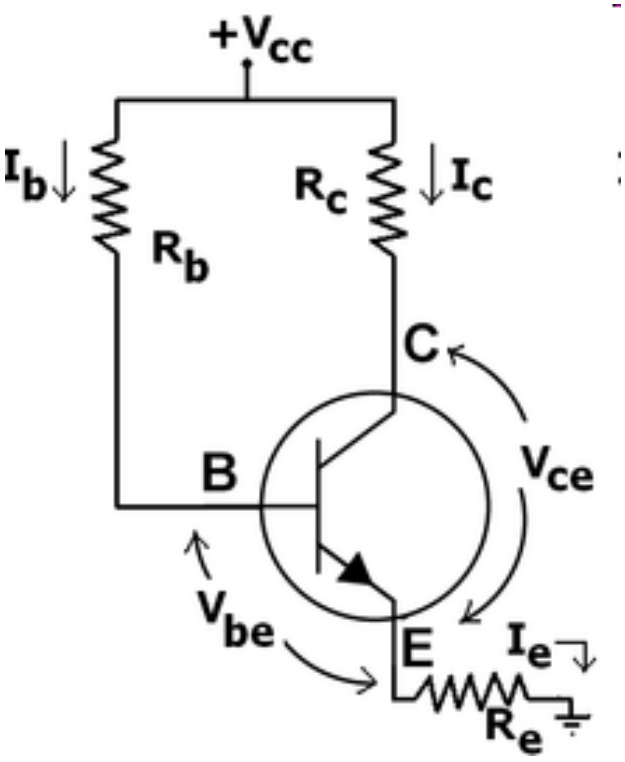
- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.
- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

Fixed bias with emitter resistor

The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point.



Merits:

• The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits:

• As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.

➢ If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.

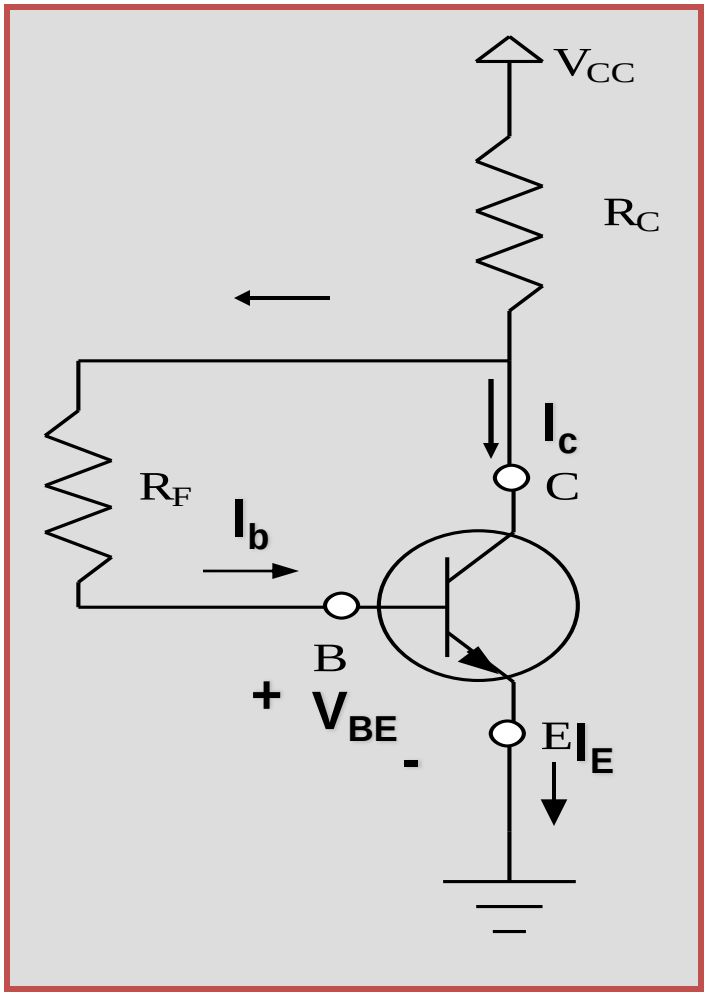
➢ If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.

• In addition to the above, R_E causes ac feedback which reduces the voltage gain of the amplifier.

Usage:

The feedback also increases the input impedance of the amplifier when seen from the base, which can be advantageous. Due to the above disadvantages, this type of biasing circuit is used only with careful consideration of the trade-offs involved.

The Collector to Base Bias Circuit



- This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point.
- In this form of biasing, the base resistor R_F is connected to the collector instead of connecting it to the DC source V_{cc}.
- So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

Applying KVL through base circuit

we can write $(I_b + I_C) R_C + I_b R_f + V_{be} = V_{cc}$

Diff. w. r. t. I_C we get

$$(\partial I_b / \partial I_c) = - R_C / (R_f + R_C)$$

Therefore, $$S = \frac{(1+\beta)}{1+[\beta R_C/(R_C+R_f)]}$$

Which is less than (1+β), signifying better thermal stability

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

• As β -value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_C fairly large or making R_f very low.

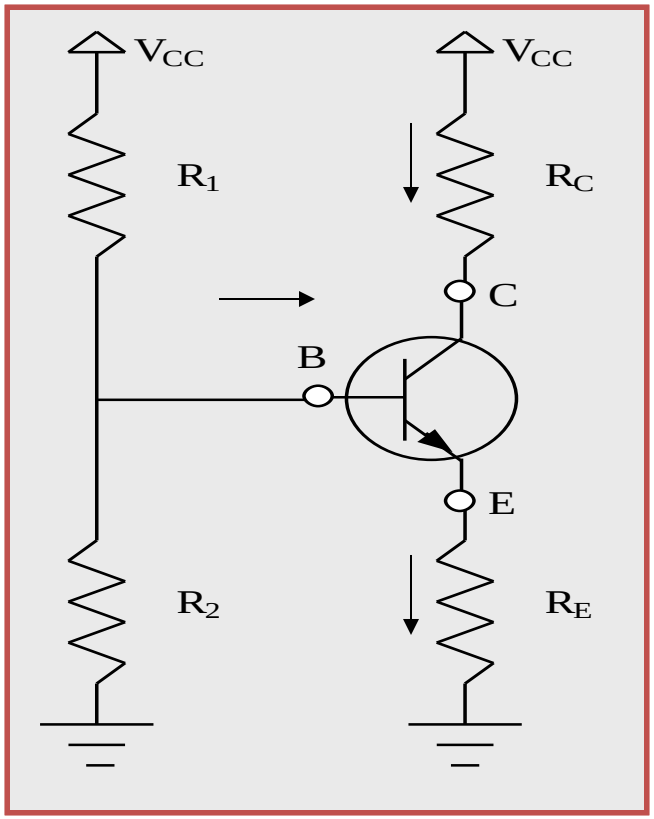
- If R_C is large, a high V_{CC} is necessary, which increases cost as well as precautions necessary while handling.
- If R_f is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_f causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

The Potential Divider Bias Circuit

This is the most commonly used arrangement for biasing as it provide good bias stability. In this arrangement the emitter resistance '$R_{E'}$ provides stabilization. The resistance '$R_{E'}$ cause a voltage drop in a direction so as to reverse bias the emitter junction. Since the emitter-base junction is to be forward biased, the base voltage is obtained from R_1-R_2 network. The net forward bias across the emitter base junction is equal to V_B- dc voltage drop across '$R_{E'}$. The base voltage is set by Vcc and R_1 and R_2. The dc bias circuit is independent of transistor current gain. In case of amplifier, to avoid the loss of ac signal, a capacitor of large capacitance is connected across R_E. The capacitor offers a very small reactance to ac signal and so it passes through the condensor.

The Potential Divider Bias Circuit

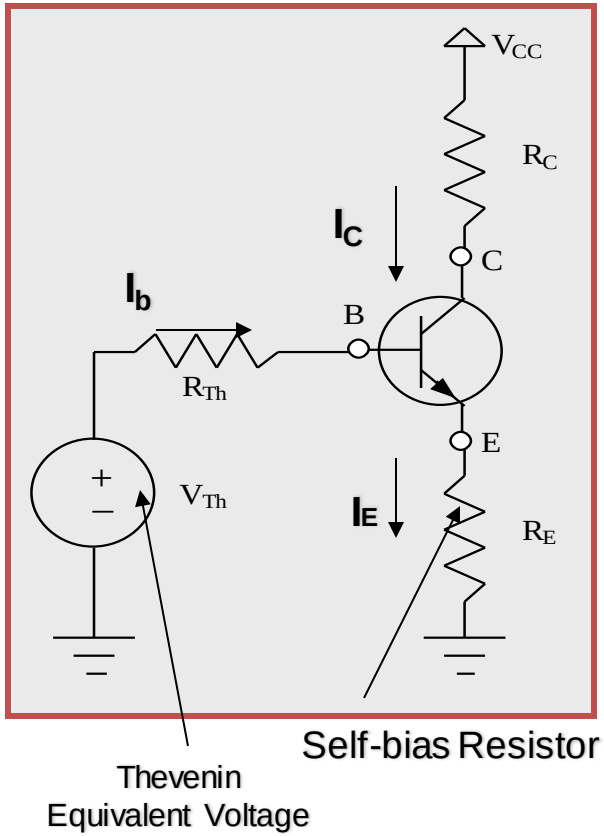


To find the stability of this circuit we have to convert this circuit into its Thevenin's Equivalent circuit

$$R_{th} = \frac{R_1 * R_2}{R_1 + R_2} \quad \& \quad V_{th} = \frac{Vcc\ R_2}{R_1 + R_2}$$

The Potential Divider Bias Circuit

Thevenin Equivalent Ckt



Applying KVL through input base circuit

we can write $I_b R_{Th} + I_E R_E + V_{be} = V_{Th}$

Therefore, $I_b R_{Th} + (I_C + I_b) R_E + V_{BE} = V_{Th}$

Diff. w. r. t. I_C & rearranging we get

$$(\partial I_b / \partial I_c) = - R_E / (R_{Th} + R_E)$$

Therefore,

$$S = \frac{1+\beta}{1+\left[\beta \frac{R_E}{R_E + R_{Th}}\right]}$$

This shows that S is inversely proportional to R_E and It is less than (1+β), signifying better thermal stability

Merits:

- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making R1||R2 very low.
  - If R_E is of large value, high V_{CC} is necessary. This increases cost as well

  as precautions necessary while handling.
  - If R1 || R2 is low, either R1 is low, or R2 is low, or both are low. A low R1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R2 lowers Vbe, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
  - AC as well as DC feedback is caused by RE, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage:

The circuit's stability and merits as above make it widely used for linear circuits.

CALCULATION OF STABILITY FACTORS

❖ **Stability Factor *S*:-** The stability factor *S, as the change of collector current with respect to the reverse saturation* current, keeping β *and* V_{BE} *constant. This can be written as:*

$$S \equiv \frac{\partial I_C}{\partial I_{CO}}$$

Or,

$$S = (1+\beta)\frac{1 + R_b/R_e}{1 + \beta + R_b/R_e}$$

❖ **Stability Factor *S'*:-** The variation of I_C *with* V_{BE} *is given by the stability factor S defined by the partial derivative:*

$$S' \equiv \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

❖ **Stability Factor *S"*:-** The variation of I_C *with respect to β is represented by the stability factor, S", given as:*

$$S'' \equiv \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta}$$

❖ **General Remarks on Collector Current Stability:-** The stability factors have been defined earlier keeping in mind the change in collector current with respect to changes in I_{CO} , V_{BE} *and β. These stability factors are repeated here for simplicity.*

$$\frac{\Delta I_C}{\Delta_{C1}} = \left(1 + \frac{R_b}{R_e}\right)\frac{M_1 \Delta I_{CO}}{I_{C1}} - \frac{M_1 \Delta V_{BE}}{I_{C1} R_e} + \left(1 + \frac{R_b}{R_e}\right)\frac{M_2 \Delta \beta}{\beta_1 \beta_2}$$

Thermal Runaway

The maximum average power $P_{D(max)}$ which a transistor can dissipate depends upon the transistor construction and may lie in the range from a few milliwatts to 200 W. As mentioned earlier, the power dissipated within a transistor is predominantly the power dissipated at its collector base junction. Thus maximum power is limited by the temperature that the collector-base junction can withstand. For silicon transistor this temperature is in the range 150 to 225 °C, and for germanium it is between 60 to 100 °C. The collector-base junction temperature may rise because of two reasons :

- Due to rise in ambient temperature
- Due to self heating.

The self heating can be explained as follows :

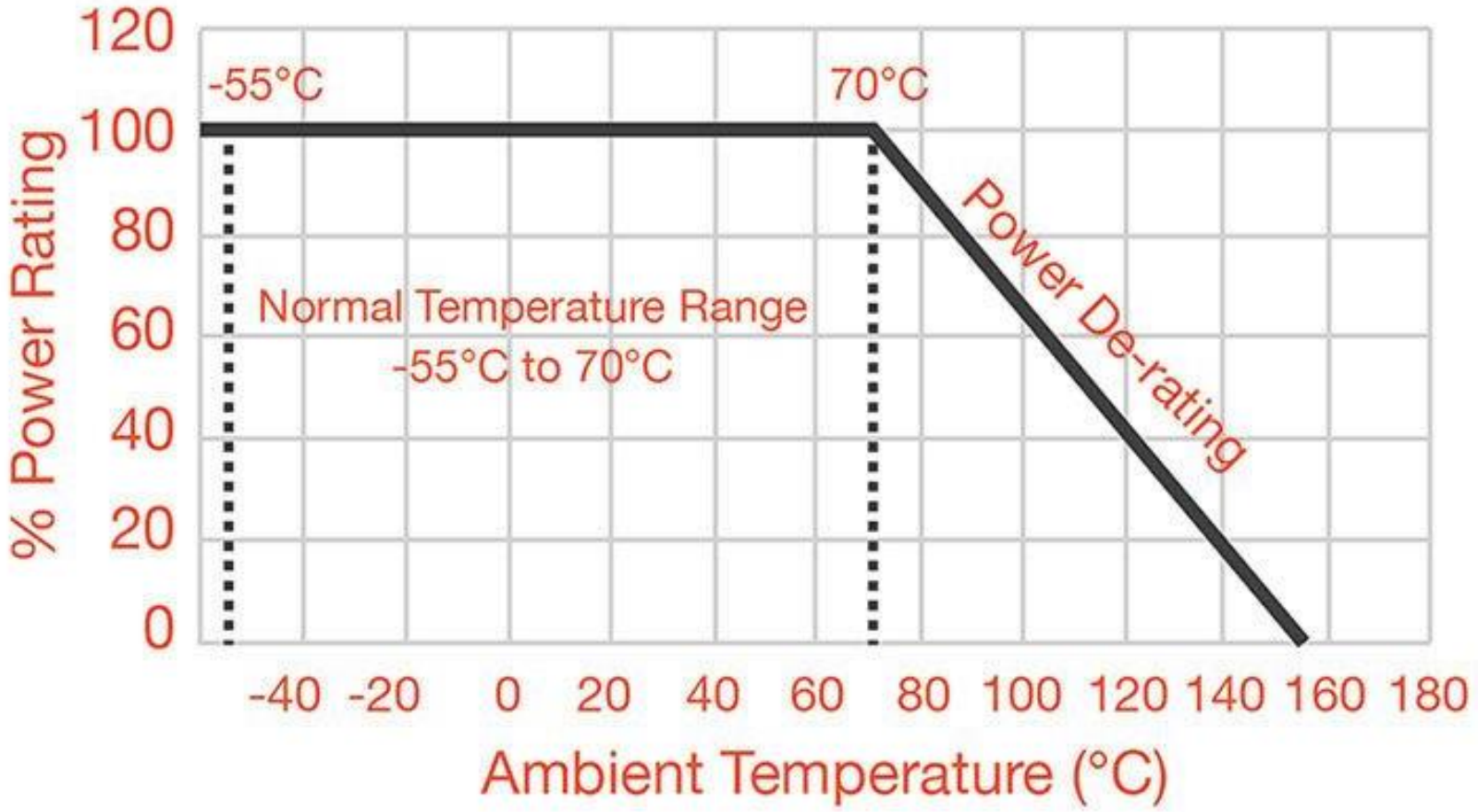
The increase in the collector current increases the power dissipated at the collector junction. This, in turn further increases the temperature of the junction and hence increase in the collector current. The process is cumulative and it is referred to as **self heating**. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called '**Thermal runaway**' of the transistor.

Thermal Resistance

The steady state temperature rise at the collector junction is proportional to the power dissipated at the junction. It is given as

$$\partial T = T_j - T_A = \theta P_D \quad \ldots (1)$$

Power Temperature De-rating curve



The Condition for Thermal Stability

As we know, the thermal runaway may even burn and destroy the transistor, it is necessary to avoid thermal runaway. The required condition to avoid thermal runaway is that the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated. It is given by,

$$\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad \ldots (3)$$

If we differentiate equation (1)

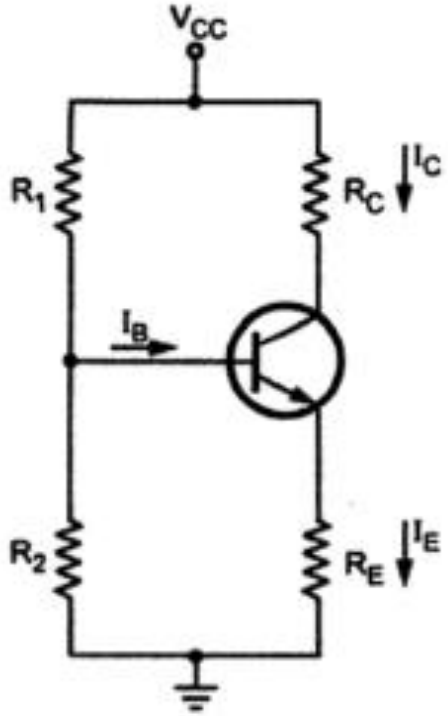
$T_j - T_A = \theta P_D$ with respect to T_j we get,

$$1 = \theta \frac{\partial P_D}{\partial T_j}$$

$$\therefore \quad \frac{\partial P_D}{\partial T_j} = \frac{1}{\theta} \quad \ldots (4)$$

Now substituting equation (4) in equation (3) we get

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta} \quad \ldots (5)$$



This condition must be satisfied to prevent thermal runaway. By proper design of biasing circuit it is possible to ensure that the transistor cannot runaway below a specified ambient temperature or even under any condition.

Let us consider voltage divider bias circuit for the analysis.

From the Fig. 1.73 we can say that,

P_C = Heat generated at the collector junction

= D.C. Power input to the circuit – The power lost as I^2R in R_C and R_E

$$P_C = V_{CC} \times I_C - I_C^2 R_C - I_E^2 R_E \quad \ldots (6)$$

If we consider $I_C \cong I_E$ we get

$$P_C = V_{CC} \times I_C - I_C^2 (R_C + R_E) \quad \ldots (7)$$

Differentiating equation (7) with respect to I_C we get

$$P_C = V_{CC} \times I_C - I_C^2 (R_C + R_E) \quad \ldots (7)$$

Differentiating equation (7) with respect to I_C we get

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2 I_C (R_C + R_E) \quad \ldots (8)$$

Referring and rewriting condition equation (5) to avoid thermal runaway we get,

$$\frac{\partial P_C}{\partial I_C} \cdot \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta} \quad \ldots (9)$$

In the above equation $\frac{\partial I_D}{\partial T_j}$ can be written as,

$$\frac{\partial I_D}{\partial T_j} = S \frac{\partial I_{CO}}{\partial T_j} + S' \frac{\partial V_{BE}}{\partial T_j} + S'' \frac{\partial \beta}{\partial T_j} \quad \ldots (10)$$

Since junction temperature affects collector current by affecting I_{CO}, V_{BE}, and β. But as we are doing analysis for thermal runaway the affect of I_{CO} dominates. Thus we can write

$$\frac{\partial I_C}{\partial T_j} = \frac{\partial I_{CO}}{\partial T_j} \quad \ldots (11)$$

As the reverse saturation current for both silicon and germanium increases about 7 percent per °C, we can write

$$\frac{\partial I_{CO}}{\partial T_j} = 0.07\, I_{CO} \qquad \ldots (12)$$

Now substituting value of $\frac{\partial I_C}{\partial T_j}$ and $\frac{\partial P_C}{\partial I_C}$ in equation (11) we get,

$$\frac{\partial I_C}{\partial T_j} = S \times 0.07\, I_{CO} \qquad \ldots (13)$$

Now substituting value of $\frac{\partial I_C}{\partial T_j}$ and $\frac{\partial P_C}{\partial I_C}$ from equations (13) and (8) into equation (9) we get,

$$[V_{CC} - 2\, I_C\, (R_C + R_E)]\, (S)\, (0.07\, I_{CO}) < \frac{1}{\theta} \qquad \ldots (14)$$

As S, I_{CO} and θ are positive, we see that the inequality in equation (14) is always satisfied provided that the quantity in the square bracket is negative.

$$\therefore \quad V_{CC} < 2 I_C (R_C + R_E)$$

$$\therefore \quad \frac{V_{CC}}{2} < I_C (R_C + R_E) \qquad \ldots (15)$$

Applying KVL to the collector circuit of Fig. 1.73 we get,

$$V_{CE} = V_{CC} - I_C (R_E + R_C) \quad \because \quad I_C \cong I_E$$

$$\therefore \quad I_C (R_E + R_C) = V_{CC} - V_{CE}$$

Substituting value of $I_C (R_E + R_C)$ in equation (15) we get,

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

$$\therefore \quad V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

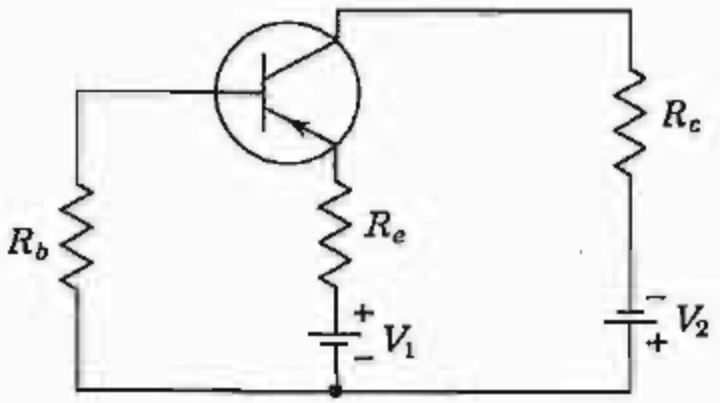
$$\therefore \quad V_{CE} < \frac{V_{CC}}{2}$$

Thus if $V_{CE} < \frac{V_{CC}}{2}$, the stability is ensured. But in transformer coupled circuit, R_C and R_E are quite small and $V_{CE} \cong V_{CC}$. Hence it is necessary to design transformer coupled circuits with stability factor as close to 1 as possible to avoid thermal runaway.

Numerical

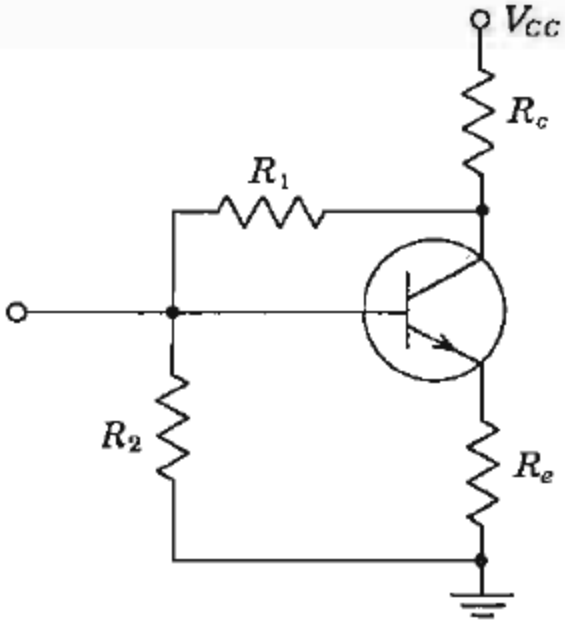
For the two-battery transistor circuit shown, prove that the stabilization factor S is given by

$$S = \frac{1 + \beta}{1 + \beta R_e'/(R_e + R_b)}$$



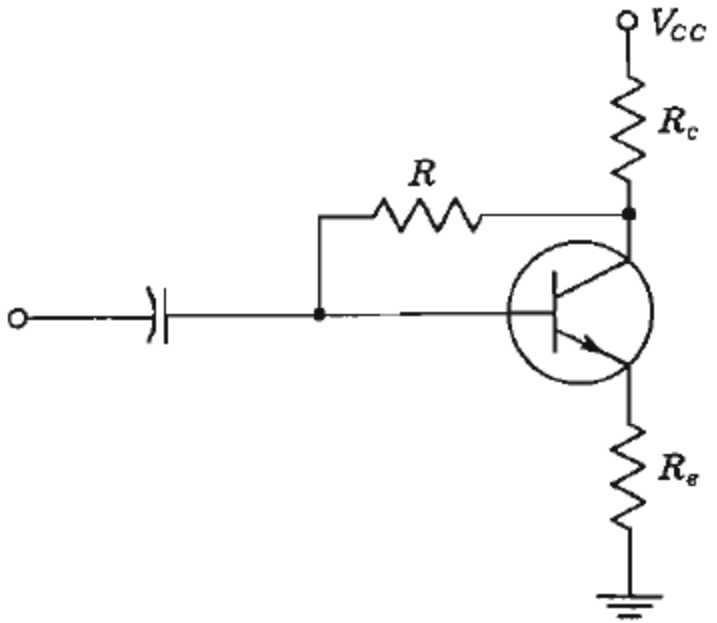
Prob. 9-7

Determine the stability factor S for the circuit shown.



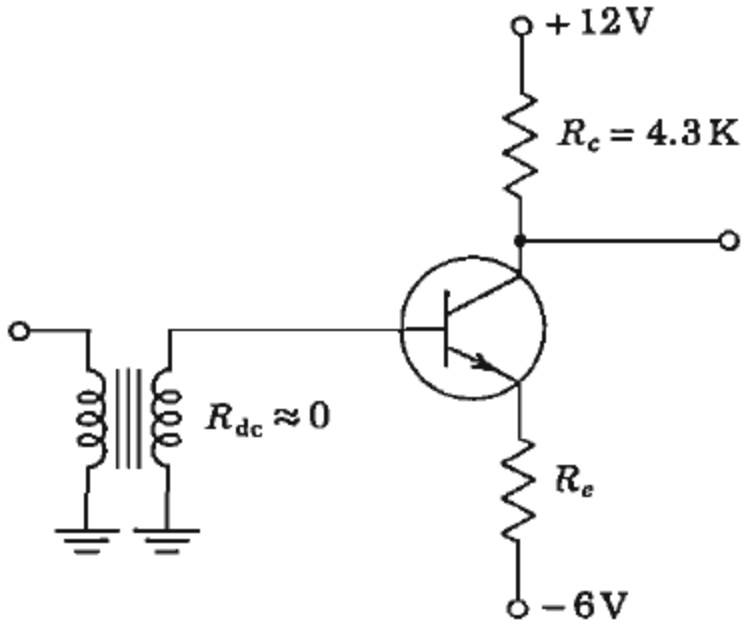
Prob. 9-10

In the circuit shown, $V_{CC} = 24$ V, $R_c = 10$ K, and $R_e = 270\ \Omega$. If a silicon transistor is used with $\beta = 45$ and if under quiescent conditions $V_{CE} = 5$ V, determine (*a*) R, (*b*) the stability factor S.



Prob. 9-11

In the transformer-coupled amplifier stage shown, $V_{BE} = 0.7$ V, $\beta = 50$, and the quiescent voltage is $V_{CE} = 4$ V. Determine (*a*) R_c, (*b*) the stability factor S.

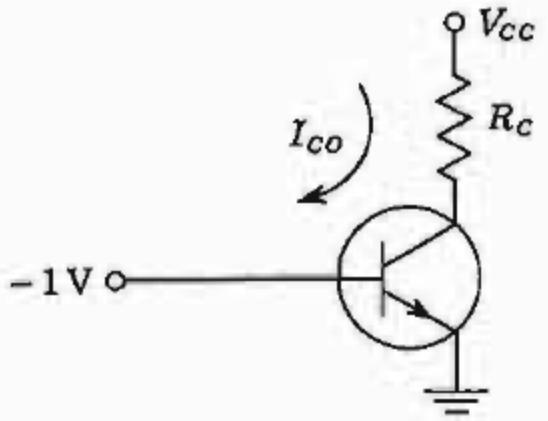


The transistor used in the circuit is at cutoff.

(*a*) Show that runaway will occur for values of I_{CO} in the range

$$\frac{V_{CC} - \sqrt{V_{CC}^2 - 8R_c/0.07\Theta}}{4R_c} \leq I_{CO} \leq \frac{V_{CC} + \sqrt{V_{CC}^2 - 8R_c/0.07\Theta}}{4R_c}$$

(*b*) Show that if runaway is not destructive, the collector current I_{CO} after runaway can never exceed $I_{CO} = V_{CC}/2R_c$.

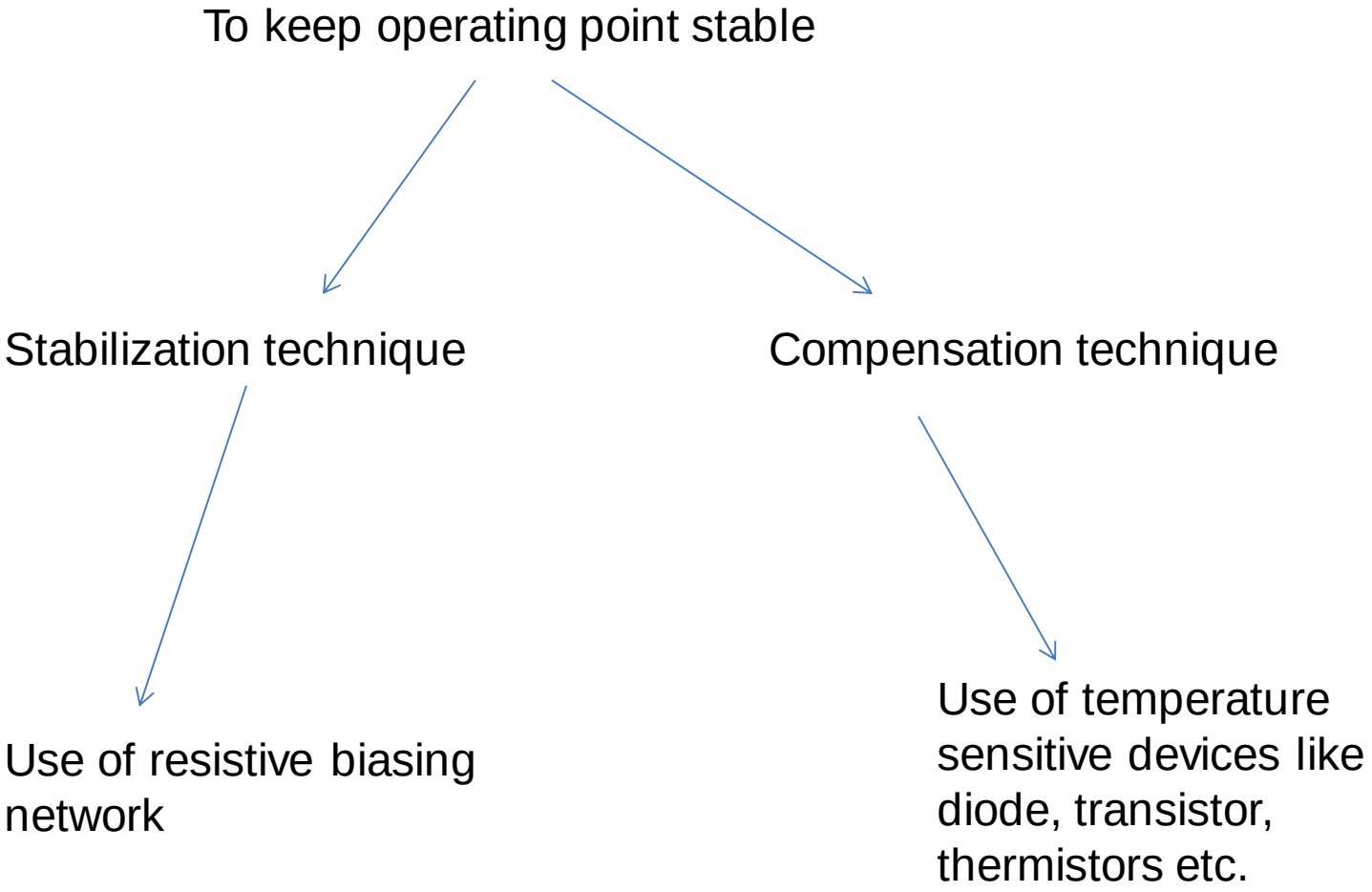


Prob. 9-33

A germanium transistor with $\Theta = 250°C/W$, $I_{CO} = 10\ \mu A$ at 25°C, $R_c = 1$ K, and $V_{CC} = 30$ V is used in the circuit of Prob. 9-33.

(*a*) Find I_{CO} at the point of runaway.

(*b*) Find the ambient temperature at which runaway will occur.


To keep operating point stable
Stabilization technique
Compensation technique
Use of resistive biasing network
Use of temperature sensitive devices like diode, transistor, thermistors etc.

For silicon BJT← I_{CO} is less sensitive → need not to compensate

Diode Compensation Techniques

Compensation for V_{BE} :

a) Diode in Emitter Circuit

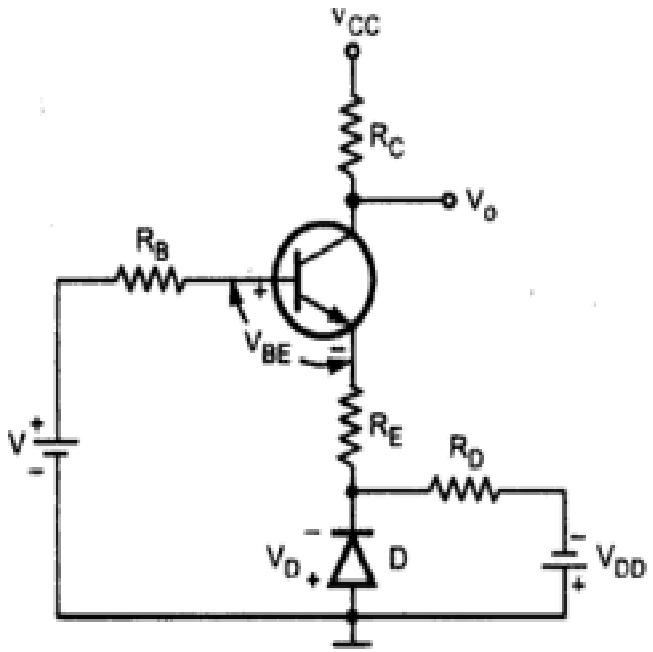


Fig. Stabilization by means of voltage divider bias and diode compensation technique

Fig. shows the voltage divider bias with bias compensation technique.

Here, separate supply V_{DD} is used to keep diode in forward biased condition. If the diode used in the circuit is of same material and type as the transistor, the voltage across the diode will have the same temperature coefficient (−2.5 mV/°C) as the base to emitter voltage V_{BE}. So when V_{BE} changes by ∂V_{BE} with change in temperature, V_D changes by ∂V_D and

Applying KVL in the input loop—

$V = I_B R_B + V_{BE} + (I_B + I_C) R_E - V_0$

$I_B = (V - V_{BE} + V_D - I_C R_E) / (R_E + R_B)$

Hence putting this in equation

$I_C = \beta I_B + (1 + \beta) I_{CO}$

We get—

$$I_C = \frac{\beta [V - (V_{BE} - V_D)] + (R_B + R_E)(\beta + 1) I_{CO}}{[R_B + R_E(1 + \beta)]}$$

It is clear that V_{BE} tracks V_D and effect of temperature is nullified.

Compensation for I_{CO}→ Germanium diode

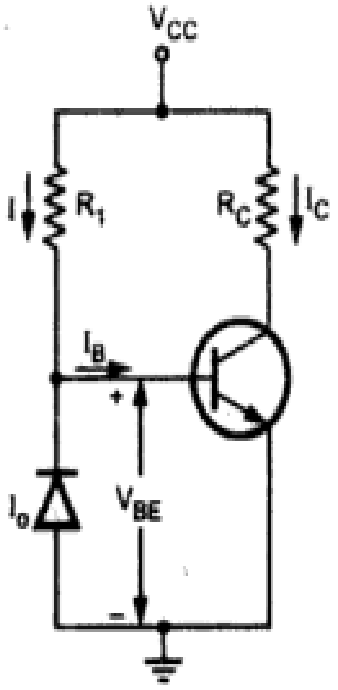


Fig. Diode compensation for a germanium transistor

I_{CO} in Germanium is high and variation can be hazardous→ attention needed. Diode compensation technique should be applied.

$I=(V_{CC}-V_{BE})/R_1$

$\approx V_{CC}/R_1$

=constant

$I_B=I-Io$

Hence putting this IB in —

$I_C=\beta I_B+(1+\beta)I_{CO}$

We get—

$I_C=\beta I-I_o+(1+\beta)I_{CO}$

$= \beta I-\beta I_o+\beta I_{CO}$ (if $\beta>>1$)

$= \beta I$ ($if\ I_o=I_{CO}$)

=constant

Thermistor Compensation

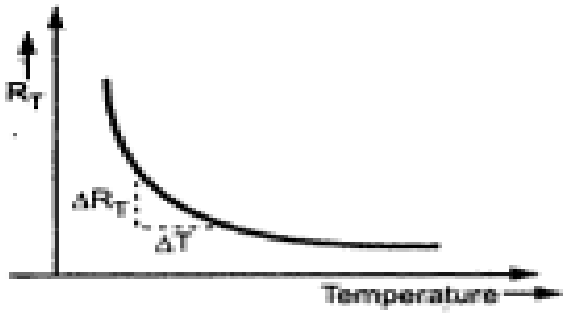


Fig. Temperature Vs R_T resistance of thermistor

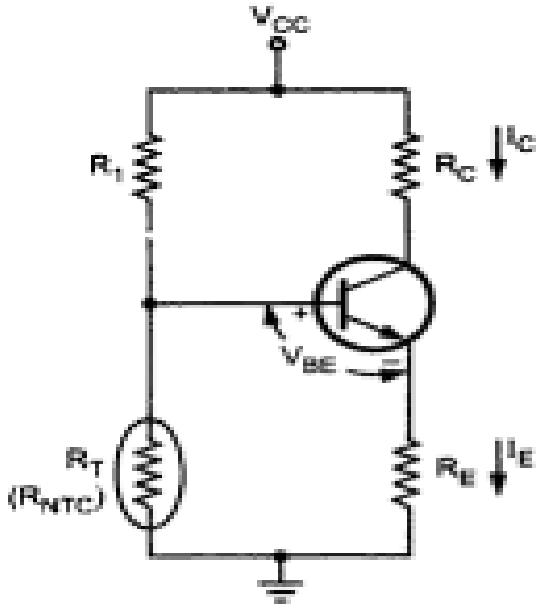


Fig. (a) Thermistor compensation technique

Uses temperature sensitive element, Thermistor
IB proportional to VBE
T(inc)=> R_T(dec)=> V_B(dec) =>V_{BE}(dec)=> I_B(dec)=> I_C(dec)

But

$$I_C=\beta I_B+(1+\beta)I_{CO}$$

Hence increase in I_{CO} is compensated by decrease in I_B.

Sensistor Compensation Technique

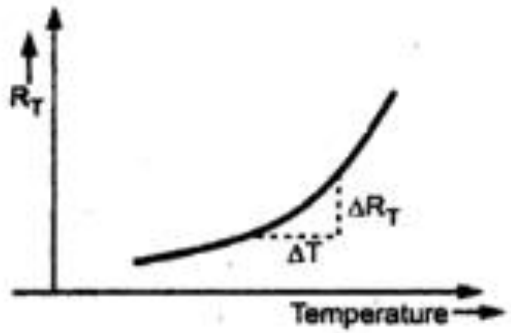
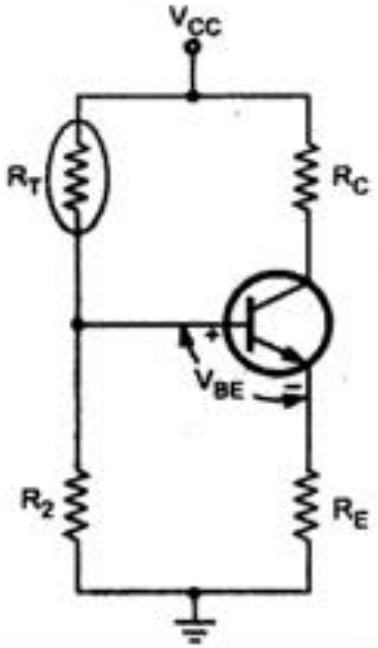


Fig. 1 Temperature Vs resistance of sensistor, R_T



This method of transistor compensation uses temperature sensitive resistive element, sensistors rather than diodes or transistors. It has a positive temperature coefficient, its resistance increases exponentially with increasing temperature as shown in the Fig. 1 .

$$\text{Slope of this curve} = \frac{\partial R_T}{\partial T}$$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor, and the slope is positive.

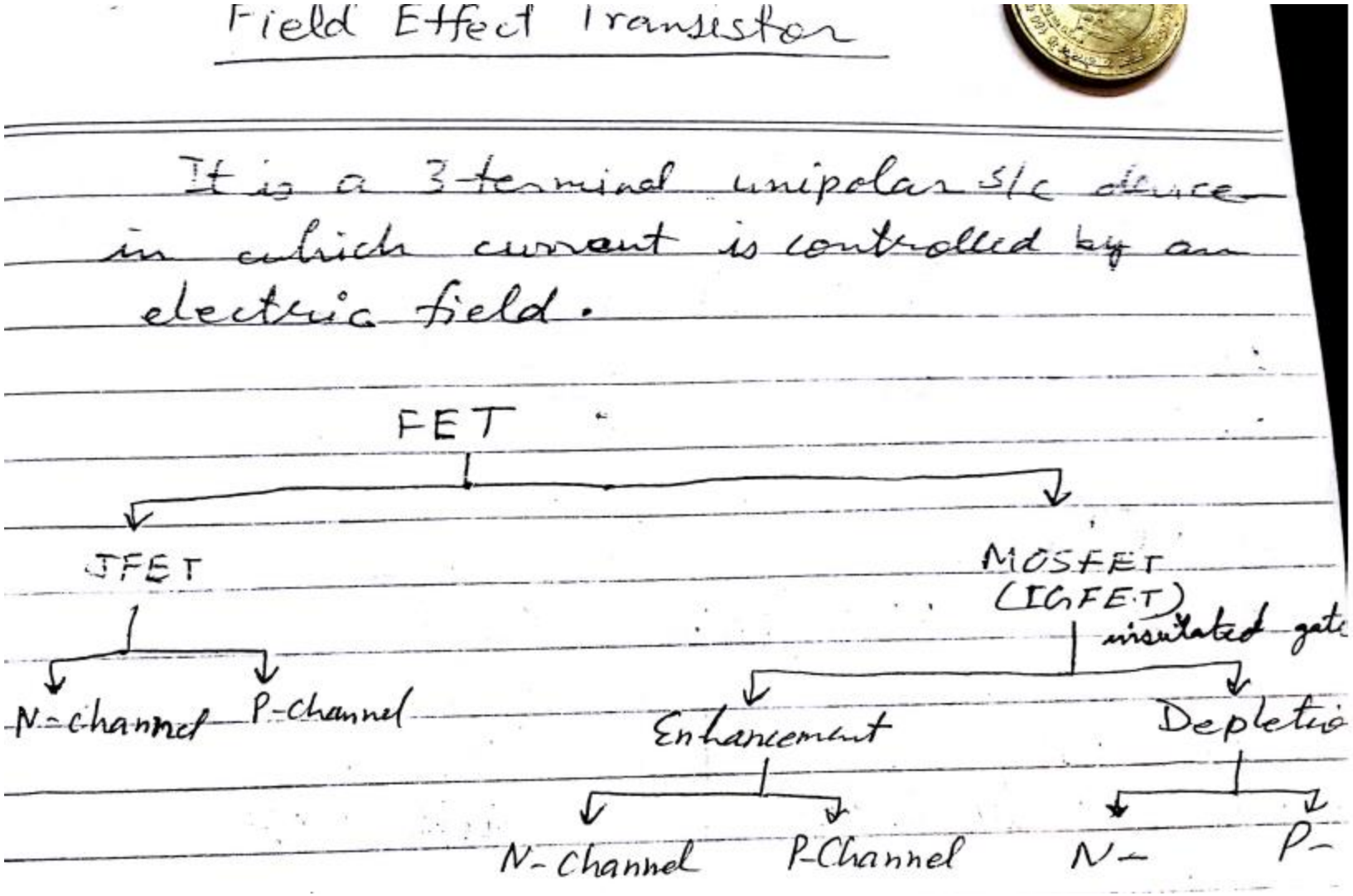
So we can say that sensistor has positive temperature coefficient of resistance (PTC).

Fig. shows sensistor compensation technique.

As shown in Fig. 1.39, R_1 is replaced by sensistor R_T in self bias circuit. Now, R_T and R_2 are the two resistors of the potential divider.

Introduction to FET’s

Classification



Advantage

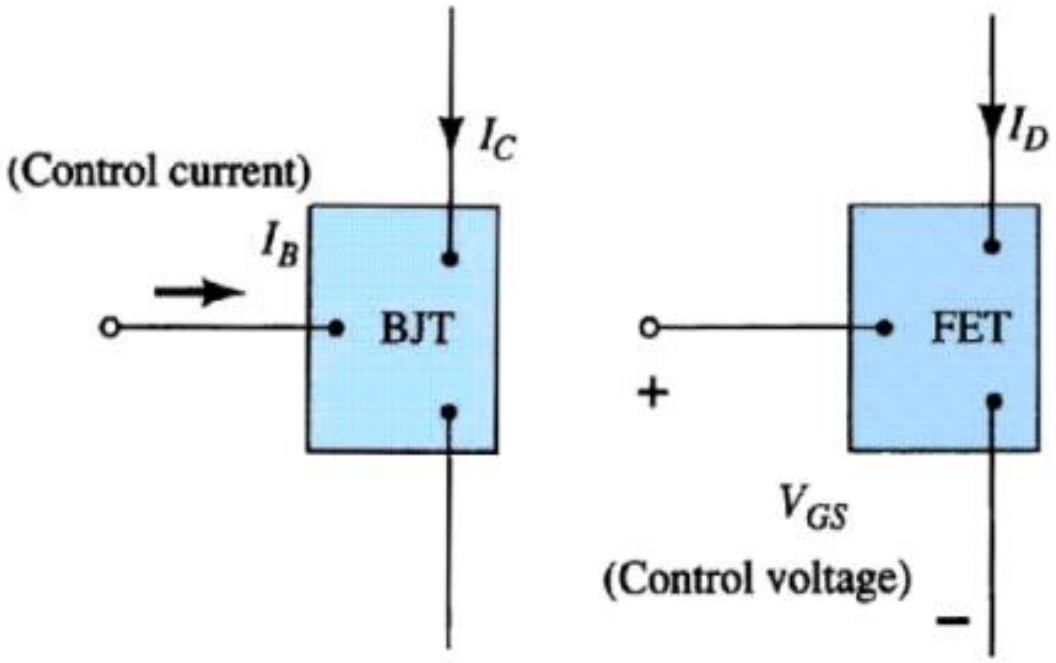
Advantage of FET over BJT :-

1) FET is Unipolar device.
2) I/p impedence is very high [MΩ]
3) Lessen Noisy (No ∫)
4) FET less affected by radiations.
5) Better thermal stability
6) Higher fabrication density
7) Smaller size, longer life, higher η
8) Higher Power gain.

Comparision

JFET	BJT
1) Unipolar	Bipolar
2) Voltage driven	Current controlled
3) Low Noise level	High
4) High I/P impedence	Low
5) Better Thermal stability	Less
6) Low Av	high (CE)
7) Costly	Cheaper
8) Small G x BW	high G x BW

Current Controlled vs Voltage Controlled Devices



Types of FET's

- JFET – Junction Field Effect Transistor
- MOSFET – Metal Oxide Semiconductor Field Effect Transistor
  - D-MOSFET - Depletion Mode MOSFET
  - E- MOSFET - Enhancement Mode MOSFET

Transfer Characteristics

The input-output transfer characteristic of the JFET is not as straight forward as it is for the BJT

In a BJT, β (h_{FE}) defines the relationship between I_B (input current) and I_C (output current).

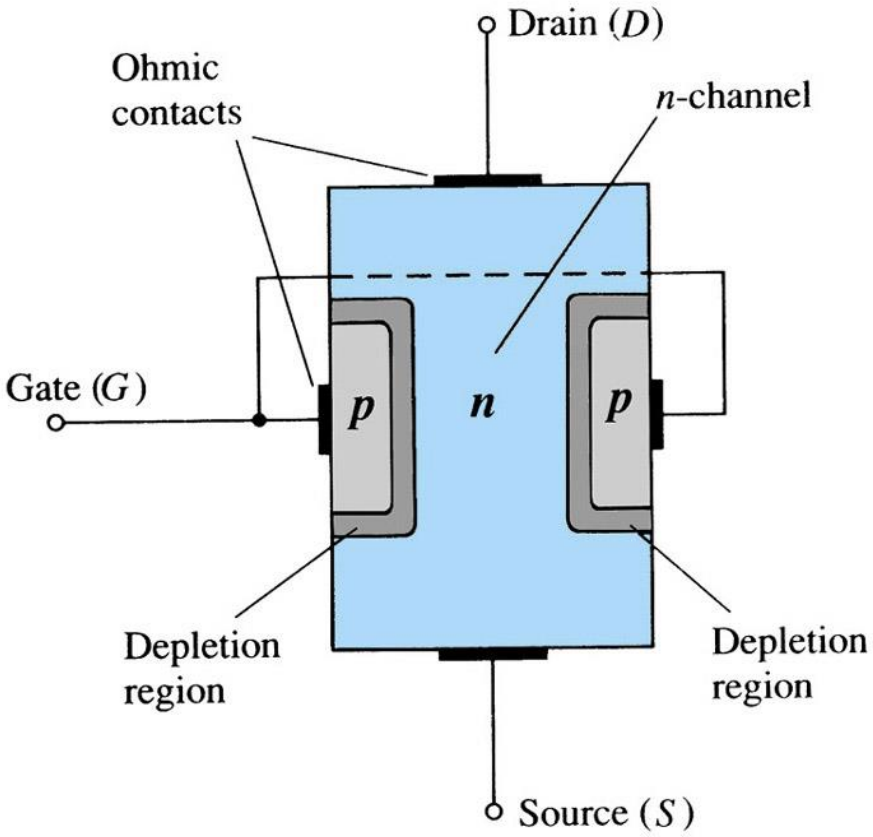
In a JFET, the relationship (Shockley's Equation) between V_{GS} (input voltage) and I_D (output current) is used to define the transfer characteristics, and a little more complicated (and not linear):

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

As a result, FET's are often referred to a square law devices

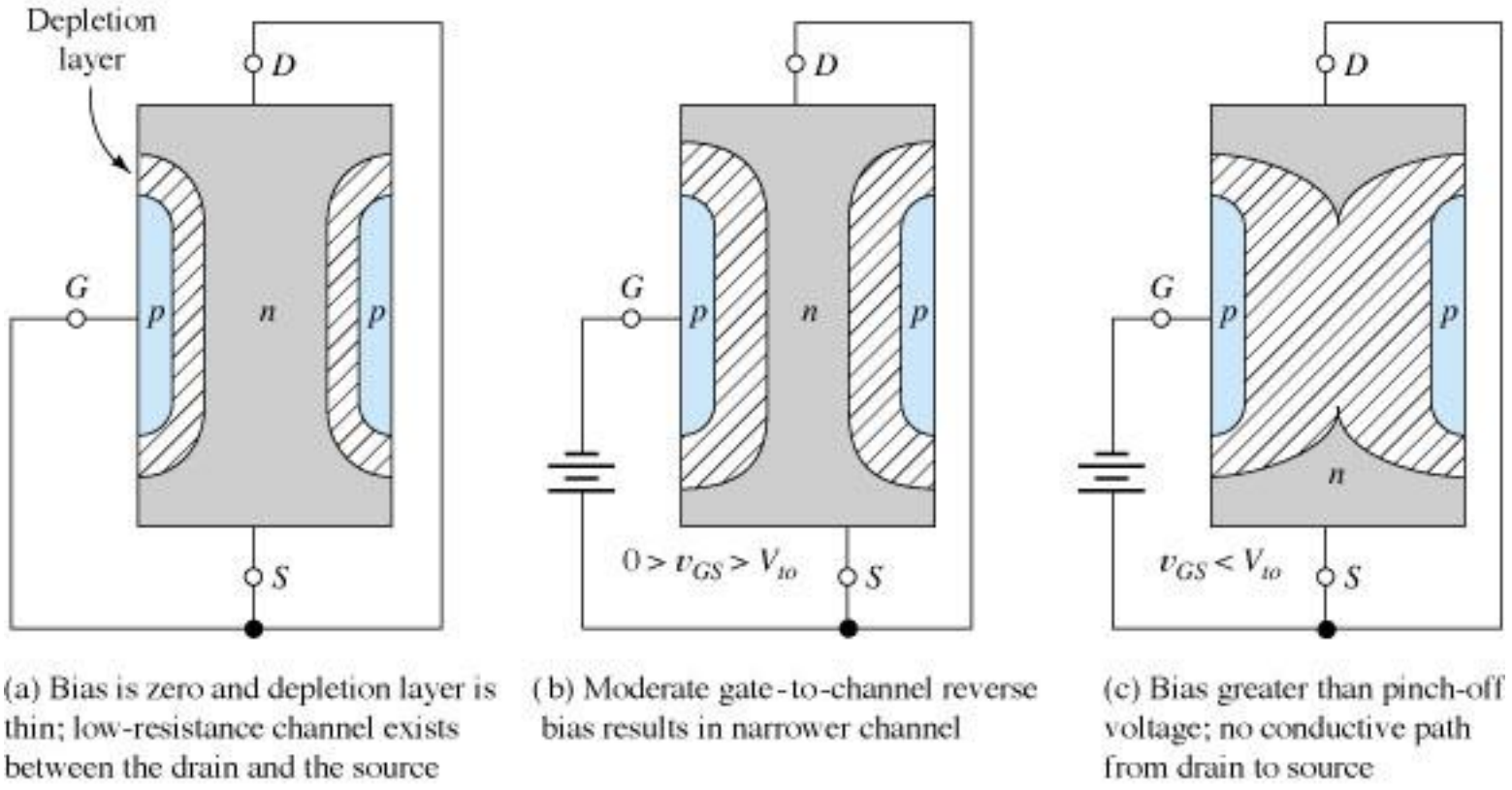
JFET Construction

There are two types of JFET's: n-channel and p-channel.
The n-channel is more widely used.



There are three terminals: Drain (D) and Source (S) are connected to n-channel
Gate (G) is connected to the p-type material

N-Channel JFET Operation



(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source

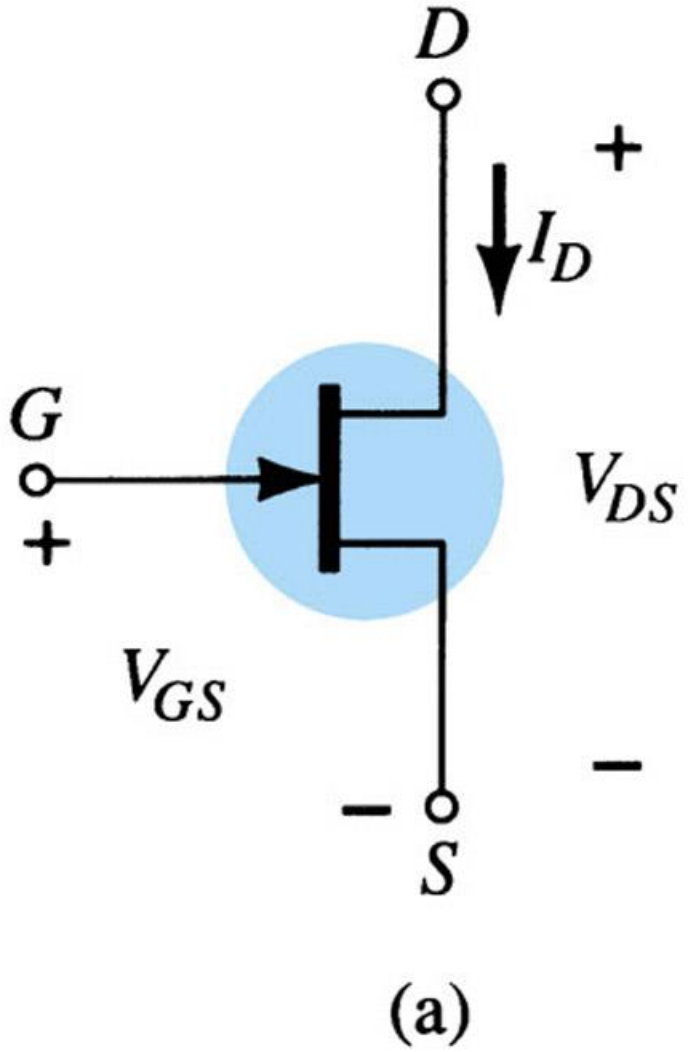
(b) Moderate gate-to-channel reverse bias results in narrower channel

(c) Bias greater than pinch-off voltage; no conductive path from drain to source

The nonconductive depletion region becomes thicker with increased reverse bias.

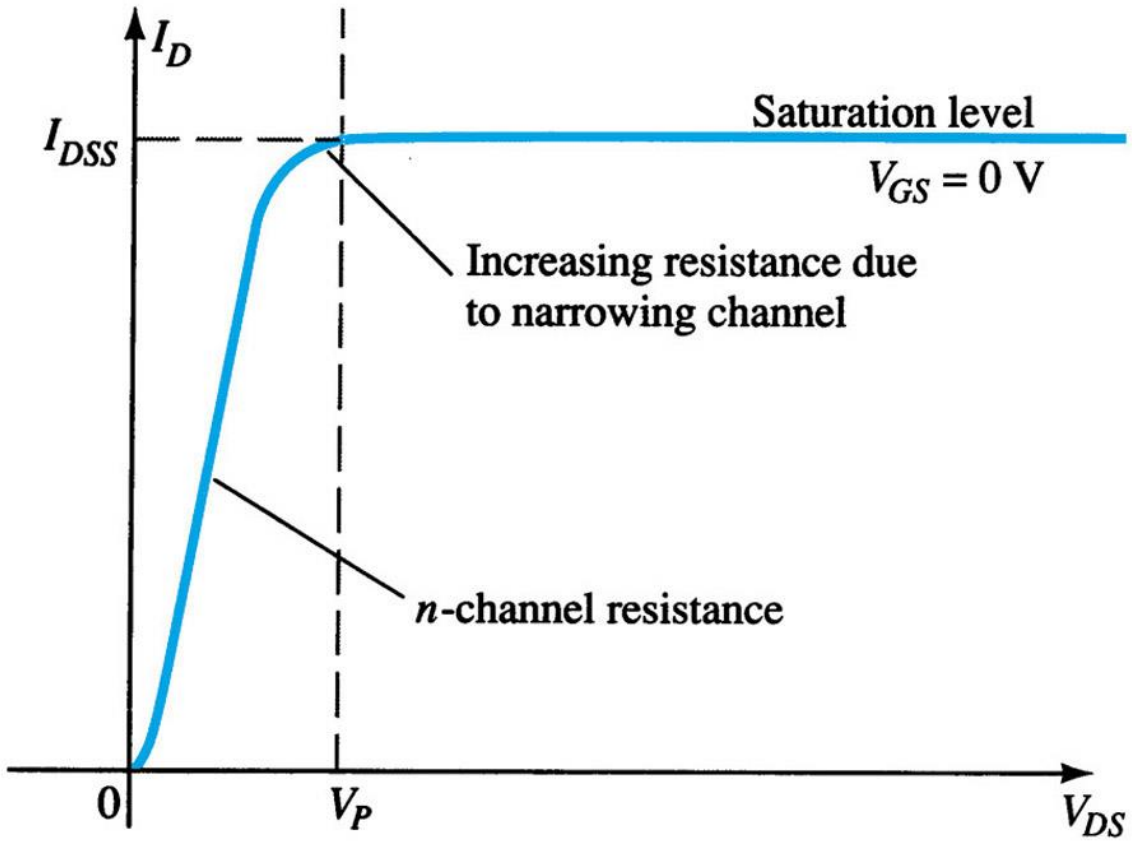
(*Note:* The two gate regions of each FET are connected to each other.)

N-Channel JFET Symbol



(a)

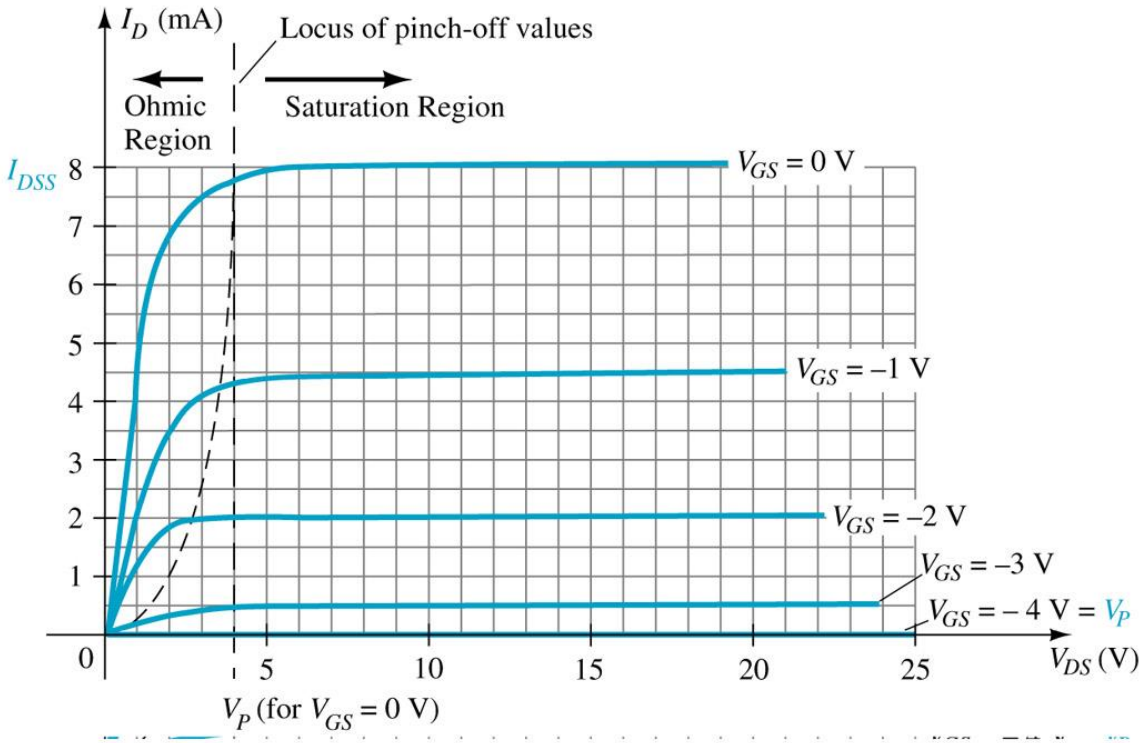
Saturation



At the pinch-off point:

- any further increase in V_{DS} does not produce any increase in I_D. V_{DS} at pinch-off is denoted as Vp.
- I_D is at saturation or maximum. It is referred to as I_{DSS}.
- The ohmic value of the channel is at maximum.

$I_D \leq I_{DSS}$

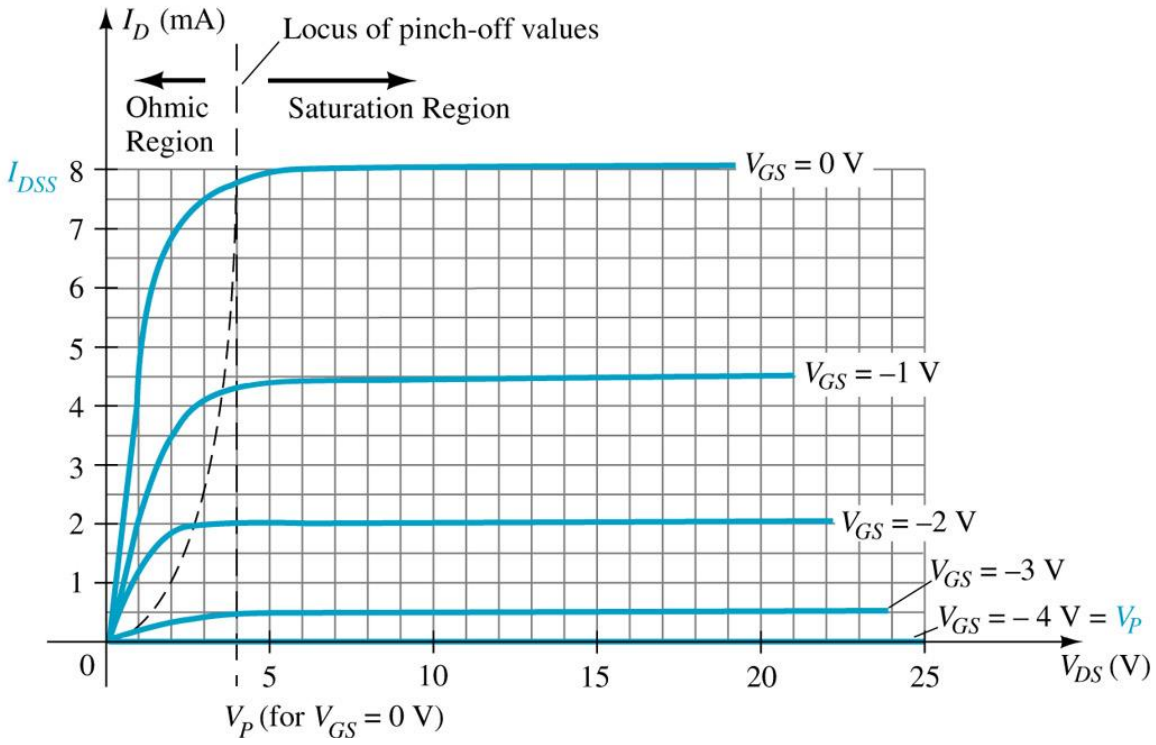


As V_{GS} becomes more negative:

- the JFET will pinch-off at a lower voltage (Vp).
- I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.
- Eventually I_D will reach 0A. V_{GS} at this point is called Vp or $V_{GS(off)}$.
- Also note that at high levels of V_{DS} the JFET reaches a breakdown situation.

ID will increases uncontrollably if $V_{DS} > V_{DSmax}$.

FET as a Voltage-Controlled Resistor

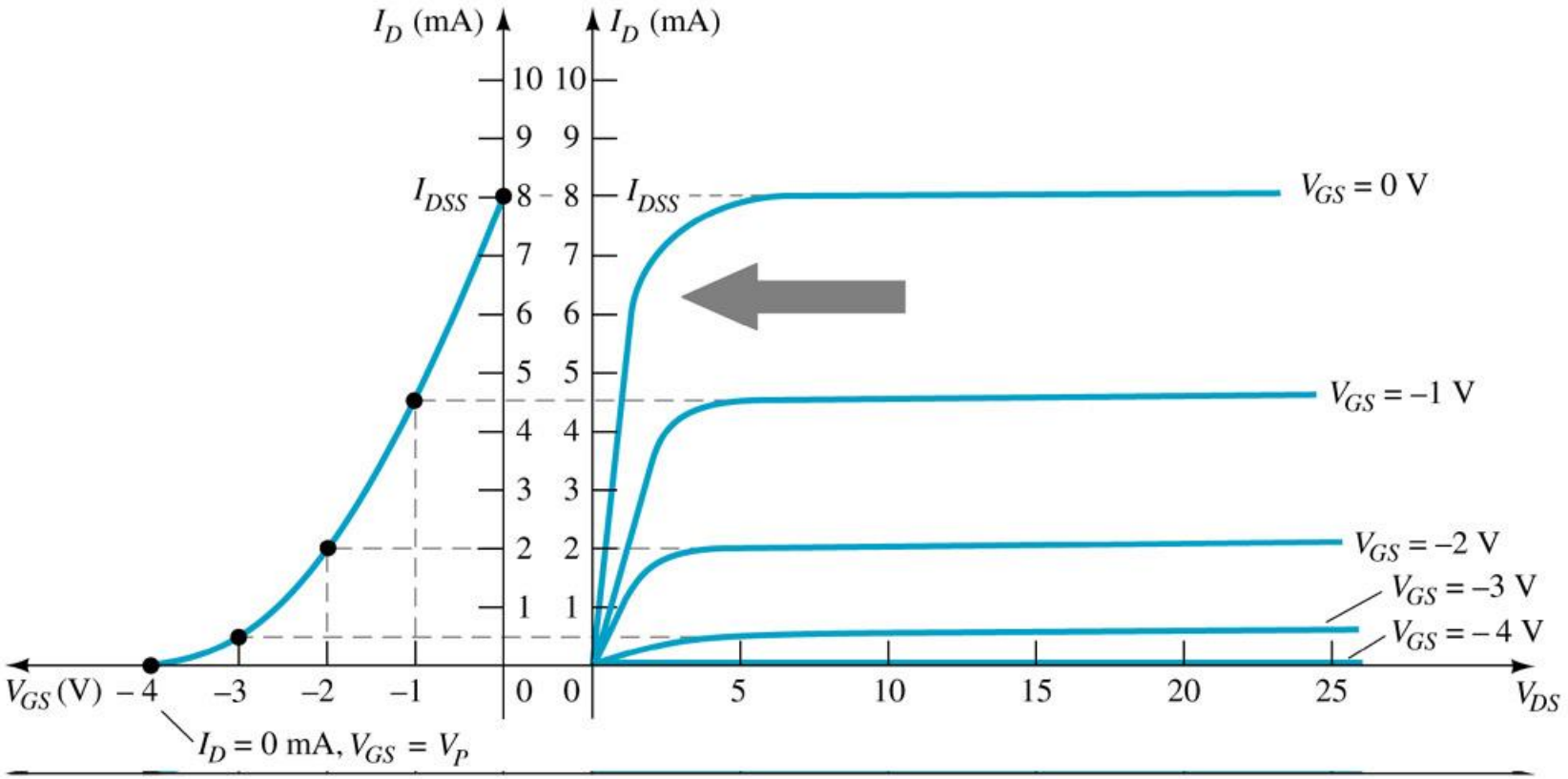


The region to the left of the pinch-off point is called the ***ohmic region***.

The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d). As V_{GS} becomes more negative, the resistance (r_d) increases.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

Transfer (Transconductance) Curve



From this graph it is easy to determine the value of I_D for a given value of V_{GS}
It is also possible to determine I_{DSS} and V_P by looking at the knee where V_{GS} is 0

Plotting the Transconductance Curve

Using I_{DSS} and V_P (or $V_{GS(off)}$) values found in a specification sheet, the Family of Curves can be plotted by making a table of data using the following 3 steps:

Step 1:

Solve $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ for $V_{GS} = 0V$

Step 2

Solve $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ for $V_{GS} = V_P$ (aka $V_{GS(off)}$)

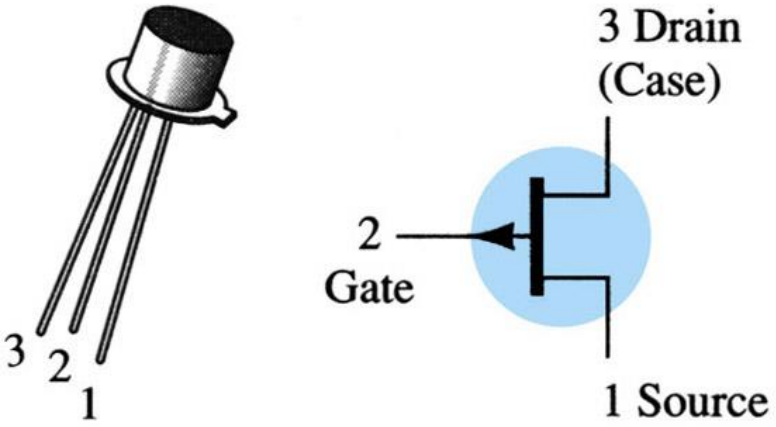
Step 3:

Solve $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ for $0V \geq V_{GS} \geq V_P$ in 1V increments for V_{GS}

Case Construction and Terminal Identification

2N2844

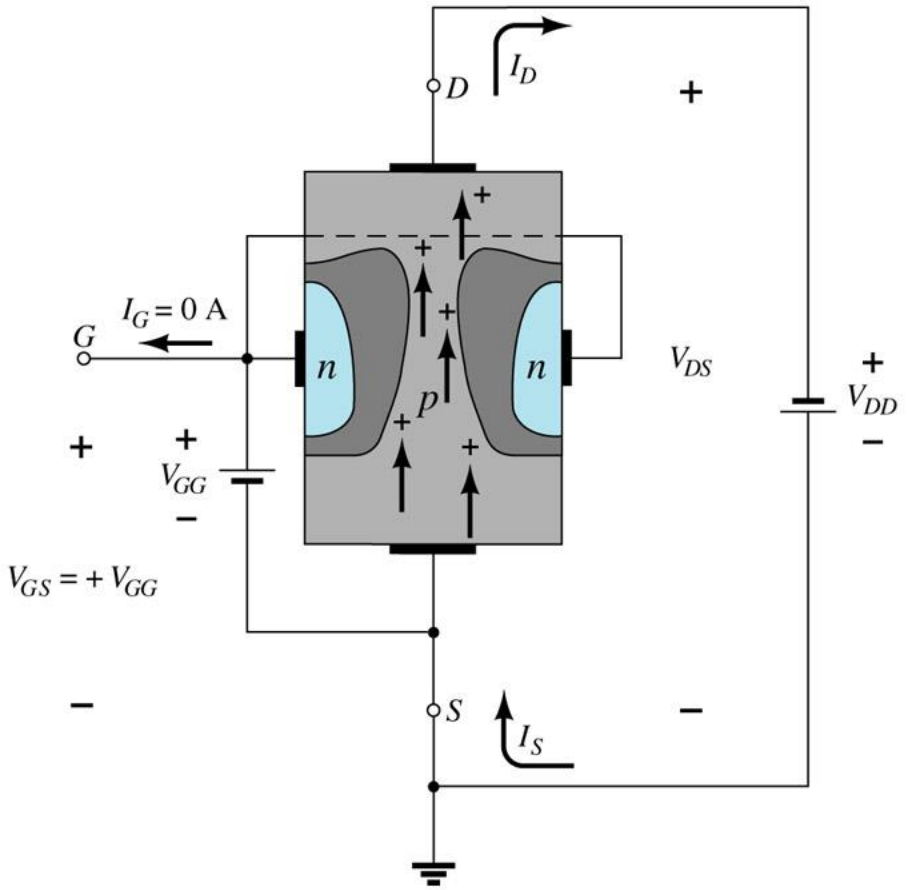
CASE 22-03, STYLE 12
TO-18 (TO-206AA)



JFETs
GENERAL PURPOSE
P-CHANNEL

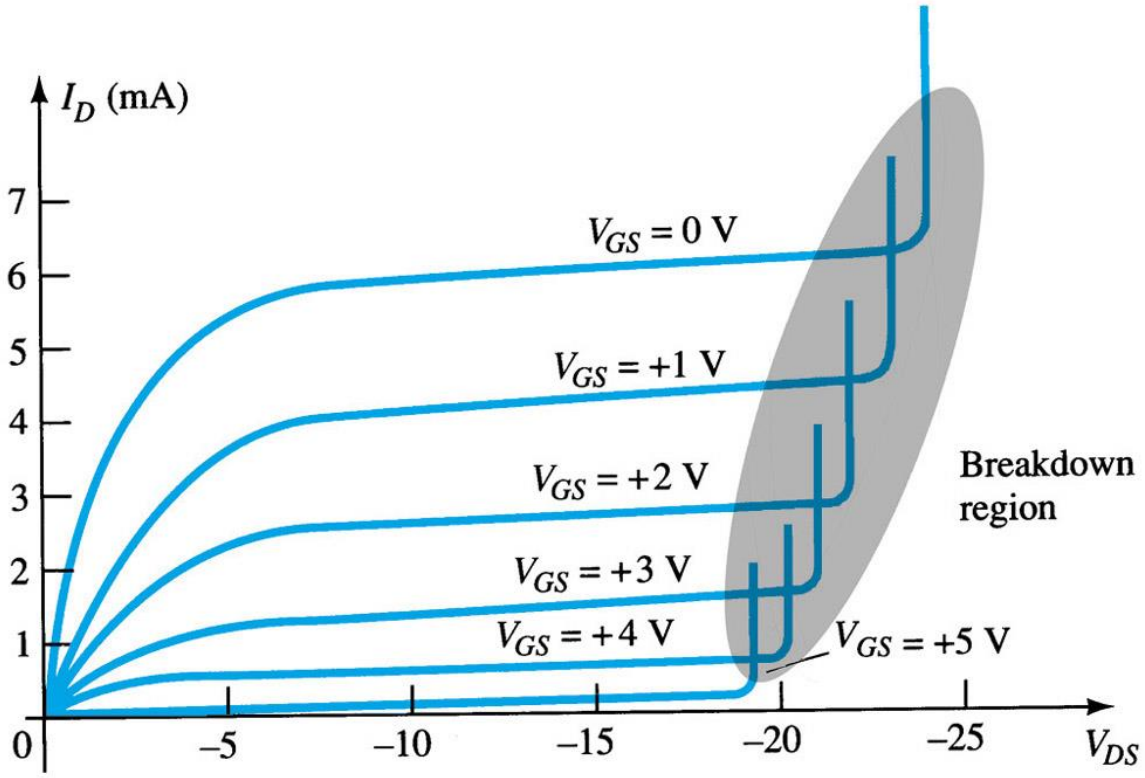
This information is found on the specification sheet

p-Channel JFET's



p-Channel JFET operates in a similar manner as the n-channel JFET except the voltage polarities and current directions are reversed

P-Channel JFET Characteristics



As V_{GS} increases more positively

- the depletion zone increases
- I_D decreases ($I_D < I_{DSS}$)
- eventually $I_D = 0A$

Also note that at high levels of VDS the JFET reaches a breakdown situation. ID increases uncontrollably if $V_{DS} > V_{DSmax}$.

MOSFET’s

MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make them very useful

There are 2 types of MOSFET's:

- Enhancement Mode MOSFET (E-MOSFET)
  - Operates in Enhancement mode
  - $I_{DSS} = 0$ until $V_{GS} > V_T$ (threshold voltage)
- Depletion mode MOSFET (D-MOSFET)
  - Operates in Depletion mode the same way as a JFET when $V_{GS} \leq 0$
  - Operates in Enhancement mode like E-MOSFET when $V_{GS} > 0$

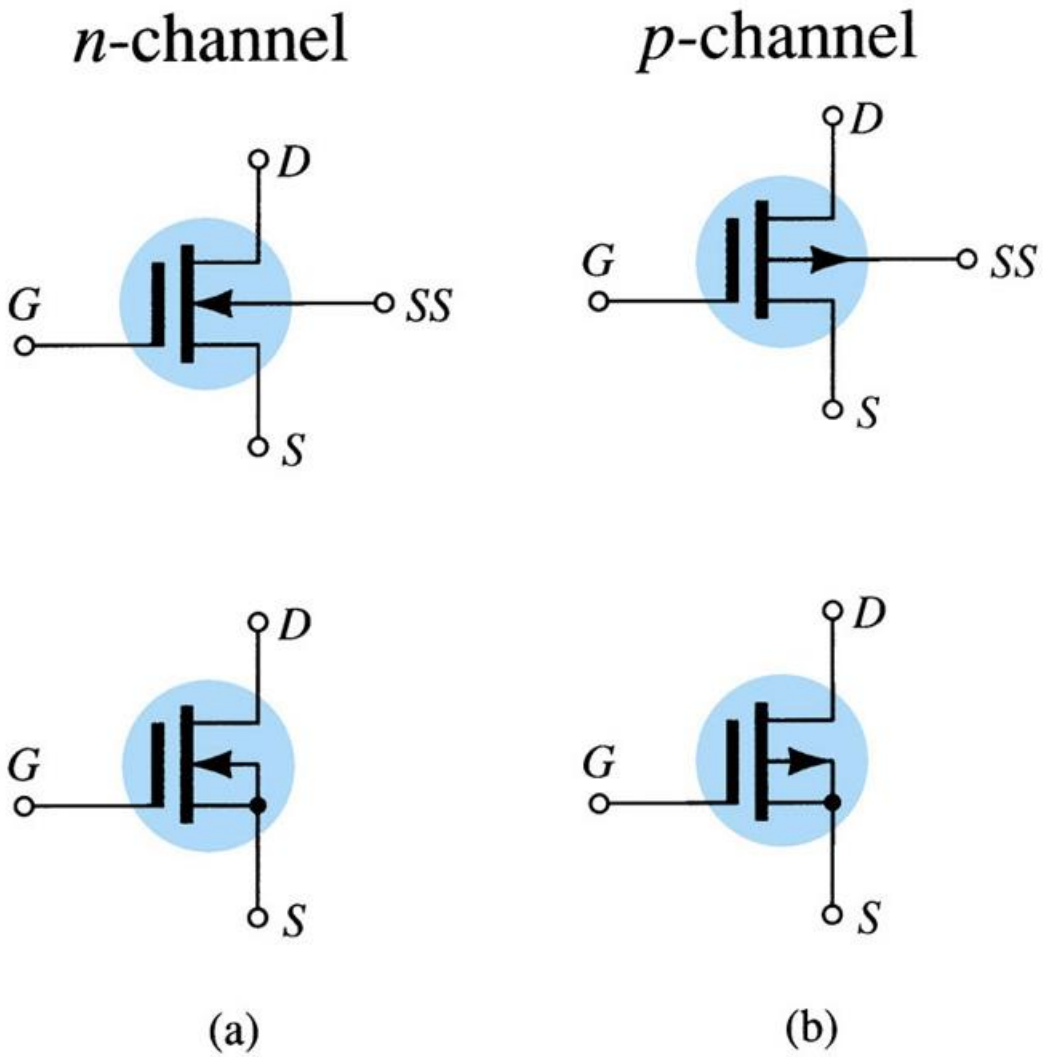
MOSFET Handling

MOSFETs are very static sensitive. Because of the very thin SiO_2 layer between the external terminals and the layers of the device, any small electrical discharge can stablish an unwanted conduction.

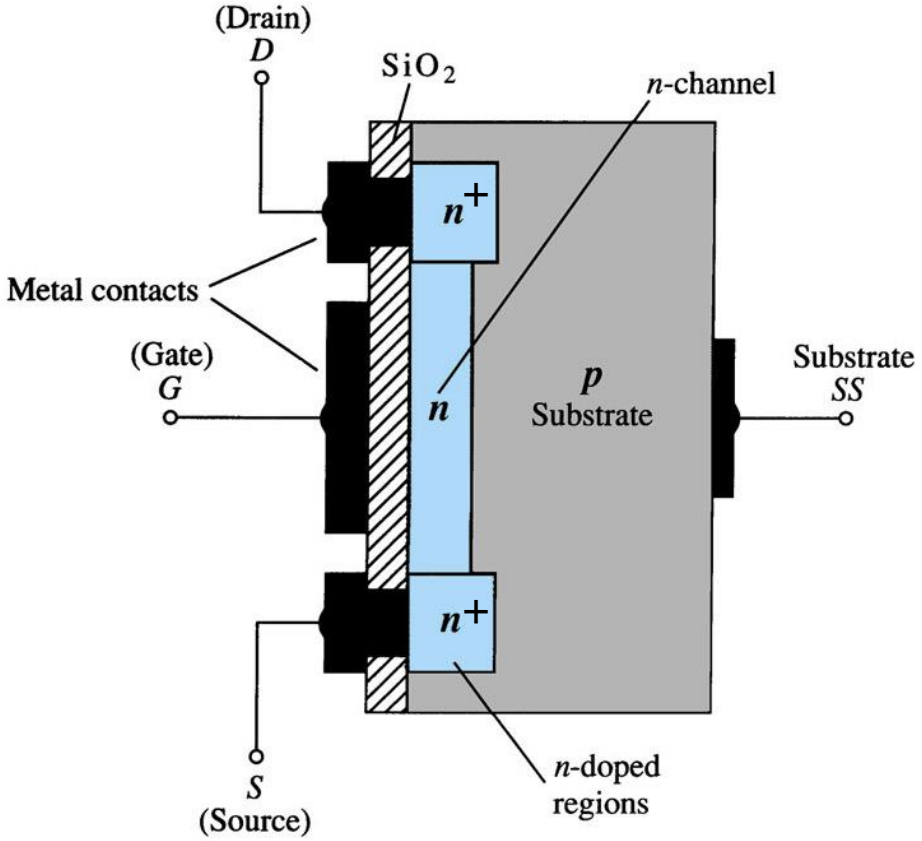
Protection:

- Always transport in a static sensitive bag
- Always wear a static strap when handling MOSFETS
- Apply voltage limiting devices between the Gate and Source, such as back-to-back Zeners to limit any transient voltage

D-MOSFET Symbols

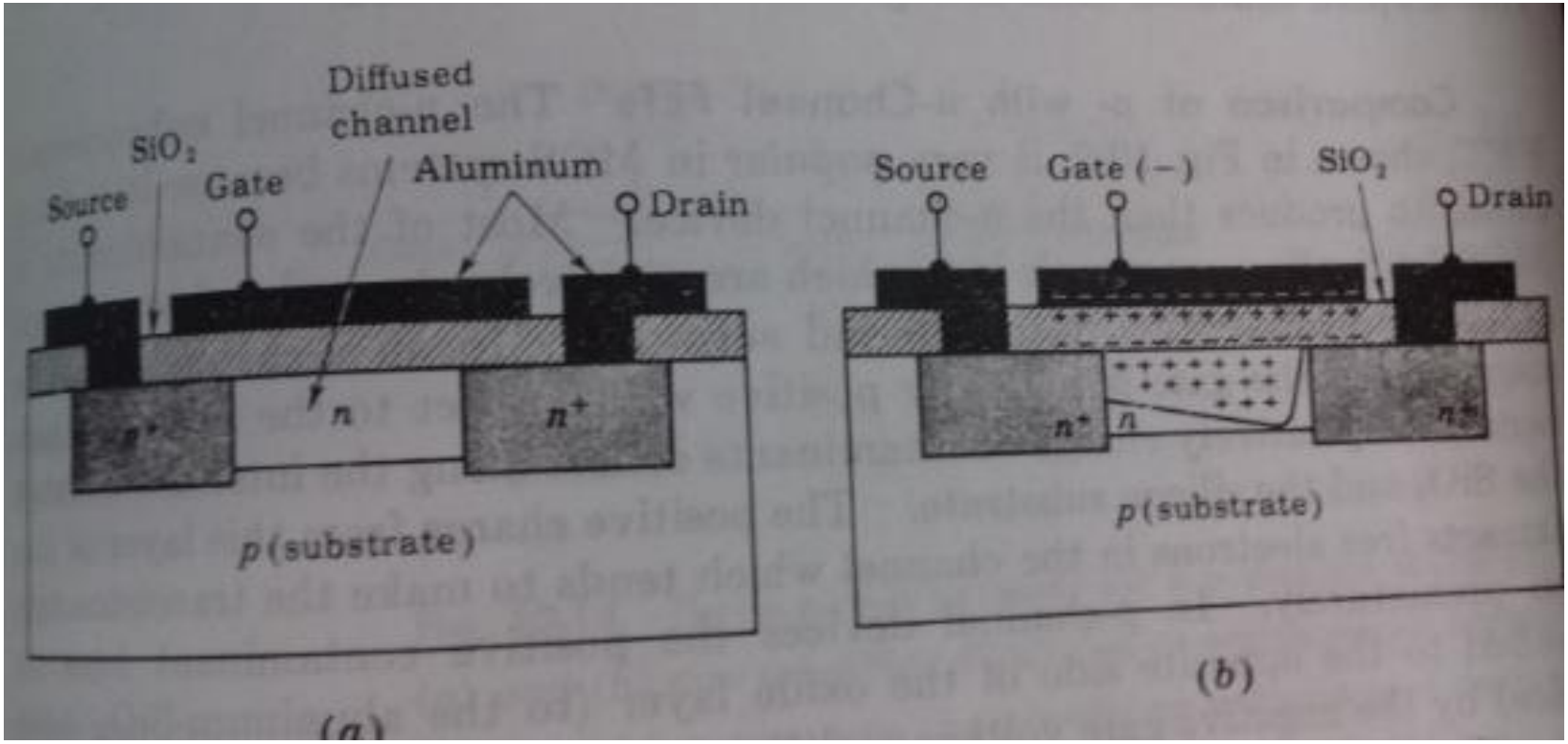


Depletion Mode MOSFET Construction



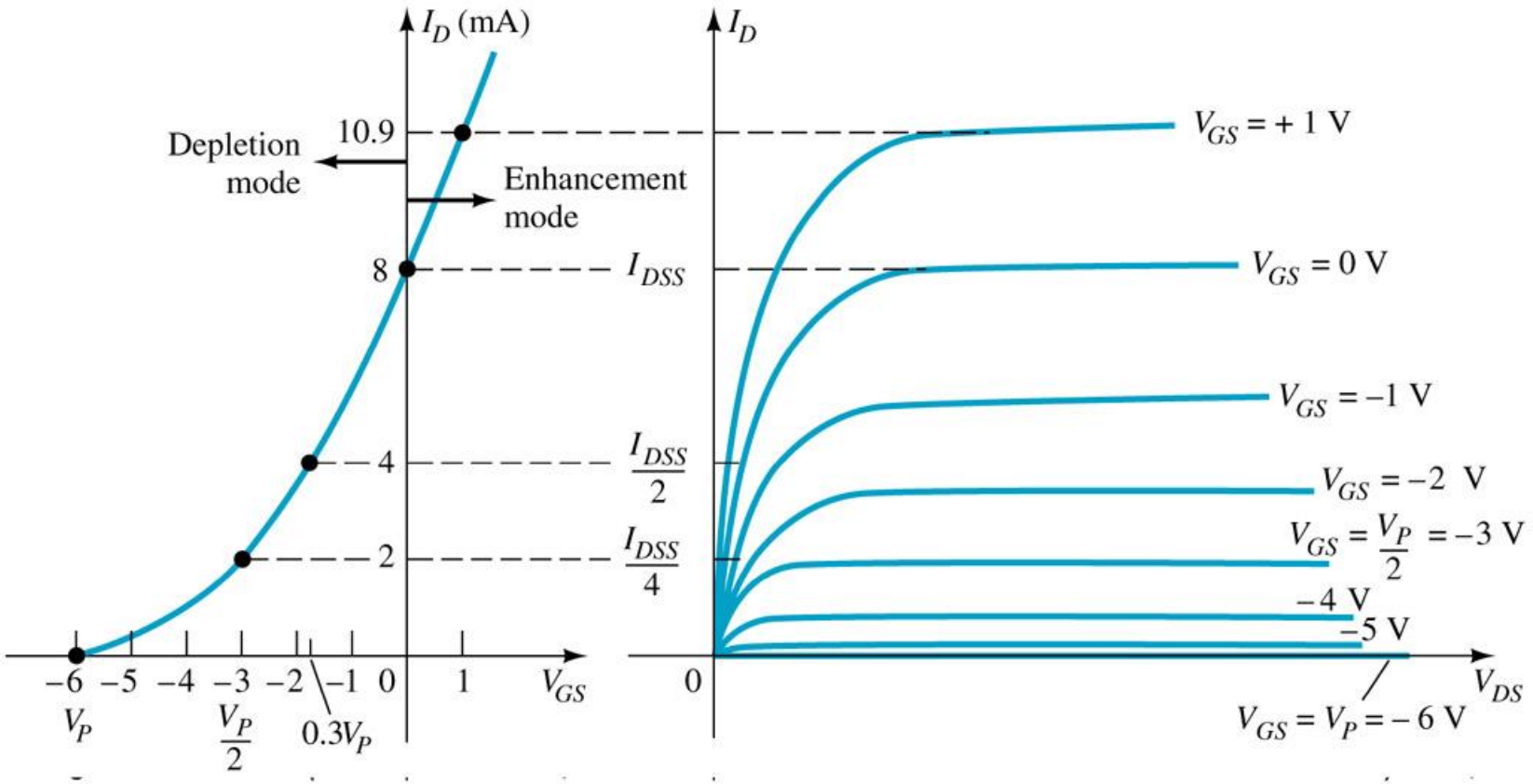
The Drain (D) and Source (S) leads connect to the to n-doped regions
These N-doped regions are connected via an n-channel
This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

Working

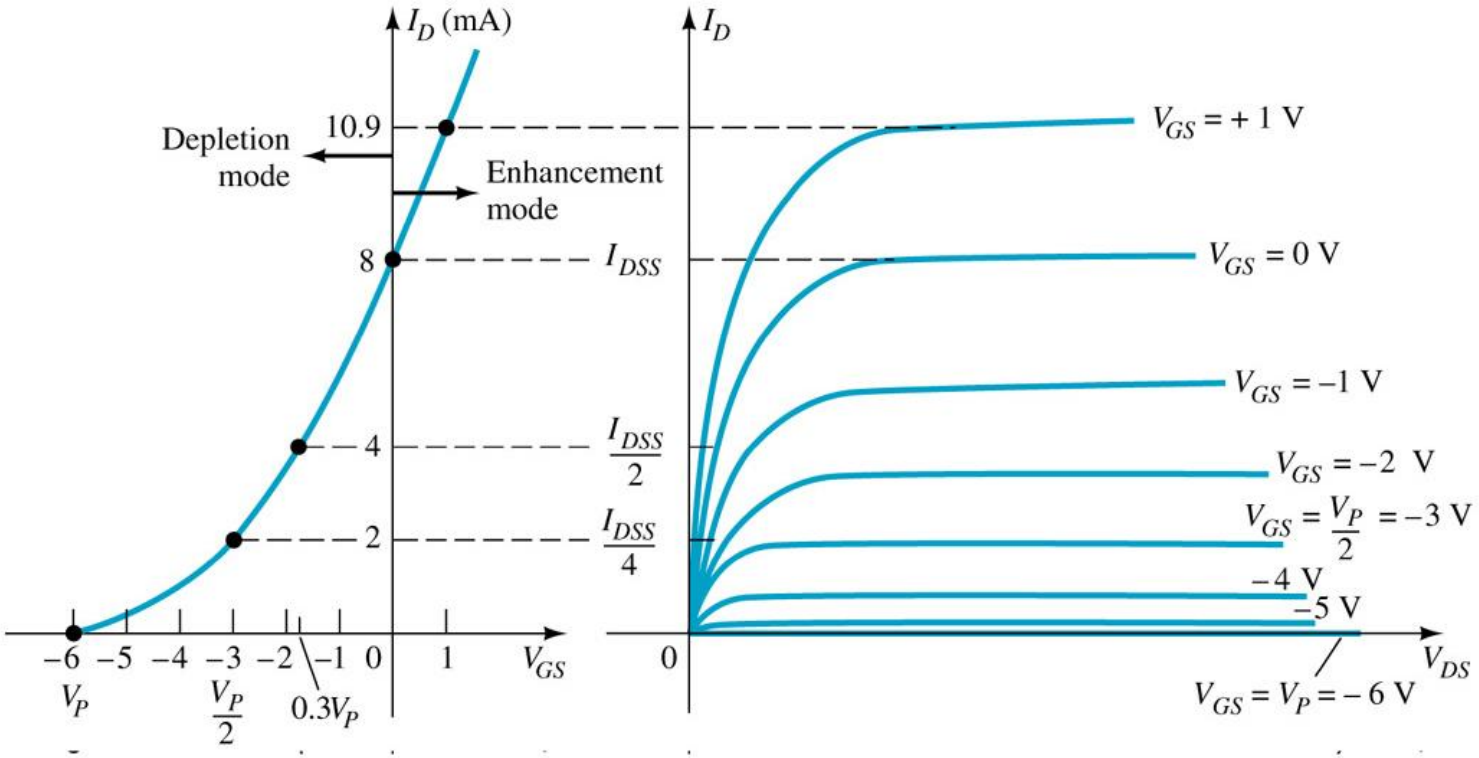

Diffused
channel
SiO_2
Source
Gate
Aluminum
Drain
n^+
n
n^+
p(substrate)
(a)
Source
Gate (−)
SiO_2
Drain
n^+
n
n^+
p(substrate)
(b)

Basic Operation

A D-MOSFET may be biased to operate in two modes:
the **Depletion** mode or the **Enhancement** mode



D-MOSFET Depletion Mode Operation



The transfer characteristics are similar to the JFET

In Depletion Mode operation:

When $V_{GS} = 0V$, $I_D = I_{DSS}$

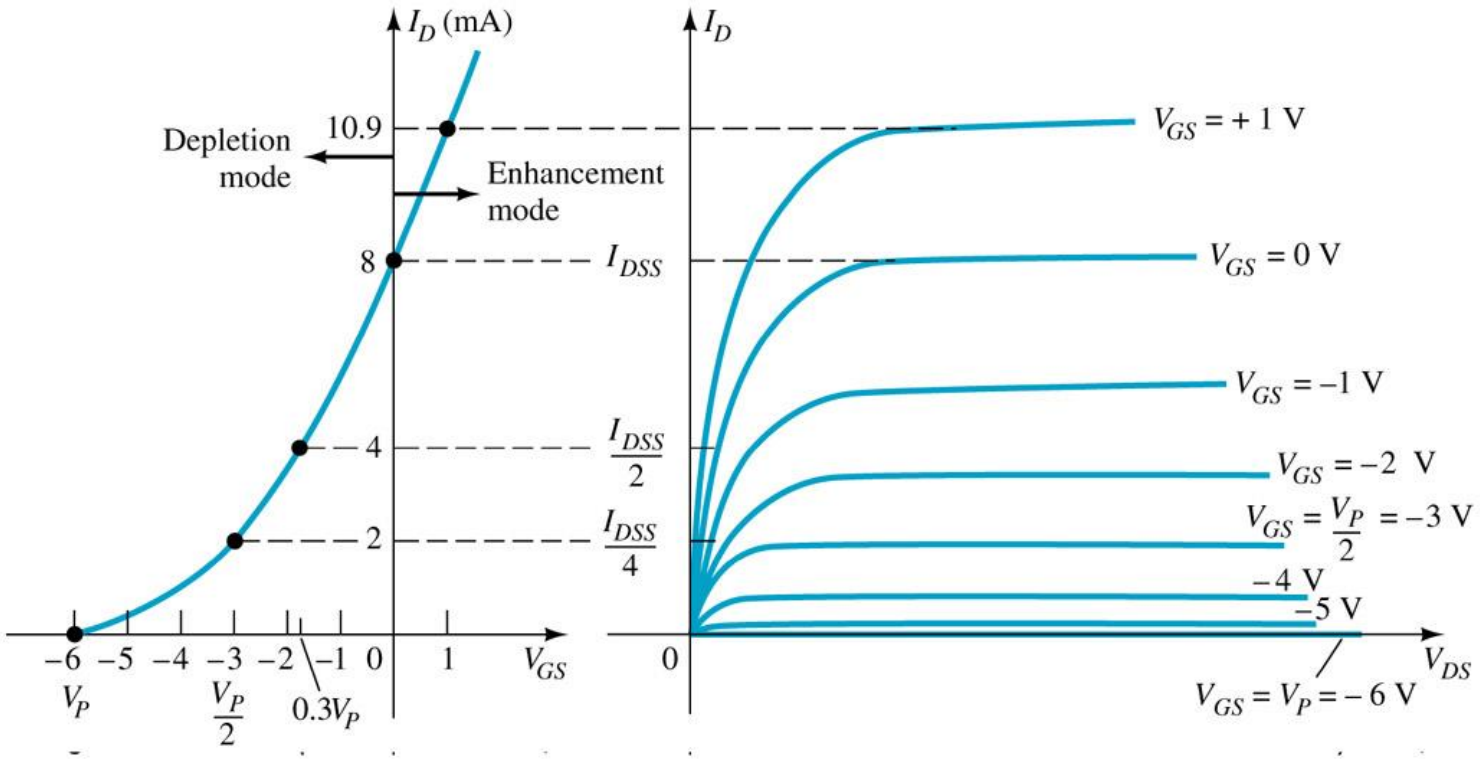
When $V_{GS} < 0V$, $I_D < I_{DSS}$

When $V_{GS} > 0V$, $I_D > I_{DSS}$

The formula used to plot the Transfer Curve, is:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

D-MOSFET Enhancement Mode Operation

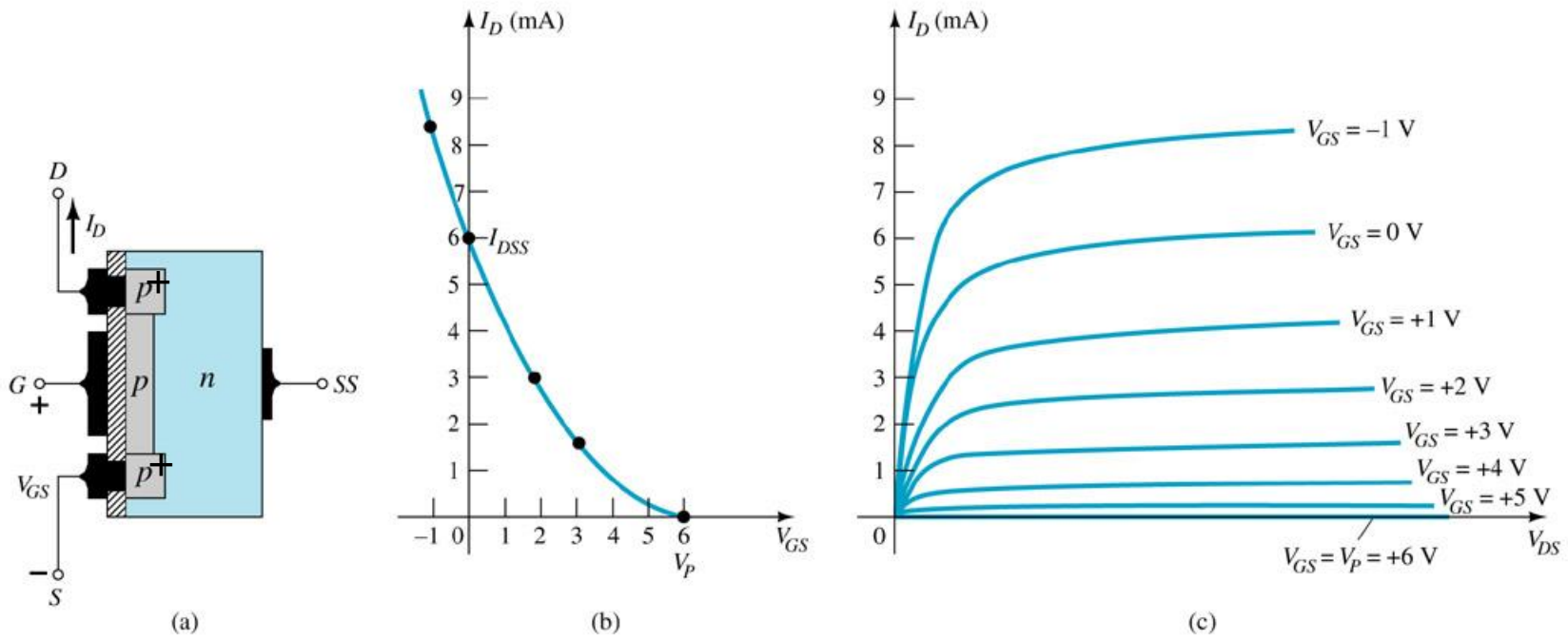


Enhancement Mode operation

In this mode, the transistor operates with $V_{GS} > 0V$, and I_D increases above I_{DSS} Shockley's equation, the formula used to plot the Transfer Curve, still applies but V_{GS} is positive:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

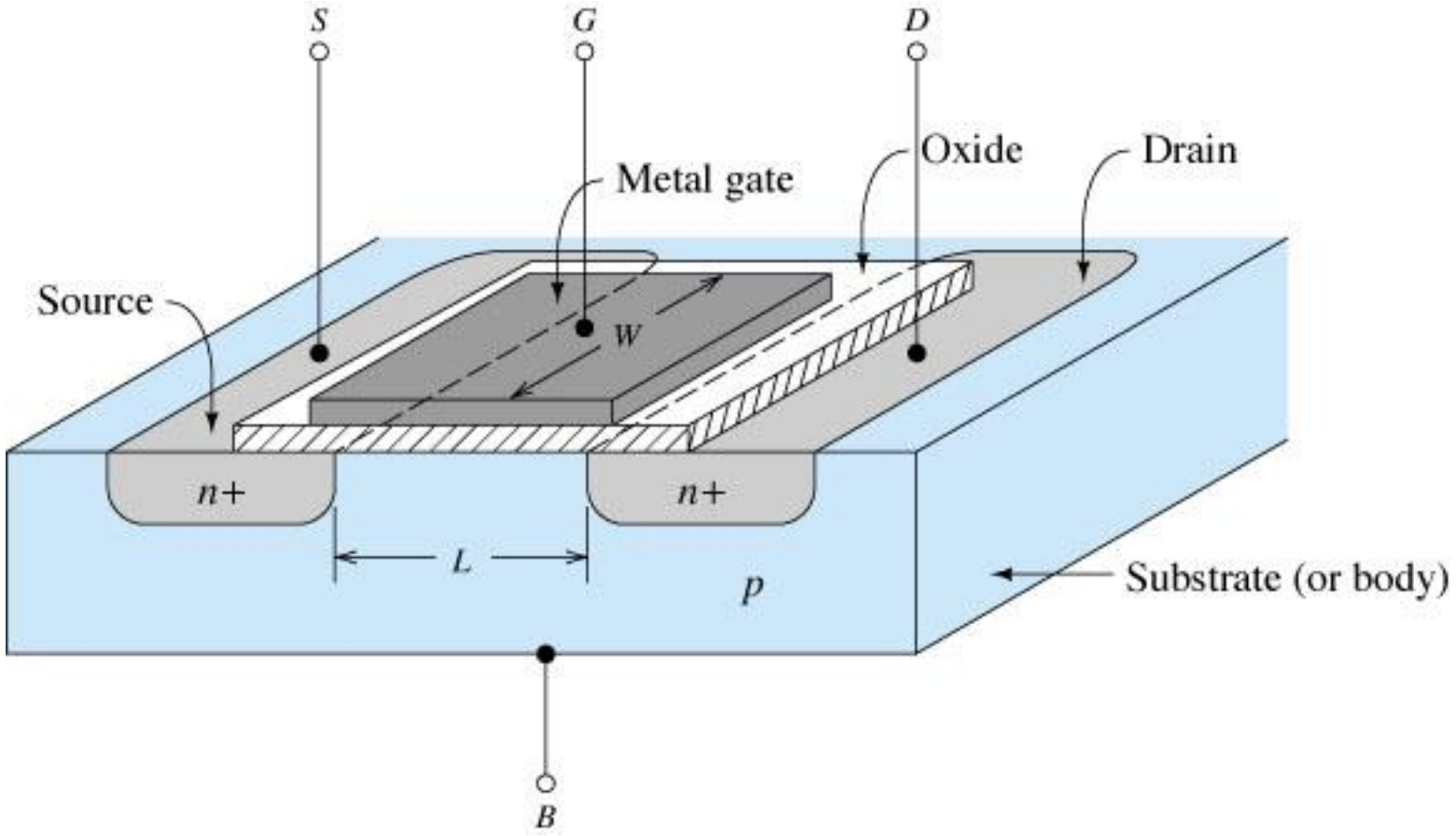
p-Channel Depletion Mode MOSFET



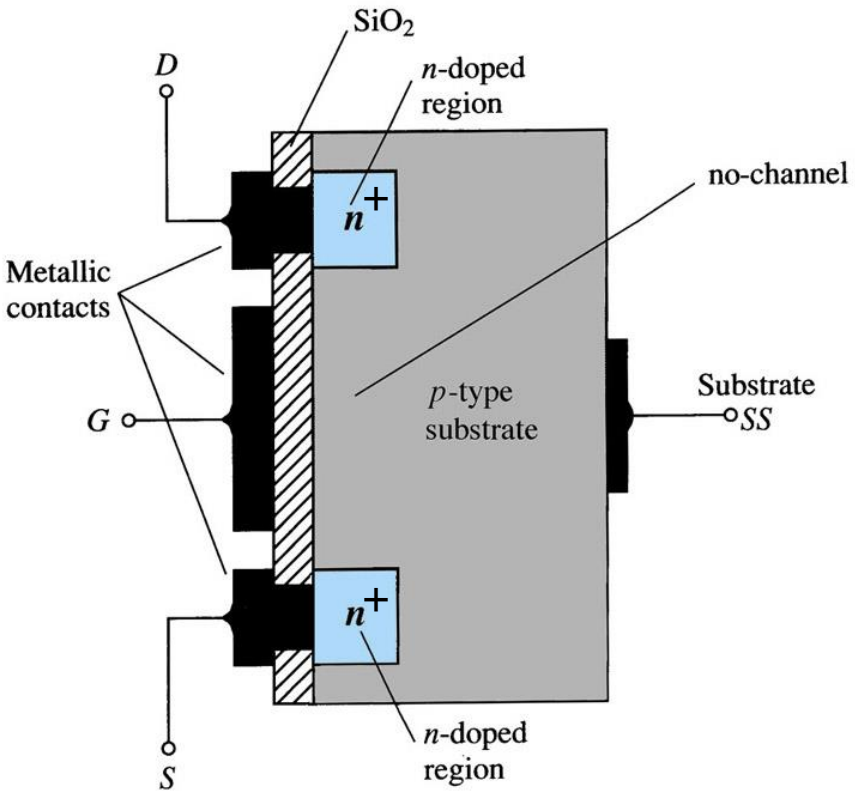
The p-channel Depletion mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed

Enhancement Mode MOSFET's

n-Channel E-MOSFET showing channel length L and channel width W



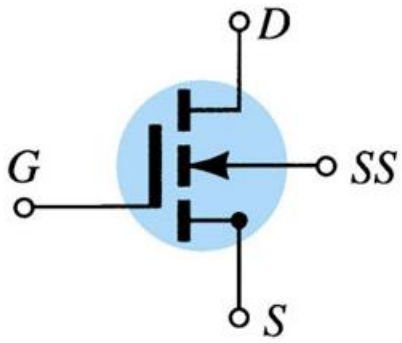
Enhancement Mode MOSFET Construction

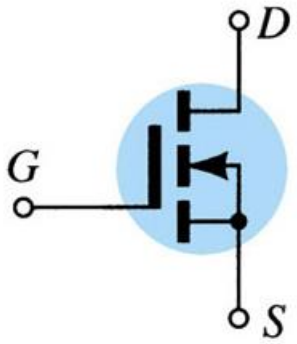


The Drain (D) and Source (S) connect to the to n-doped regions
These n-doped regions are not connected via an n-channel without an external voltage
The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO_2
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

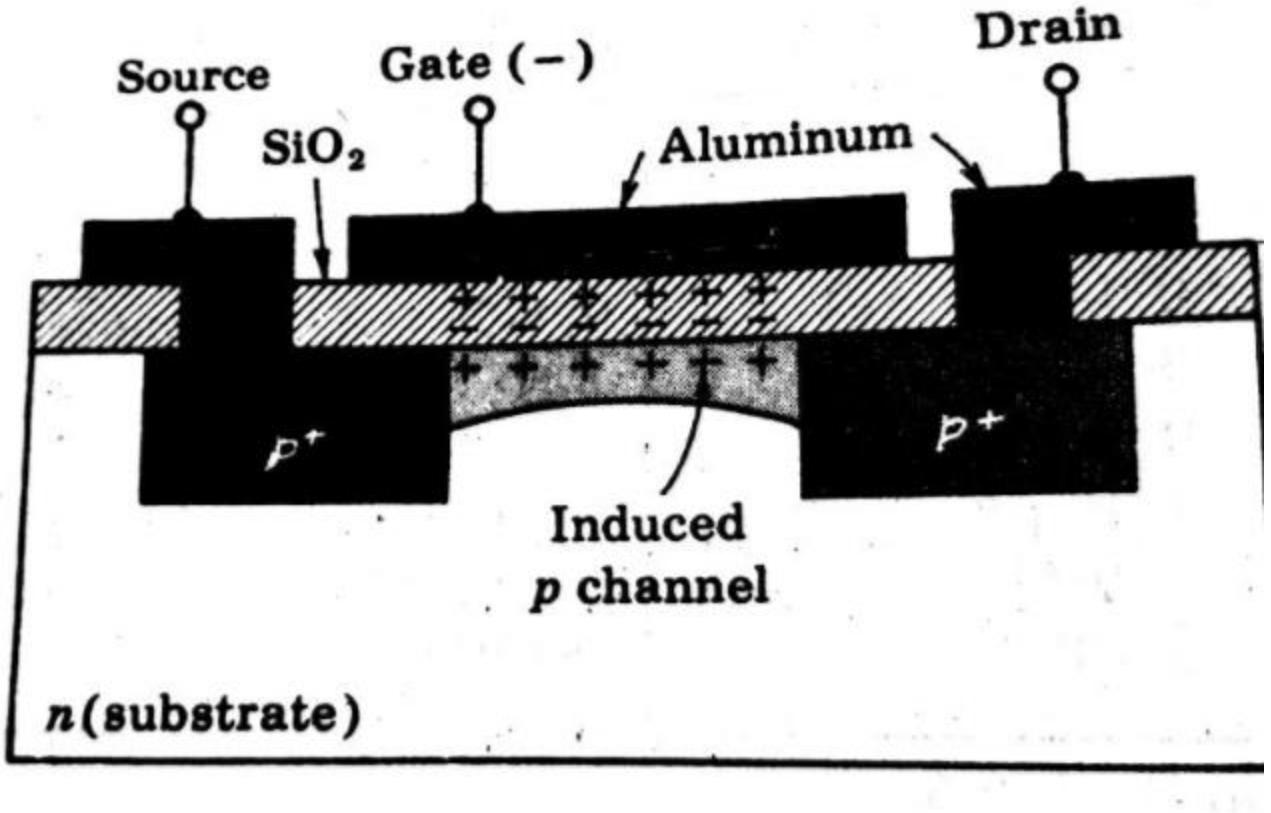
E-MOSFET Symbols

n-channel



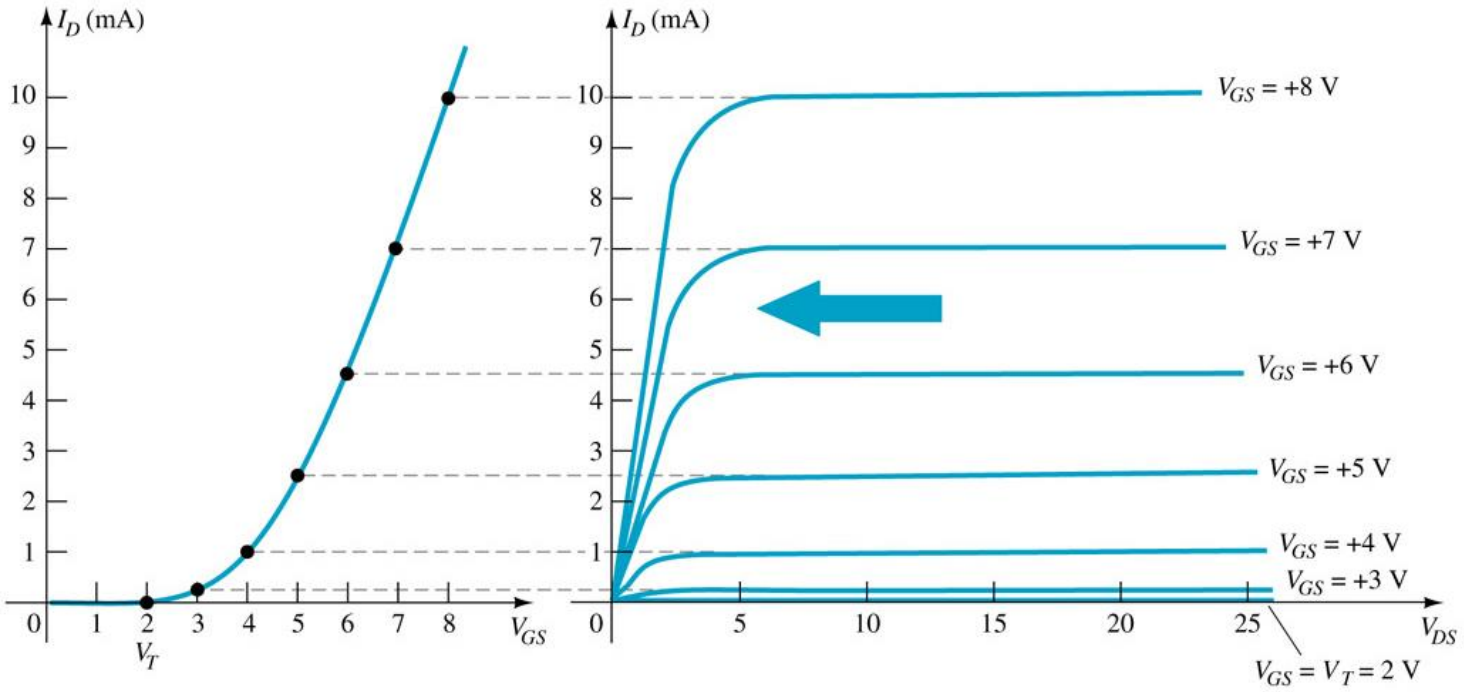


p-channel Enhancement MOSFET--Working



Basic Operation

The Enhancement mode n-channel MOSFET only operates in the enhancement mode.



V_{GS} is always positive

$I_{DSS} = 0$ when $V_{GS} < V_T$

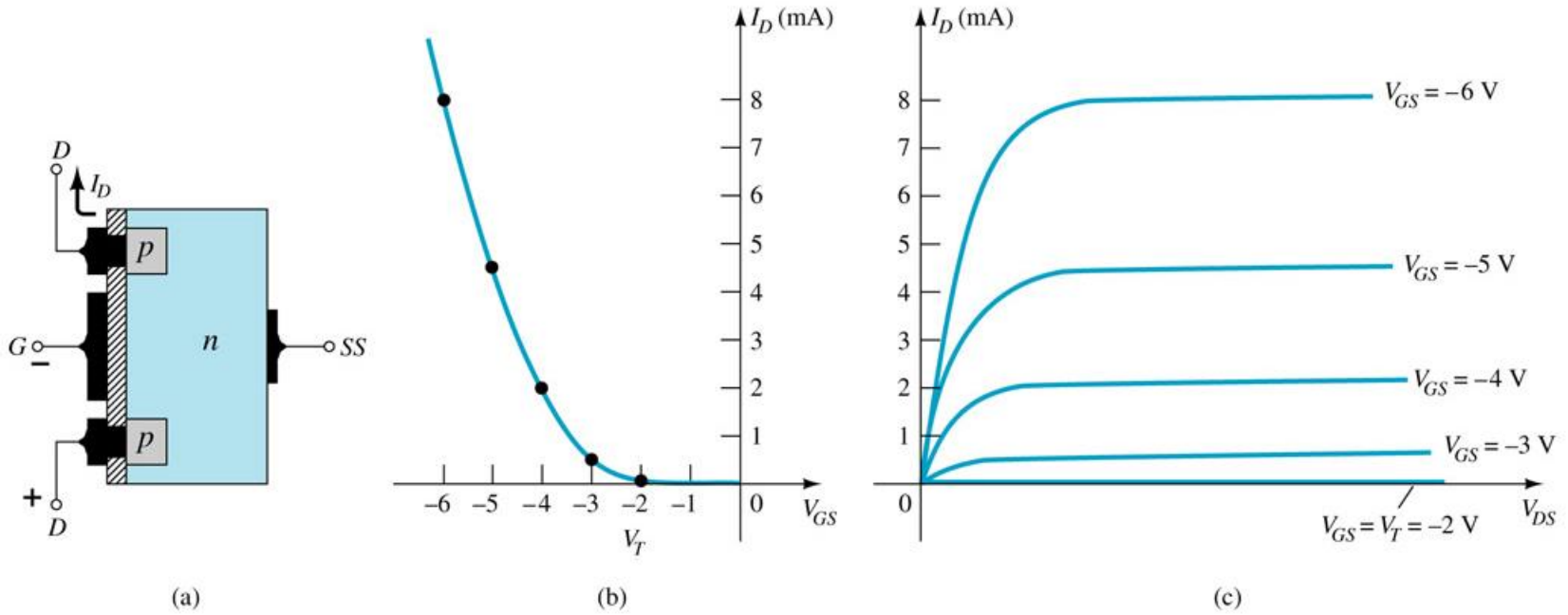
As V_{GS} increases above V_T, I_D increases

If V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS})

The saturation level, V_{DSsat} is reached.

p-Channel Enhancement Mode MOSFETs

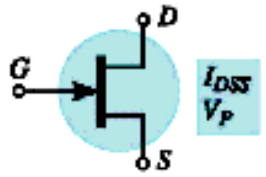
The p-channel Enhancement mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.



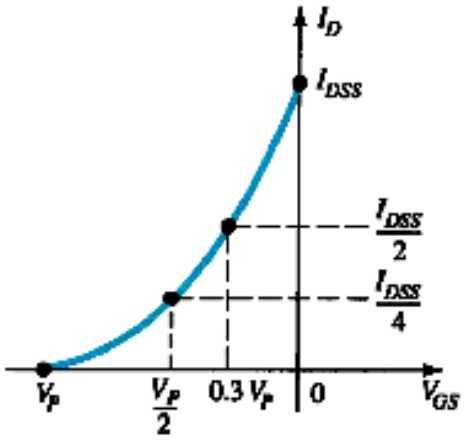
Summary Table

JFET

$I_G = 0\ \text{A}, I_D = I_S$

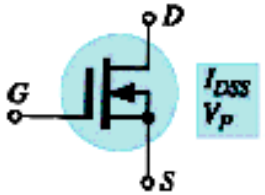


$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

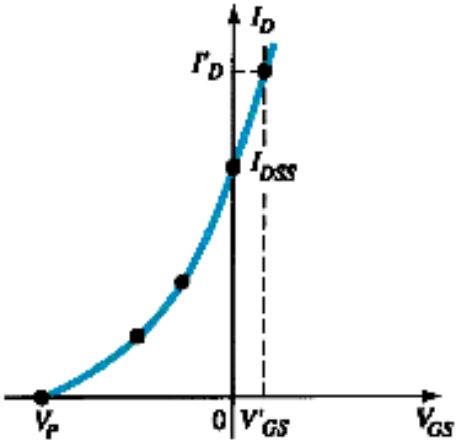


D-MOSFET

$I_G = 0\ \text{A}, I_D = I_S$

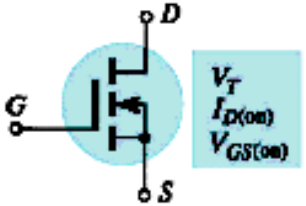


$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



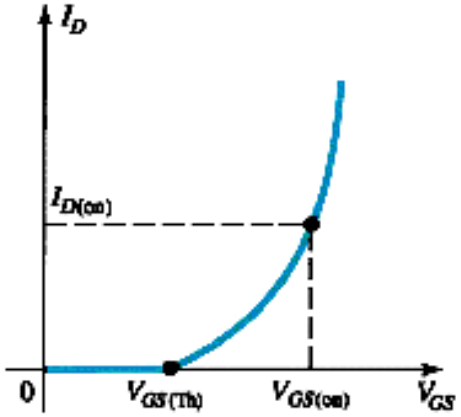
E-MOSFET

$I_G = 0\ \text{A}, I_D = I_S$



$$I_D = k(V_{GS} - V_{GS(Th)})^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

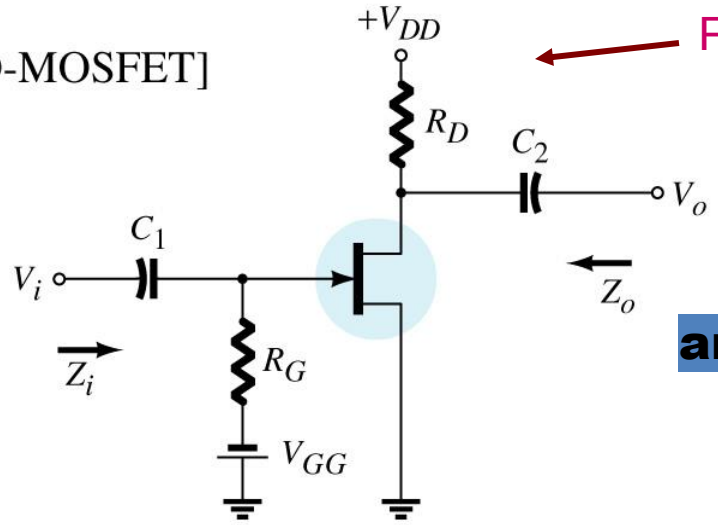


Biasing Circuits used for JFET

- Fixed bias circuit
- Self bias circuit
- Potential Divider bias circuit

JFET (n-channel) Biasing Circuits

Fixed-bias
[JFET or D-MOSFET]



For Fixed Bias Circuit

Applying KVL to gate circuit we get

$$V_{GG} = I_G R_G + V_{GS} = V_{GS} = Fixed, \because I_G = 0$$

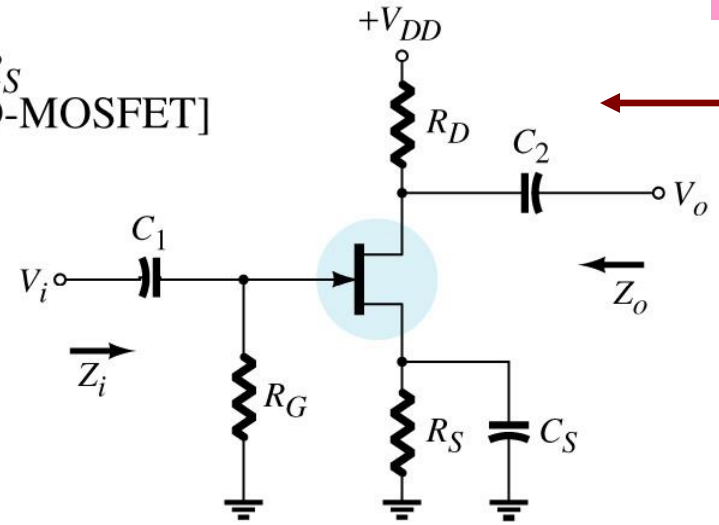
and

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\text{and } V_{DS} = V_{DD} - I_{DS} R_D$$

Where, $V_p = V_{GS\text{-}off}$ & I_{DSS} is Short ckt. I_{DS}

Self-bias
bypassed R_S
[JFET or D-MOSFET]



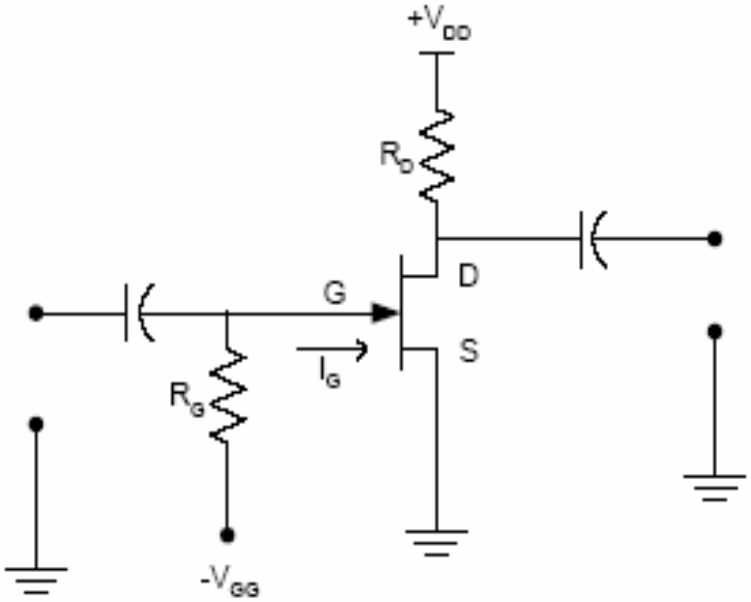
For Self Bias Circuit

$$V_{GS} + I_{DS} R_S = 0$$

$$\therefore I_{DS} = -\frac{V_{GS}}{R_S}$$

JFET Biasing Circuits Count…

Gate Bias: or Fixed Bias Ckt.



Since $I_G = 0$,

$$V_{GS} = V_{GG}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

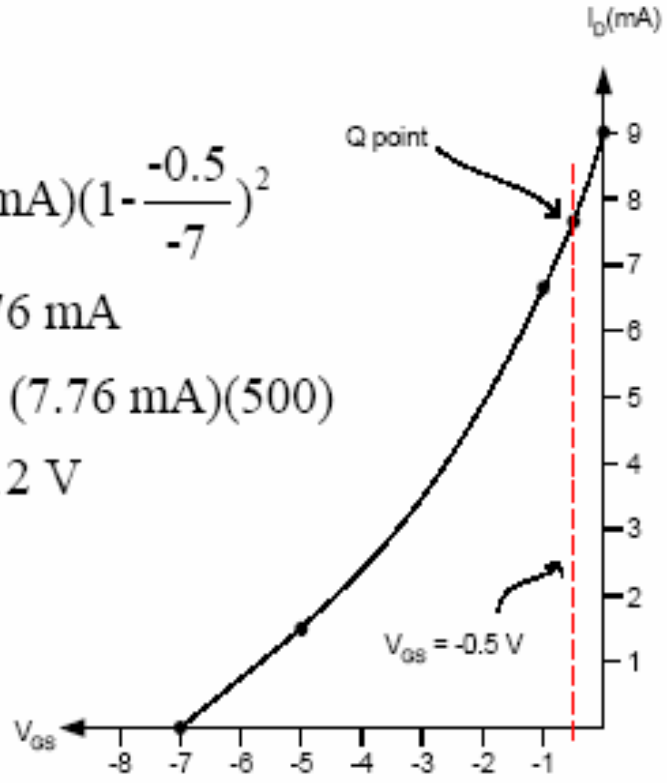
- Example: Determine the Q-point values for the gate biasing circuit if $V_{GG} = -0.5$ V, $V_{GS(off)} = -7$ V, $I_{DSS} = 9$ mA, $V_{DD} = 5$ V and $R_D = 500\Omega$.

$$I_D = (9\text{mA})\left(1 - \frac{-0.5}{-7}\right)^2$$

$$= 7.76 \text{ mA}$$

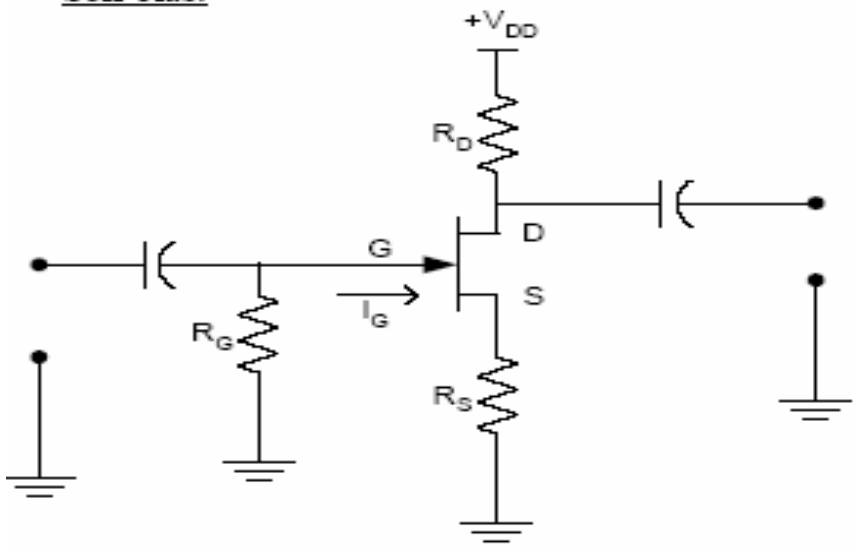
$$V_{DS} = 5 - (7.76 \text{ mA})(500)$$

$$= 1.12 \text{ V}$$



JFET Self (or Source) Bias Circuit

Self bias:



Since $I_G = 0$, $V_G = 0$

$V_S = I_D R_S$

$V_{GS} = -I_D R_S$

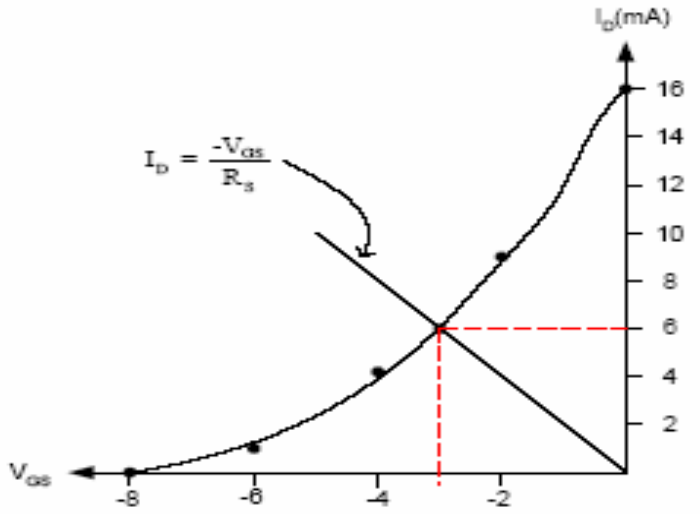
$I_D = \dfrac{-V_{GS}}{R_S}$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$$\text{and } I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\therefore I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = -\frac{V_{GS}}{R_S}$$

- Example: Determine the Q-point values for the self biasing circuit if $V_{GS(off)} = -8$ V , $I_{DSS} = 16$ mA , $V_{DD} = 10$ V , $R_D = 500\ \Omega$, $R_G = 1$ MΩ and $R_S = 500\ \Omega$.



$I_D = 6$ mA

$V_{DS} = 10 - (6\text{mA})(500+500)$

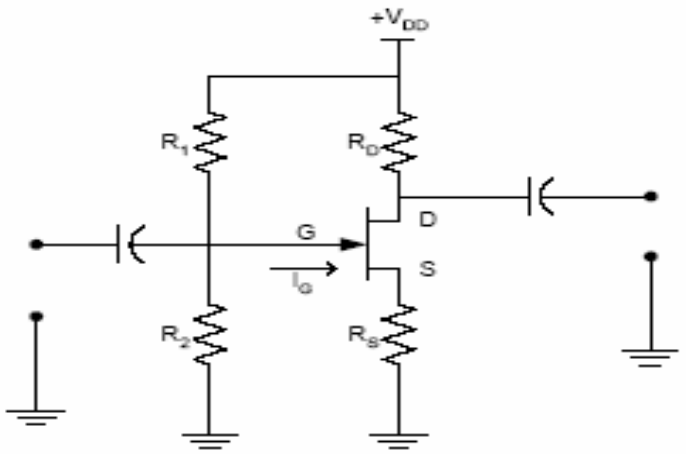
$= 4$ V

$$I_{DSS}\left[1 - 2\frac{V_{GS}}{V_P} + \left(\frac{V_{GS}}{V_P}\right)^2\right] + \frac{V_{GS}}{R_S} = 0$$

This quadratic equation can be solved for V_{GS} & I_{DS}

The Potential (Voltage) Divider Bias

Voltage-divider bias:



Since $I_G = 0$,

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$

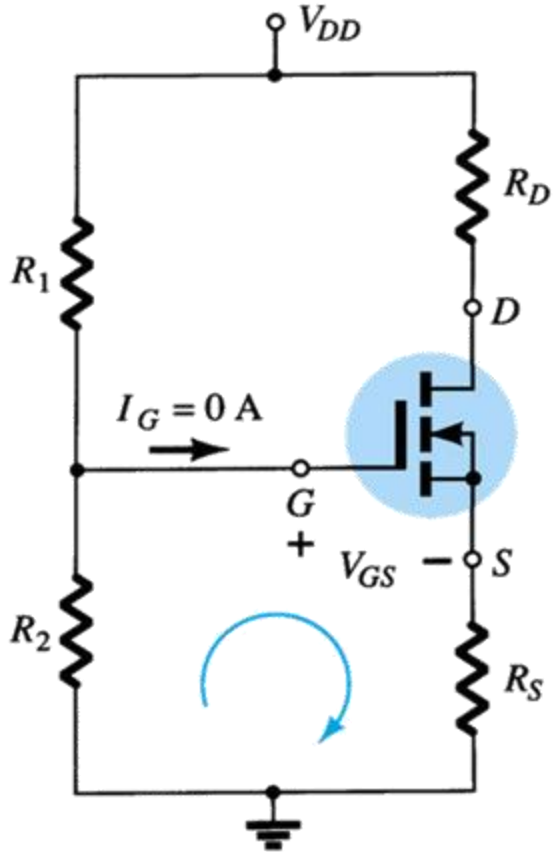
The method used to plot the dc bias line for the voltage-divider bias is as follows:

1. Plot the transconductance curve for the specific JFET.
2. Calculate V_G.
3. Plot V_G on the positive x-axis.
4. Solve for I_D using
$$I_D = \frac{V_G}{R_S}$$
5. Plot I_D found in (4) on the y-axis.
6. Extend the line to intersect the transconductance curve to obtain the Q-point values.

$$\therefore I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 - \frac{V_G - V_{GS}}{R_S} = 0$$

Solving this quadratic equation gives V_{GS} *and* I_{DS}

Voltage-Divider Biasing



Again plot the line and the transfer curve to find the Q-point.
Using the following equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Input loop : $V_{GS} = V_G - I_D R_S$

Output loop : $V_{DS} = V_{DD} - I_D (R_S + R_D)$