DDCO Assignment

Week 1

Basic Gates, Universal Gates, XOR, XNOR Gates and Full Adder

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1. AND Gate

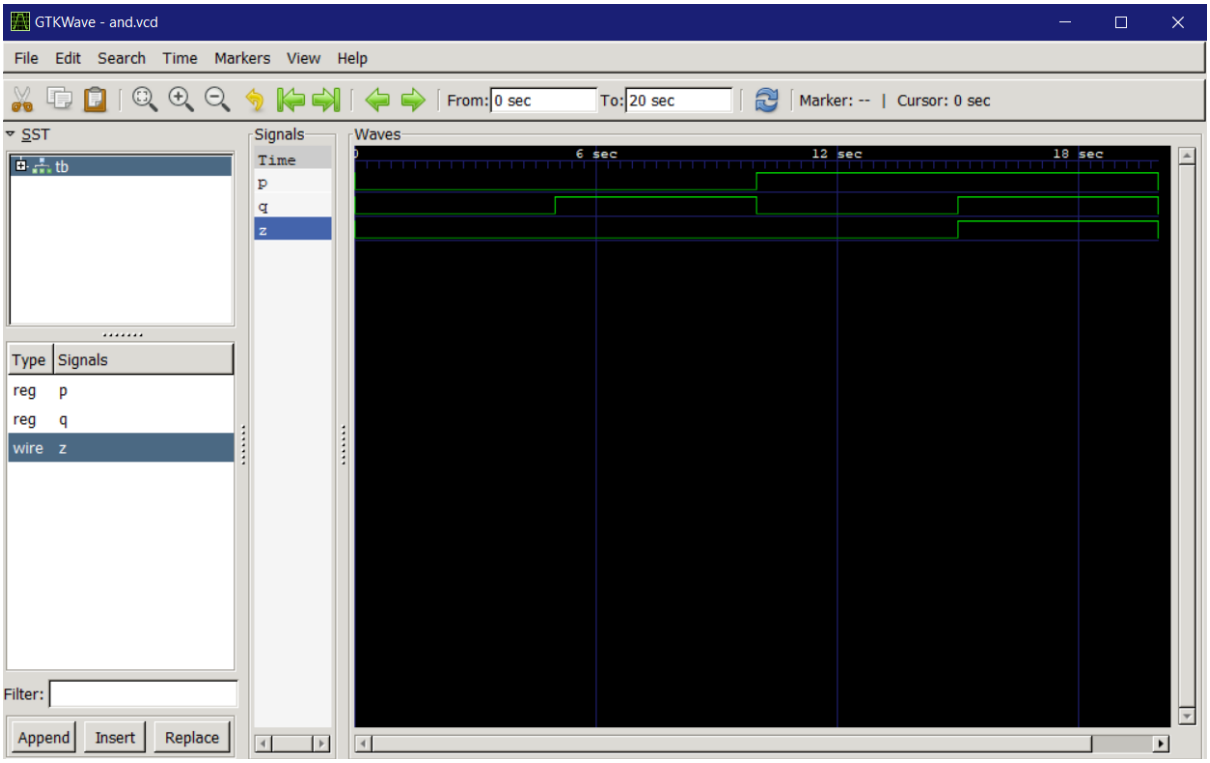
```
module and1(input wire A,B, output wire Y);
assign Y = A & B;
endmodule
```

Testbench file –

```
module tb;
reg p,q;
wire z;

//instantiation
and1 a1(.A(p),.B(q),.Y(z));
initial begin
$dumpfile("and.vcd");
$dumpvars(0,tb);
end

initial begin
$monitor(p,q,z);
p=1'b0;
q=1'b0;
#5
p=1'b0;
q=1'b1;
#5
p=1'b1;
q=1'b0;
#5
p=1'b1;
q=1'b1;
#5
p=1'b0;
q=1'b0;
end
endmodule
```

Output –

```
C:\PES1UG20CS331\iverilog\bin>iverilog -o and gates1.v TB_Gates.v

C:\PES1UG20CS331\iverilog\bin>vvp and
VCD info: dumpfile and.vcd opened for output.
000
010
100
111
000

C:\PES1UG20CS331\iverilog\bin>gtkwave and.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[20] end time.
WM Destroy
```



2. OR Gate

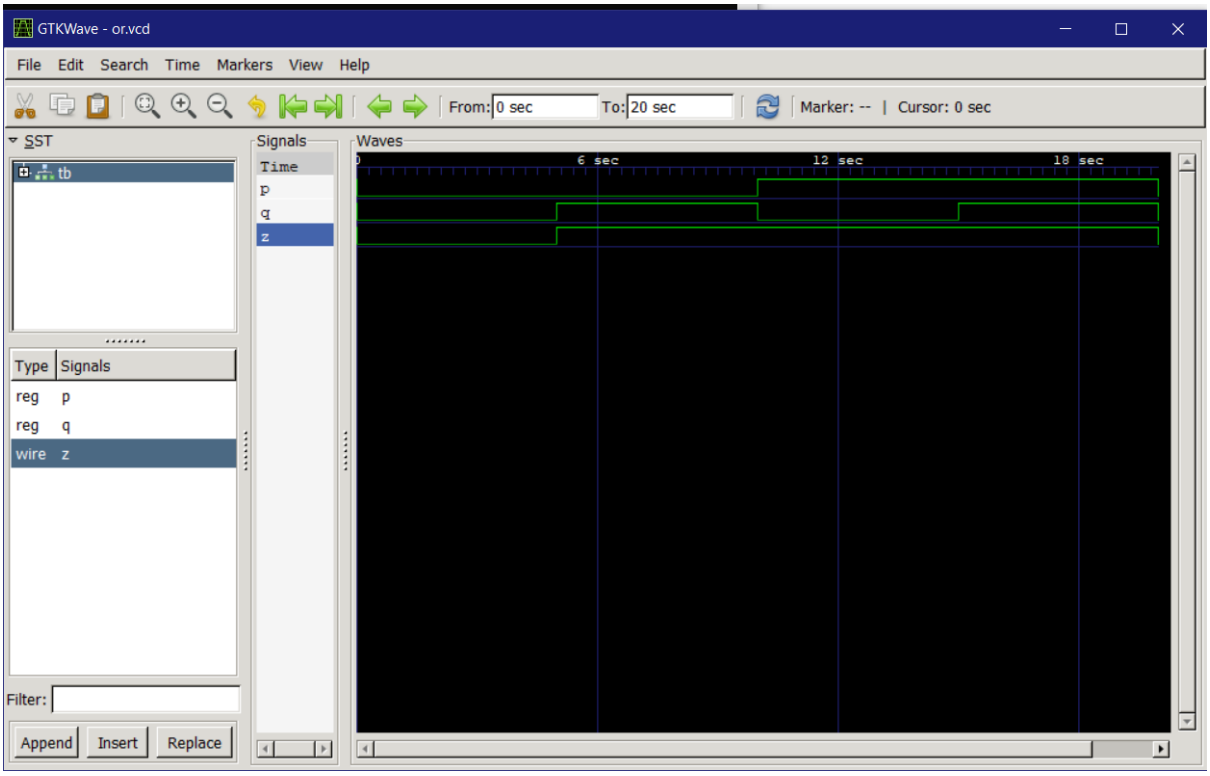
```
module or1(input wire A,B, output wire Y);
assign Y = A | B;
endmodule
```

Testbench file –

```
module tb;
reg p,q;
wire z;

//instantiation
or1 a1(.A(p),.B(q),.Y(z));
initial begin
$dumpfile("or.vcd");
$dumpvars(0,tb);
end

initial begin
$monitor(p,q,z);
p=1'b0;
q=1'b0;
#5
p=1'b0;
q=1'b1;
#5
p=1'b1;
q=1'b0;
#5
p=1'b1;
q=1'b1;
#5
p=1'b0;
q=1'b0;
end
endmodule
```

Output –

```
C:\PES1UG20CS331\iverilog\bin>iverilog -o or gates1.v TB_Gates.v

C:\PES1UG20CS331\iverilog\bin>vvp or
VCD info: dumpfile or.vcd opened for output.
000
011
101
111
000
```


GTKWave - or.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 20 sec
Marker: -- | Cursor: 0 sec
SST
tb
Type Signals
reg p
reg q
wire z
Filter:
Append Insert Replace
Signals
Time
p
q
z
Waves
6 sec
12 sec
18 sec

3. NOT Gate

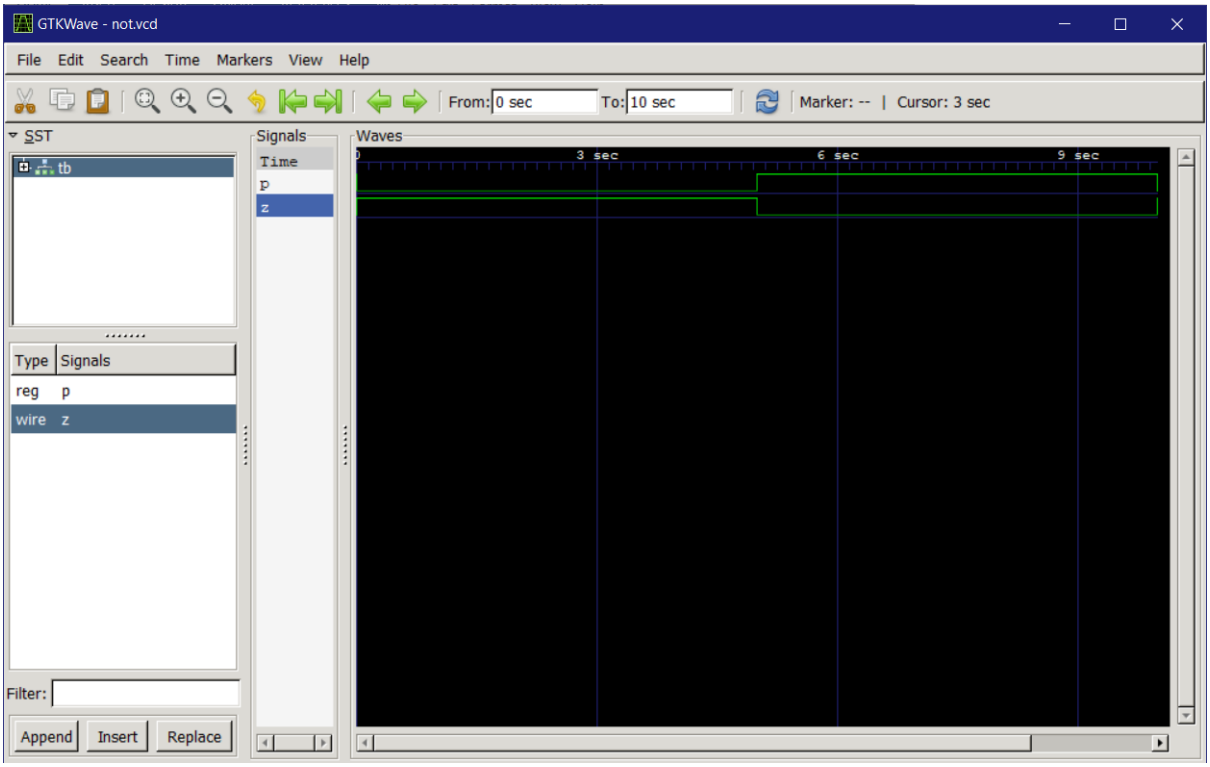
```
module not1(input wire A, output wire Y);
assign Y=~A;
endmodule
```

Testbench file –

```
module tb;
reg p;
wire z;

//instantiation
not1 a1(.A(p),.Y(z));
initial begin
$dumpfile("not.vcd");
$dumpvars(0,tb);
end

initial begin
$monitor(p,z);
p=1'b0;
#5
p=1'b1;
#5
p=1'b0;
end
endmodule
```

Output –

```
C:\PES1UG20CS331\iverilog\bin>iverilog -o not gates1.v TB_Gates.v

C:\PES1UG20CS331\iverilog\bin>vvp not
VCD info: dumpfile not.vcd opened for output.
01
10
01
```


GTKWave - not.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 10 sec
Marker: -- | Cursor: 3 sec
SST
tb
Type Signals
reg p
wire z
Filter:
Append Insert Replace
Signals
Time
p
z
Waves
3 sec
6 sec
9 sec

4. NOR Gate

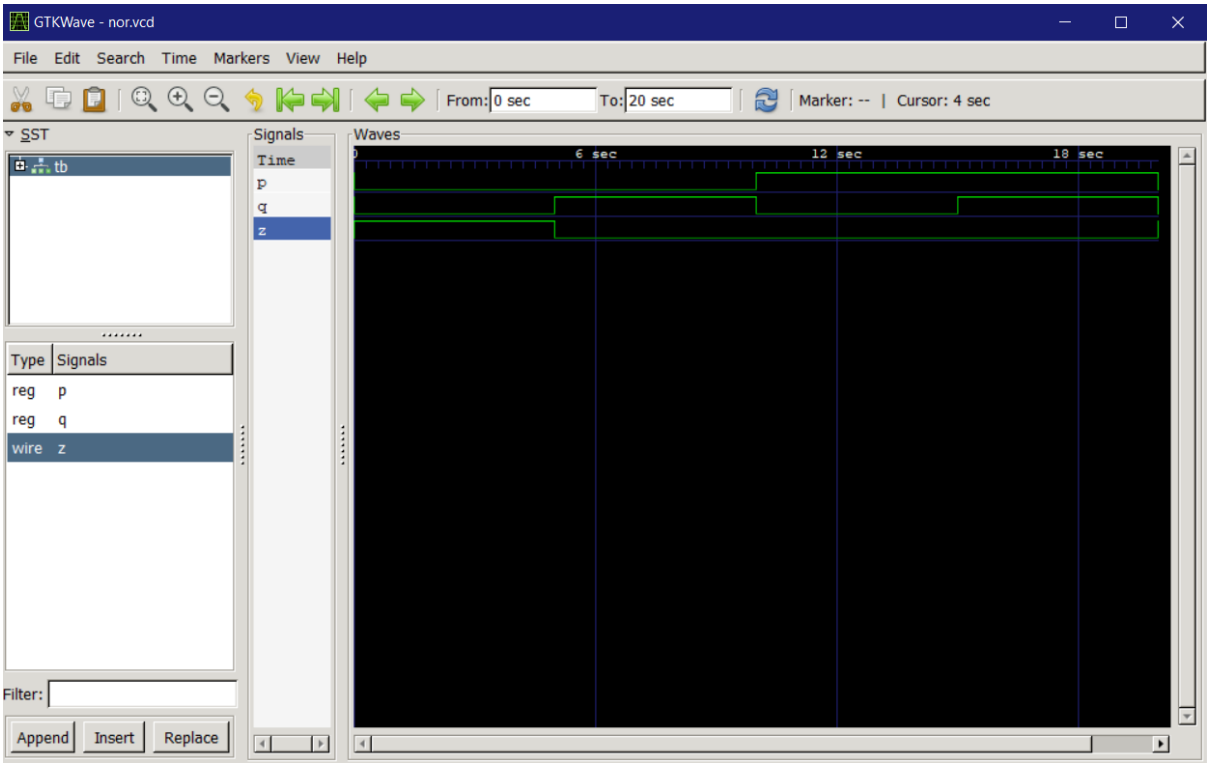
```
module nor1(input wire A,B, output wire Y);
wire x;
or1 a1(A,B,x);
not1 a2(x,Y);
endmodule
```

Testbench file –

```
module tb;
reg p,q;
wire z;

//instantiation
nor1 a1(.A(p),.B(q),.Y(z));
initial begin
$dumpfile("nor.vcd");
$dumpvars(0,tb);
end

initial begin
$monitor(p,q,z);
p=1'b0;
q=1'b0;
#5
p=1'b0;
q=1'b1;
#5
p=1'b1;
q=1'b0;
#5
p=1'b1;
q=1'b1;
#5
p=1'b0;
q=1'b0;
end
endmodule
```

Output –

```
C:\PES1UG20CS331\iverilog\bin>iverilog -o nor gates1.v TB_Gates.v

C:\PES1UG20CS331\iverilog\bin>vvp nor
VCD info: dumpfile nor.vcd opened for output.
001
010
100
110
001
```


GTKWave - nor.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 20 sec
Marker: --
Cursor: 4 sec
SST
tb
Type Signals
reg p
reg q
wire z
Filter:
Append Insert Replace
Signals
Time
p
q
z
Waves
6 sec
12 sec
18 sec

5. NAND Gate

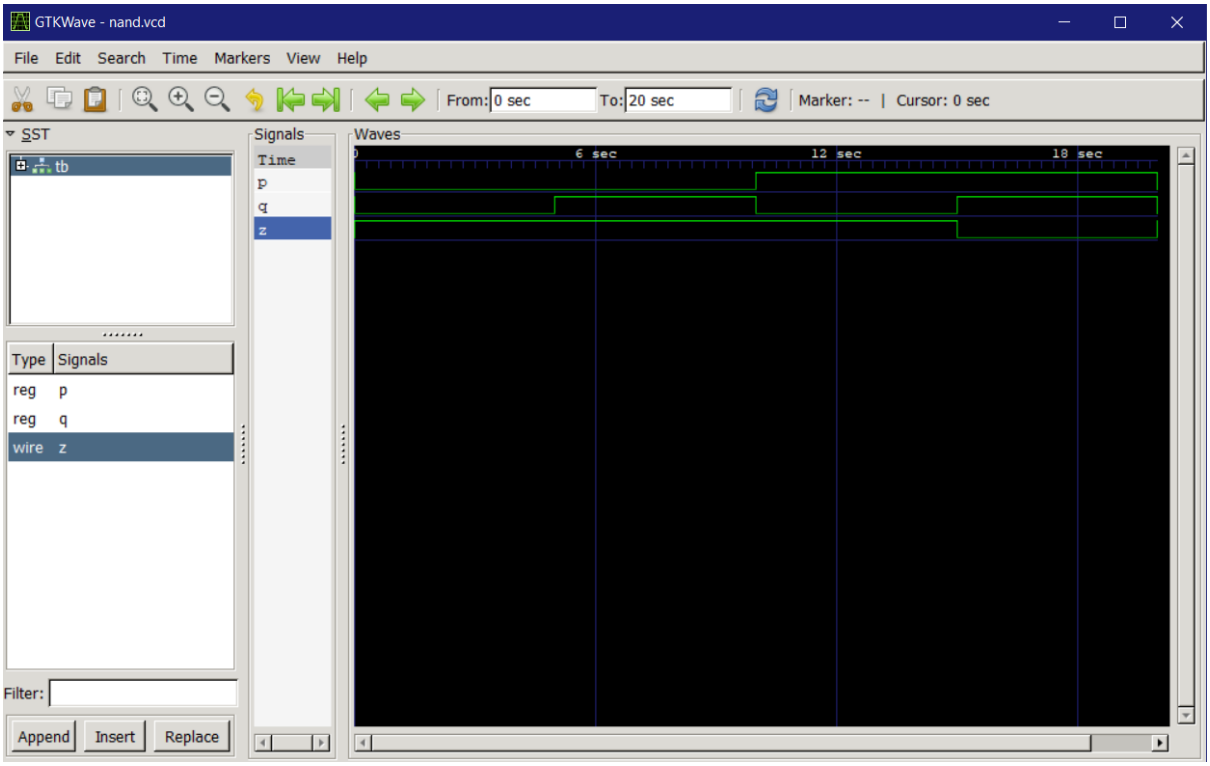
```
module nand1(input wire A,B, output wire Y);
wire x;
and1 a1(A,B,x);
not1 a2(x,Y);
endmodule
```

Testbench file –

```
module tb;
reg p,q;
wire z;

//instantiation
nand1 a1(.A(p),.B(q),.Y(z));
initial begin
$dumpfile("nand.vcd");
$dumpvars(0,tb);
end

initial begin
$monitor(p,q,z);
p=1'b0;
q=1'b0;
#5
p=1'b0;
q=1'b1;
#5
p=1'b1;
q=1'b0;
#5
p=1'b1;
q=1'b1;
#5
p=1'b0;
q=1'b0;
end
endmodule
```

Output –

```
C:\PES1UG20CS331\iverilog\bin>iverilog -o nand gates1.v TB_Gates.v

C:\PES1UG20CS331\iverilog\bin>vvp nand
VCD info: dumpfile nand.vcd opened for output.
001
011
101
110
001
```


GTKWave - nand.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 20 sec
Marker: -- | Cursor: 0 sec
SST
tb
Type Signals
reg p
reg q
wire z
Filter:
Append Insert Replace
Signals
Time
p
q
z
Waves
6 sec
12 sec
18 sec

6. XOR Gate

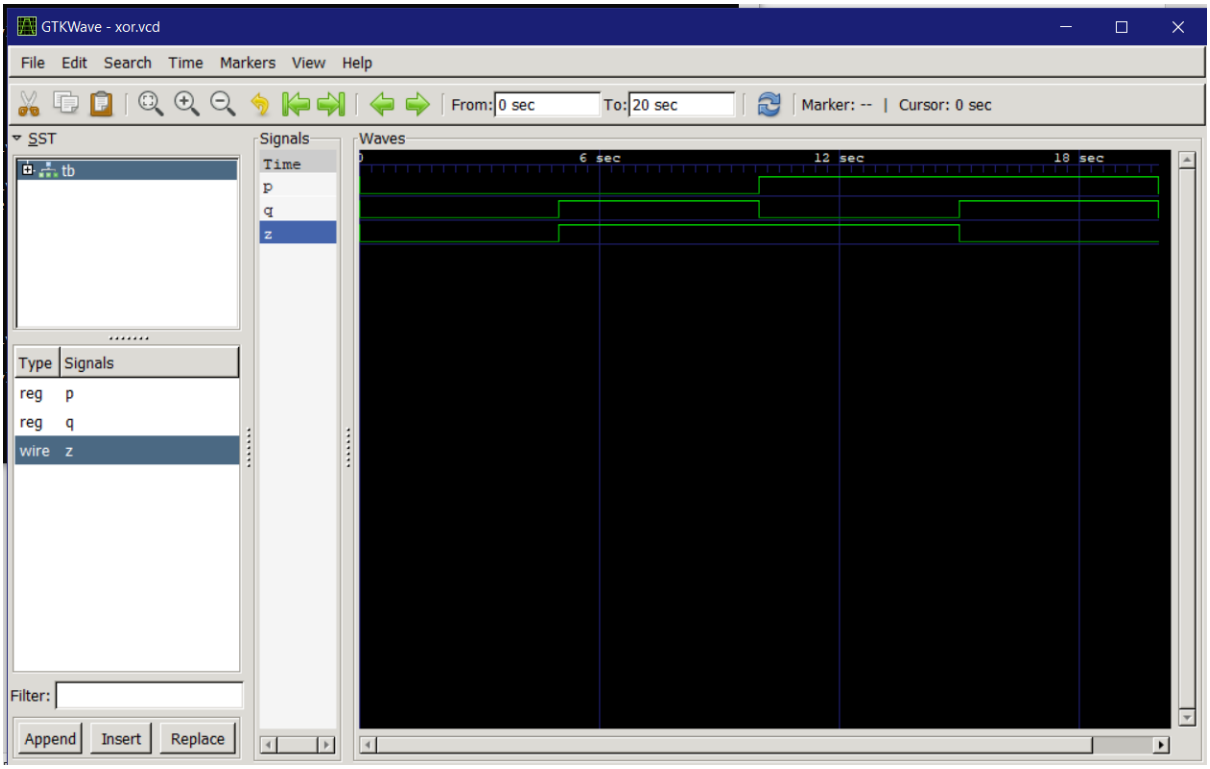
```
module xor1(input wire A,B, output wire C);
wire x,y,p,q;
not1 n1(A,x);
not1 n2(B,y);
and1 a1(B,x,p);
and1 a2(A,y,q);
or1 o1(p,q,C);
endmodule
```

Testbench file –

```
module tb;
reg p,q;
wire z;

//instantiation
xor1 a1(.A(p),.B(q),.C(z));
initial begin
$dumpfile("xor.vcd");
$dumpvars(0,tb);
end

initial begin
$monitor(p,q,z);
p=1'b0;
q=1'b0;
#5
p=1'b0;
q=1'b1;
#5
p=1'b1;
q=1'b0;
#5
p=1'b1;
q=1'b1;
#5
p=1'b0;
q=1'b0;
end
endmodule
```

Output –

```
C:\PES1UG20CS331\iverilog\bin>iverilog -o xor gates1.v TB_Gates.v

C:\PES1UG20CS331\iverilog\bin>vvp xor
VCD info: dumpfile xor.vcd opened for output.
000
011
101
110
000

C:\PES1UG20CS331\iverilog\bin>gtkwave xor.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[20] end time.
WM Destroy
```



7. XNOR Gate

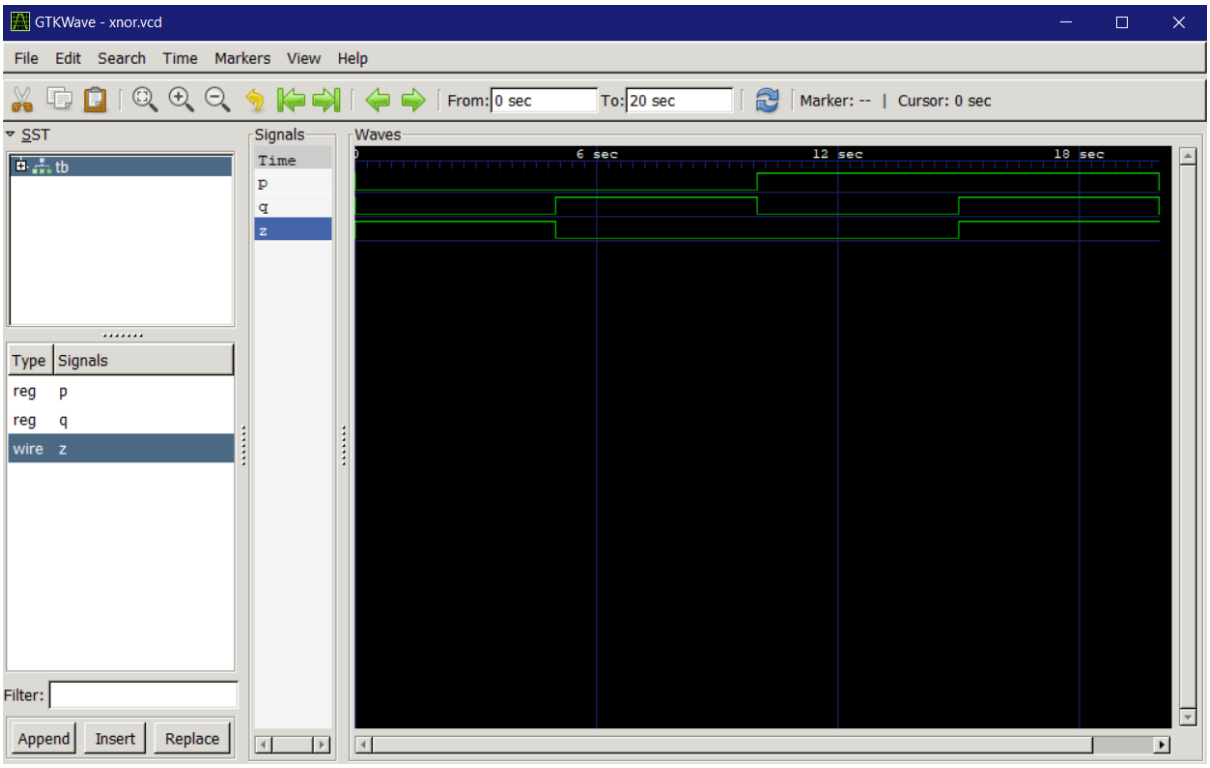
```
module xnor1(input wire A,B, output wire C);
wire x,y,p,q;
not1 n1(A,x);
not1 n2(B,y);
and1 a1(y,x,p);
and1 a2(A,B,q);
or1 o1(p,q,C);
endmodule
```

Testbench file –

```
module tb;
reg p,q;
wire z;

//instantiation
xnor1 a1(.A(p),.B(q),.C(z));
initial begin
$dumpfile("xnor.vcd");
$dumpvars(0,tb);
end

initial begin
$monitor(p,q,z);
p=1'b0;
q=1'b0;
#5
p=1'b0;
q=1'b1;
#5
p=1'b1;
q=1'b0;
#5
p=1'b1;
q=1'b1;
#5
p=1'b0;
q=1'b0;
end
endmodule
```

Output –

```
C:\PES1UG20CS331\iverilog\bin>iverilog -o xnor gates1.v TB_Gates.v

C:\PES1UG20CS331\iverilog\bin>vvp xnor
VCD info: dumpfile xnor.vcd opened for output.
001
010
100
111
001
```



8. Full Adder

```
module fulladd(input wire a, b, cin, output wire sum, cout);
wire [4:0] t;
    xor1 x0(a, b, t[0]);
    xor1 x1(t[0], cin, sum);

    and1 a0(a, b, t[1]);
    and1 a1(a, cin, t[2]);
    and1 a2(b, cin, t[3]);

    or1 o0(t[1], t[2], t[4]);
    or1 o1(t[3], t[4], cout);
endmodule
```

Testbench file –

```
module TB;
reg aa,bb,cc;
wire ss,cy;
fulladd add1(.a(aa), .b(bb), .cin(cc), .sum(ss), .cout(cy));
initial
begin
$dumpfile("dump.vcd");
$dumpvars(0, TB);
end

initial begin $monitor(aa,bb,cc,ss,cy);
aa = 1'b0;
bb = 1'b0;
cc=1'b0;
#5
aa = 1'b0;
bb = 1'b1;
cc=1'b1;
#5
aa = 1'b1;
bb = 1'b0;
cc=1'b0;
#5
aa = 1'b1;
bb = 1'b1;
cc=1'b0;
#5
aa = 1'b0;
bb = 1'b0;
cc=1'b1;
#5
aa = 1'b0;
bb = 1'b0;
cc=1'b0;
end
endmodule
```

Output –

```
C:\PES1UG20CS331\iverilog\bin>iverilog -o fa gates1.v fulladd.v TB_FA.v

C:\PES1UG20CS331\iverilog\bin>vvp fa
VCD info: dumpfile dump.vcd opened for output.
00000
01101
10010
11001
00110
00000

C:\PES1UG20CS331\iverilog\bin>gtkwave dump.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[25] end time.
WM Destroy
```