R·I·T | KATE GLEASON College of ENGINEERING

Engineering Report

From: Tommy Choephel

Date: Sep 29, 2021

Subject: Project 1 Tech Memo

Abstract

This project consisted of designing seven digital logic gate cells from the schematic level and functional Verilog model to the final layout using Cadence Virtuoso. The cells in particular are: INVX1, INVX2, NAND2X1, NOR2X1, MUX2X1, XOR2X1 and OAI22X1. Symbols were also made that were placed in a test circuit to verify the functionality through simulation waveforms. Then parasitic elements were simulated and relevant device characteristics such as rise and fall times, and delay times were obtained and compared preroute and post-route. Generally, the post-route delay times proved to be slower in most cases, however, fall times at times diminished.

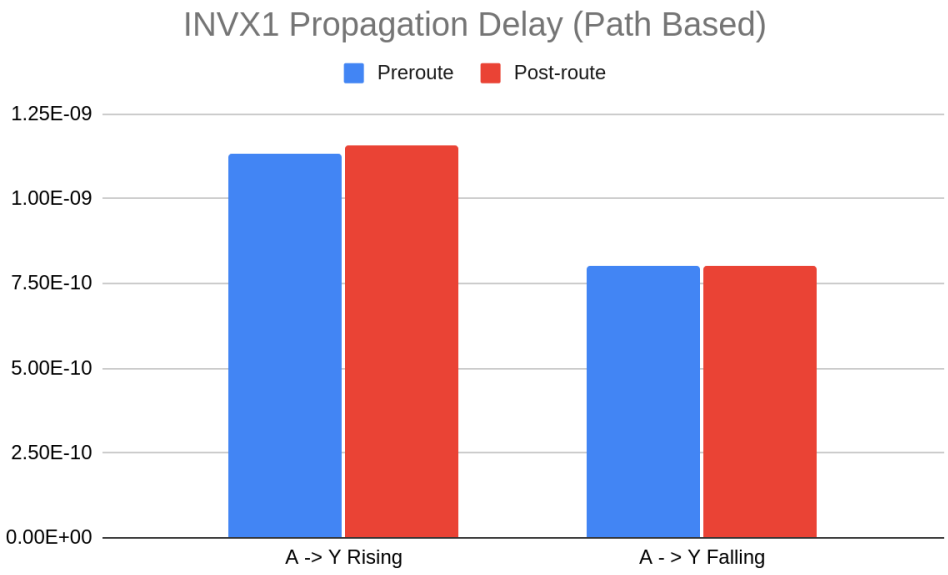
Theory

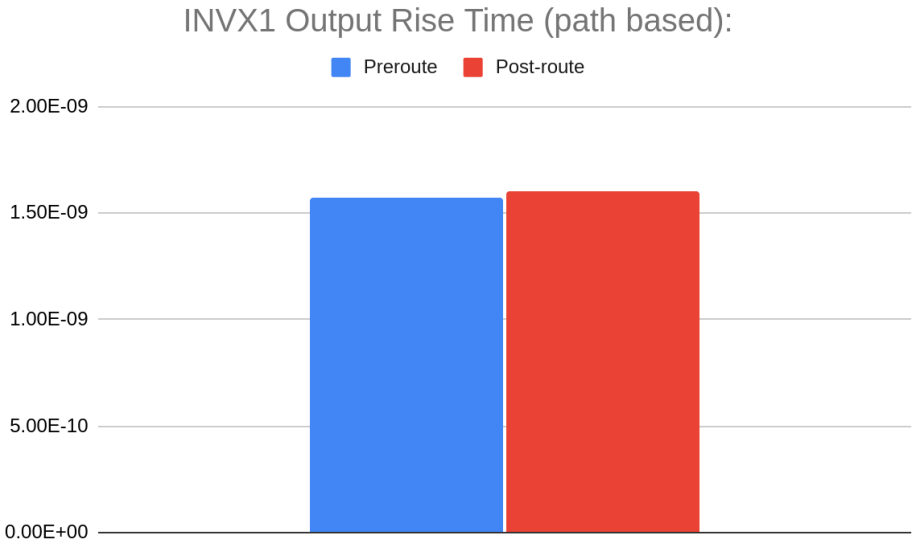
The elementary logic gates such as INVERTER, NAND, NOR, XOR, MUX, and OAI22X1 all can be fundamentally modelled using CMOS logic - that is modelled using NMOS and PMOS transistors in particular arrangements. Each gates have particular behaviors that distinguish their uses, such as an INVERTER when the input requires inversion, a NAND gate when two inputs need to be and(ed) and inverted, etc., all of which can be seen with their respective truth tables in the appendix section. These should be foundational knowledge in the electrical engineering field. Consideration must also be made when two transistors are in series (stacked) to double their width such that their resistance remains congruent to a unit inverter. There are parasitic elements in forms of resistance and capacitance found throughout the implementation of a logic gate that will affect the performance of the devices that must be taken into account, which can be simulated using powerful tools of the trade such as Cadence Virtuoso. Beware that, although this tool is powerful, one must keep one's wits about them while using it, lest one makes mistakes that may demand the user to make frequent overnight stays at the venue of this project experimentation.

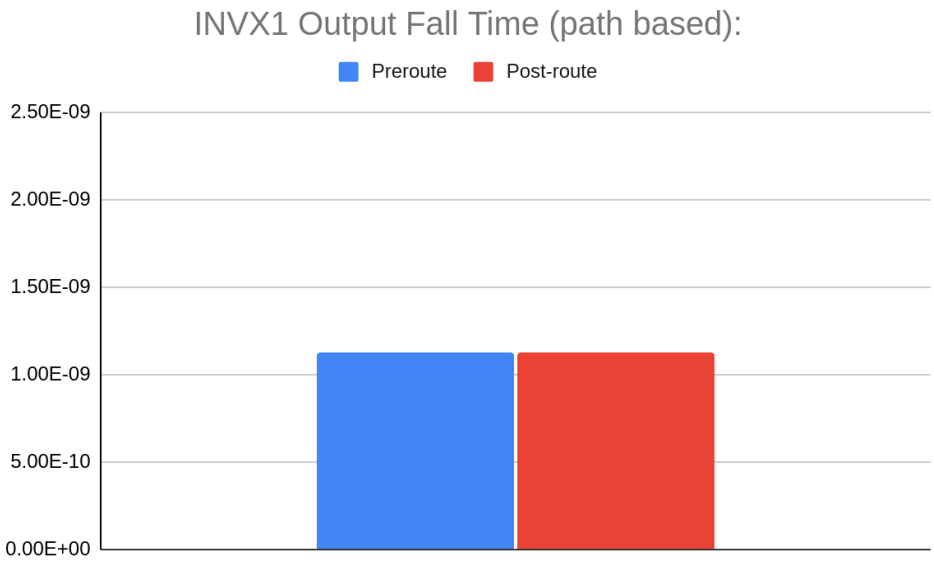
Results and Discussion

INVX1

Propagation Delay (path based):	
Preroute	Post-route
A -> Y Rising: 1.135E-9	A -> Y Rising: 1.158E-9
A -> Y Falling: 802.4E-12	A -> Y Falling: 804.0E-12
Output Rise Time (path based):	
Preroute: 1.575E-9	Post-route: 1.606E-9
Output Fall Time (path based):	
Preroute: 1.125E-9	Post-route: 1.125E-9

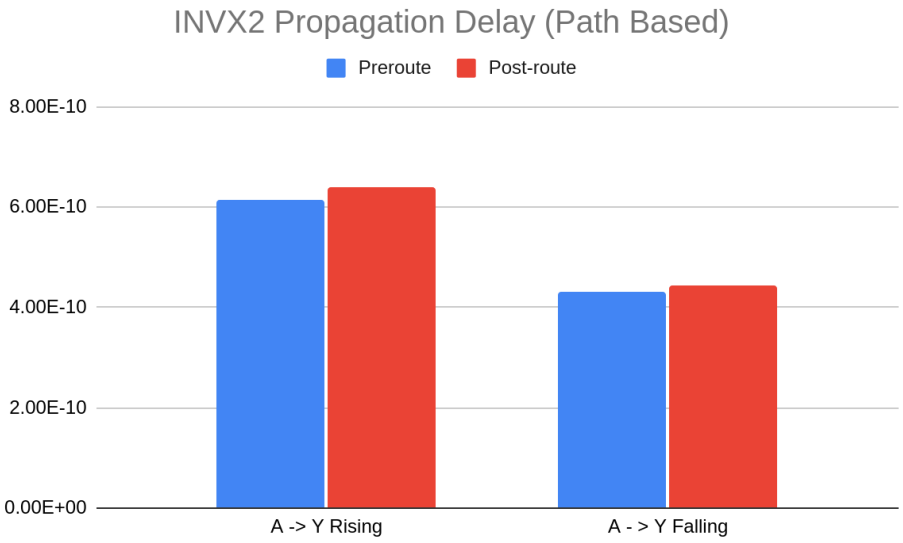


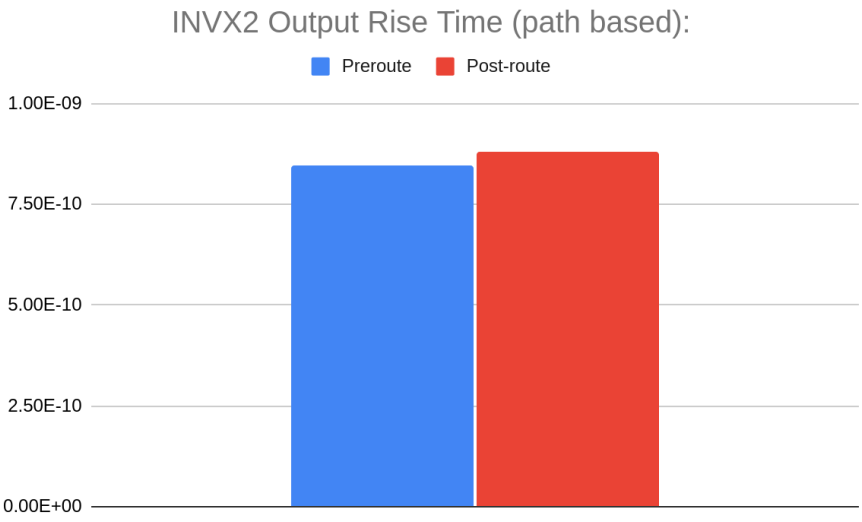


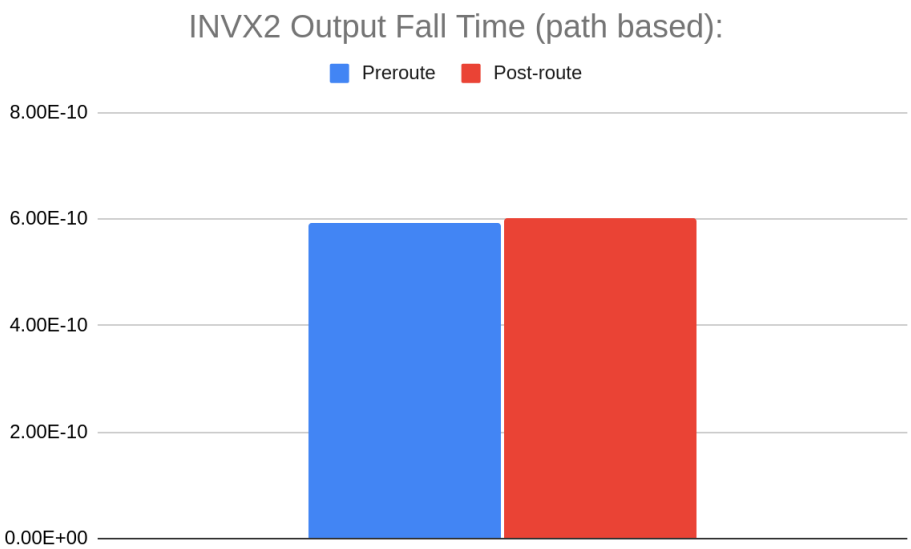


INVX2

Propagation Delay (path based):	
Preroute	Post-route
A -> Y Rising: 614.9E-12	A -> Y Rising: 639.2E-12
A -> Y Falling: 431.6E-12	A -> Y Falling: 443.6E-12
Output Rise Time (path based):	
Preroute: 844.8E-12	Post-route: 879.8E-12
Output Fall Time (path based):	
Preroute: 592.7E-12	Post-route: 602.9E-12


INVX2 Propagation Delay (Path Based)
Preroute
Post-route
8.00E-10
6.00E-10
4.00E-10
2.00E-10
0.00E+00
A -> Y Rising
A - > Y Falling


INVX2 Output Rise Time (path based):
Preroute
Post-route
1.00E-09
7.50E-10
5.00E-10
2.50E-10
0.00E+00

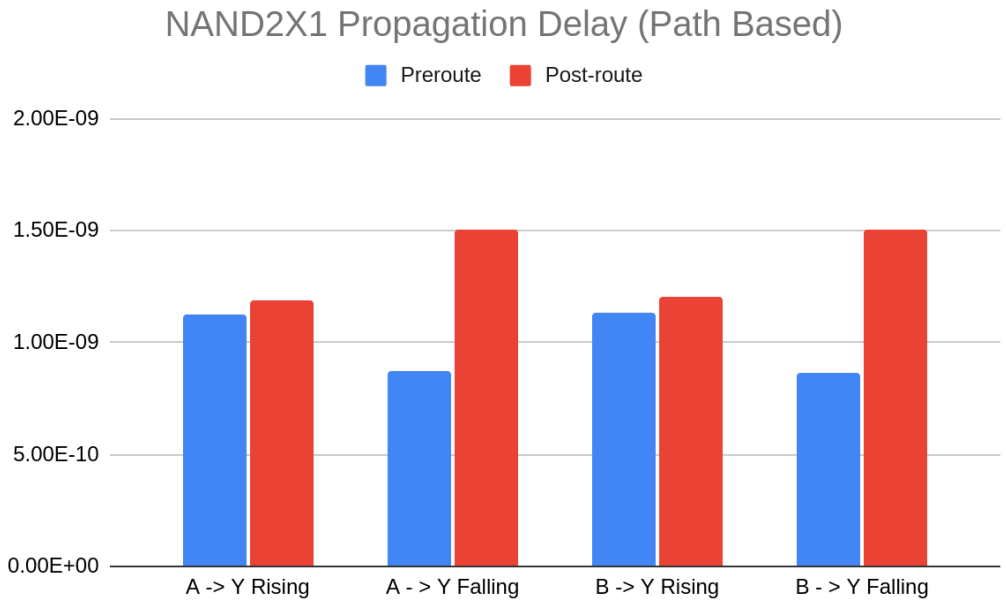

INVX2 Output Fall Time (path based):
Preroute
Post-route
8.00E-10
6.00E-10
4.00E-10
2.00E-10
0.00E+00

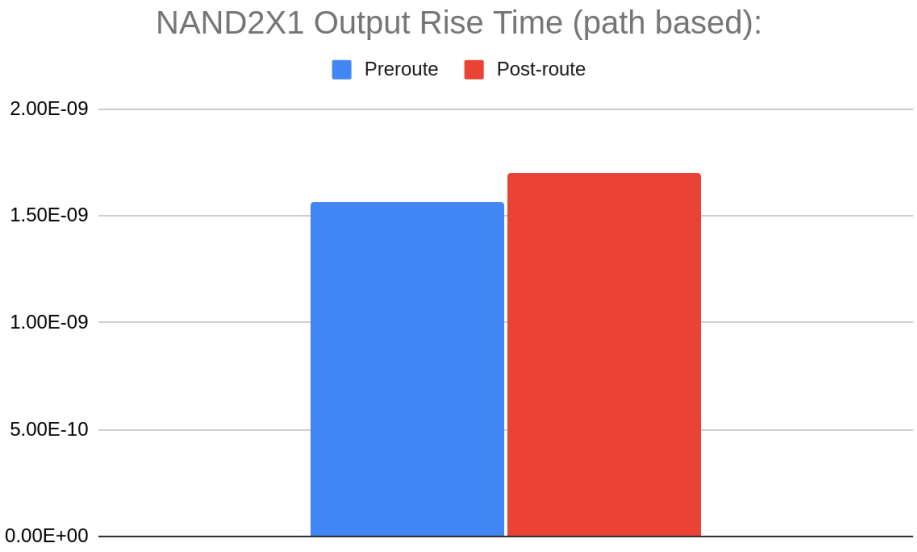
NAND2X1

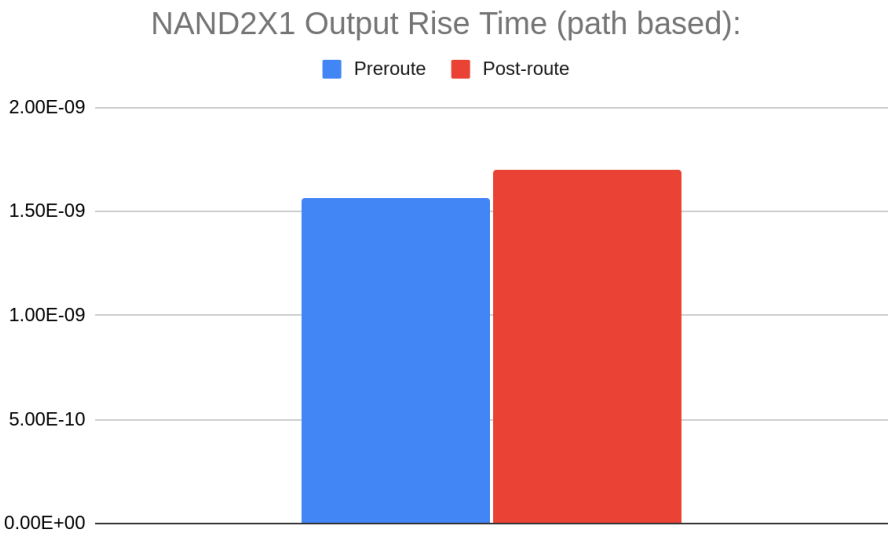
Propagation Delay (path based):

Preroute		Post-route	
A -> Y Rising	1.126E-9	A -> Y Rising	1.186E-9
A -> Y Falling	872.1E-12	A -> Y Falling	1.501E-9
B -> Y Rising	1.130E-9	B -> Y Rising	1.201E-9
B -> Y Falling	862.2E-12	B -> Y Falling	1.501E-9

Output Rise Time (path based):	
Preroute: 1.562E-9	**Post-route: 1.704E-9**
Output Fall Time (path based):	
Preroute: 2.162E-9	**Post-route: 2.029E-9**




NAND2X1 Output Rise Time (path based):
Preroute
Post-route
2.00E-09
1.50E-09
1.00E-09
5.00E-10
0.00E+00


NAND2X1 Output Rise Time (path based):
Preroute
Post-route
2.00E-09
1.50E-09
1.00E-09
5.00E-10
0.00E+00

NOR2X1

Propagation Delay (path based):

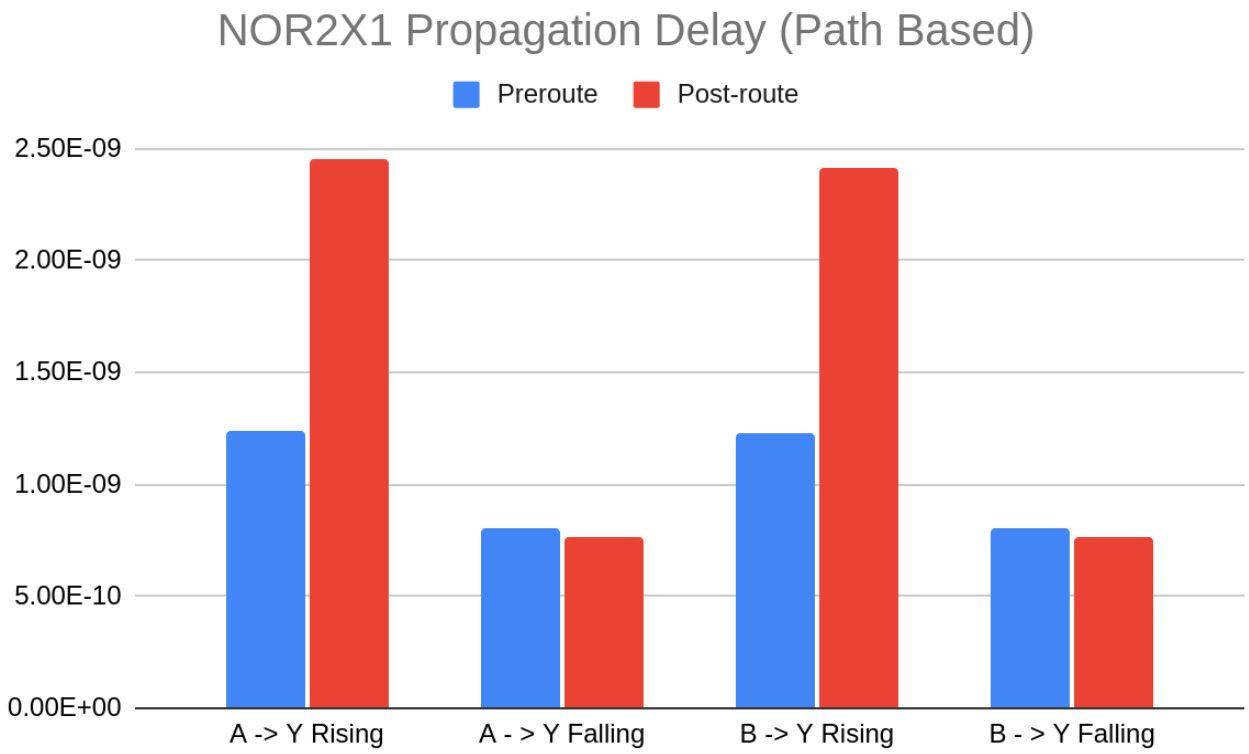
Preroute		Post-route	
A -> Y Rising	1.237E-9	A -> Y Rising	2.455E-9
A -> Y Falling	799.4E-12	A -> Y Falling	762.5E-12
B -> Y Rising	1.232E-9	B -> Y Rising	2.416E-9
B -> Y Falling	799.8E-12	B -> Y Falling	766.0E-12

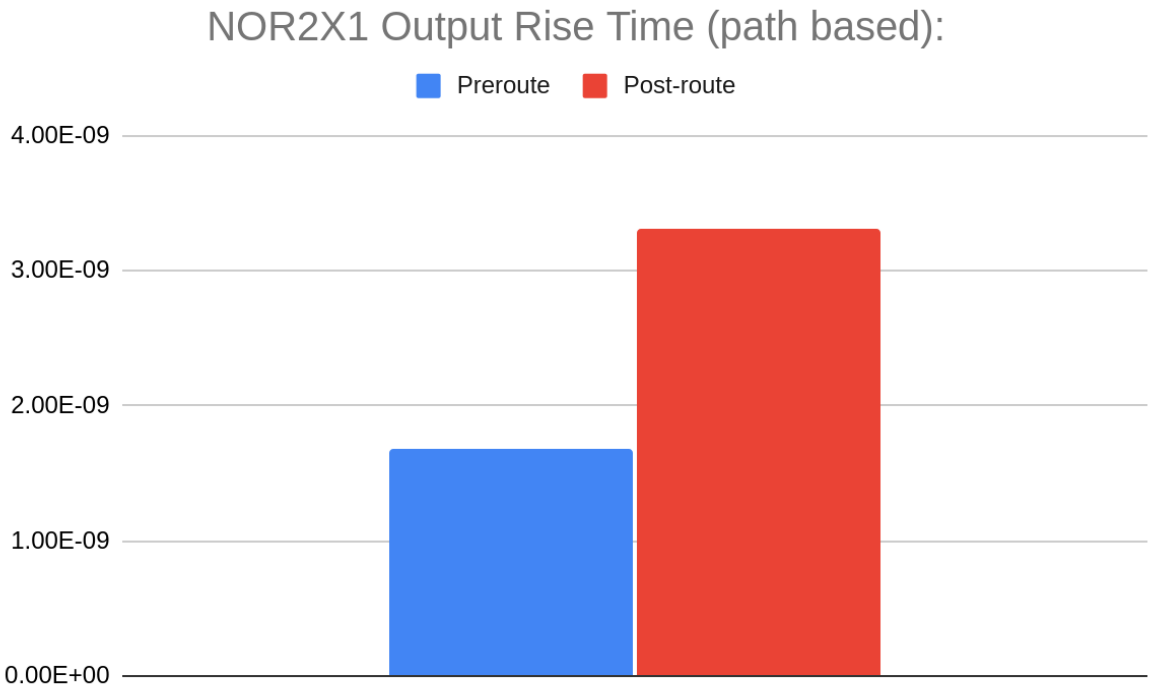
Output Rise Time (path based):

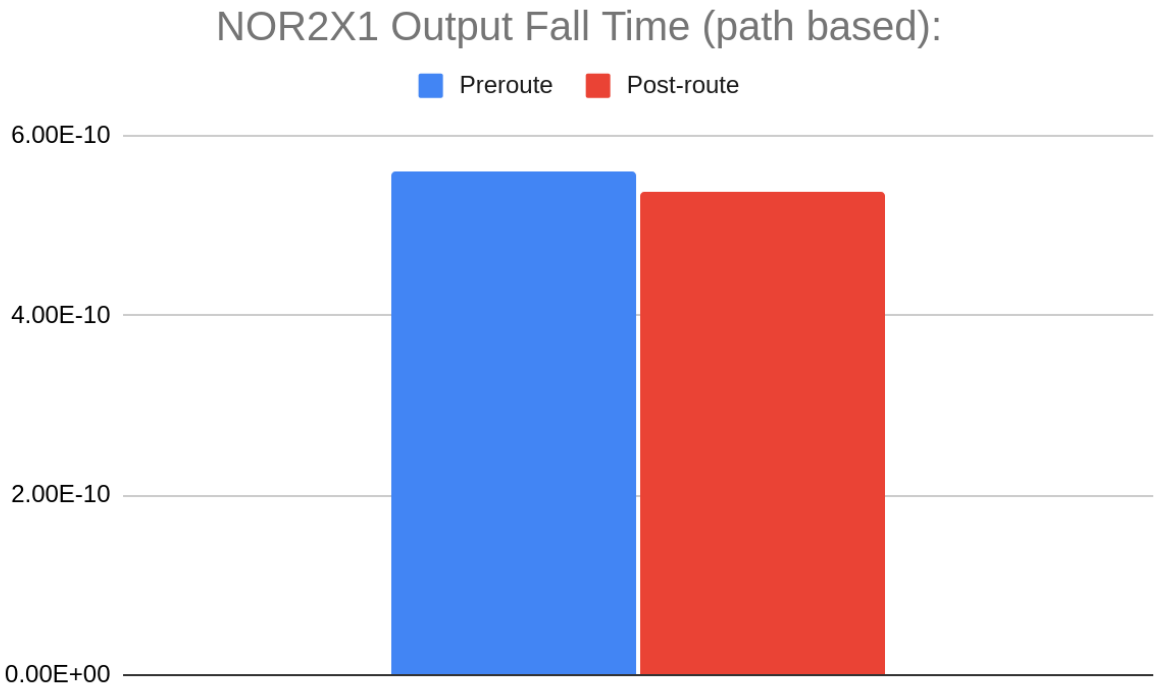
Preroute: 1.676E-9	Post-route: 3.311E-9

Output Fall Time (path based):

Preroute: 558.8E-12	Post-route: 537.3E-12




NOR2X1 Output Rise Time (path based):
Preroute
Post-route
4.00E-09
3.00E-09
2.00E-09
1.00E-09
0.00E+00

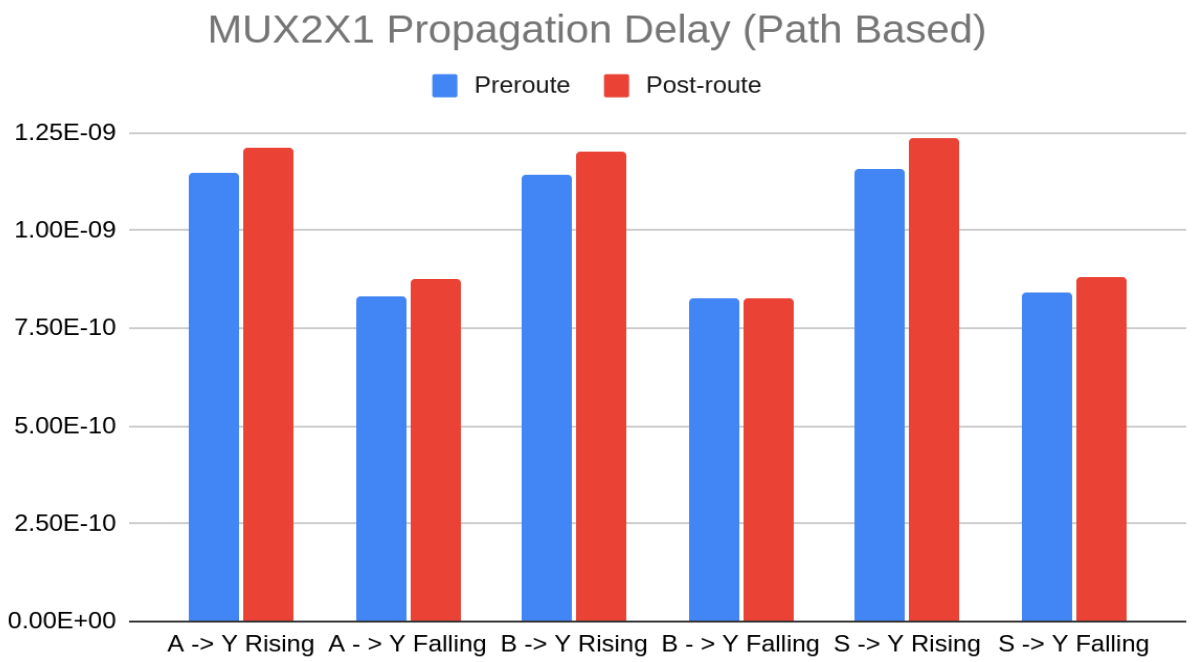

NOR2X1 Output Fall Time (path based):
Preroute
Post-route
6.00E-10
4.00E-10
2.00E-10
0.00E+00

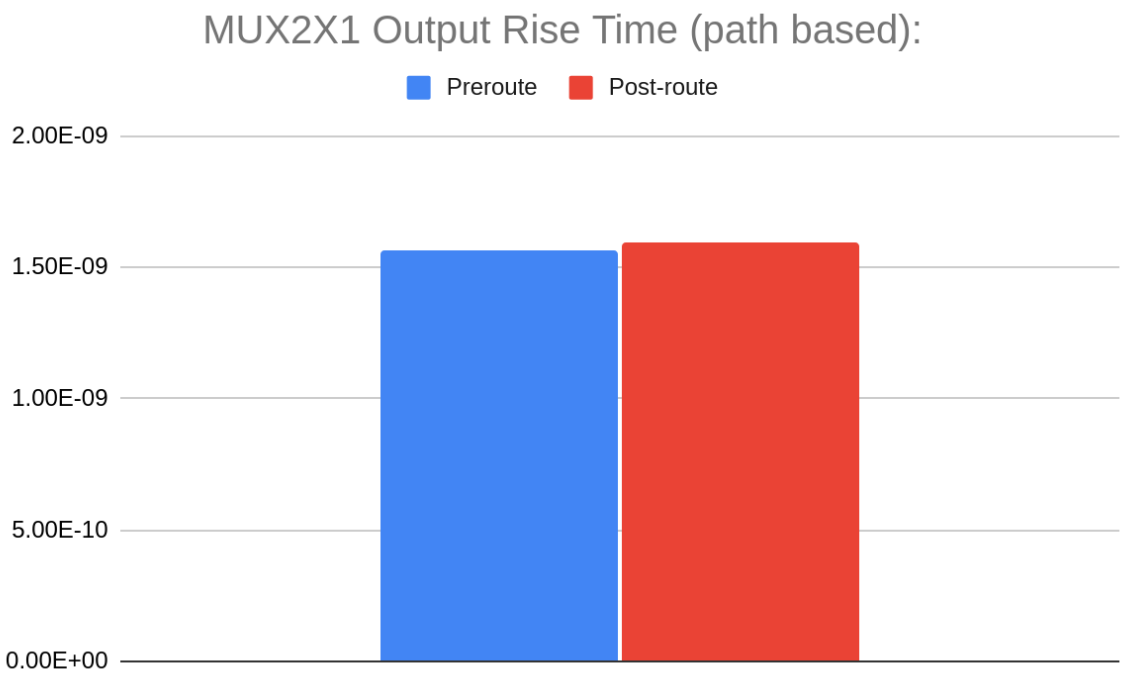
MUX2X1

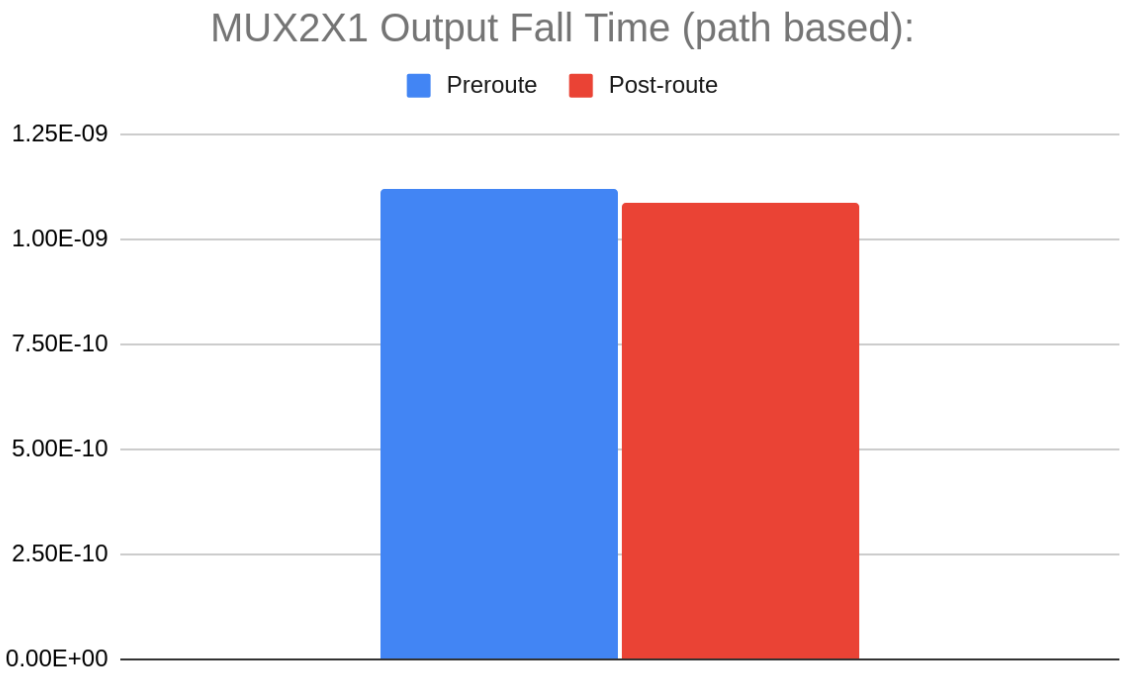
Propagation Delay (path based):

Preroute		Post-route	
A -> Y Rising	1.148E-9	A -> Y Rising	1.211E-9
A -> Y Falling	830.7E-12	A -> Y Falling	877.7E-12
B -> Y Rising	1.143E-9	B -> Y Rising	1.200E-9
B -> Y Falling	827.4E-12	B -> Y Falling	826.1E-12
S -> Y Rising	1.160E-9	S -> Y Rising	1.238E-9
S -> Y Falling	840.0E-12	S -> Y Falling	880.0E-12

Output Rise Time (path based):	
Preroute: 1.567E-9	**Post-route: 1.598E-9**
Output Fall Time (path based):	
Preroute: 1.119E-9	**Post-route: 1.086E-9**




MUX2X1 Output Rise Time (path based):
Preroute
Post-route
2.00E-09
1.50E-09
1.00E-09
5.00E-10
0.00E+00


MUX2X1 Output Fall Time (path based):
Preroute
Post-route
1.25E-09
1.00E-09
7.50E-10
5.00E-10
2.50E-10
0.00E+00

XOR2X1

Propagation Delay (path based):

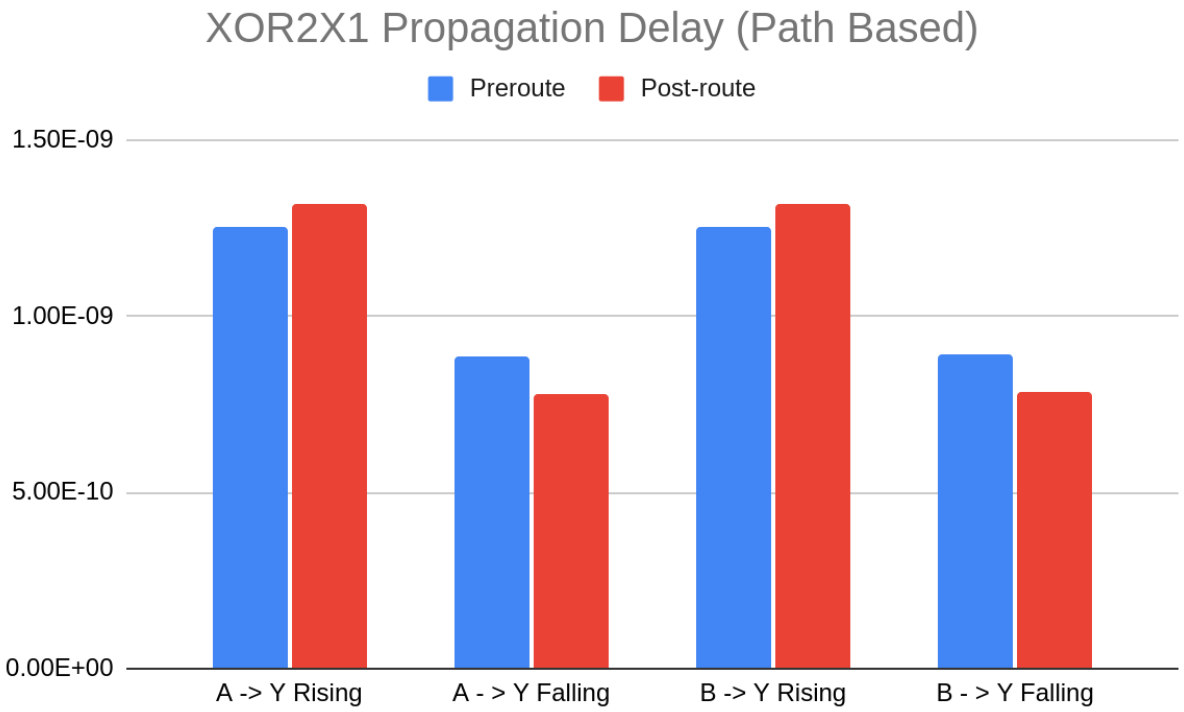
Preroute		Post-route	
A -> Y Rising	1.251E-9	A -> Y Rising	1.319E-9
A -> Y Falling	884.8E-12	A -> Y Falling	780.0E-12
B -> Y Rising	1.255E-9	B -> Y Rising	1.316E-9
B -> Y Falling	890.4E-12	B -> Y Falling	784.6E-12

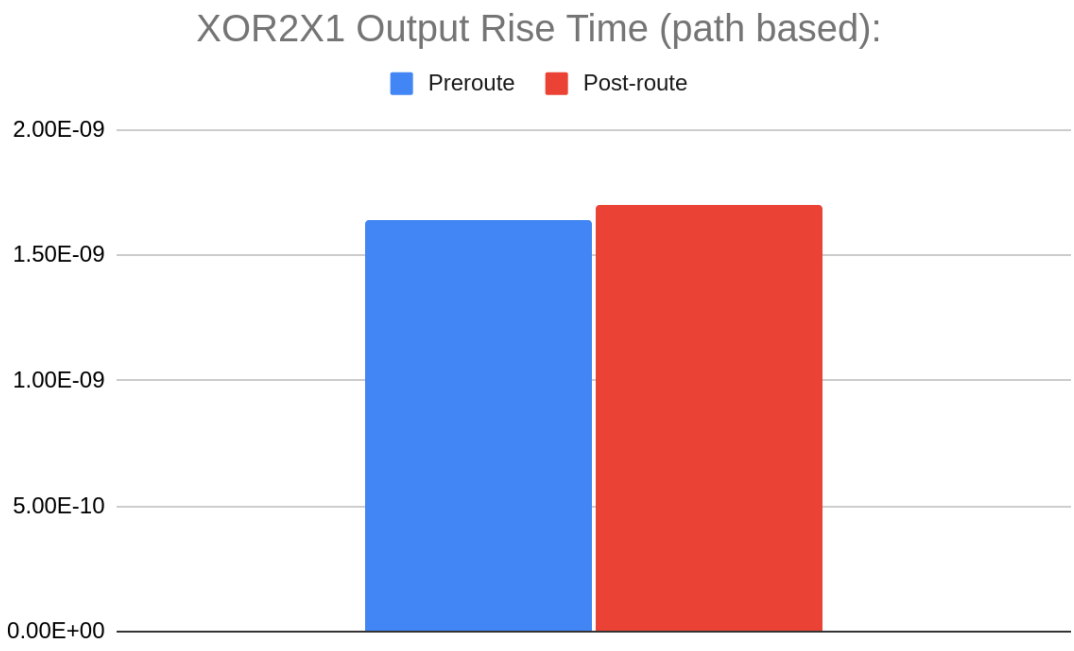
Output Rise Time (path based):

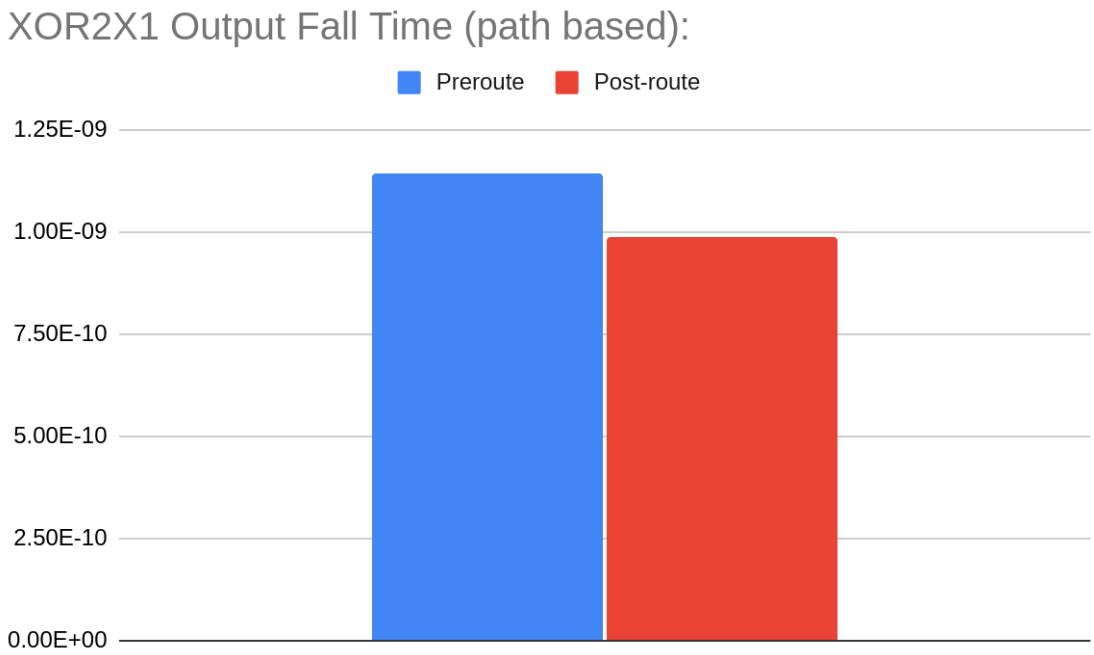
Preroute: 1.642E-9	**Post-route: 1.699E-9**

Output Fall Time (path based):

Preroute: 1.144E-9	**Post-route: 988.1E-12**




XOR2X1 Output Rise Time (path based):
Preroute
Post-route
2.00E-09
1.50E-09
1.00E-09
5.00E-10
0.00E+00


XOR2X1 Output Fall Time (path based):
Preroute
Post-route
1.25E-09
1.00E-09
7.50E-10
5.00E-10
2.50E-10
0.00E+00

OAI22X1

Propagation Delay (path based):

Preroute

A0 -> Y Rising	1.233E-9
A0 -> Y Falling	871.9E-12
A1 -> Y Rising	1.232E-9
A1 -> Y Falling	871.9E-12
B0 -> Y Rising	1.229E-9
B0 -> Y Falling	866.9E-12
B1 -> Y Rising	1.239E-9
B1 -> Y Falling	880.0E-12

Post-route

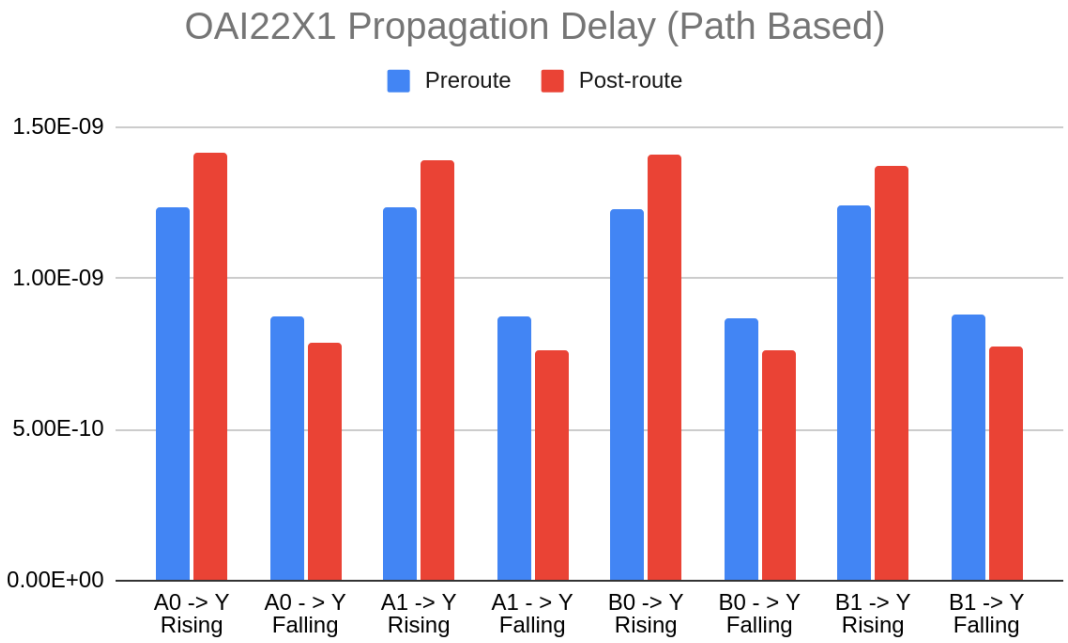
A0 -> Y Rising	1.416E-9
A0 -> Y Falling	784.2E-12
A1 -> Y Rising	1.389E-9
A1 -> Y Falling	763.5E-12
B0 -> Y Rising	1.409E-9
B0 -> Y Falling	759.7E-12
B1 -> Y Rising	1.372E-9
B1 -> Y Falling	773.1E-12

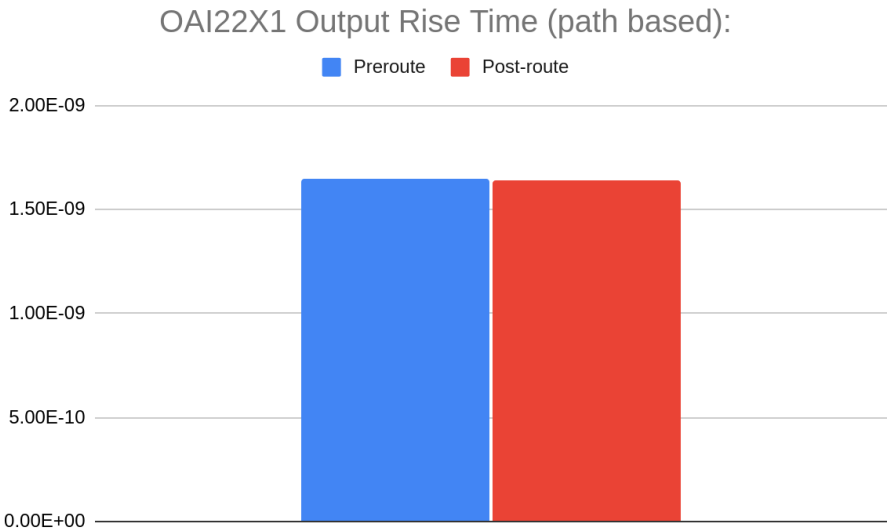
Output Rise Time (path based):

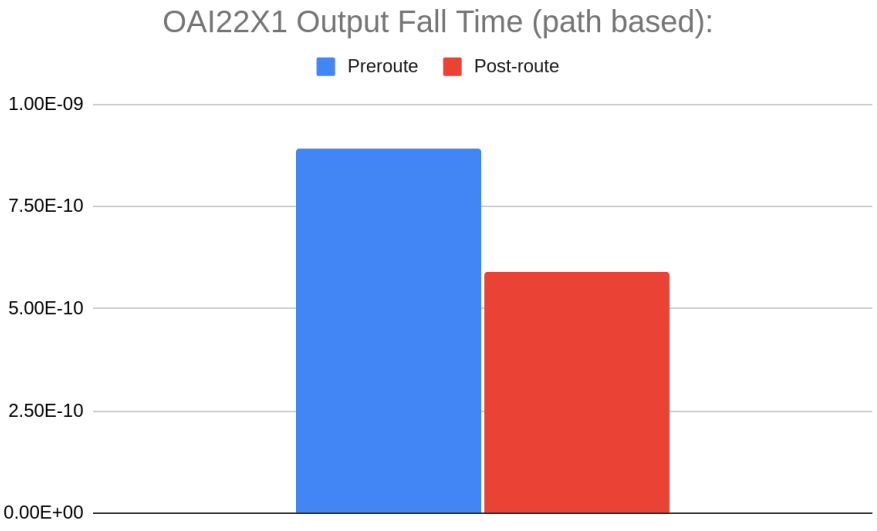
Preroute: 1.644E-9	Post-route: 1.643E-9

Output Fall Time (path based):

Preroute: 890.5E-12	Post-route: 589.6E-12


OAI22X1 Propagation Delay (Path Based)
Preroute
Post-route
1.50E-09
1.00E-09
5.00E-10
0.00E+00
A0 -> Y Rising
A0 - > Y Falling
A1 -> Y Rising
A1 - > Y Falling
B0 -> Y Rising
B0 - > Y Falling
B1 -> Y Rising
B1 -> Y Falling


OAI22X1 Output Rise Time (path based):
Preroute
Post-route
2.00E-09
1.50E-09
1.00E-09
5.00E-10
0.00E+00


OAI22X1 Output Fall Time (path based):
Preroute
Post-route
1.00E-09
7.50E-10
5.00E-10
2.50E-10
0.00E+00

As evident by the delay number tables and the accompanying charts, generally the post-route delay times are slower than the preroute times. There are few instances where the opposite is true, particularly in the fall times. The OAI22X1 is an example of this as it exhibits fall times that are across the board faster. This is caused by shared capacitances achieved during the layout process.

Conclusions

This project sought to cover the thorough study and design process of the seven elementary logic gates beginning with a schematic and symbol, and finishing with the layout of the cells. The preliminary work started on paper with the determination of the truth tables, schematic sketches and stick diagrams. Then the work translated over to the lab computers with Cadence software, in which all the simulations were performed. The layout was also completed in Cadence Virtuoso. The outcome of this project validated all the theory and truth tables as well as the effect of parasitic elements in the logic gates' performance. This project provided a thorough and painstaking understanding of the design process of the logic gates.

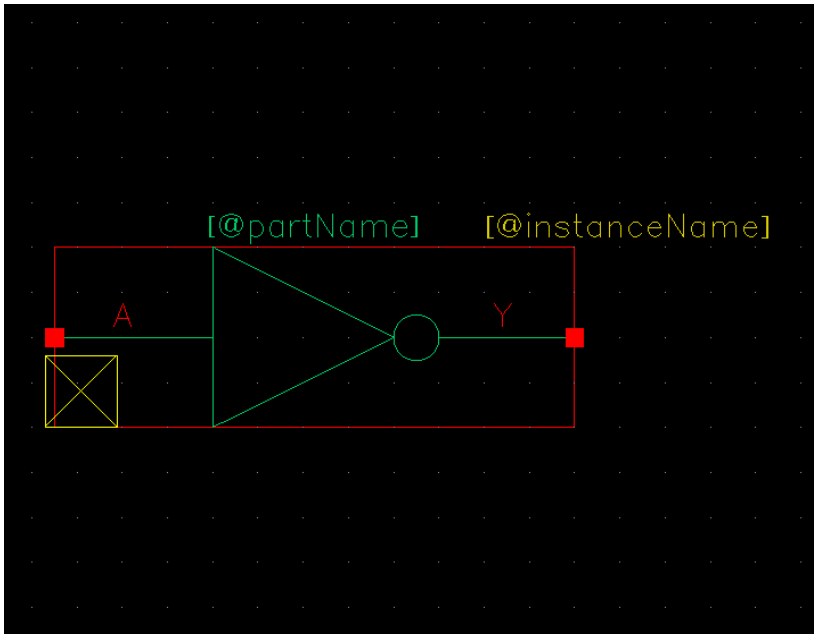
Appendix

Name: Tommy Choephel

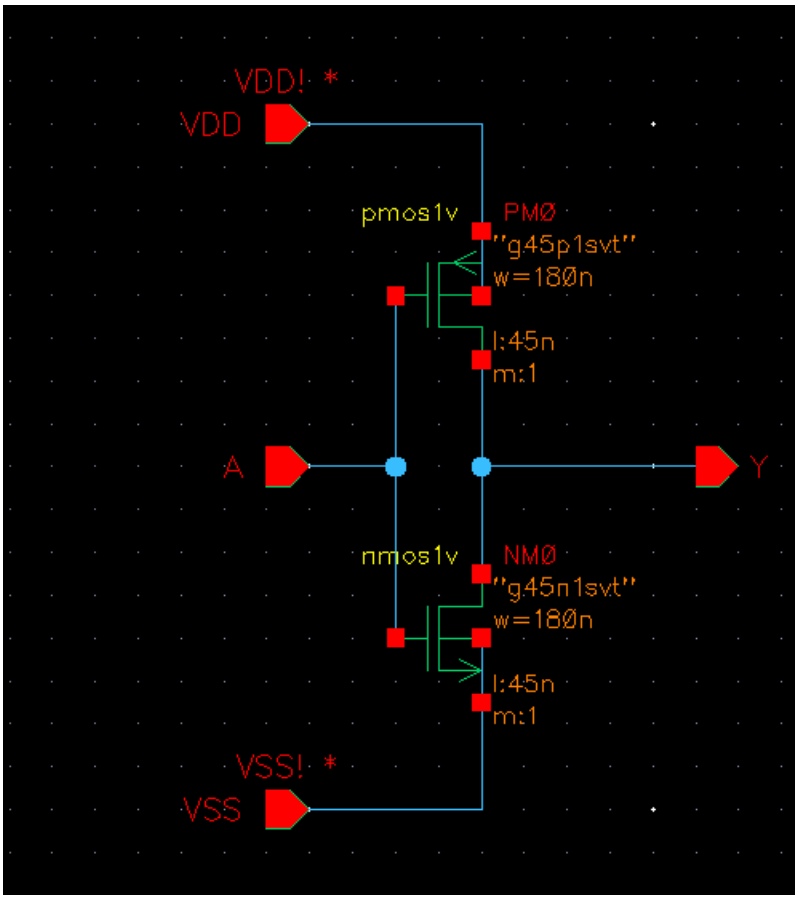
Library Name:	tc6652_tc_lib
Cell Name:	TC_INVX1
Function/Truth Table:	
A	Y
0	1
1	0
Propagation Delay (path based):	
Preroute	Post-route
A -> Y Rising: 1.135E-9	A -> Y Rising: 1.158E-9
A -> Y Falling: 802.4E-12	A -> Y Falling: 804.0E-12
Output Rise Time (path based):	
Preroute: 1.575E-9	Post-route: 1.606E-9
Output Fall Time (path based):	
Preroute: 1.125E-9	Post-route: 1.125E-9
Layout Height: 1.71 um	
Layout Width: 0.4 um	
Layout Area: 0.684 um^2	

Name: Tommy Choephel

Symbol with Port Names:

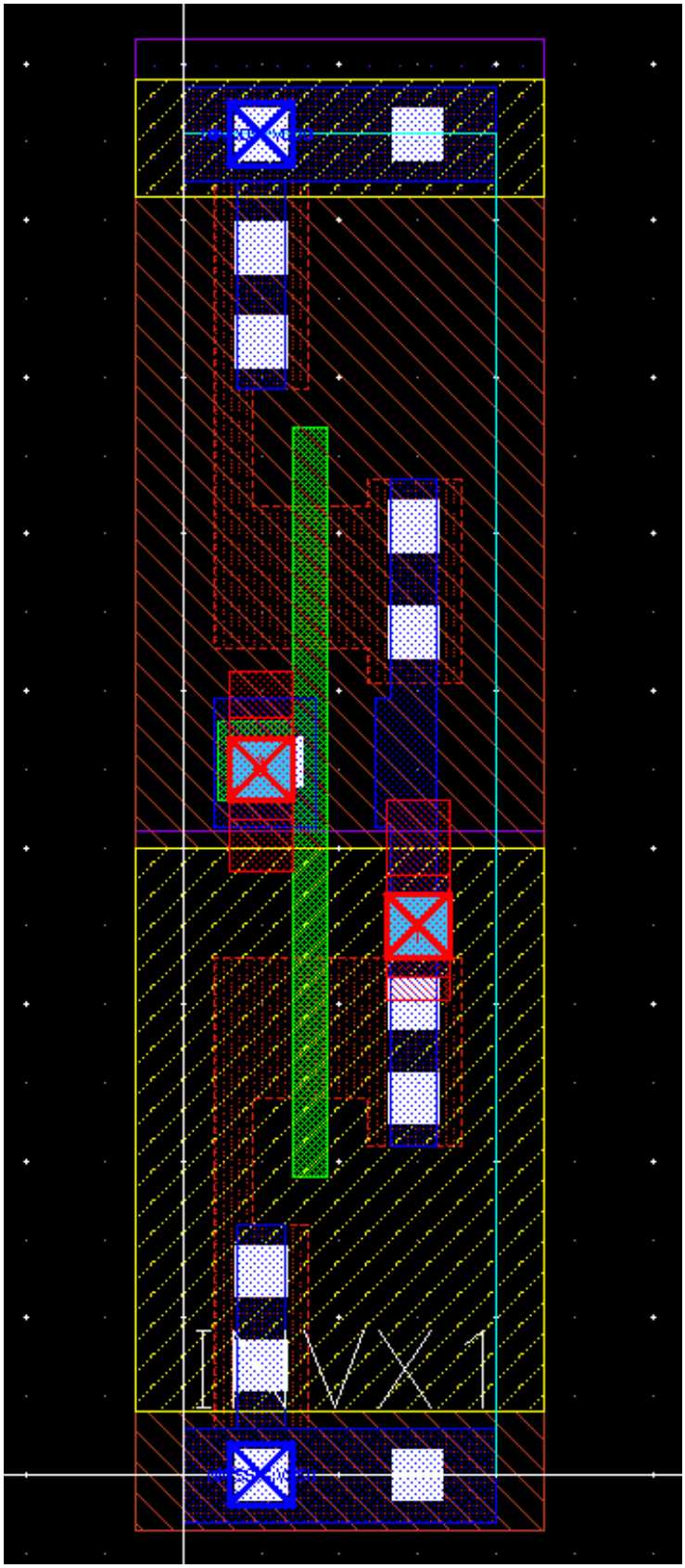


Schematic:



Name: Tommy Choephel

Layout:

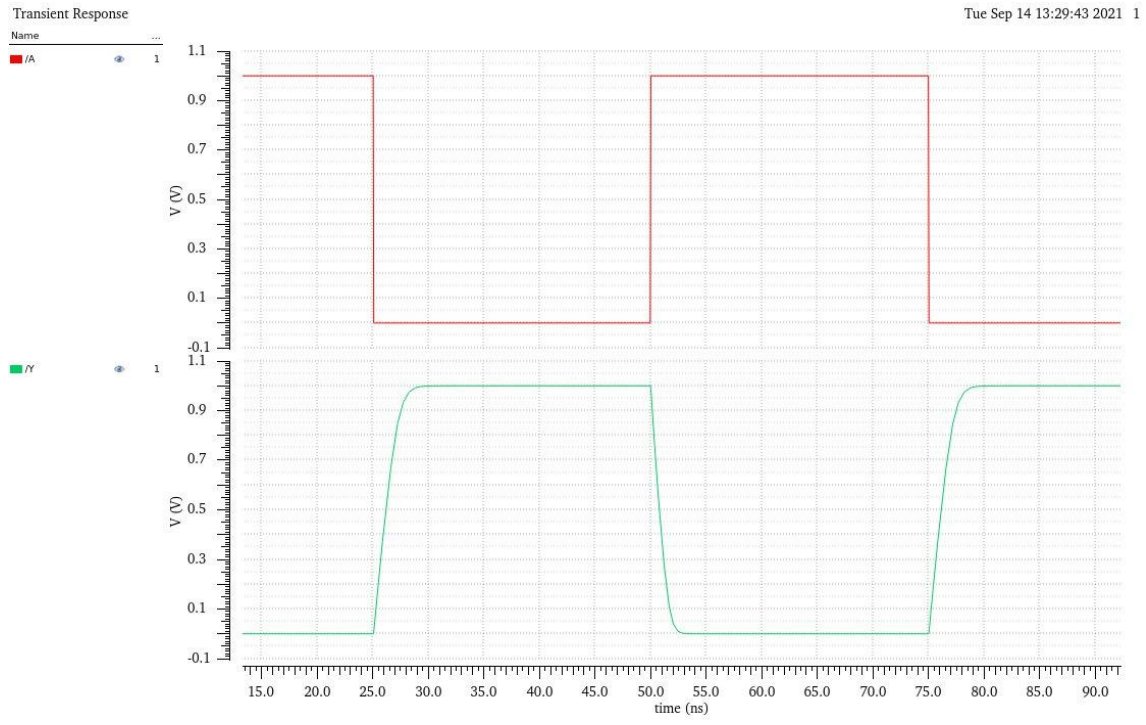


Name: Tommy Choephel

Verilog Model:

```
//Verilog HDL for "tc6652_tc_lib", "TC_INVX1" "functional"


module TC_INVX1 ( Y, A, .VDD(\VDD! ), .VSS(\VSS! ) );

 input A;
 output Y;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
 \VDD! ;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
 \VSS! ;

not U1(Y, A);

endmodule
```

Functional Simulation Waveforms



Name: Tommy Choephel

Comments/Notes:

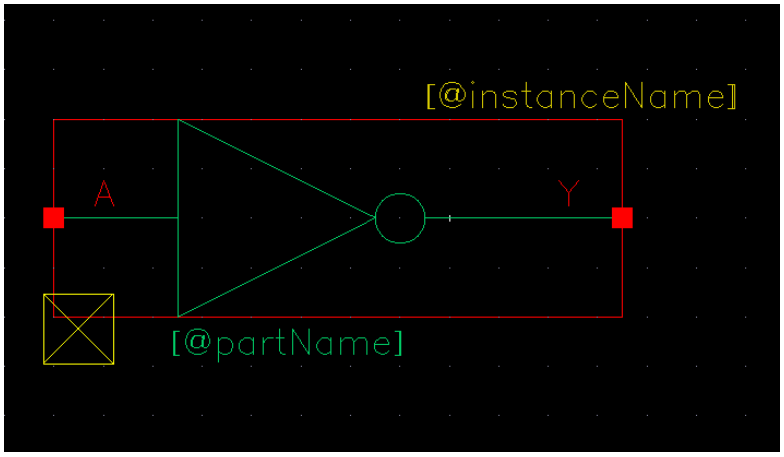
This is rather interesting...

Name: Tommy Choephel

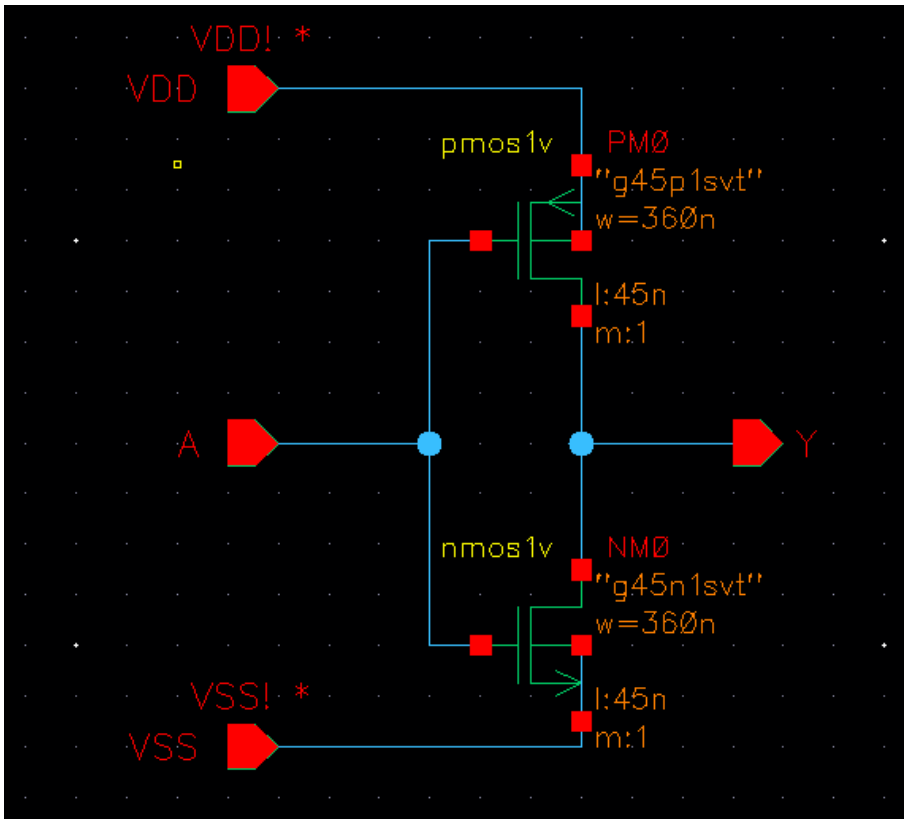
Library Name:	tc6652_tc_lib
Cell Name:	TC_INVX2
Function/Truth Table:	
A	Y
0	1
1	0
Propagation Delay (path based):	
Preroute	Post-route
A -> Y Rising: 614.9E-12	A -> Y Rising: 639.2E-12
A -> Y Falling: 431.6E-12	A -> Y Falling: 443.6E-12
Output Rise Time (path based):	
Preroute: 844.8E-12	Post-route: 879.8E-12
Output Fall Time (path based):	
Preroute: 592.7E-12	Post-route: 602.9E-12
Layout Height: 1.71 um	
Layout Width: 0. 4 um	
Layout Area: 0.684 um^2	

Name: Tommy Choephel

Symbol with Port Names:

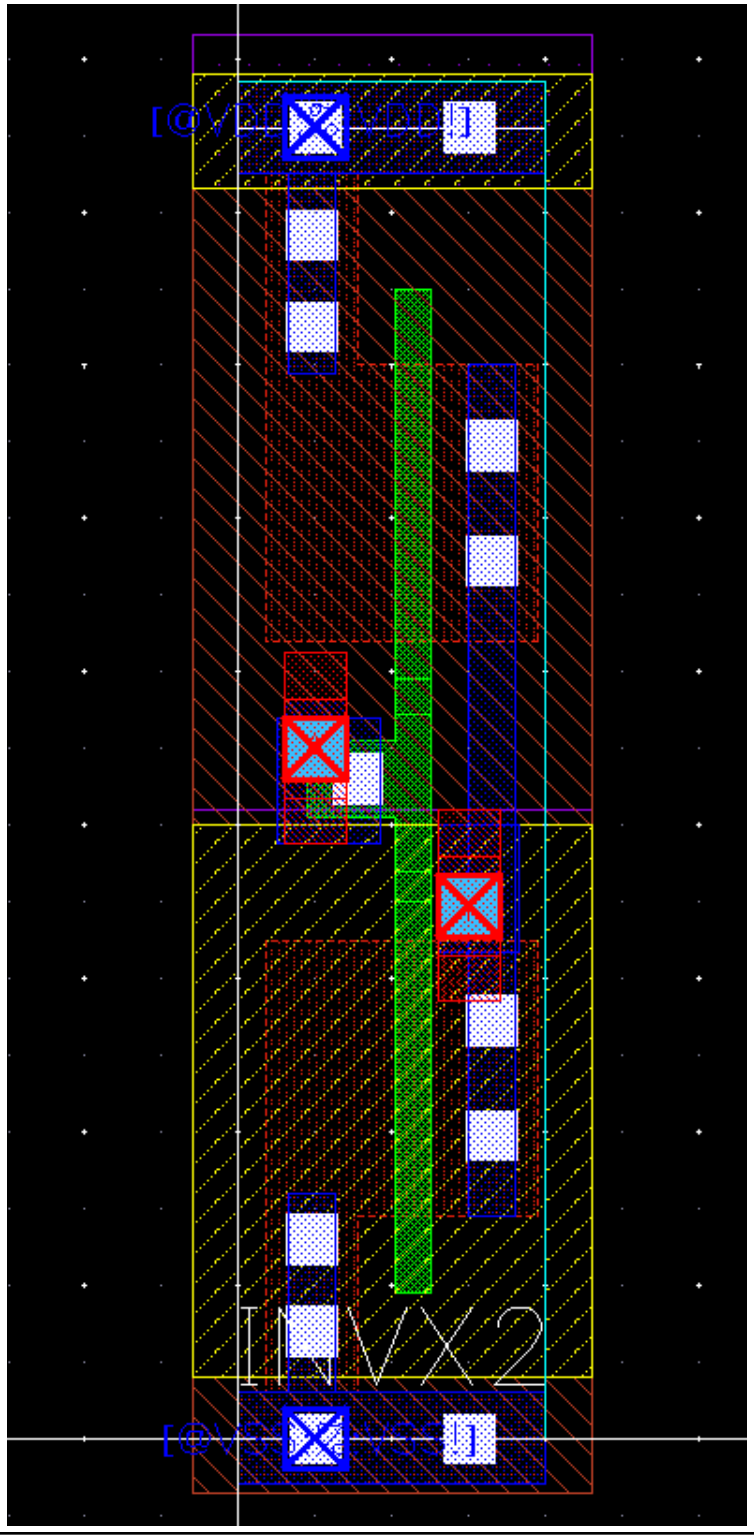


Schematic:



Name: Tommy Choephel

Layout:

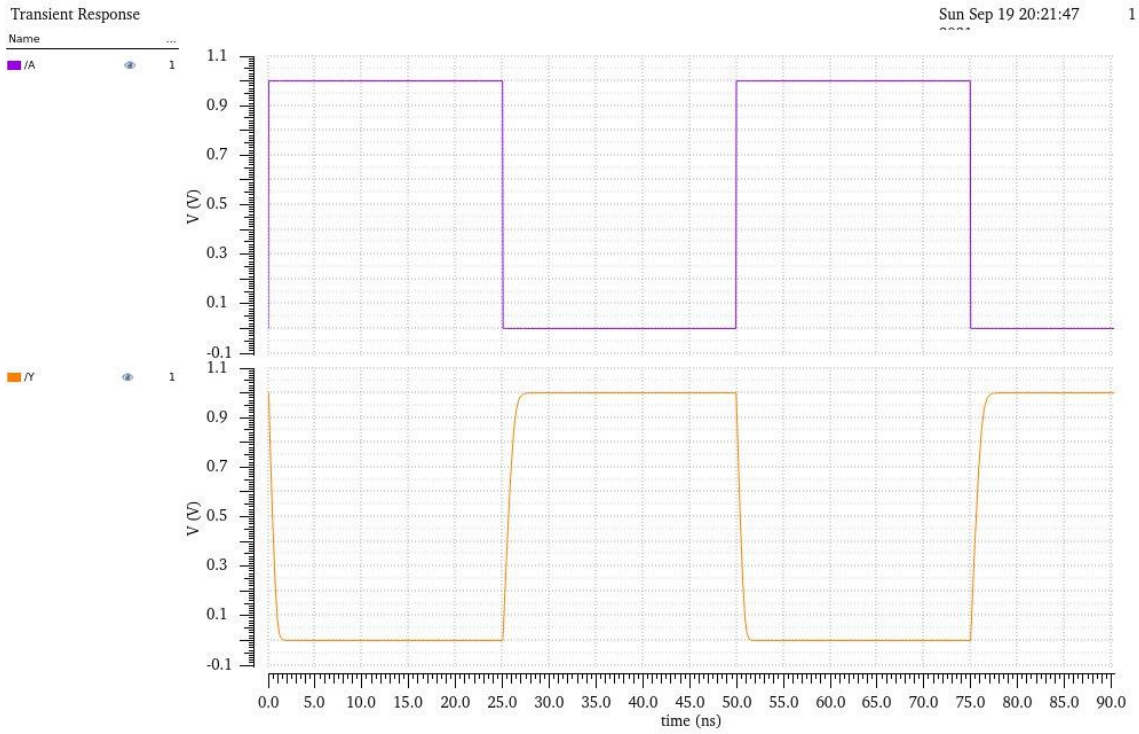


Verilog Model:

```
//Verilog HDL for "tc6652_tc_lib", "TC_INVX2" "functional"


module TC_INVX2 ( Y, A, .VDD(\VDD! ), .VSS(\VSS! ) );

 input A;
 output Y;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
 \VDD! ;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
 \VSS! ;

not U1(Y, A);

endmodule
```

Name: Tommy Choephel

Functional Simulation Waveforms



Comments/Notes:

Ah yes yes...

Name: Tommy Choephel

Library Name:	tc6652_tc_lib
Cell Name:	TC_NAND2X1

Function/Truth Table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Propagation Delay (path based):

Preroute

A -> Y Rising	**1.126E-9**
A -> Y Falling	**872.1E-12**
B -> Y Rising	**1.130E-9**
B -> Y Falling	**862.2E-12**

Post-route

A -> Y Rising	**1.186E-9**
A -> Y Falling	**1.501E-9**
B -> Y Rising	**1.201E-9**
B -> Y Falling	**1.501E-9**

Output Rise Time (path based):

Preroute: 1.562E-9	**Post-route: 1.704E-9**

Output Fall Time (path based):

Preroute: 2.162E-9	**Post-route: 2.029E-9**

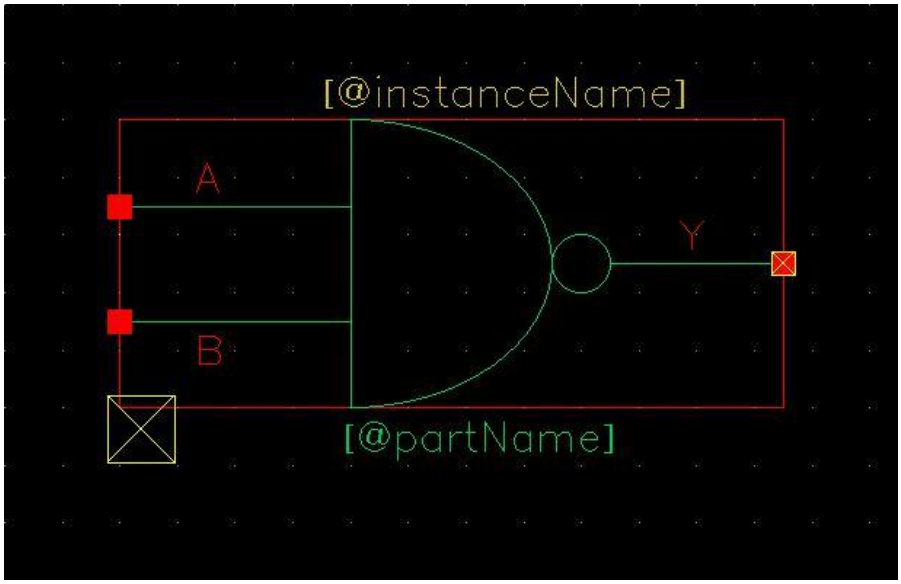
Layout Height: 1.71 um

Layout Width: 0.8 um

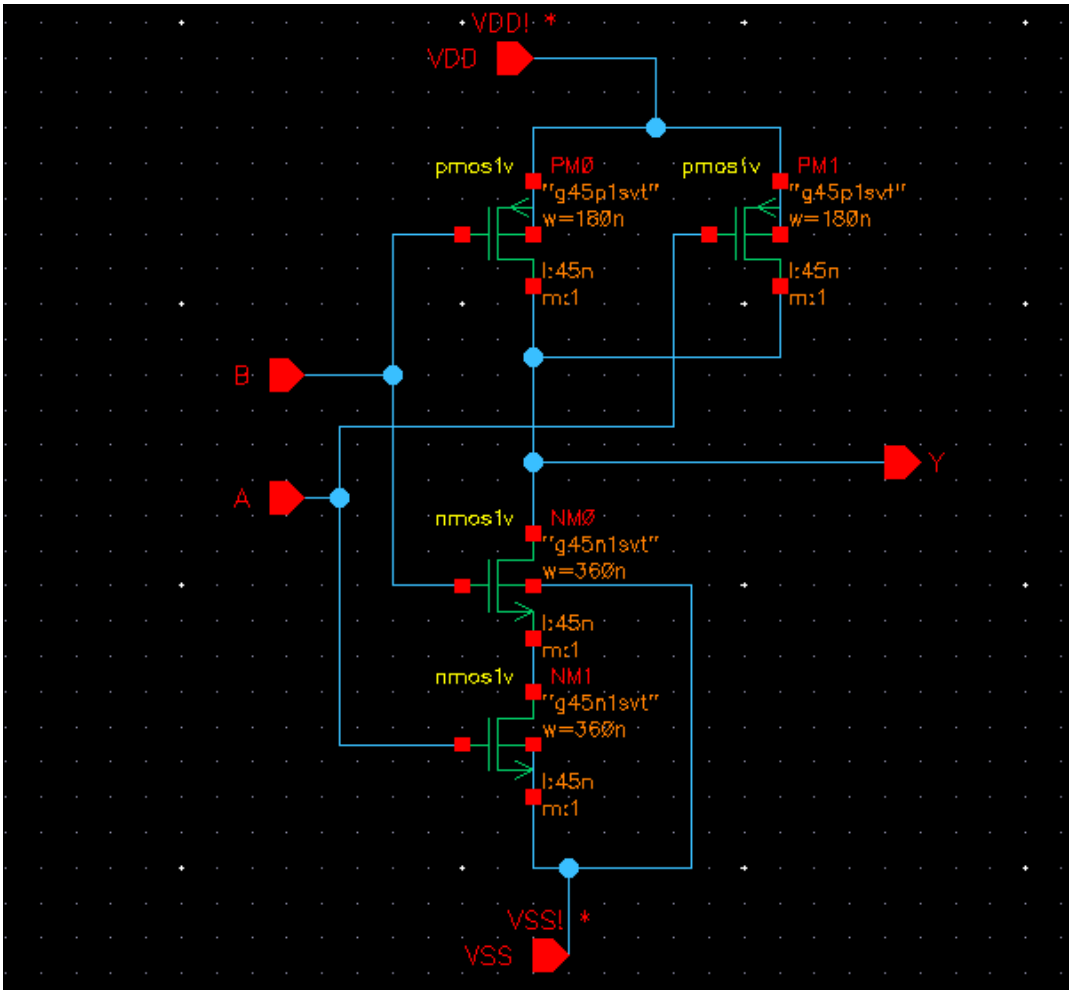
Layout Area: 1.368 um^2

Name: Tommy Choephel

Symbol with Port Names:

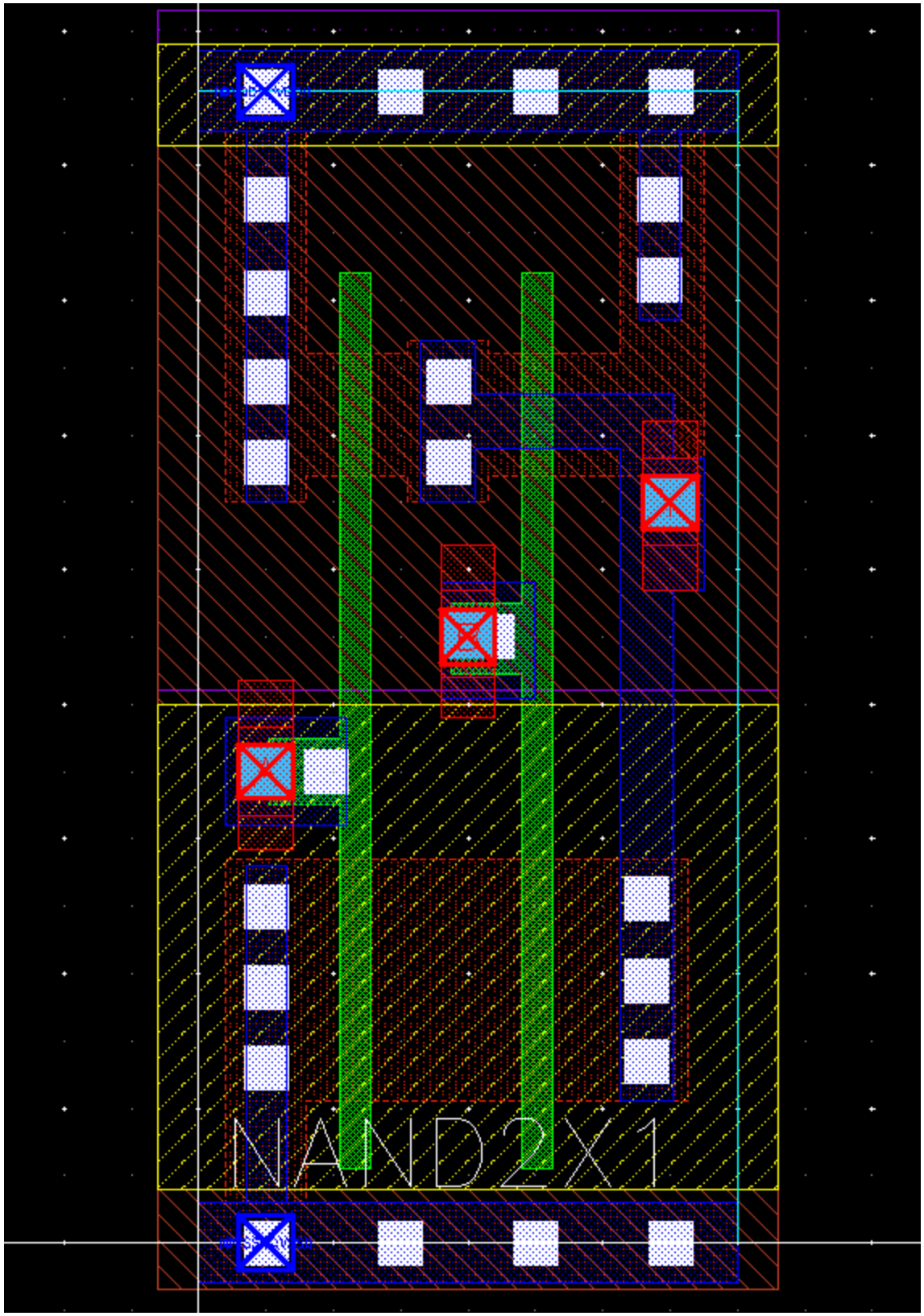


Schematic:



Name: Tommy Choephel

Layout:

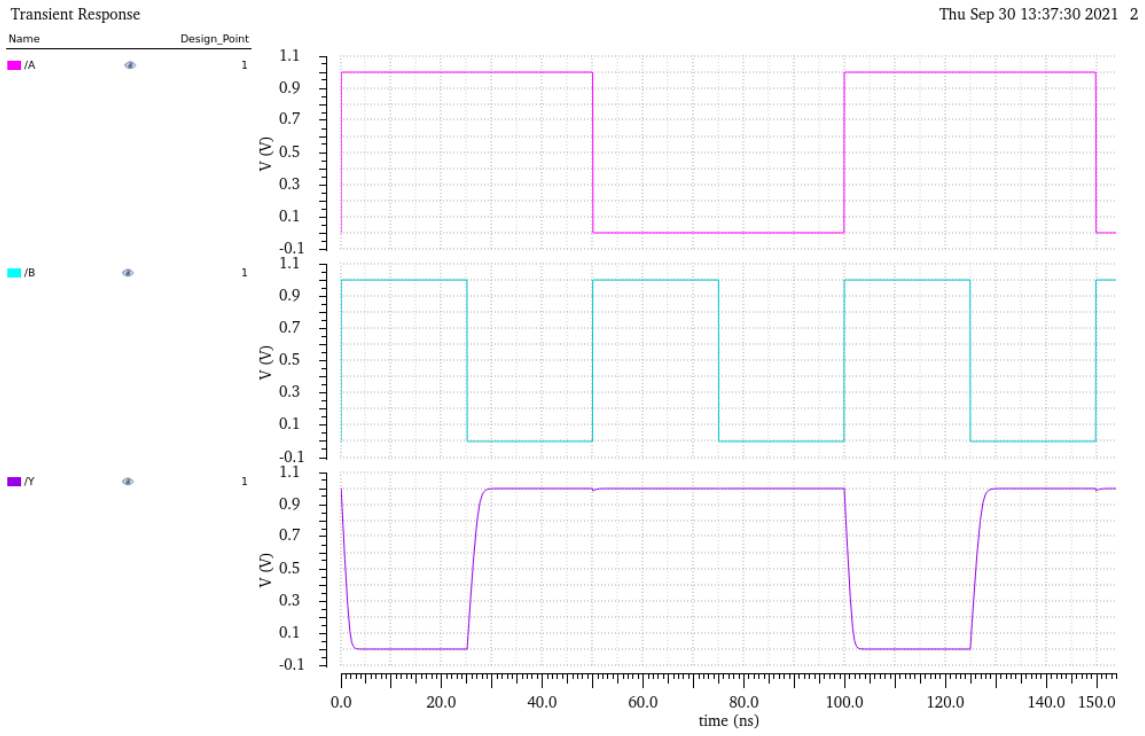


Name: Tommy Choephel

Verilog Model:

```
//Verilog HDL for "tc6652_tc_lib", "TC_NAND2X1" "functional"


module TC_NAND2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  output Y;
  input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
  input B;

    assign Y = ~(A & B);

endmodule
```

Functional Simulation Waveforms



Comments/Notes:

I suppose that's interesting...

Name: Tommy Choephel

Library Name:	tc6652_tc_lib
Cell Name:	TC_NOR2X1

Function/Truth Table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Propagation Delay (path based):

Preroute

A -> Y Rising	**1.237E-9**
A -> Y Falling	**799.4E-12**
B -> Y Rising	**1.232E-9**
B -> Y Falling	**799.8E-12**

Post-route

A -> Y Rising	**2.455E-9**
A -> Y Falling	**762.5E-12**
B -> Y Rising	**2.416E-9**
B -> Y Falling	**766.0E-12**

Output Rise Time (path based):

Preroute: 1.676E-9	**Post-route: 3.311E-9**

Output Fall Time (path based):

Preroute: 558.8E-12	**Post-route: 537.3E-12**

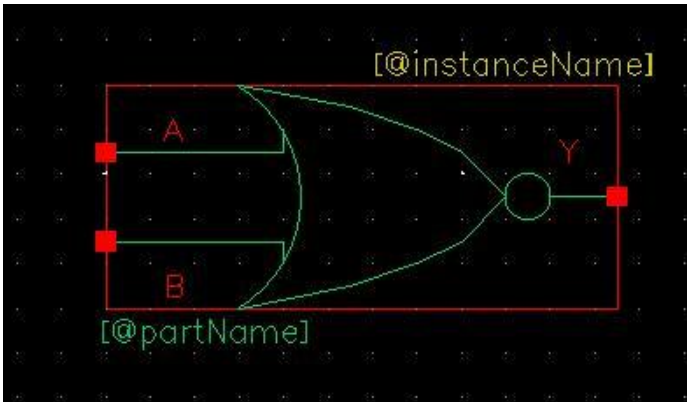
Layout Height: 1.71 um

Layout Width: 0.8 um

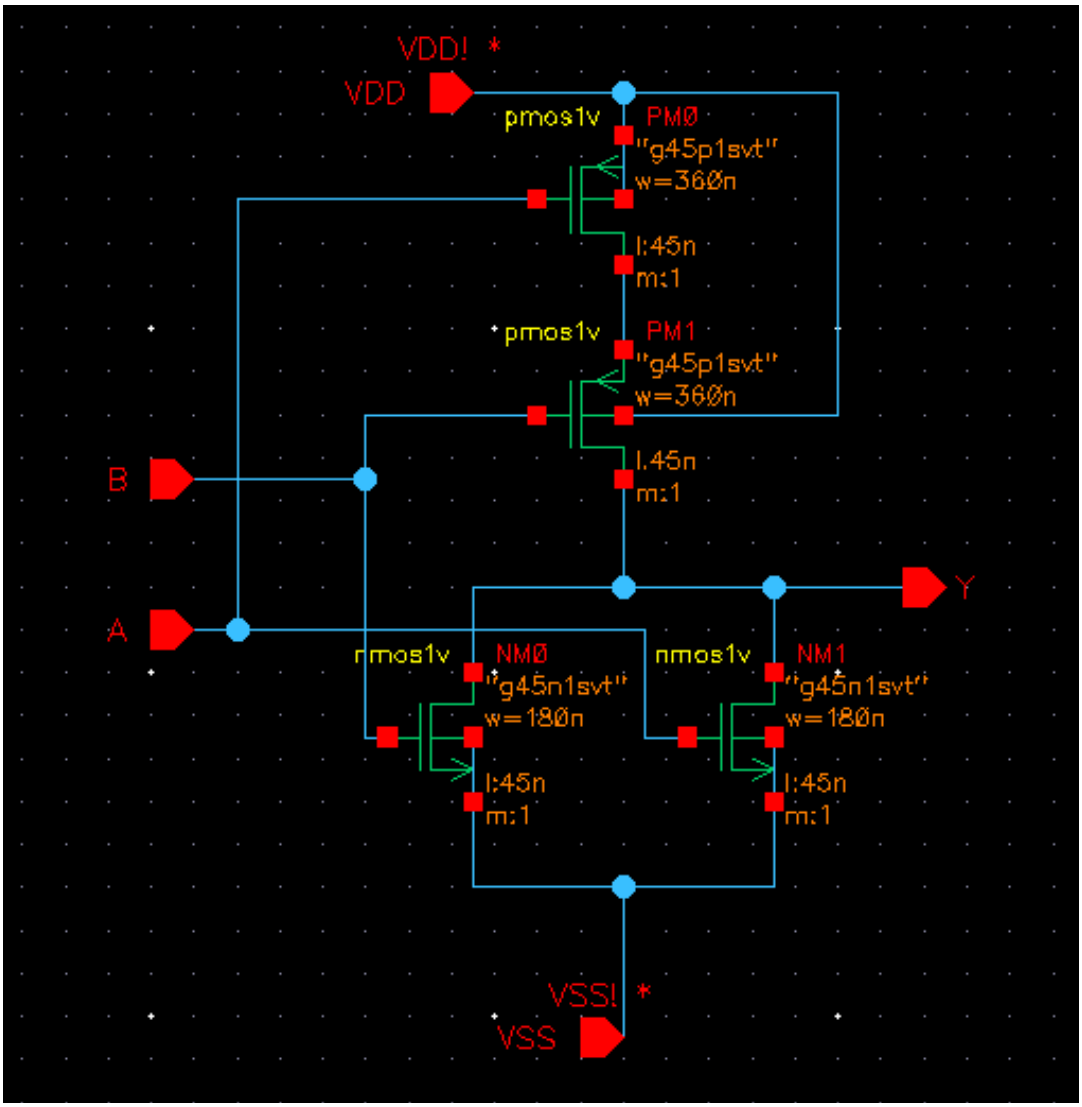
Layout Area: 1.368 um^2

Name: Tommy Choephel

Symbol with Port Names:

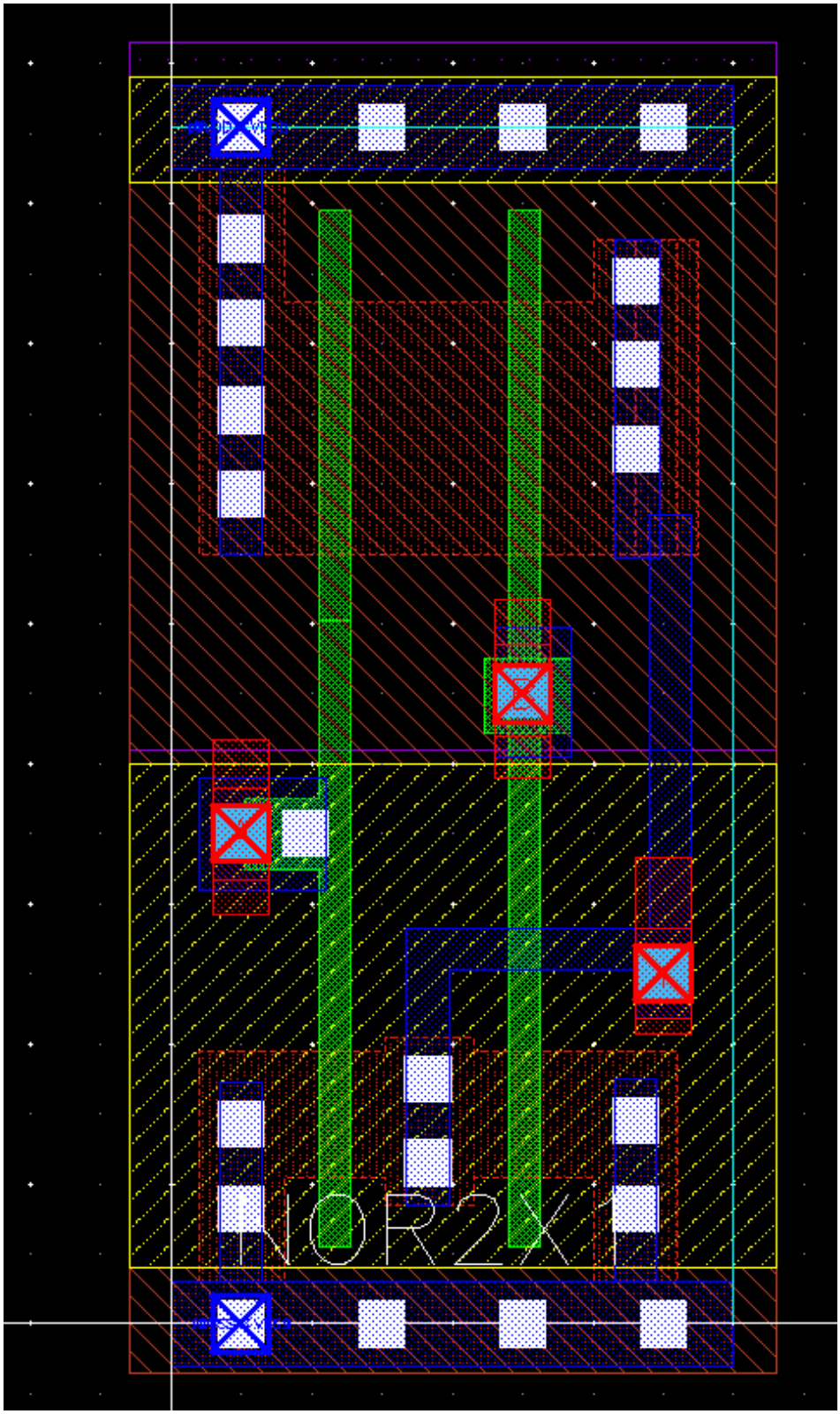


Schematic:



Name: Tommy Choephel

Layout:

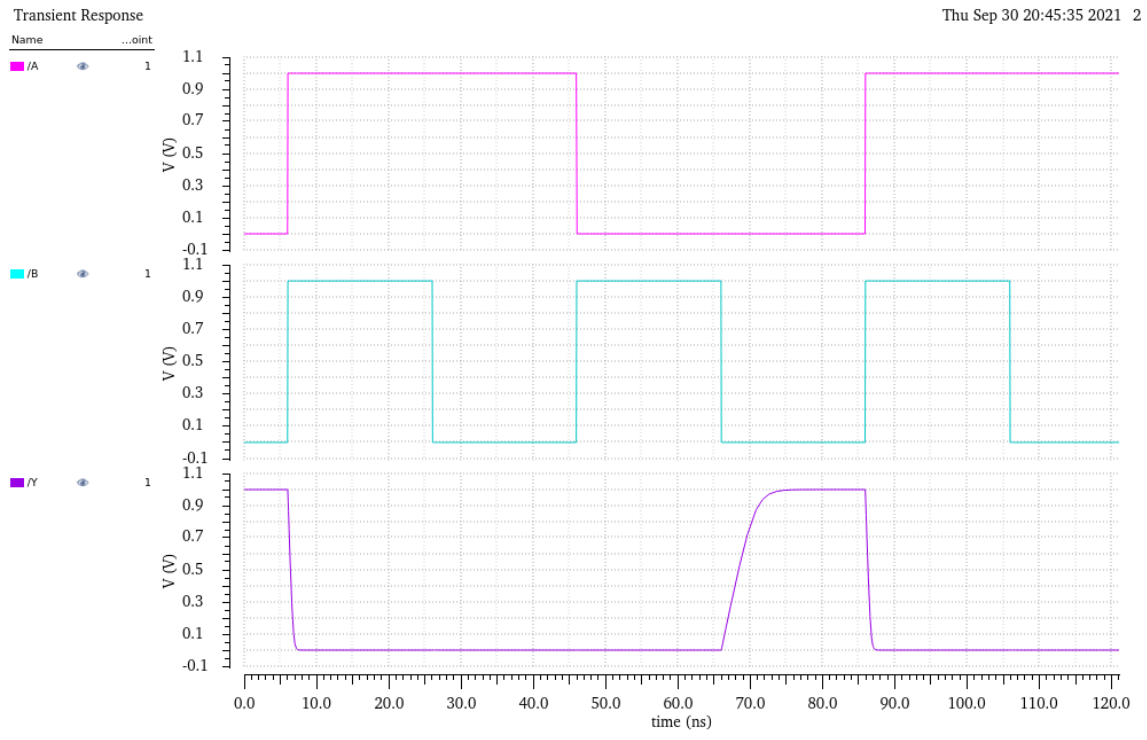


Name: Tommy Choephel

Verilog Model:

```
//Verilog HDL for "tc6652_tc_lib", "TC_NOR2X1" "functional"

module TC_NOR2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

 input A;
 output Y;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
 \VDD! ;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
 \VSS! ;
 input B;

  assign Y = ~(A | B);

endmodule
```

Functional Simulation Waveforms



Name: Tommy Choephel

Comments/Notes:
Neither I NOR you will want to do this project again.

Name: Tommy Choephel

Library Name:	tc6652_tc_lib
Cell Name:	TC_MUX2X1

Function/Truth Table:

S	A	B	Y
1	0	X	0
1	1	X	1
0	X	0	0
0	X	1	1

Propagation Delay (path based):

Preroute

A -> Y Rising	1.148E-9
A -> Y Falling	830.7E-12
B -> Y Rising	1.143E-9
B -> Y Falling	827.4E-12
S -> Y Rising	1.160E-9
S -> Y Falling	840.0E-12

Post-route

A -> Y Rising	1.211E-9
A -> Y Falling	877.7E-12
B -> Y Rising	1.200E-9
B -> Y Falling	826.1E-12
S -> Y Rising	1.238E-9
S -> Y Falling	880.0E-12

Output Rise Time (path based):

Preroute: 1.567E-9	**Post-route: 1.598E-9**

Output Fall Time (path based):

Preroute: 1.119E-9	**Post-route: 1.086E-9**

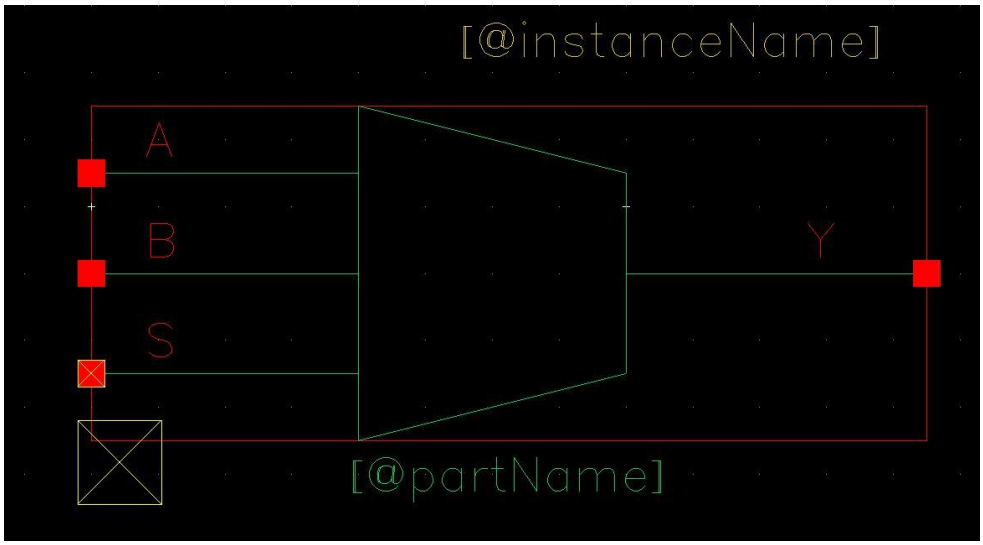
Name: Tommy Choephel

Layout Height: 1.71 um

Layout Width: 4 um

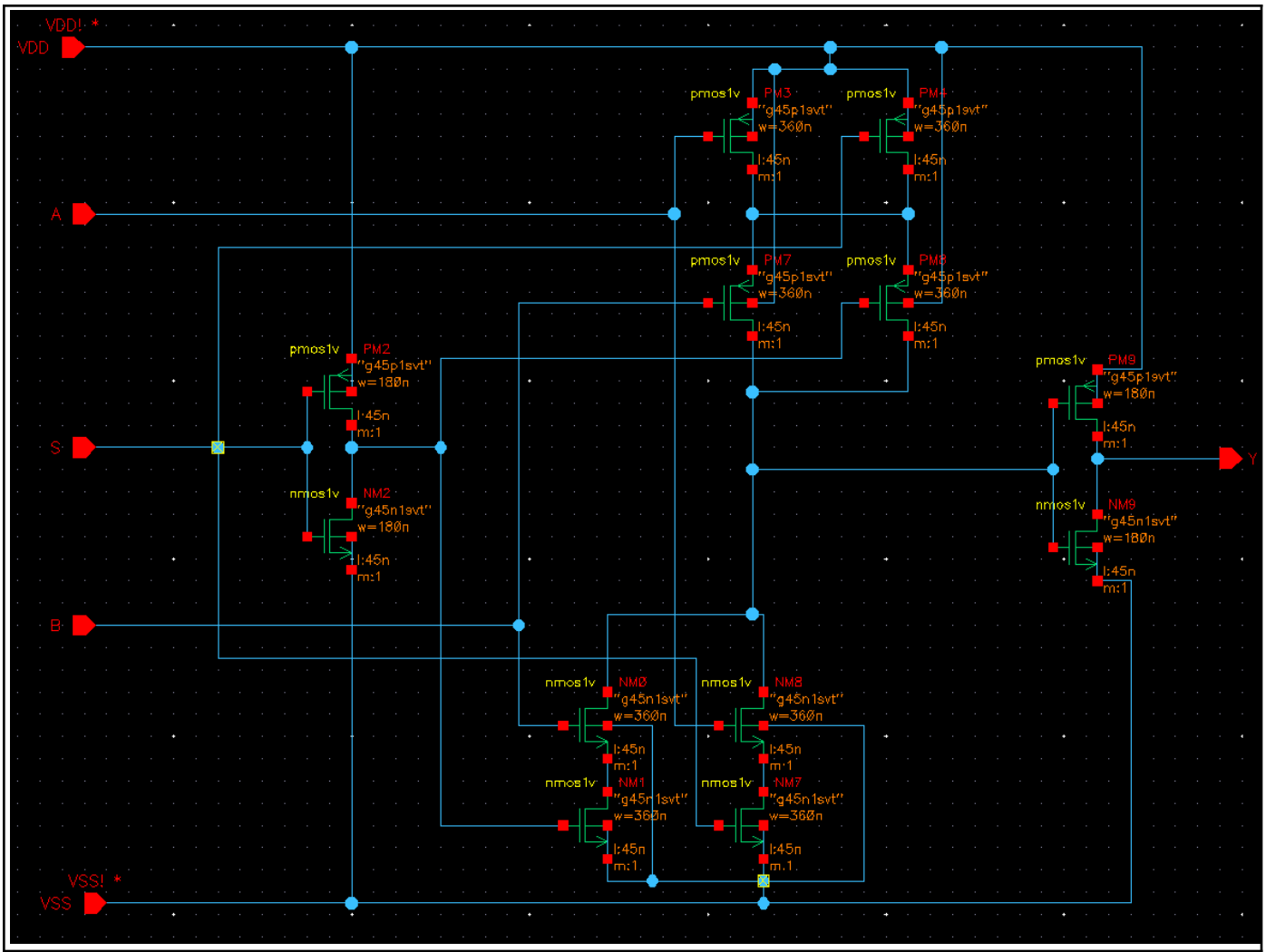
Layout Area: 6.84 um^2

Symbol with Port Names:

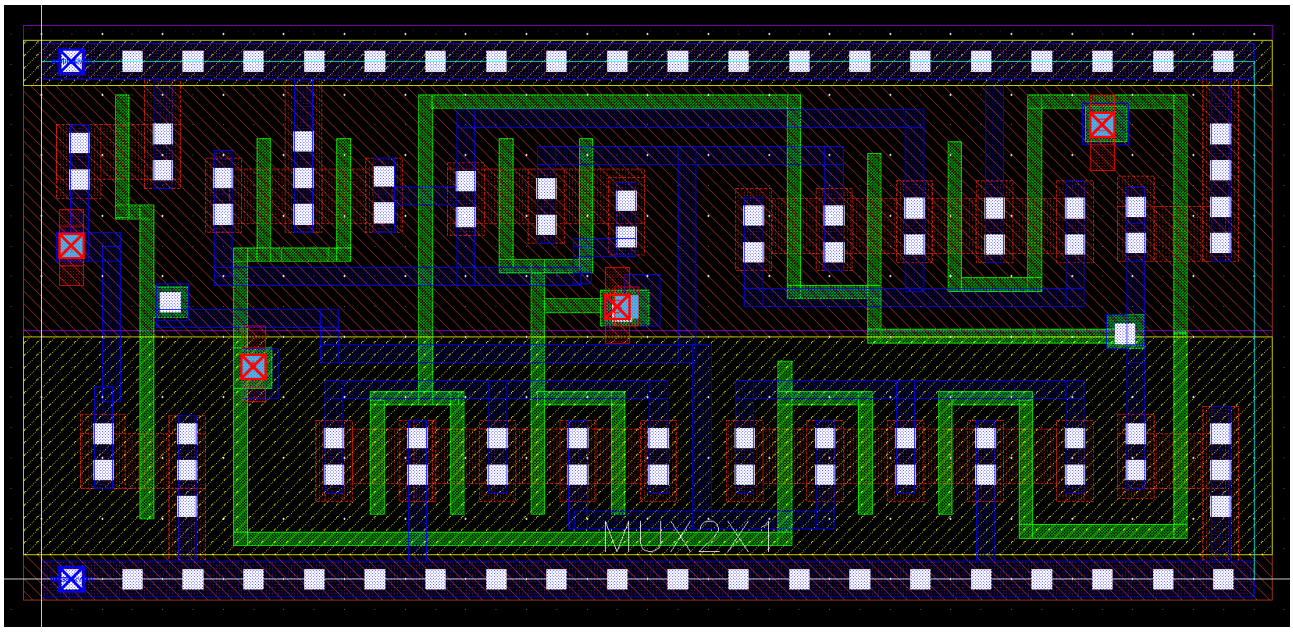


Schematic:

Name: Tommy Choephel



Layout:

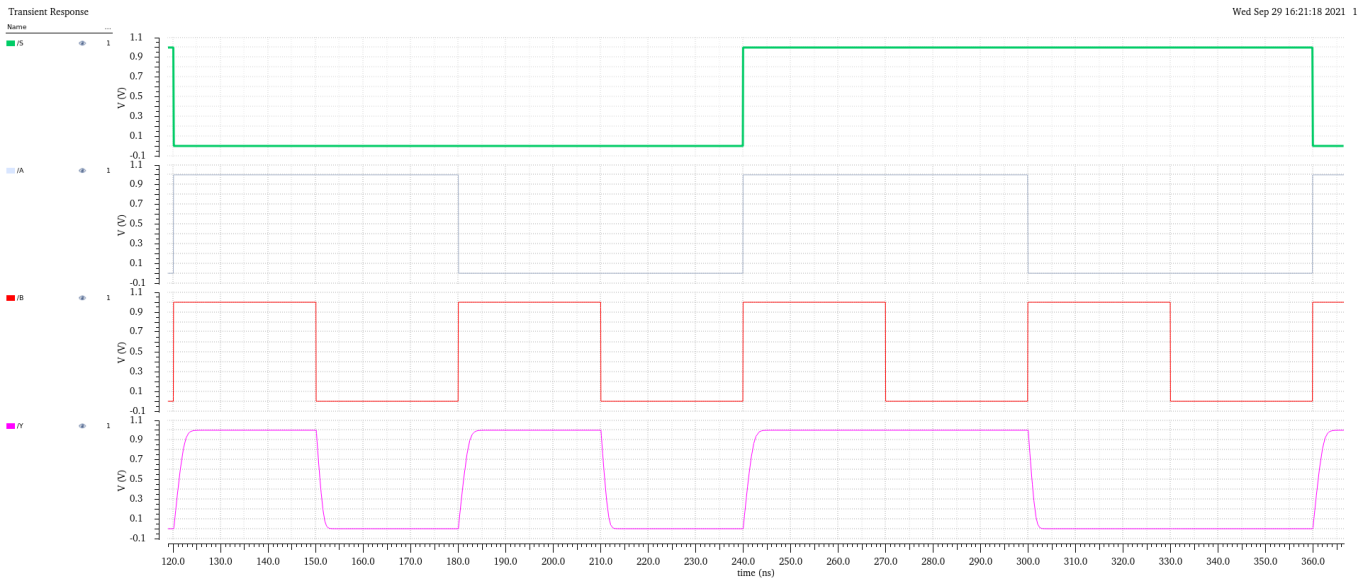


Name: Tommy Choephel

Verilog Model:

```
//Verilog HDL for "tc6652_tc_lib", "TC_MUX2X1" "functional"


module TC_MUX2X1 ( Y, A, B, S, .VDD(\VDD! ), .VSS(\VSS! ) );

 input S;
 input A;
 output Y;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
 \VDD! ;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
 \VSS! ;
 input B;

   assign Y = (S) ? A : B; // Y = A if Select is true, B otherwise.
endmodule
```

Functional Simulation Waveforms



Name: Tommy Choephel

Comments/Notes:
Most interesting...

Name: Tommy Choephel

Library Name:	tc6652_tc_lib	
Cell Name:	TC_XOR2X1	
Function/Truth Table:		
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Propagation Delay (path based):

Preroute	
A -> Y Rising	**1.251E-9**
A -> Y Falling	**884.8E-12**
B -> Y Rising	**1.255E-9**
B -> Y Falling	**890.4E-12**

Post-route	
A -> Y Rising	**1.319E-9**
A -> Y Falling	**780.0E-12**
B -> Y Rising	**1.316E-9**
B -> Y Falling	**784.6E-12**

Output Rise Time (path based):	
Preroute: 1.642E-9	**Post-route: 1.699E-9**
Output Fall Time (path based):	
Preroute: 1.144E-9	**Post-route: 988.1E-12**

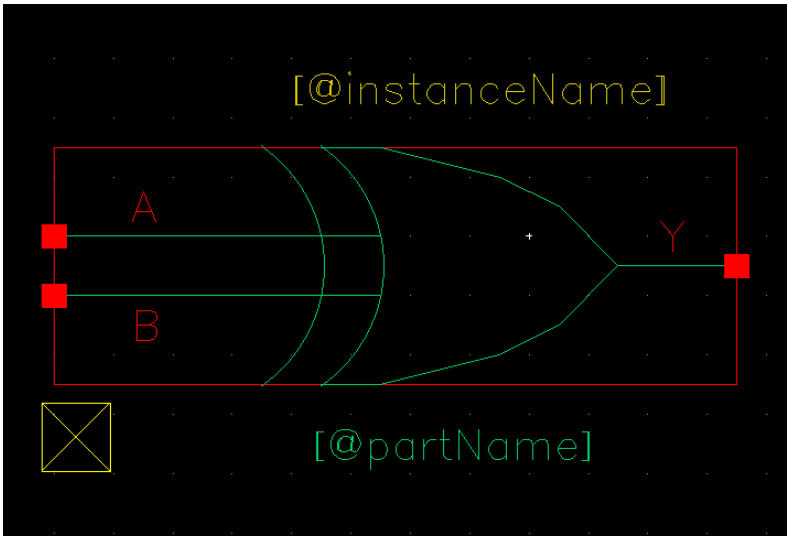
Layout Height: 1.71 um

Layout Width: 4 um

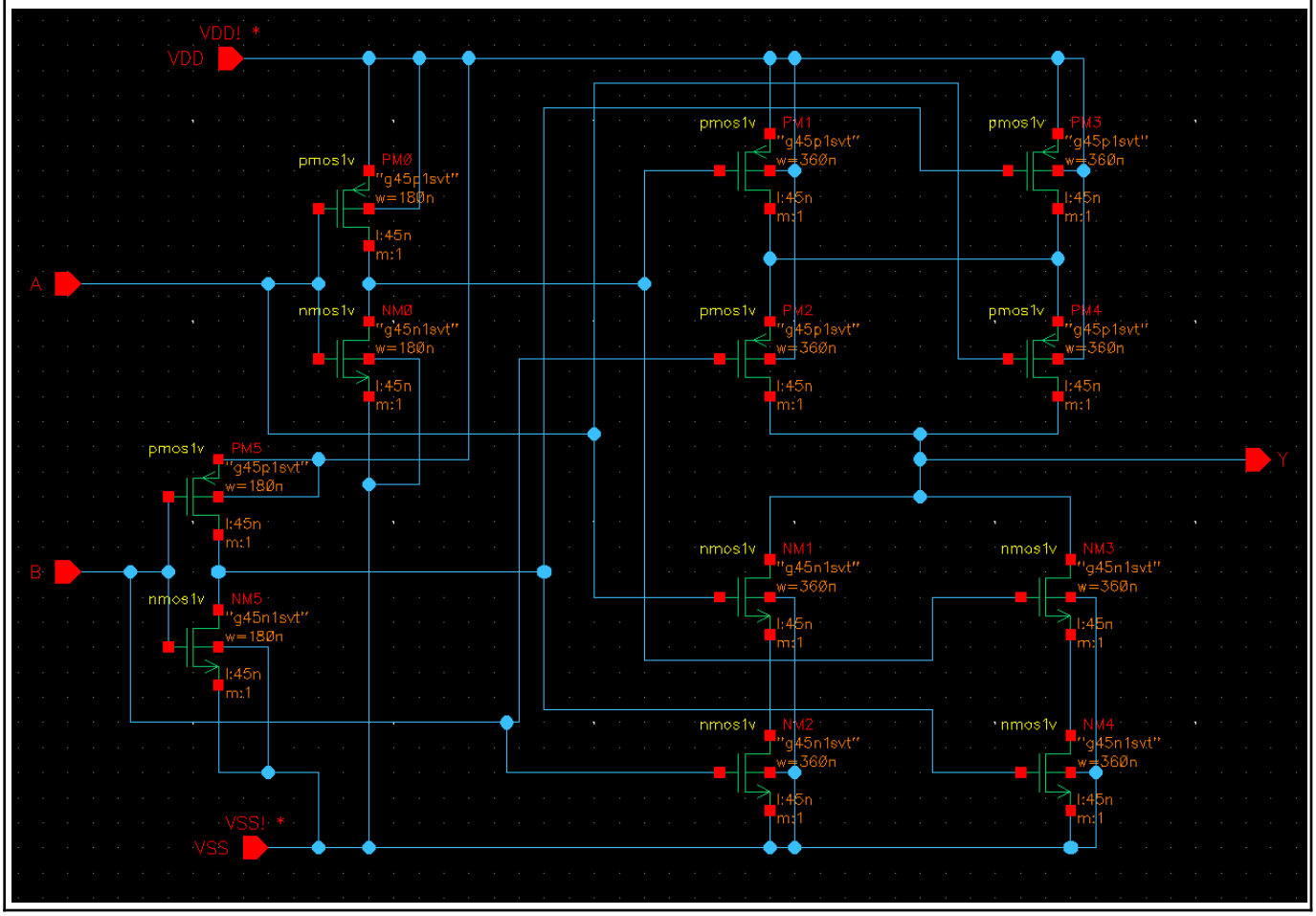
Layout Area: 6.84 um^2

Name: Tommy Choephel

Symbol with Port Names:

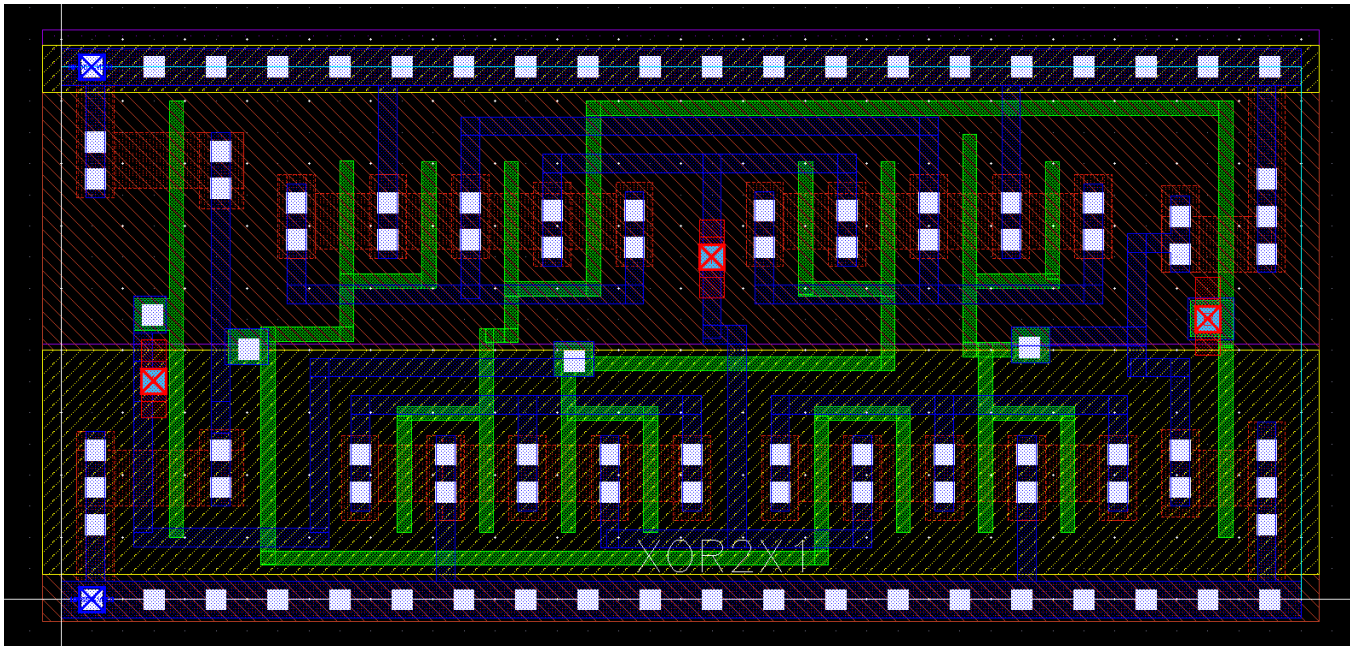


Schematic:



Name: Tommy Choephel

Layout:

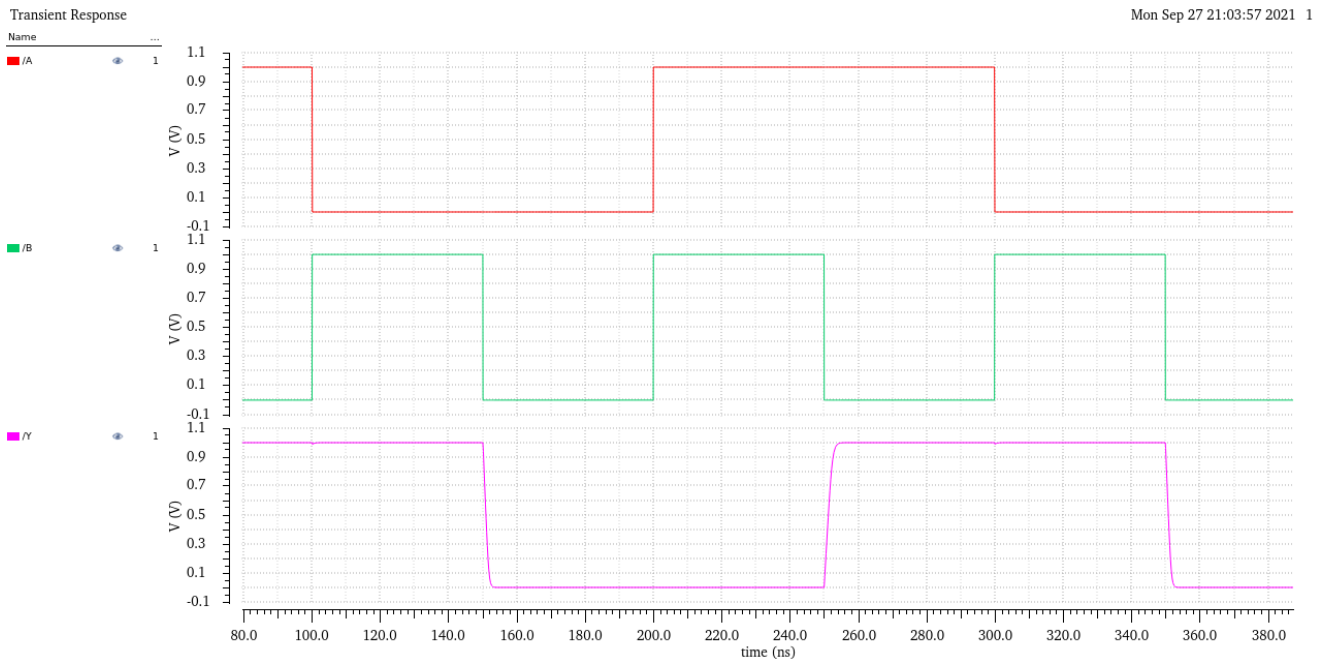


Verilog Model:

```
//Verilog HDL for "tc6652_tc_lib", "TC_XOR2X1" "functional"

module TC_XOR2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

 input A;
 output Y;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
 \VDD! ;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
 \VSS! ;
 input B;

   assign Y = A ^ B;

endmodule
```

Name: Tommy Choephel

Functional Simulation Waveforms



Comments/Notes:

Ah yes yes… quite interesting...

Name: Tommy Choephel

Library Name:	tc6652_tc_lib
Cell Name:	TC_OAI22X1

Function/Truth Table:

A0	B0	A1	B1	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Propagation Delay (path based):

Name: Tommy Choephel

Preroute

A0 -> Y Rising	1.233E-9
A0 -> Y Falling	871.9E-12
A1 -> Y Rising	1.232E-9
A1 -> Y Falling	871.9E-12
B0 -> Y Rising	1.229E-9
B0 -> Y Falling	866.9E-12
B1 -> Y Rising	1.239E-9
B1 -> Y Falling	880.0E-12

Post-route

A0 -> Y Rising	1.416E-9
A0 -> Y Falling	784.2E-12
A1 -> Y Rising	1.389E-9
A1 -> Y Falling	763.5E-12
B0 -> Y Rising	1.409E-9
B0 -> Y Falling	759.7E-12
B1 -> Y Rising	1.372E-9
B1 -> Y Falling	773.1E-12

Output Rise Time (path based):

Preroute: 1.644E-9	Post-route: 1.643E-9

Output Fall Time (path based):

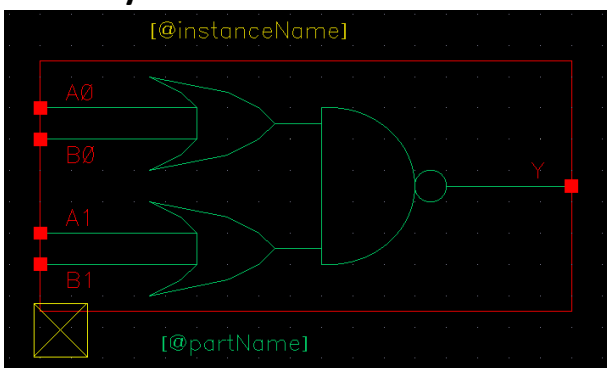
Preroute: 890.5E-12	Post-route: 589.6E-12

Layout Height: 1.71 um

Layout Width: 1.6 um

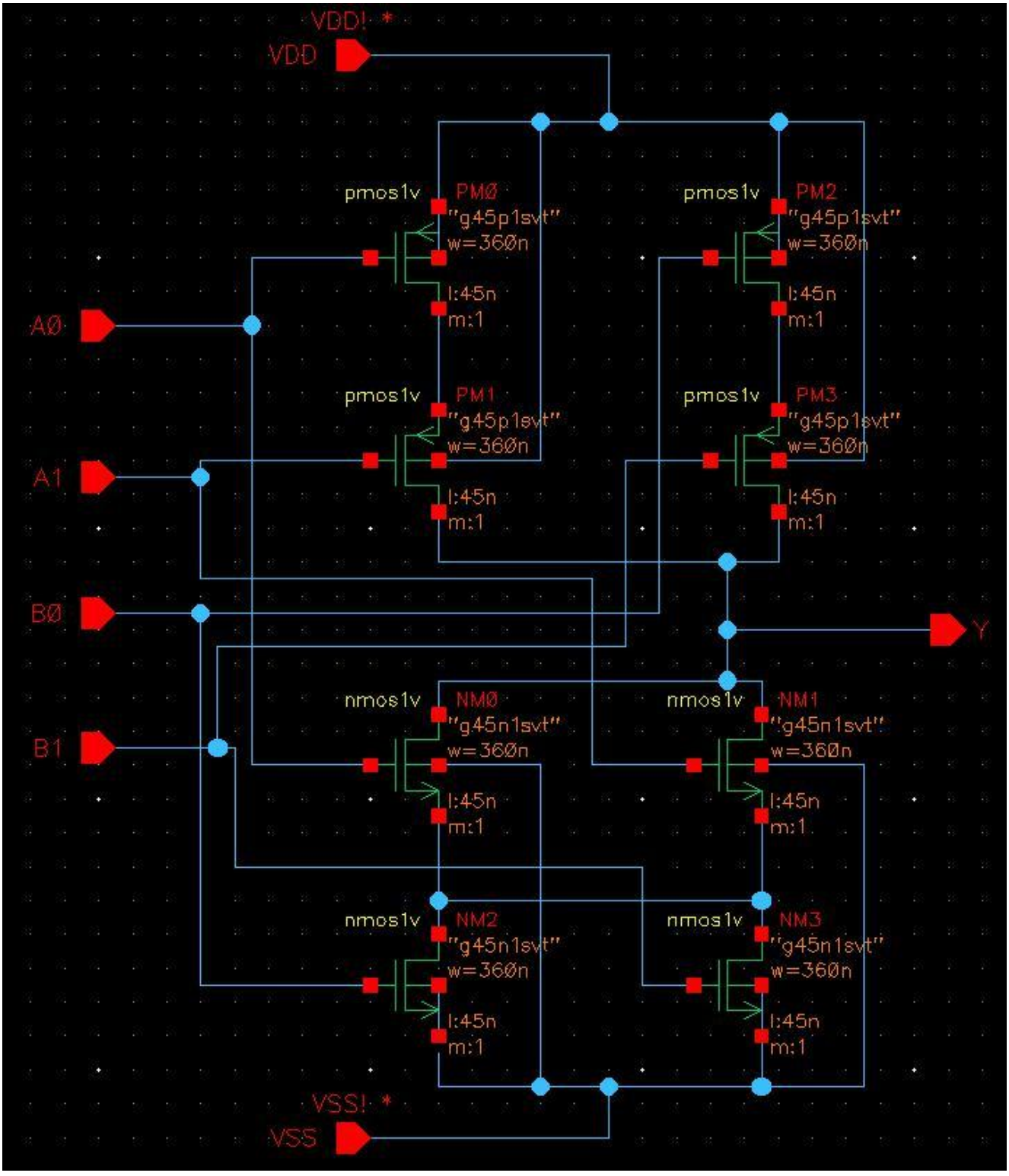
Layout Area: 2.736 um^2

Symbol with Port Names:



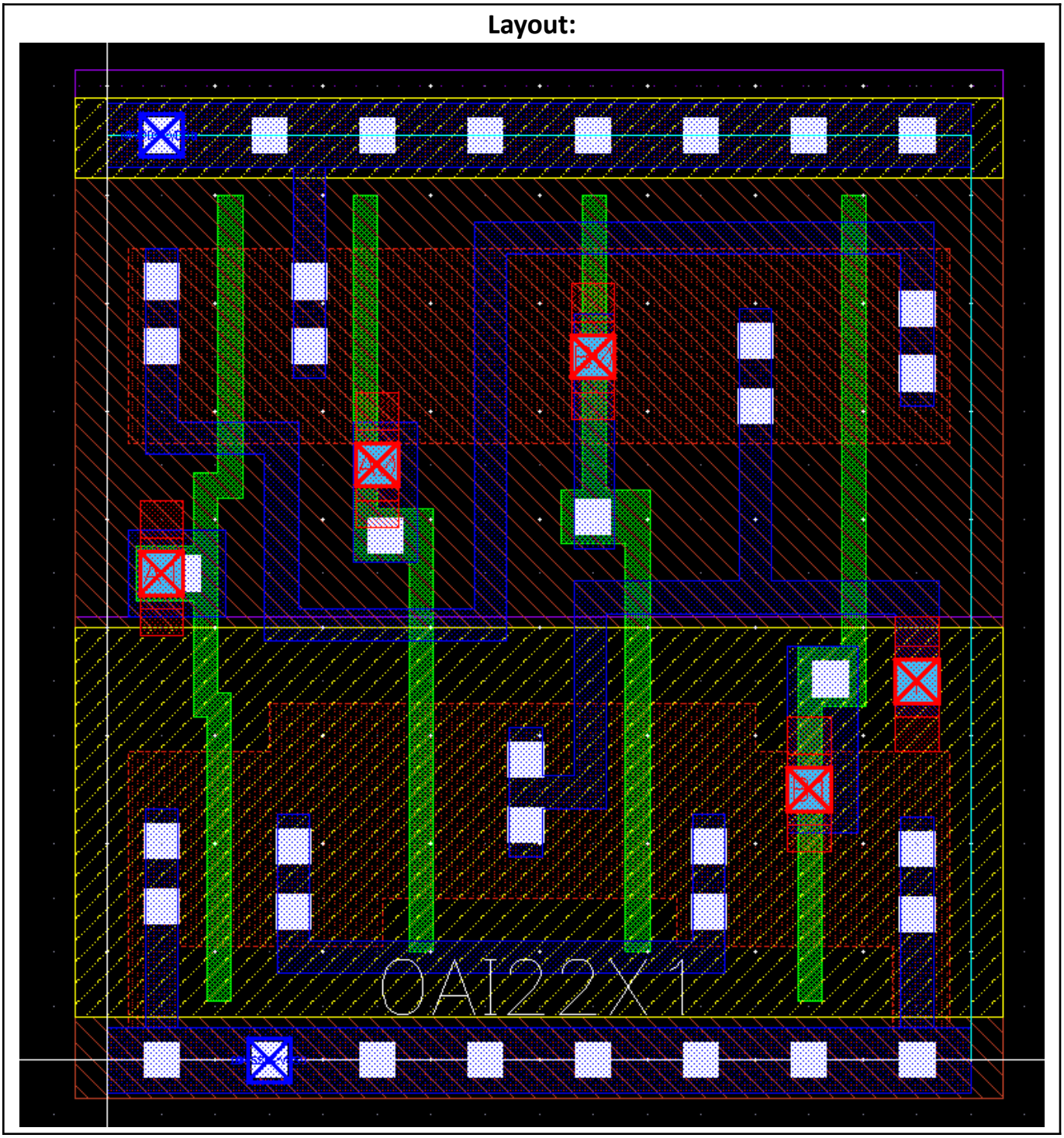
Name: Tommy Choephel

Schematic:



Name: Tommy Choephel

Layout:



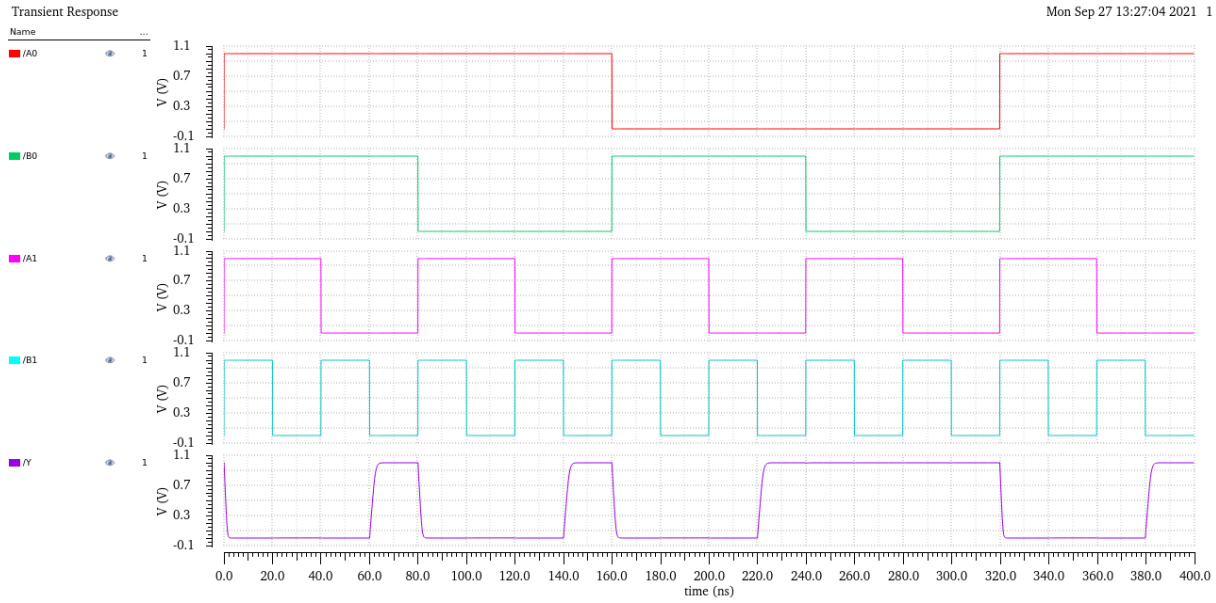
Name: Tommy Choephel

Verilog Model:

```
//Verilog HDL for "tc6652_tc_lib", "TC_OAI22X1" "functional"


module TC_OAI22X1 ( Y, A0, A1, B0, B1, .VDD(\VDD! ), .VSS(\VSS! ) );

 input A0;
 output Y;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
 \VDD! ;
 input B0;
 input B1;
 input A1;
 input
`ifdef XCELIUM
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
 \VSS! ;

assign Y = ~((A0 | B0) & (A1 | B1));

endmodule
```

Name: Tommy Choephel

Functional Simulation Waveforms



Comments/Notes:

For a cascaded logic, this was rather easy to implement… certainly when compared to the XOR gate.