EE520 | EE620 Project 1 Assignment

Assigned: Friday, September 03, 2021

Project 1 Due: Monday, September 27, 2021, 11:59 PM

The grade for this project will be based on:

1. Completion of the EDA Tutorial 1 assignment by indicated date and time - No Exceptions!
2. Completion of the Project 1 assignment by indicated date and time - No Exceptions!
3. A 5 min. oral presentation and defense of your work as organized by the instructor and TA during the week Project 1 is due.
4. The following files uploaded to the mycourses Project 1 Report dropbox:
    a. The Project 1 Engineering Report (use template *EE520_EE620_tech_memo.doc* on mycourses, engineering report details are described later in this document), uploaded as a PDF copy to the mycourses Project 1 Report drop box (PDF only), due: Monday, September 27, 2021, 11:59 PM.
    b. The Project 1 database copy, uploaded to the mycourses Project 1 Database drop box, due: Monday, September 27, 2021, 11:59 PM.
    c. NOTE: Due to the size of the files submitted, the mycourses Project 1 Report dropbox is configured to only keep one submission, therefore if you complete 3 submissions, only the files included with the last submission are kept. However, a submission is one or more files, therefore all required Project 1 files must be uploaded simultaneously as one submission to the mycourses dropbox.

Revision History:

V14 R1	Updates for EE520 | EE 620 by: Mark A. Indovina
V13 R2	Updates for EE520 | EE 620 by: Mark A. Indovina
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V8 R1	Updates for EE520 | EE 620 by: Mark A. Indovina
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V6 R1	Diffusion region extensions and other updates for EE520 | EE 620 by: Mark A. Indovina
V5 R2	Updates for EE520 | EE 620 by: Mark A. Indovina
V5 R1	Updates for EE520 | EE 620 by: Mark A. Indovina
V4 R1	Updates for EE520 | EE 620 by: Mark A. Indovina
V3 R2	Updates for EE520 | EE 620 by: Mark A. Indovina
V3 R1	Updates for EE520 | EE 620 by: Mark A. Indovina
V2 R1	Updates for EE651 by: Mark A. Indovina
V1 R1	Original created by:

	Dorin Patru, PhD

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1. PROJECT DESIGN REQUIREMENTS

Using the Generic 45 nm process design kit (PDK), design a library of CMOS digital standard cells. The name of your library as previously created in EDA Tutorial 1 will be **userid_fml_lib**, where:

- userid stands for your Unix logon username
- **fml** stands for the initials of your **first**, **middle** and **last** names.

NOTE:
THE CELL LIBRARY AND CELL NAME CONVENTION SPECIFIED HEREIN IS MANDATORY FOR GRADING

During this project you will have to:

1. Draw the transistor level schematic of each gate; size transistors appropriately.
2. Analyze the time domain behavior of the gates using transient analysis. For simulation purposes, load the output node of each gate with a capacitance of 100 fF. Simulate for all specified input combinations.
3. Include labeled plots to document the functional behavior of the cell within the Functional Simulation Waveforms section of the datasheet; these plots are generated using extracted parasitic data from the layout.
4. Include the measured propagation delays and rise/fall time of the cell output within the timing section of the datasheet; propagation delays and rise/fall times are generated using extracted parasitic data from the layout.
5. Layout all required gates.
6. Create a symbol, and a Verilog® gate level primitive model for all required gates
7. Create a Project 1 Engineering Report (use template *EE520_EE620_tech_memo.doc* on mycourses**)** which includes: (i) Introduction; (ii) Discussion; (iii) Results section which includes a table of all timing data collected and any observations regarding the timing data; (iv) Conclusion; (v) Appendix which includes full datasheets for all required gates and cells.

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The following gates are mandatory for all students (cell names are MANDATORY):

1. Inverter: FML_INVX1 – redesign as necessary to meet all cell design guidelines herein and transistor sizes to meet your individual design specifications[1]
2. Inverter: FML_INVX2 or FML_INVX4[1]
3. Two input NAND gate: FML_NAND2X1
4. Two input NOR gate: FML_NOR2X1
5. Four Input, two-level complex logic function[1]: FML_AOI22X1 or FML_OAI22X1
6. 2-to-1 MUX[1]: FML_MUX2X1 or FML_TMUX2X1
7. Two input XOR[1]: FML_XOR2X1 or FML_XNOR2X1

Note: FML_INVX2 or FML_INVX4 is a NEW cell designed from scratch to the specifications described in this document; it is NOT a copy of the inverter, FML_INVX1, you created in EDA Tutorial 1.

Each student must also follow the INDIVIDUAL DESIGN SPECIFICATIONS described in this document. Individual Design Specifications are determined by decoding the assigned 6-bit code per requirements defined in Table 1. In addition, each gate will be designed per the CELL DESIGN GUIDELINES, and GENERAL STANDARD CELL LAYOUT GUIDELINES also described in this document.

Publish an engineering project report (use template *EE520_EE620_tech_memo.doc* on mycourses, details described in Section 5) and datasheets for each cell designed following the template datasheet for each gate, as shown in the document:

mai_ee520_ee620_proj1_cell_datasheet_template.doc

The datasheet template is posted on mycourses. Print to PDF and upload your report to Project 1 drop box on mycourses. No printed version is necessary for the instructor. Your final report must be ONE file containing all datasheets and a suitable cover sheet.

If you plan to print a hardcopy for yourself, you may want to change the black background to white before sending to the printer (instructions shown below). Do not change the background to white for the PDF version of your report.

[1] INDIVIDUAL DESIGN SPECIFICATIONS are determined by decoding the assigned 6-bit code per requirements defined in Table 1.

2. INDIVIDUAL DESIGN SPECIFICATIONS

NAME: _____ Bit Code: _____
B5/B4/B3/B2/B1/B0

Table 1 Individual Design Specifications

Bit	Value='1'	Value='0'	Comments
B5	Inverter X4	Inverter X2	The Inverter X2[2] (X2 Drive Strength) is designed using PMOS and NMOS transistors that are double in width, i.e. (2*W), with W defined per B3 & B2[3]; X4 Drive Strength has 4*W
B4	XNOR	XOR	Defines the type of the XOR gate to be implemented
B3	12/2	8/2[4]	Defines the W/L ratio of the NMOS transistors; the final size MUST be in terms of L_{min}
B2	2xB3	1xB3	Defines the W/L ratio of the PMOS transistors; the final size MUST be in terms of L_{min} Note: PMOS size is defined as a multiple of the W/L ratio of the NMOS transistors; L is always drawn as $L_{min.}$
B1	AOI (4 input)	OAI (4 input)	Defines the type of the complex gate to be implemented Where: A ~ AND O ~ OR I ~ Invert
B0	Transmission Gate 2-to-1 MUX (FML_TMUX2X1)	CMOS 2-to-1 MUX (FML_MUX2X1)	Defines the type of the MUX to be implemented

[2] A gate with X2 drive strength should have essentially the same rise/fall time while driving a capacitance of 2C farads as that of a gate with X1 drive strength driving a capacitance of C farads.
[3] The sizes defined in B2 and B3 are the transistor sizes of your Inverter X1 or reference Inverter.
[4] See section 3 A)c for more details on transistor sizing.

3. STANDARD CELL CIRCUIT DESIGN GUIDELINES

A) Target Process:
   a. Generic 45 nm PDK
   b. Transistors will be drawn with L_{min} as 45 nm
   c. Due to L_{min} being 45 nm, λ rules will not apply to transistors
      i. $W/L = 8/2 = 4 \approx 4*L_{min}/L_{min}$ = 180 nm /45 nm
      ii. $W/L = 16/2 = 8 \approx 8*L_{min}/L_{min}$ = 360 nm /45 nm
      iii. $W/L = 32/2 = 16 \approx 16*L_{min}/L_{min}$ = 720 nm /45 nm
      iv. $W/L = 64/2 = 32 \approx 32*L_{min}/L_{min}$ = 1440 nm /45 nm
      v. $W/L = 128/2 = 64 \approx 64*L_{min}/L_{min}$ = 2880 nm /45 nm
      vi. $W/L = 12/2 = 6 \approx 6*L_{min}/L_{min}$ = 270 nm /45 nm
      vii. $W/L = 24/2 = 12 \approx 12*L_{min}/L_{min}$ = 540 nm /45 nm
      viii. $W/L = 48/2 = 24 \approx 24*L_{min}/L_{min}$ = 1080 nm /45 nm
      ix. $W/L = 96/2 = 48 \approx 48*L_{min}/L_{min}$ = 2160 nm /45 nm
      x. $W/L = 192/2 = 96 \approx 96*L_{min}/L_{min}$ = 4320 nm /45 nm
   d. For all other items such as wiring, routing grid
      i. λ = 25 nm or 0.025 μm
      ii. Detailed layout guidelines are discussed in Section 4

B) Using the *delay* function the ADE calculator, document Propagation Delay for the circuit schematic first, and then using parasitic data extracted from the layout for the following paths – see *mai_delay_def.pdf* for details on how to measure propagation delay (note that this section also defines the MANDATORY pin names of your cells):
   1) For the Inverter (FML_INVX1 and FML_INVX2 or FML_INVX4):
      a. A → Y ↑
      b. A → Y ↓
   2) For the NAND2:
      a. A → Y ↑
      b. A → Y ↓
      c. B → Y ↑
      d. B → Y ↓
   3) For the NOR2:
      a. A → Y ↑
      b. A → Y ↓
      c. B → Y ↑
      d. B → Y ↓

4) For the AOI22:
    a. A0 → Y ↑
    b. A0 → Y ↓
    c. A1 → Y ↑
    d. A1 → Y ↓
    e. B0 → Y ↑
    f. B0 → Y ↓
    g. B1 → Y ↑
    h. B1 → Y ↓
5) For the OAI22:
    a. A0 → Y ↑
    b. A0 → Y ↓
    c. A1 → Y ↑
    d. A1 → Y ↓
    e. B0 → Y ↑
    f. B0 → Y ↓
    g. B1 → Y ↑
    h. B1 → Y ↓
6) For the MUX2:
    a. A → Y ↑
    b. A → Y ↓
    c. B → Y ↑
    d. B → Y ↓
    e. S → Y ↑
    f. S → Y ↓
7) For the XOR2:
    a. A → Y↑
    b. A → Y↓
    c. B → Y↑
    d. B → Y↓

C) Using the *risetime* and *falltime* functions the ADE calculator, document Rise and Fall times for the cell output pin for the circuit schematic first, and then using parasitic data extracted from the layout for the same paths as used for Propagation Delay – see *mai_delay_def.pdf* for details on how to measure rise and fall times.
   a. For rise time use (see Figure 1):
      i. Initial Value 0 and Final value 1
      ii. Percent Low = 20 %
      iii. Percentage high = 80%
   b. For fall time use (see Figure 2):
      i. Initial Value 1 and Final Value 0
      ii. Percent Low = 80 %
      iii. Percentage high = 20%

D) For simulation purposes, VDD = 1.0v ; VSS = 0.0v

E) Use 100 ps for the input waveform rise and fall times when simulating with Spice (Cadence Spectre).

F) For simulation purposes, load the output of node each gate with a capacitance of 100 fF.

G) As taught in EDA Tutorial 1, you MUST use a test schematic to simulate your cells.

H) Cell port/label/pin names are defined above in section B), and MUST MATCH on all views (symbol, schematic, layout, Verilog®, functional). Industry standard is to use UPPERCASE letters for standard cell pin names and you must follow the cell naming conventions and pin names noted in the assignment handout. Note that use of any special characters in pin names will cause errors in downstream tools.

I) The tools are sensitive to cell view names (such symbol, schematic, layout, Verilog®, functional). DO NOT CHANGE the cell view names or you will have trouble in later projects.

J) You MUST simulate your cells to check functionality to confirm your circuit design works as desired.

K) Design rules and other information related to the Generic 45 nm PDK can be found in the file *GPDK045_PDK_DESIGN_RULES.pdf* on mycourses.

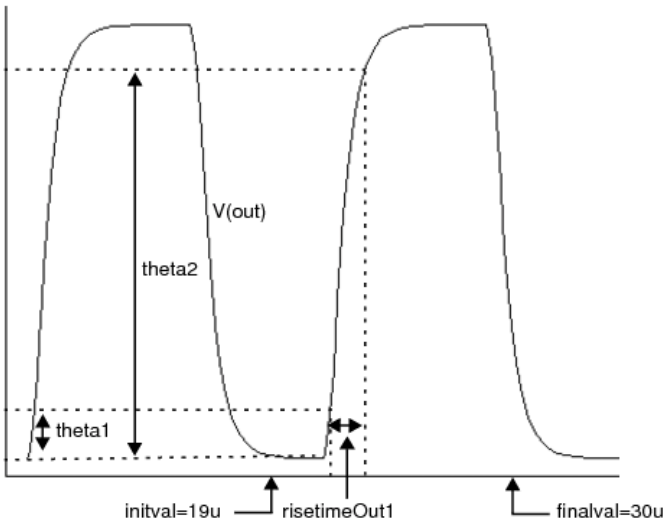

Figure 1 ADE Rise Time Calculation

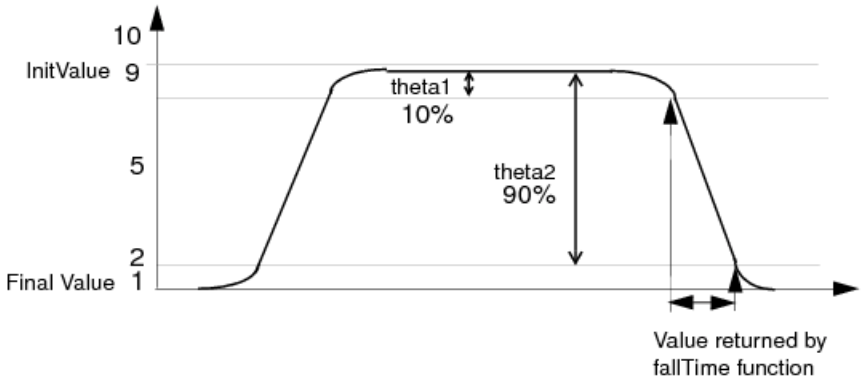

Figure 2 ADE Fall Time Calculation

4. STANDARD CELL LAYOUT GUIDELINES

1. λ = 25 nm or 0.025 µm
2. Required wiring tracks
    a. 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
3. As taught in EDA Tutorial 1, all cells will be designed starting with the parameterized layout template.
    a. PR boundary Height is 1.71 µm.
    b. PR boundary Width is a multiple of 8 lambda (8 λ = 0.2 µm).
    c. 0,0 Origin of cell at lower left hand corner cell PR boundary.
4. nMOS at bottom and pMOS at top.
5. All gates include well and substrate contacts (these are included within the cell template).
6. If a transistor will not fit in the space allotted due to its channel width, use the multi-finger technique shown in Figure 3, Figure 4, and Figure 5 to draw the device. Note that if you use multi-finger transistors, for proper simulation and LVS, you need to define the number of fingers drawn as a parameter setting of the appropriate transistors in the schematic view.
7. I/O and VDD / VSS Pins:
    a. I/O Pins (and labels) on Metal 2 | Pin only.
    b. VDD / VSS Pins (and labels) on Metal 1 | Pin only.
    c. VDD at top, and VSS at bottom of cell.
    d. For labeling purposes, recall the special treatment of VDD / VSS as these are global signals VDD! and VSS!
8. Top Level Clock lines:
    a. Should be at least 10 λ = 0.25 µm
9. Cells must be designed so that they can abut horizontally without introducing design rule violations - test that your cells can be abutted in rows by placing multiple cells (of various types) in rows in a test layout and running DRC.
10. Cells must be designed so that they can be flipped and abut vertically VSS to VSS without introducing DRC or LVS violations - test that your cells can be flipped and abutted in rows by placing multiple cells (of various types) in a test schematic and rows in a test layout and running DRC and LVS.
11. Cells designs will be restricted to using the following layers: (i) diffusion (any direction, minimal length); (ii) Poly (any direction); (iii) M1 (any direction); and (iv) M2 (vertical) for wiring exclusively.
    a. Note that the auto router used in later labs will be routing using M2 (vertical direction). Any deviation from the strict direction [horizontal / vertical] rules on layers M2 and above and the router WILL create shorts.

12. Cells must be prepared for use with routing tools:
    a. Finish wiring at Metal 2 | Drawing only.
    b. As noted earlier, all I/O ports must have pins and labels on M2|Pin only.
    c. As noted earlier, VDD / VSS Pins must have pins and labels on Metal 1 | Pin only.
    d. Per Figure 6, to help guide the routing tools and minimize DRC violations, all I/O ports should fall within the PR Boundary and in the center of horizontal (x-direction) and vertical (y-direction) routing tracks or channels with a pitch of 8 λ.
        i. A cell is designed using an 8 λ grid and has the first possible I/O port location in the center of the first full vertical routing track - 4 λ inside the left edge of the PR Boundary.
        ii. The final width of the cell PR Boundary must be a multiple of 8 λ
    e. As shown in Figure 6, routing is done in the channels between cell rows.

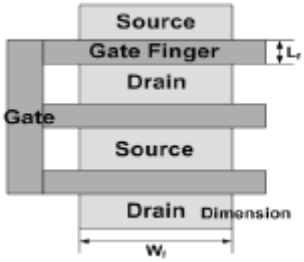

Figure 3 Multi-finger MOS Transistor

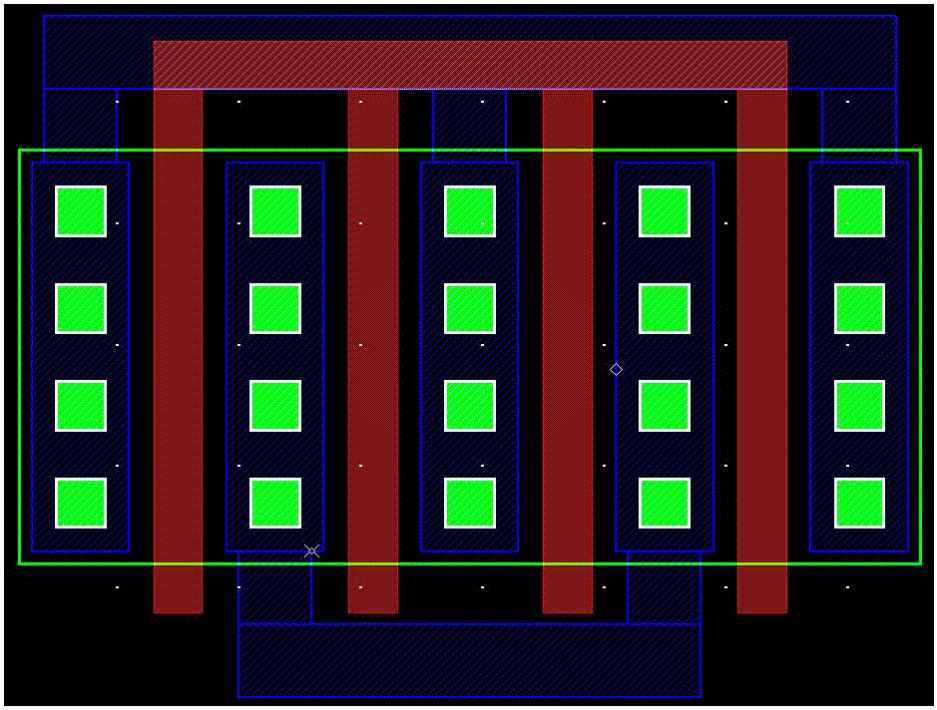

Figure 4 Wired Multi-finger MOS Transistor (layers colors to not match the Generic 45 nm PDK)

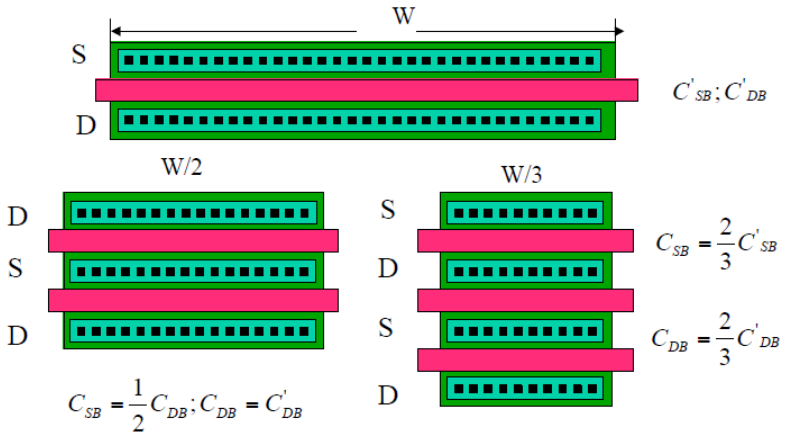

Figure 5 Multi-finger MOS Transistor Examples

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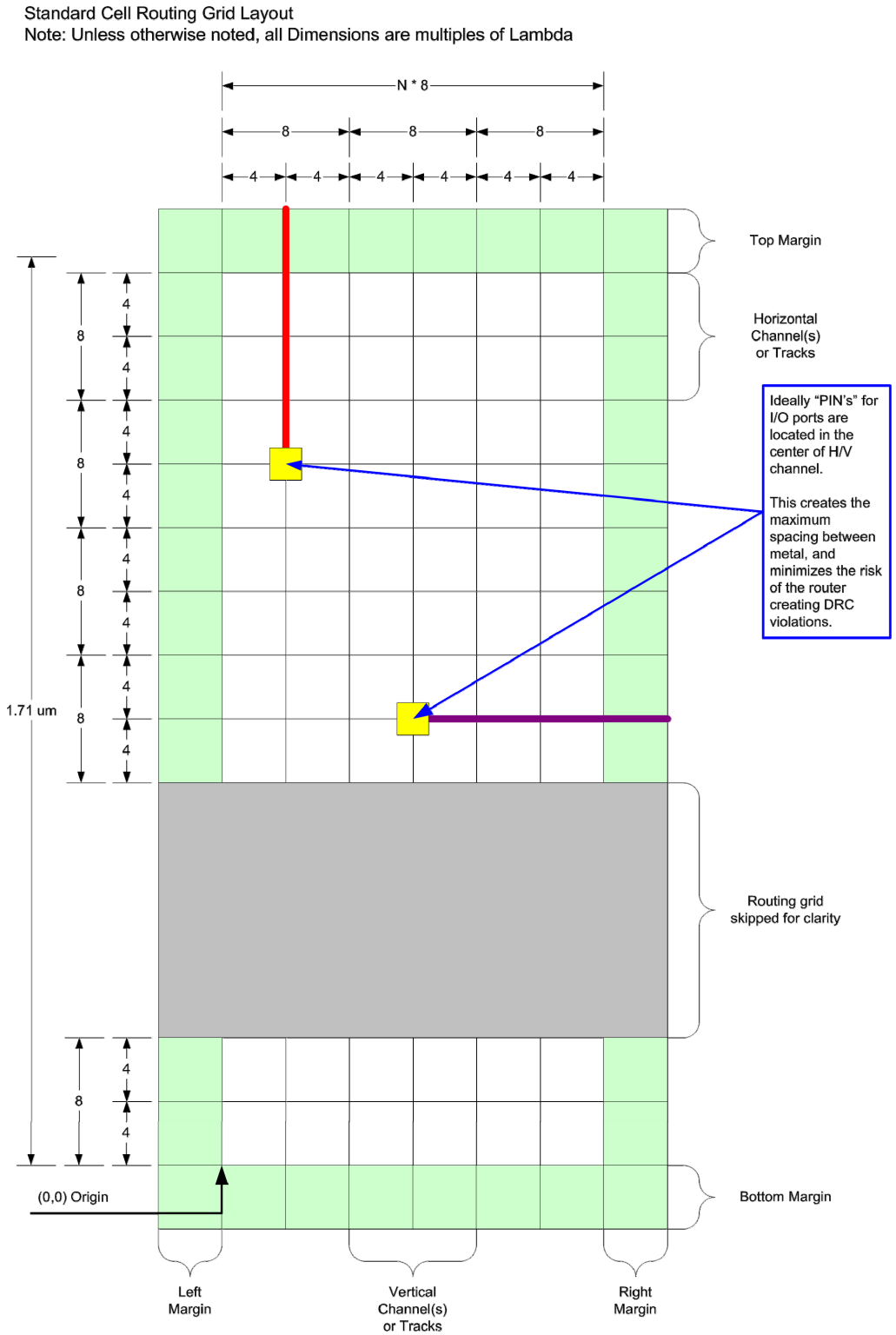

Figure 6 Routing Grid Layout

13. Utilize the Virtuoso display grid to make drawing layout objects with respect to the routing grid easier as shown in Figure 7.
14. Transistors must be well formed with appropriate contacts as shown in Figure 8.
15. All cells must DRC and LVS clean (NO WARNINGS or ERRORS).

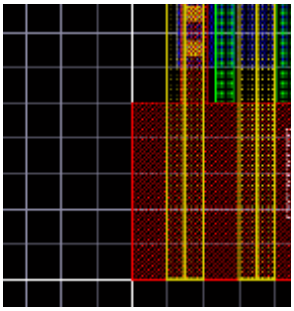

Figure 7 Cutout of Layout Window Showing 4 λ Display Grid

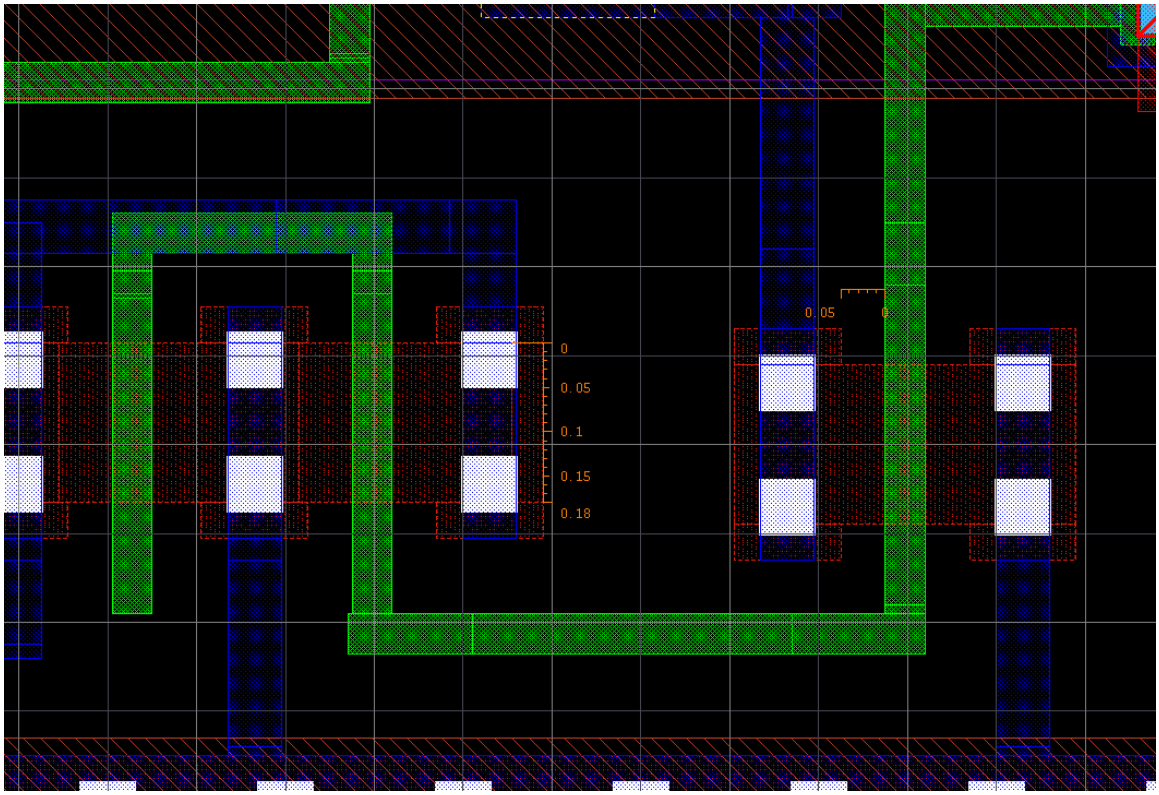

Figure 8 Diffusion Region Extensions (Hats) for contacts

5. EXAMPLE DATASHEET

Library Name:	
Cell Name:	
Function/Truth Table:	
Propagation Delay (path based):	
Output Rise Time (path based):	
Output Fall Time (path based):	
Layout Height:	
Layout Width:	
Layout Area:	
Symbol with Port Names:	
Schematic:	
Layout:	

Verilog Model:
Functional Simulation Waveforms
Comments/Notes:

Figure 9 Example Cell Date Sheet

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5. PROJECT GRADING

As noted earlier, the grade for this project will be based on:

1. Completion of the EDA Tutorial 1 assignment by indicated date and time - No Exceptions!
2. Completion of the Project 1 assignment by indicated date and time - No Exceptions!
3. A 5 min. oral presentation and defense of your work as organized by the instructor and TA during the week Project 1 is due. Cell(s) will be picked at random and you will be asked to run DRC and LVS checks during your presentation.
4. The Project 1 Engineering Report (PDF only) uploaded to the mycourses Project 1 Report dropbox due: Monday, September 27, 2021, 11:59 PM. Your report will include the following sections: (i) Introduction; (ii) Discussion; (iii) Results section which includes a tables and graphs of ALL TIMING DATA collected and discuss any observations regarding the timing data; (iv) Conclusion; (v) Appendix which includes full datasheets for all required gates and cells. The report and all datasheets are to be submitted as one merged file.
5. For requirement 4 (iii):
    a. You are to provide tables for the timing data, and also graphs of the timing data as follows:
        i. Rise propagation delay for all cells, for all paths, for pre- and post-layout timing data, on one graph
        ii. Fall propagation delay for all cells, for all paths, for pre- and post-layout timing data, on one graph
        iii. Rise time for all cells, for all paths, for pre- and post-layout timing data, on one graph
        iv. Fall time for all cells, for all paths, for pre- and post-layout timing data, on one graph
    b. The graphs will help you discuss any observations you may find regarding the timing data. Note that you can use Matlab, or the graphing tools available in most spreadsheet tools to create suitable graphs.
6. On a copy of your database uploaded to mycourses Project 1 Database dropbox per instructions found in *mai_520_620-database-upload.pdf* due: Monday, September 27, 2021, 11:59 PM.

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Table 2 Project 1 Grading:

EDA Tutorial 1 Score	5%
All Cell Schematics Score	20%
All Cell Layouts Score	20%
All Cell Simulation Results Score	20%
Project 1 Engineering Report including All Cell Datasheets and Timing Table Score (Including readability, grammar, spelling, format)	25%
Defense Score	5%
Overall Quality Score	5%
Late Deduction	0%
Graded Total	**100%**

NOTE: Due to the size of the files submitted, the mycourses Project 1 Report dropbox is configured to only keep one submission, therefore if you complete 3 submissions, only the files included with the last submission are kept. However, a submission is one or more files; therefore all required Project 1 files must be uploaded simultaneously as one submission to the mycourses dropbox.

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6. APPENDIX

Please use the following instructions if you are going to print a hardcopy of your data sheet(s).

Using ALT-PRT_SCR, copy/paste the window containing the schematic into a word file.

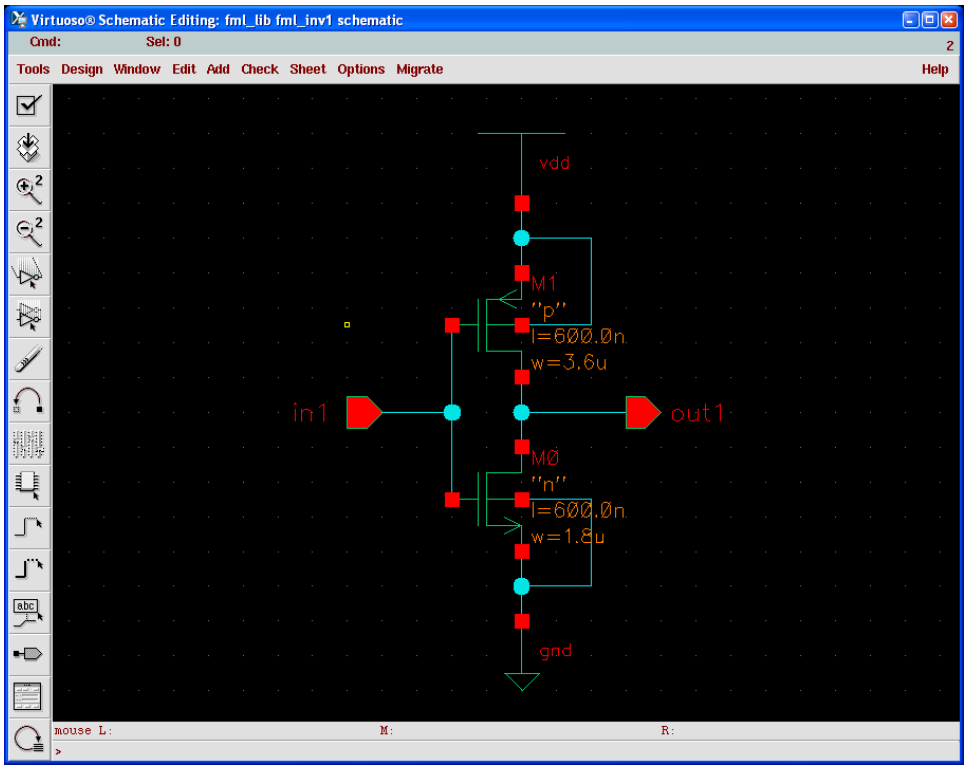

Figure 10 Original Composer Schematic Image

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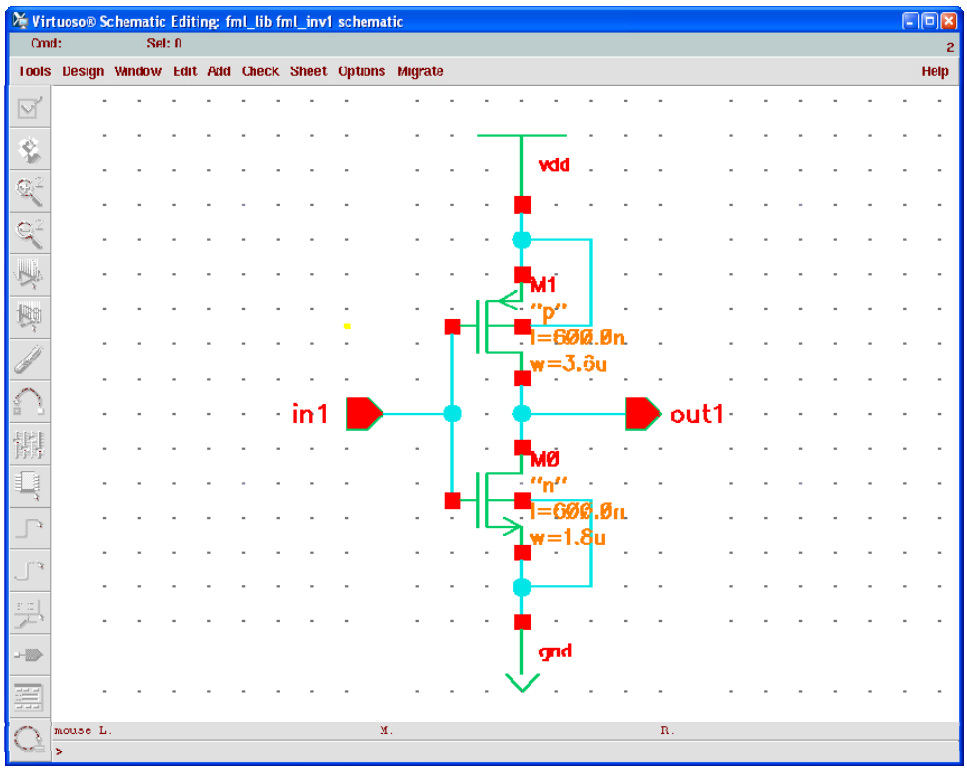

Figure 11 Color Modified Composer Schematic Image

Once placed into your word file, right click on the image and select SHOW PICTURE TOOLBAR. Once this opens, towards the right hand side there is a command SELECT TRANSPARENT COLOR. Click on it and then click anywhere on the black background in your window. See the result above.