EE520 | EE620 Project 2 Assignment

Assigned: Monday, October 04, 2021

Project 2 Due: Monday, November 01, 2021, 11:59 PM

The grade for this project will be based on:

1. Completion of the EDA Tutorial 2 assignment by indicated date and time - No Exceptions!
2. Completion of the Project 2 assignment by indicated date and time - No Exceptions!
3. A ~10 min. oral presentation and defense of your work, which you will give during lab as organized by the instructor and TA during the week the Project 2 is due, using the presentation template *mai_ee520_ee620_proj2_def_template.ppt* on mycourses. Your Project 2 Presentation (PPT only) is due online **1 hour before class on the day of your presentation** - No Exceptions!
4. The following files uploaded to the mycourses Project 2 Report dropbox:
    a. The Project 2 engineering report (use template *EE520_EE620_tech_memo.doc* on mycourses, engineering report details are described later in this document), uploaded as a PDF copy to the mycourses Project 2 Report drop box (PDF only), due: Monday, November 01, 2021, 11:59 **PM**.
    b. The Project 2 database copy, uploaded to the mycourses Project 2 Database drop box, due: Monday, November 01, 2021, 11:59 **PM**.
    c. NOTE: Due to the size of the files submitted, the mycourses Project 2 Report dropbox is configured to only keep one submission, therefore if you complete 3 submissions, only the files included with the last submission are kept. However, a submission is one or more files, therefore all required Project 2 files must be uploaded simultaneously as one submission to the mycourses dropbox.

Revision History:

V14 R2	Updates for EE520 | EE620 by: Mark A. Indovina
V14 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V13 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V12 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V11 R6	Updates for EE520 | EE620 by: Mark A. Indovina
V11 R5	Updates for EE520 | EE620 by: Mark A. Indovina
V11 R4	Updates for EE520 | EE620 by: Mark A. Indovina
V11 R3	Updates for EE520 | EE620 by: Mark A. Indovina
V11 R2	Updates for EE520 | EE620 by: Mark A. Indovina
V11 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V10 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V9 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V8 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V7 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V6 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V5 R3	Updates for EE520 | EE620 by: Mark A. Indovina
V5 R2	Updates for EE520 | EE620 by: Mark A. Indovina
V5 R1	Update BSSUM wiring for EE520 | EE620 by: Mark A. Indovina
V4 R4	Updates for EE520 | EE620 by: Mark A. Indovina
V4 R3	Updates for EE520 | EE620 by: Mark A. Indovina

V4 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V3 R3	Updates for EE520 | EE620 by: Mark A. Indovina
V3 R2	Updates for EE520 | EE620 by: Mark A. Indovina
V3 R1	Updates for EE520 | EE620 by: Mark A. Indovina
V2 R1	Updates for EE651 by: Mark A. Indovina
V1 R1	Original created by: Dorin Patru, PhD

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1. INTRODUCTION

1. Follow the all library and cell naming conventions for Project 1.
2. Follow all design and layout guidelines as noted in the Project 1 handout, including unique requirements per your assigned "bit code".
3. Cell port/label/pin names can only use letters and numbers, must start with a letter, are case sensitive and MUST MATCH on all views (symbol, schematic, layout, Verilog, functional). Industry standard is to use UPPERCASE letters for standard cell pin names. Note that use of any special characters in pin names will cause errors in downstream tools.

NOTE:
THE CELL LIBRARY AND CELL NAME CONVENTION SPECIFIED HEREIN IS MANDATORY FOR GRADING

A WARNING BEFORE YOU START PLACE AND ROUTE

Before you start any place and route, please take time to look at the pad frame cell, placement of I/O signals, measure things, and preplan by sketching a floor plan or two of how you're going to approach the placement and routing of your hierarchal cells.

If you choose to ignore this warning there is a 99.5% chance that you WILL be ripping up and redoing work once you start pulling your final design together.

2. PROJECT DESIGN REQUIREMENTS

1. Enhance your standard cell library with the following gates/cells:
   a. A TIELO pull-down cell (library cell FML_TIELO); see Figure 1
   b. A TIEHI pull-up cell (library cell FML_TIEHI); see Figure 2
   c. A rising edge triggered D Flip Flop, DFF (library cell FML_DFFX1), and using two-phase non-overlapping clocks, per the MUX2 Implementation as shown in handout *mai_proj2_req_update.pdf*. The result is a circuit with 3 inputs, and 2 outputs.
2. Using gates from your standard cell library capture the schematic of a Full Adder (FA) in a new cell at one hierarchical level (library cell FML_FA). Place the cells, and auto-route following steps similar to those taught in EDA Tutorial 2. The result is a circuit with 3 inputs, and 2 outputs. Note the following exceptions to EDA Tutorial 2:
   a. When placing FML_FA, you must calculate the PR boundary to be the same width and height of the placed cell so that the final FML_FA has the **same height as your standard cells** (without routing channels), and can abut cleanly with your standard cells, see Figure 3.
   b. The I/O pins must be placed as follows:
      i. Ideally, they should be placed on M2 exactly like your standard cells
      ii. The alternative is to place the I/O pins on M4
   c. Regardless of your I/O pin layer choice, you are restricted to using M2, M3, and M4 for routing these cells
   d. VDD and VSS are on M1
3. For the DFF, and FA, you must create all cell views as required in the Project 1 handout. Note: the Verilog module for your DFF is coded as a D-type master-slave flip-flop modeled using gate level primitives.
4. Document Propagation Delay for the following paths:
   a. For the FA:
      i. A → S↑
      ii. A → S↓
      iii. B → S↑
      iv. B → S↓
      v. CI → S↑
      vi. CI → S↓
      vii. A → CO↑
      viii. A → CO↓
      ix. B → CO↑
      x. B → CO↓
      xi. CI → CO↑
      xii. CI → CO↓

b. For the DFF (see mai_ff_clock_constraint_measure.pdf):
    i. Ø1 → Q↑
    ii. Ø1 → Q↓
    iii. Ø1 → QN↑
    iv. Ø1 → QN↓
    v. Ø1 → minimum pulse width high
    vi. Ø2 → minimum pulse width high
    vii. Ø1↓ → Ø2↑ minimum guard time
    viii. A sample testbench is provided to measure minimum pulse width and minimum guard time, see **DFFX1_TESTBENCH_MINPW.pdf**

5. Using gates from your standard cell library capture the schematic of a Boundary Scan Cell (BSC) in a new cell at one hierarchical level (library cell FML_BSC). The schematic of a typical boundary scan cell is shown in Figure 11. Place the cells, and auto-route following steps similar to those taught in EDA Tutorial 2. See the file mai_boundary_scan_overview.pdf for more Boundary Scan design details. Note the following exceptions to EDA Tutorial 2:
    a. Note that when placing FML_BSC, you must calculate the PR boundary to be the same width and height of the placed cell so that the final FML_BSC has the **same height as your standard cells** (without routing channels), and can abut cleanly with your standard cells, see Figure 4.
    b. The I/O pins must be placed as follows:
        i. If possible, they should be placed on M2 exactly like your standard cells
        ii. The alternative is to place the I/O pins on M4 – this might be a better choice for most students
    c. Regardless of your I/O pin layer choice, you are restricted to using M2, M3, and M4 for routing these cells
    d. VDD and VSS are on M1 – manually place the these pins on the VDD and VSS rails
6. Using gates from your standard cell library capture the schematic of a 50-bit Boundary Scan Register (BSR) in a new cell at one hierarchical level (library cell FML_BSR50) – see Figure 10 and Figure 12 for reference. When connecting your BSR, note that BSR bit [49] is SI (scan in); BSR bit [0] is SO (scan out). Place all cells at one hierarchical level, and auto-route following the steps in EDA Tutorial 2. The schematic can be greatly simplified if you use the Composer iterated instance feature, see Figure 6. A sample testbench is provided, see **BSR50_TESTBENCH.pdf**

7. Using gates from your standard cell library capture the schematic of a 16-bit Carry Select Adder (ADD16) in a new cell at one hierarchical level (library cell FML_ADD16). A carry select adder 4-bit slice is shown in Figure 5. Your 16-bit Carry Select Adder will be designed using FOUR SLICES. Place all cells at one hierarchical level, and auto-route following the steps in EDA Tutorial 2. A sample testbench is provided, see **ADD16_TESTBENCH.pdf**
8. Instantiate the ADD16 and the BSR50 in a new cell BSSUM at one hierarchical level (library cell FML_BSSUM). Wire the BSR50 and ADD16 as follows:
    a. Connect BSR output bit [49] to ADD16 carry in bit
    b. Connect BSR output bits [48:33] to ADD16 input bits B[15:0]
    c. Connect BSR output bits [32:17] to ADD16 input bits A[15:0]
    d. Connect the carry-out of ADD16 to BSR input [16]
    e. Connect the 16 sum outputs of ADD16 to BSR inputs [15:0]
    f. Connect unused BSR inputs to VDD or VSS using your TIEHI and TIELO cells, the bonding is your choice as long as your choice is useful during simulation.
    g. Place all cells at one hierarchical level, and auto-route following the steps in EDA Tutorial 2.
    h. A sample testbench is provided, see **BSSUM_TESTBENCH.pdf**

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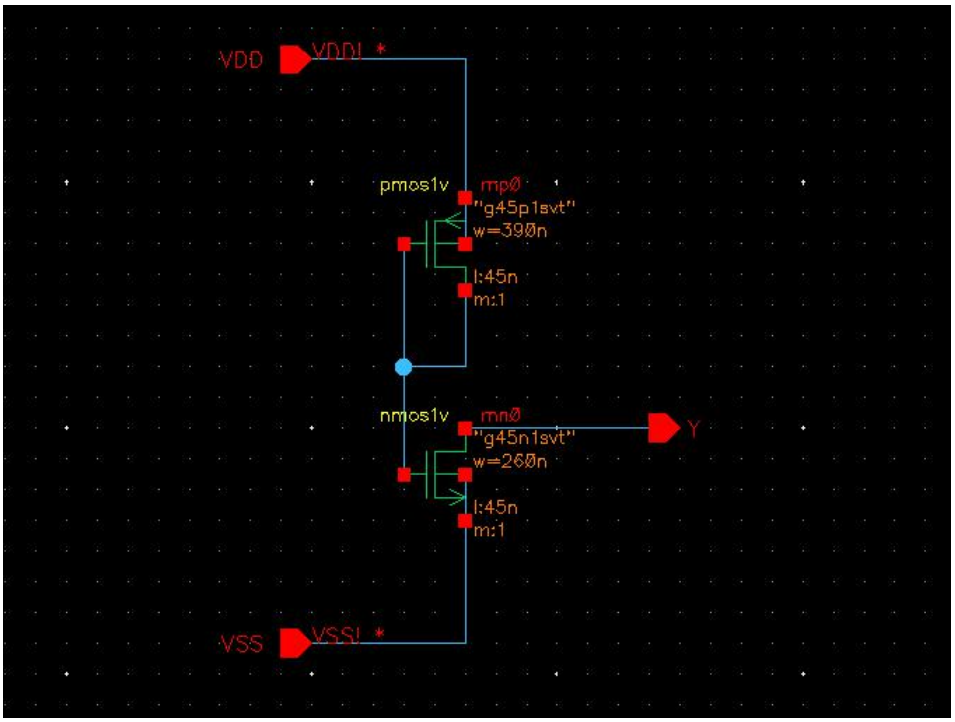

Figure 1 TIELO pull-down cell

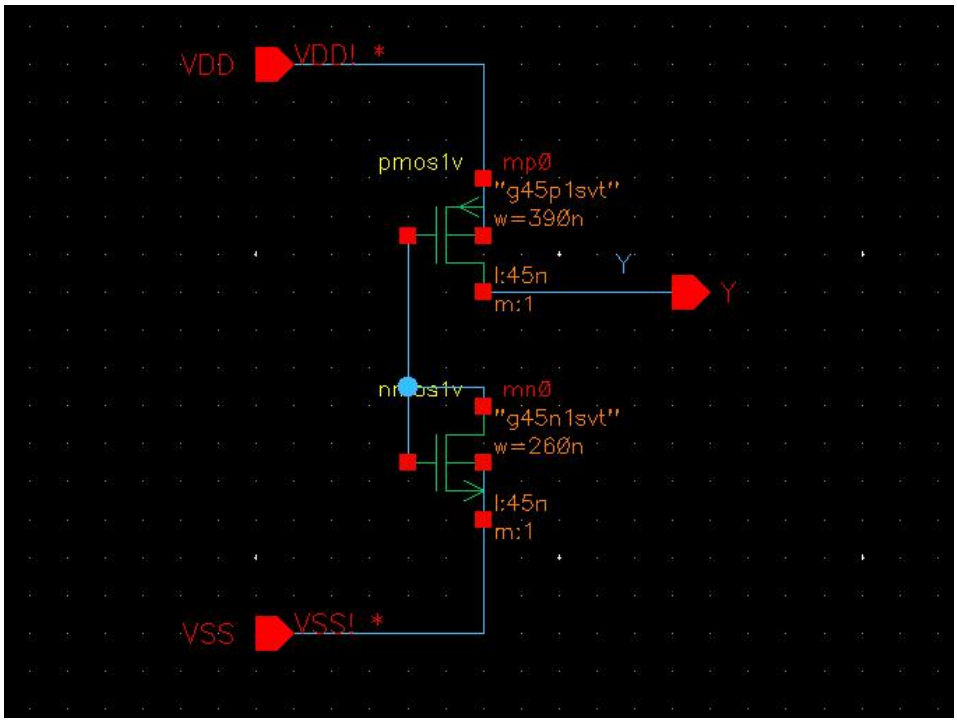

Figure 2 TIEHI pull-up cell

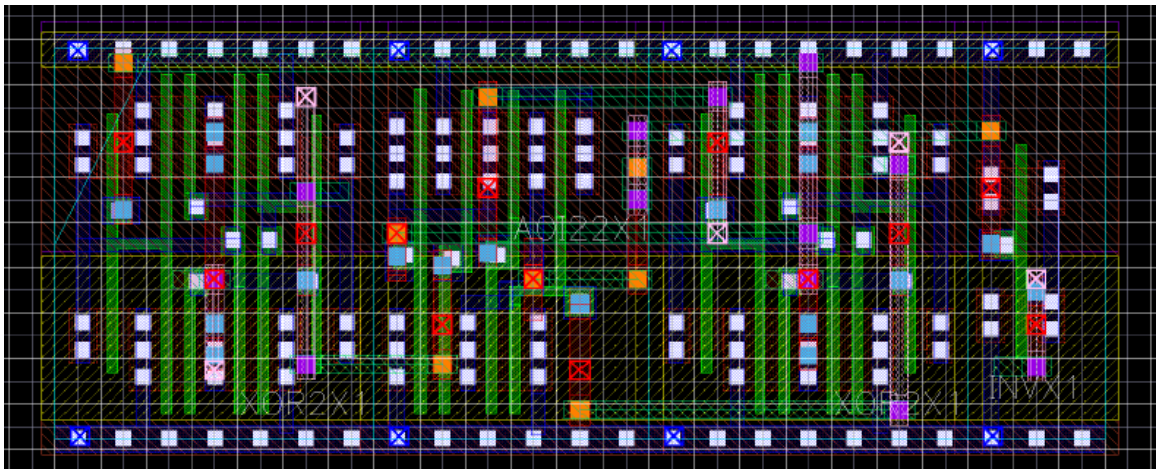

Figure 3 Example place and route of Full Adder (FA)

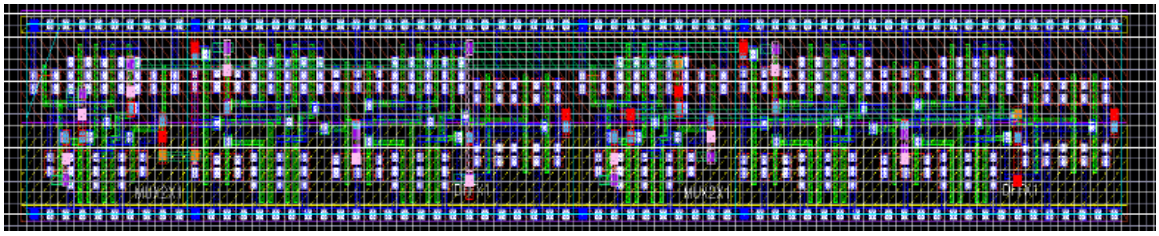

Figure 4 Example place and route of Boundary Scan Cell (BSC)

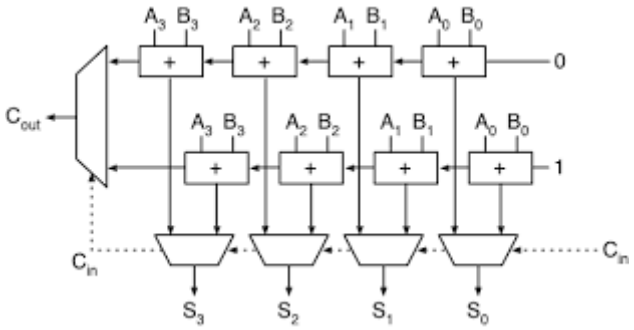

Figure 5 Generic Carry Select Adder 4-bit Slice

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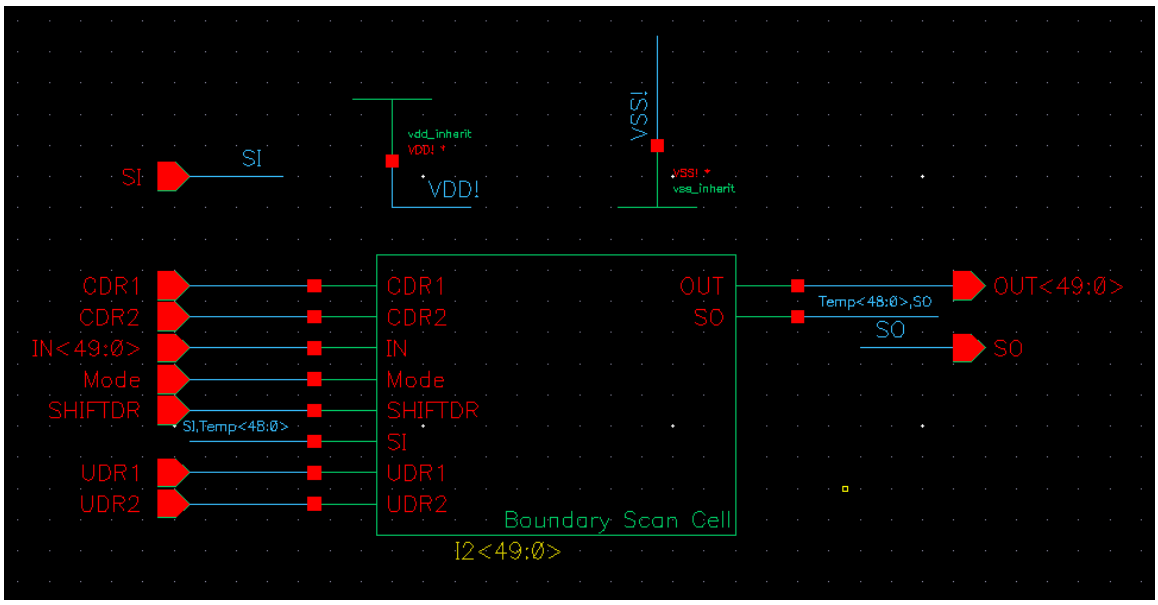

Figure 6 Iterated Instance Example

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9. Finally, instantiate both your BSSUM cell and the quarter pad frame cell provided into a new cell, BSTEST (library cell FML_BSTEST). Connect all signals to the I/O pads using the appropriate wiring layers; your standard cell pins are on M2, you can use M2 and up; you MUST honor the defined wiring direction.
10. Your DFF requires two-phase non-overlapping clocks, and the two-phase non-overlapping clocks are brought into your chip using I/O pads as follows:
    a. ClockDR:
        i. Ø1 ~ CDR1
        ii. Ø2 ~ CDR2
    b. UpdateDR:
        i. Ø1 ~ UDR1
        ii. Ø2 ~ UDR2
11. Take care with the placement of cells as you build higher level blocks. Since these cells will eventually be stitched together as larger blocks and placed in the quarter pad frame provided, poor early placement will eventually cause your final cell to not fit into the area allotted. You have been warned!
12. Build your blocks so that you can efficiently strap your rows with VDD / VSS as shown in Figure 7 (layer colors in this example are not correct). Note that left / right side power strapping should be at least 30 λ wide. The final connections from the straps to the VDD / VSS pads should be at least 40 λ wide.

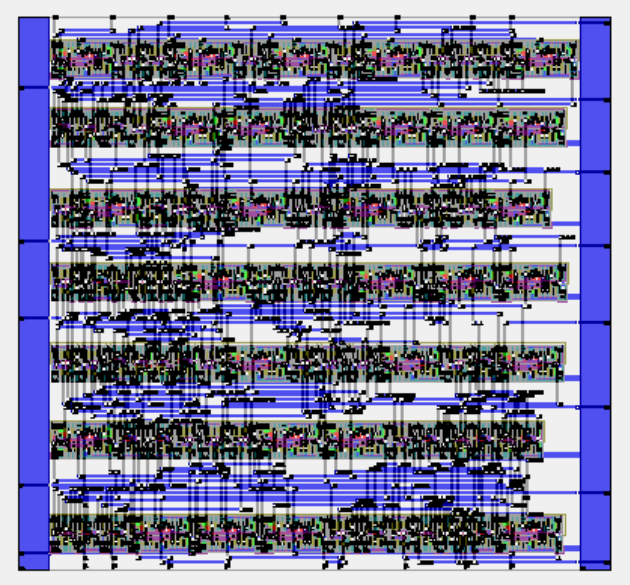

Figure 7 Example Standard Cell Block Layout

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13. When routing cells follow these guidelines:
    a. VDD and VSS pins must be on Metal 1 for all your blocks.
    b. **You are not routing VDD and VSS**. After generating the initial placement as taught in Tutorial 2, manually place the VDD and VSS pins and associated labels on top of a standard cell VDD / VSS bus. For cells with multiple rows manually insert the power strapping (as noted in section 12 above) before routing. To efficiently constrain the router, it may be necessary to move the power strapping outside the Bounding Box; as necessary, you will need to account for the power strapping in your area calculations.
    c. Signal pins should be on a vertical routing layer.
    d. Since you will be using these cells with other routed cells and the quarter pad frame cell, optimize the pin placement (top, bottom, left, and right) to minimize routing when you place cells together as you build larger blocks.
    e. Suggested routing channel height:
        i. 2 tracks top and bottom
        ii. 4 tracks between rows
    f. Connections to the IO pad must come strait into the pad port – you cannot route any signals over the pad structures.
    g. For BSTEST LVS to pass you will need to add pins and labels to the IO pads that match your schematic signal names connected to the pads (use the same names).
14. Due to the possibility of limited space in the quarter pad frame cell, floor plan your blocks to leave adequate space on the left and right sides of your rows of cells for power strapping.
15. Cells must be designed so that they can abut horizontally (including flipped horizontally) without introducing design rule violations - test that your cells can be abutted in rows by placing multiple cells (of various types, including flipping each horizontally) in rows in a test layout and running DRC.
16. Cells must be designed so that they can be flipped and abut horizontally VSS to VSS without introducing DRC or LVS violations - test that your cells can be flipped and abutted in rows by placing multiple cells (of various types) in a test schematic and rows in a test layout and running DRC and LVS.
17. All interconnections within the cell will be made per the requirements defined in the Project 1 handout.
18. All cells, including routed cells, must DRC and LVS clean (no WARNINGS or ERRORS).
19. With the exception of ADD16, BSR50, BSSUM, BSTEST, All cells MUST be simulated with extracted parasitic data to check functionality post route.

3. PROJECT GRADING

As noted earlier, the grade for this project will be based on:

1. Completion of the EDA Tutorial 2 assignment by indicated date and time - No Exceptions!
2. Completion of any required standard cell updates from Project 1 by indicated date and time - No Exceptions!
3. Completion of the Project 2 assignment by indicated date and time - No Exceptions!
4. A ~10 min. oral presentation and defense of your work, which you will give during lab as organized by the instructor and TA during the week the Project 2 is due, using the presentation template *mai_ee520_ee620_proj2_def_template.ppt* on mycourses. Your Project 2 Presentation (PPT only) is due online **1 hour before lab on the day of your presentation** - No Exceptions!
5. The Project 2 Engineering Report (use template *EE520_EE620_tech_memo.doc* on mycourses) (PDF only) uploaded to the Project 2 Report mycourses drop box, due online **Monday, November 01, 2021, 11:59 PM**. The project report MUST contain:
    a. A title page. At a minimum your name, course name, name of library described in the report.
    b. A second Design Constraints & Discussion section describing your library design constrains based on your individual "bit code". You should discuss how you approached designing your cells, including transistor sizing, etc. Include a tables and graphs of ALL TIMING DATA collected for all required cells from both projects (all cells from Project 1; only DFF, and FA for Project 2) and discuss any observations regarding the timing data. Comment here on any unfinished or work not verified.
    c. For item b:
        a. You are to provide tables for the timing data, and also graphs of the timing data as follows:
            i. Rise propagation delay for all cells, for all paths, for pre- and post-layout timing data, on one graph
            ii. Fall propagation delay for all cells, for all paths, for pre- and post-layout timing data, on one graph
            iii. Rise time for all cells, worst case measurement, for pre- and post-layout timing data, on one graph
            iv. Fall time for all cells, worst case measurement, for pre- and post-layout timing data, on one graph
        b. The graphs will help you discuss any observations you may find regarding the timing data. Note that you can use Matlab, or the graphing tools available in most spreadsheet tools to create suitable graphs.

d. A third Place & Route Cell section which includes the schematic view and description of each cell created using your library cells, i.e. your ADD16, BSR, BSSUM, and BSTEST cells.
e. A forth BSSUM Simulation section which includes labeled, detailed simulation waveforms for cell BSSUM**.**
f. A fifth Final Remarks & Conclusion section that covers a detailed summary of the project, a discussion of what went well, areas for improvement, and your overall thoughts on Project 1 and 2 and how you will utilize what you've learned as you design larger, more sophisticated digital systems.
g. An Appendix section which includes datasheets for ALL CELLS of your library you have created for Project 1 and Project 2. Include all data sheet data as specified in the Project 1 assignment handout, and include timing arc measurements and parasitic notes for the DFF, and FA cells only; for TIELO, TIEHI, ADD16, BSR, BSSUM, and BSTEST cells the data sheets will not include any timing arcs.
    a. **Note:** The Engineering Report Template and Datasheet Template are both Microsoft Word documents. The recommended approach would be to copy / paste the datasheet table from the Datasheet Template into the Engineering Report Template as necessary and use page breaks to properly format each cell datasheet to start on a new page.
h. You will be submitting a written report, and the quality of your work will be evaluated based on your ability to communicate what you designed to others. Please take care with your grammar, punctuation and style. Points WILL be docked for poorly written reports.
i. If you plan to print a hardcopy for yourself, make sure to change the black background to white before sending to the printer (instructions shown in Project 1 handout)

6. A copy of your database uploaded to the Project 2 Report mycourses drop box, per instructions found in *mai_520_620-database-upload.pdf* due: **Monday, November 01, 2021, 11:59 PM**.

Table 1 Project 2 Grading:

EDA Tutorial 2 Score	5%
Project 1 Feedback Updates Score	15%
All Cell Schematics Score	15%
All Cell Layouts Score	15%
All Cell Simulation Results Score (Except BSSUM)	15%
BSSUM Simulation Results Score	5%
Defense Score	5%
Project 2 Final Report Score (Including readability, grammar, spelling, format)	20%
Overall Quality Score	5%
Late Deduction	0%
Graded Total	**100%**

NOTE: Due to the size of the files submitted, the mycourses Project 2 Report dropbox is configured to only keep one submission, therefore if you complete 3 submissions, only the files included with the last submission are kept. However, a submission is one or more files, therefore all required Project 2 files must be uploaded simultaneously as one submission to the mycourses dropbox.

4. PROJECT PRESENTATION SUBMISSION

Create your presentation as indicated in Section 3 using PowerPoint and upload to the drop box on mycourses. No printed version is necessary for the instructor.

5. PROJECT REPORT SUBMISSION

Author your report as indicated in Section 3 (use template *EE520_EE620_tech_memo.doc* on mycourses), then print your final project report to PDF and upload to the drop box on mycourses. No printed version is necessary for the instructor. Your final report MUST be ONE PDF file containing ALL information required.

If you plan to print a hardcopy for yourself, you may want to change the black background to white before sending to the printer (instructions shown below). Do not change the background to white for the PDF version of your report.

For your records (and resume): It is recommended that you create a full color PDF plot of your final quarter pad frame cell layout. Ask for help if you cannot determine how to print to Postscript from the Cadence tools and convert your Postscript file to PDF.

6. APPENDIX A: MIXED SIGNAL SIMULATION SPEED-UP

The simulation time for the hierarchal cell designs ADD16, BSR, BSSUM will be significant due to the number of transistors involved. Simulation speed can be dramatically improved by using the Cadence Spectre eXtensive Partitioning Simulator (XPS). XPS is based on FastSPICE modeling and employs techniques that can trade accuracy (within 5% of tradition Spectre / SPICE) for simulation capacity and improved performance. Under the ADE Setup->High-Performance/Parasitic Reduction select XPS MS mode.

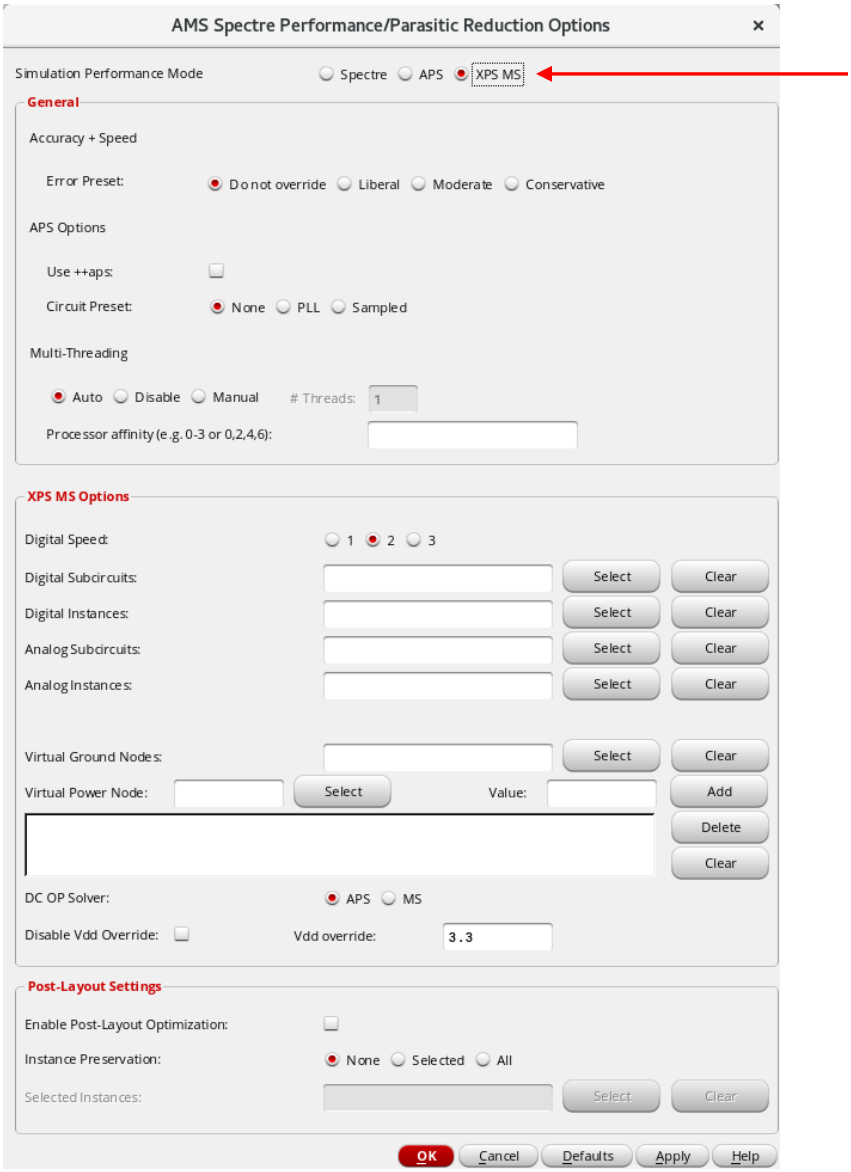

Figure 8 Spectre XPS MS Mode

7. APPENDIX B: PROJECT QUARTER PAD FRAME CELL

Directions for accessing the pad frame cell library will be discussed during the lab and can be found in the file *mai_corner_cell.pdf* posted to mycourses.

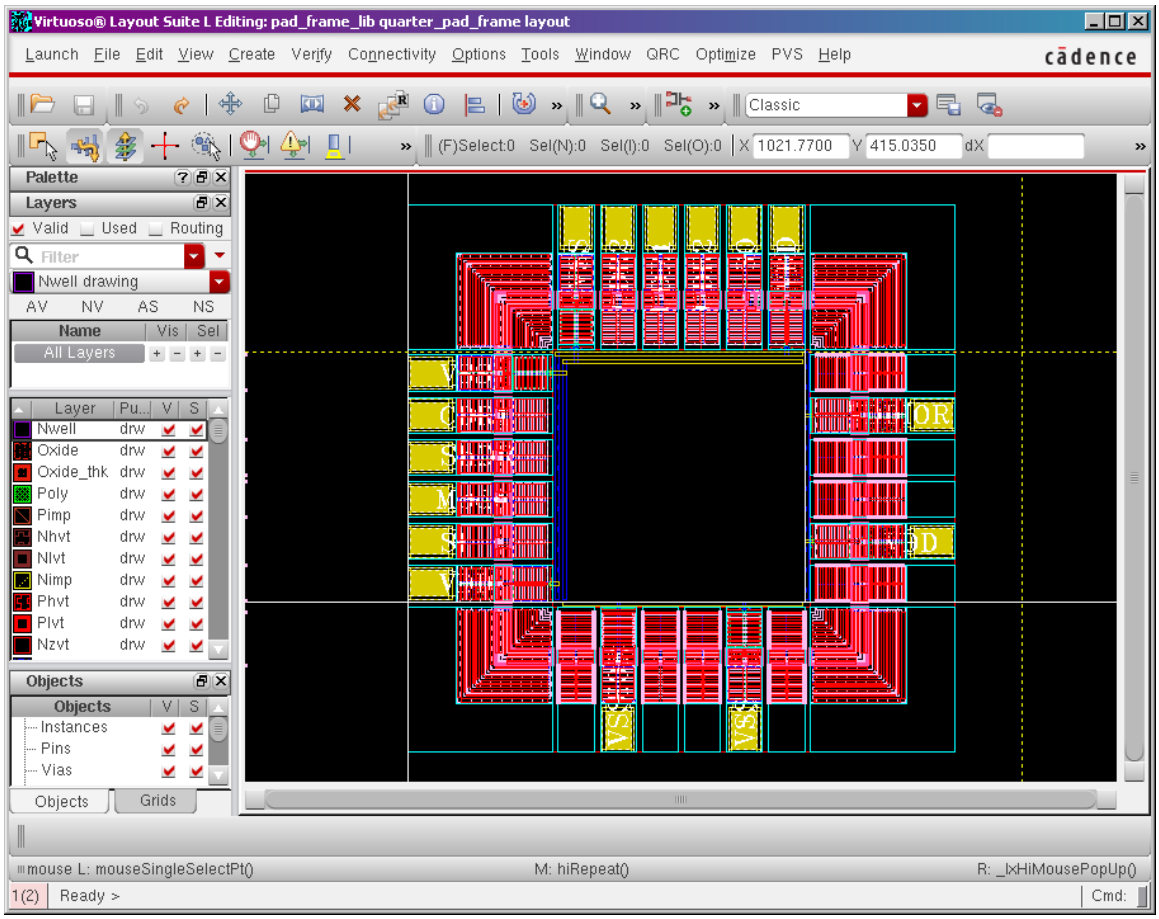

Figure 9 Project Quarter Pad Frame Cell

8. APPENDIX C: BRIEF BOUNDARY SCAN OVERVIEW

Boundary scan is a method for testing wiring on a PCB or sub-blocks within an integrated circuit. The Joint Test Action Group (JTAG) developed a specification for boundary scan testing that was standardized in 1990 as the IEEE Std. 1149.1-1990.

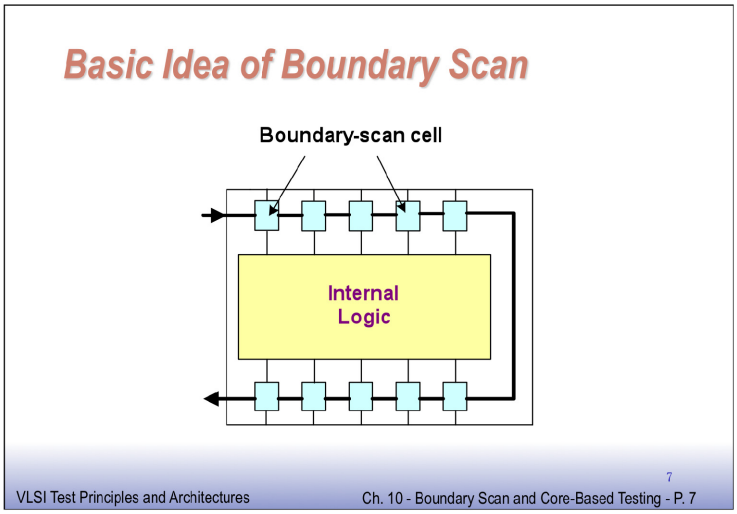

Figure 10 Boundary Scan Chain

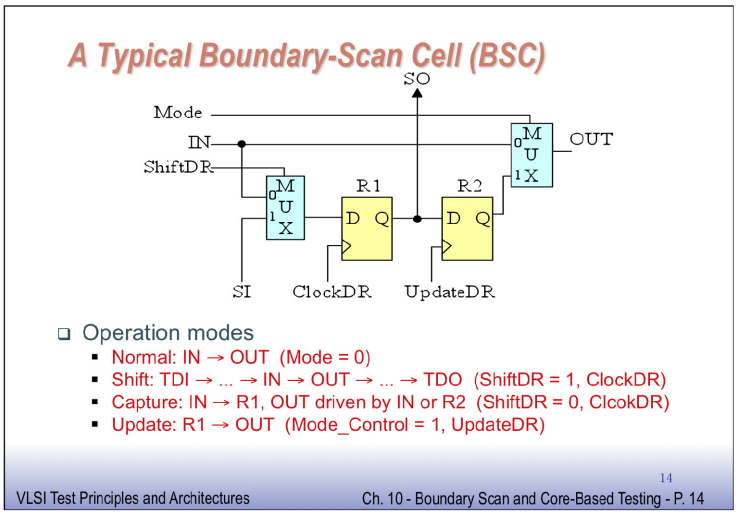

Figure 11 Boundary Scan Cell

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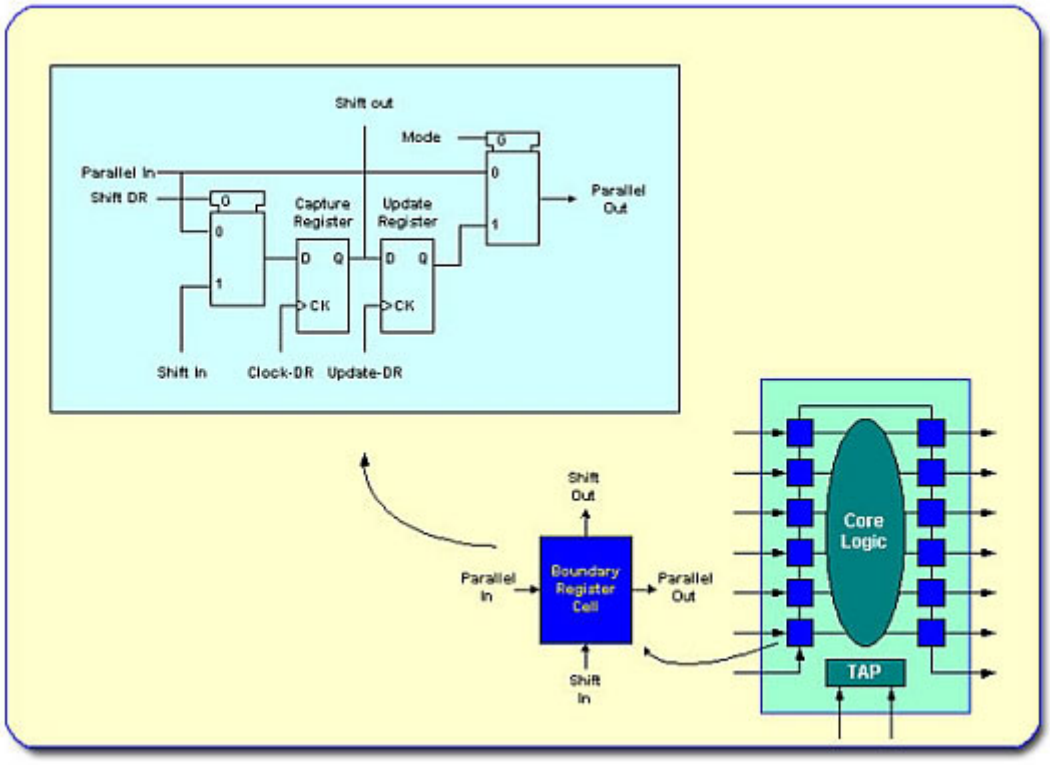

Figure 12 Boundary Scan showing TAP

Boundary Scan example only: A Test Access Port (TAP) is NOT required by Project 2