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Thalavapalayam, Karur – 639 113.

VLSI IMPLEMENTATION OF TURBO CODE FOR LTE USING VERILOG HDL

A MINOR PROJECT-II REPORT

Submitted by

RENUGA K **927621BEC165**

BACHELOR OF ENGINEERING

in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.KUMARASAMY COLLEGE OF ENGINEERING

(Autonomous)

KARUR – 639 113

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M.KUMARASAMY COLLEGE OF ENGINEERING,

KARUR

BONAFIDE CERTIFICATE

Certified that this **18ECP104L-Minor Project II** report **"VLSI IMPLEMENTATION OF TURBO CODE FOR LTE USING VERILOG HDL"** is the bonafide work of **K.RENUGA (927621BEC165)** who carried out the project work under my supervision in the academic year **2022-2023 - EVEN**.

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This Minor project-II report has been submitted for the **18ECP104L – Minor Project-II**

Review held at M. Kumarasamy College of Engineering, Karur on_____.

PROJECT COORDINATOR

INSTITUTION VISION AND MISSION

Vision

To emerge as a leader among the top institutions in the field of technical education.

Mission

M1: Produce smart technocrats with empirical knowledge who can surmount the global challenges.

M2: Create a diverse, fully -engaged, learner -centric campus environment to provide quality education to the students.

M3: Maintain mutually beneficial partnerships with our alumni, industry and professional associations

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Vision

To empower the Electronics and Communication Engineering students with emerging technologies, professionalism, innovative research and social responsibility.

Mission

M1: Attain the academic excellence through innovative teaching learning process, research areas & laboratories and Consultancy projects.

M2: Inculcate the students in problem solving and lifelong learning ability.

M3: Provide entrepreneurial skills and leadership qualities.

M4: Render the technical knowledge and skills of faculty members.

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PEO1: Core Competence: Graduates will have a successful career in academia or industry associated with Electronics and Communication Engineering

PEO2: Professionalism: Graduates will provide feasible solutions for the challenging problems through comprehensive research and innovation in the allied areas of Electronics and Communication Engineering.

PEO3: Lifelong Learning: Graduates will contribute to the social needs through lifelong learning, practicing professional ethics and leadership quality

Program Outcomes

PO 1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2: Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO 6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

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PSO1: Applying knowledge in various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of Engineering application.

PSO2: Able to solve complex problems in Electronics and Communication Engineering with analytical and managerial skills either independently or in team using latest hardware and software tools to fulfil the industrial expectations.

Abstract	Matching with POs,PSOs
Turbo codes Interleaver MAP algorithm.	PO1, PO2, PO3, PO5, PO6,PO7,PO9, PO10, PO11, PSO1, PSO2

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We offer our wholehearted thanks to our **Project Supervisor, Mr. K. Kaarthik, M.E., Assistant Professor**, Department of Electronics and Communication Engineering for his precious guidance, tremendous supervision, kind cooperation, valuable suggestions and support rendered in making our project to be successful.

We would like to thank our **Minor Project Co-ordinator**, **Dr.E.Dinesh, M.E., Ph.D., Associate Professor**, Department of Electronics and Communication Engineering for his kind cooperation and culminating in the successful completion of this project work. We are glad to thank all the Faculty Members of the Department of Electronics and Communication Engineering for extending a warm helping hand and valuable suggestions throughout the project. Words are boundless to thank our Parents and Friends for their motivation to complete this project successfully.

ABSTRACT

Communication is act of transmission of information. Everyone in the world experiences the need to receive information almost continuously. For communication to be successful, it is essential that sender and receiver understands a common language. When signal is transmitted there are 3 sources of transmission errors, they are: Signal bit errors, burst errors and erasure. Errors in signal may lead to miscommunication between systems. So, error correction is required to retrieve the original message. In order to detect and correct the errors, turbo codes are used. Turbo codes are error correction codes that are widely used in communication systems. Turbo codes exihibits high error correction capability as compared with other error correction codes. This paper proposes a Very Large Scale Intergartion (VLSI) architecture for the implementation of Turbo Encoder. VLSI architecture for the Turbo encoder implementation, Interleaves and de interleaves are employed. The number of iterations required to decode the information bits being transmitted is reduced by the use of MAP algorithm [1]. For the encoder part, this paper uses a system which contains two Recursive convolutional encoders along with pseudo random interleaver in encoder side. The Turbo encoding and decoding is done using Octave, Xilinx ISE tools. The system is implemented and synthesized in Application Specific Integrated Circuit (ASIC).

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LIST OF ABBREVIATIONS

ACRONYM		ABBREVIATION
VLSI	–	Very Large Scale Integration
LTE	–	Long Term Evolution
HDL	–	Hardware Description Language
MAP	–	Maximum-a-Posteriori
ISE	–	Integrated Synthesis Environment
SOVA	–	Soft Output Viterbi Algorithm

CHAPTER 1

INTRODUCTION

Communication is a process by which information is exchanged between individuals through a common channel. When data is transferred from source to destination system, errors can be present in signal. So, error correction is required to retrieve the original message.

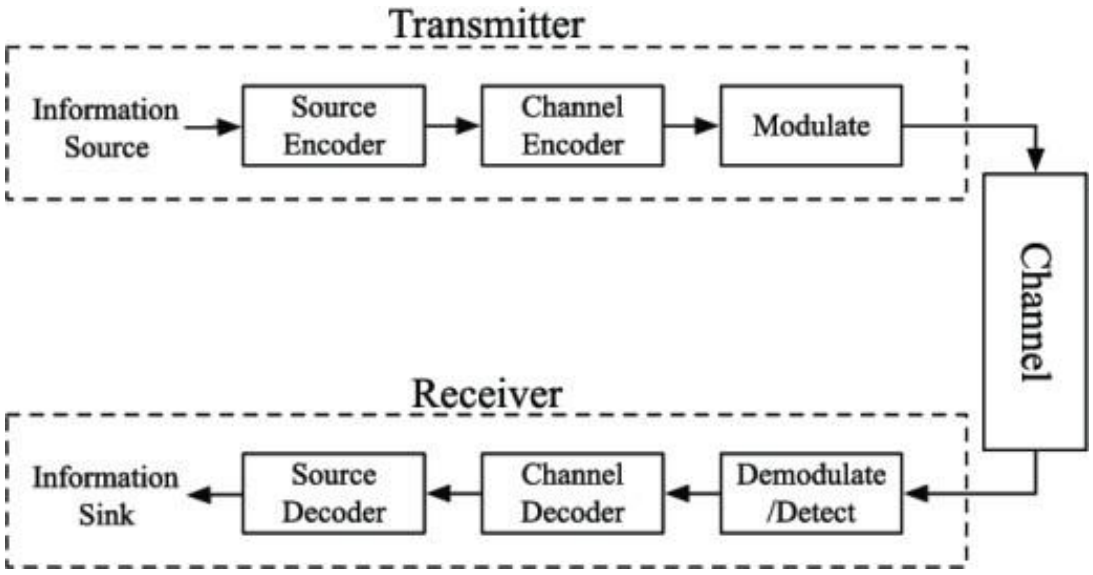

Fig 1.1 Block Diagram of Communication System

Communication is the process of establishing connection or link between two points for information exchange. Communication is simply the basic process of exchanging information.

The electronics equipment's which are used for communication purpose, are called communication equipment's. Turbo coding is a very effective technique for correcting errors, which in recent years had a huge effect on channel coding. Turbo coding in digital

communication is one of the most common and successful coding techniques for enhancing the bit error rate.

Turbo encoder is to be an integrated module in the In-Vehicle Device embedded module by using the magnitude comparator.

In the most fundamental sense, communication involves the transmission of information from one point to another through a succession of process as listed below

1. The generation of a thought pattern or image in the mind of an originator.
2. The description of that image, with a certain measure of precision, by a set of oral visual symbols.
3. The encoding of these symbols in a form that is suitable for transmission over a physical medium of interest.
4. The transmission of the encoded symbols to the desired destination.
5. The decoding and reproduction of the original symbols.
6. The recreation of the original thought pattern or image, with a definable degradation in quality, in the mind of recipient.the mind of recipient.

a) TRANSMITTER

The Transmitter has some information that it wants to transmit to receiver. The transmitter can also add error correcting codes using channel encoder block which essentially introduces redundancy by adding extra bits. The function of the transmitter is to process the electrical signal from different aspects. For example, in radio broadcasting the electrical signal obtained from sound signal, is processed to restrict its range of audio frequencies (up to 5 kHz in amplitude modulation radio broadcast) and is often amplified. Modulation is the main function of the transmitter. In modulation, the message signal is superimposed upon the high-frequency carrier signal .Inside the

transmitter, signal processing's such as restriction of range of audio frequencies, amplification and modulation of signal are achieved . All these processing's of the message signal are done just to ease the transmission of the signal through the channel.

b) CHANNEL

The channel may introduce noise in system. A channel can be a wire or air. The term channel means the medium through which the message travels from the transmitter to the receiver. In other words, we can say that the function of the channel is to provide a physical connection between the transmitter and the receiver. There are two types of channels, namely point-to-point channels and broadcast channels. Example of point-to-point channels are wire lines, microwave links and optical fibres. Wire-lines operate by guided electromagnetic waves and they are used for local telephone transmission. In case of microwave links, the transmitted signal is radiated as an electromagnetic wave in free space. Microwave links are used in long distance telephone transmission. An optical fibre is a low-loss, well-controlled, guided optical medium. Optical fibres are used in optical communications Although these three channels operate differently, they all provide a physical medium for the transmission of signals from one point to another point. Therefore, for these channels, the term point-to-point is used. On the other hand, the broadcast channel provides a capability where several receiving stations can be reached simultaneously from a single transmitter. An example of a broadcast channel is a satellite in geostationary orbit, which covers about one third of the earth's surface. During the process of transmission and reception the signal gets distorted due to noise introduced in the system. Noise is an unwanted signal which tend to interfere with the required signal. Noise signal is always random in character. Noise may interfere with signal at any point in a communication system. However, the noise has its greatest effect on the signal in the channel

c) RECEIVER

The main function of the receiver is to reproduce the message signal in electrical form from the distorted received signal. This reproduction of the original signal is accomplished by a process known as the demodulation or detection. Demodulation is the reverse process of modulation carried out in transmitter. The receiver can use the added redundancy to mitigate errors that may be introduced by channel

1.1 OBJECTIVES

The main objective of this project is

- To Implement Turbo encoder.
- To correct the errors and retrieve the original message and
- To reduce the number of iterations required to decode the information bits being transmitted.

1.2 BLOCK DIAGRAM

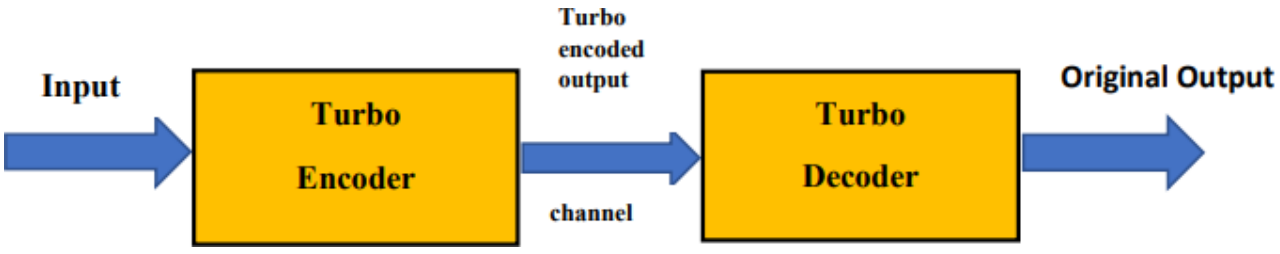

Fig 1.2 Block Diagram of Turbo Coder

1.2.1. EXPLANATION OF THE BLOCK DIAGRAM

The Basic Block Diagram of Turbo Coder consists of Turbo Encoder and Turbo Decoder. A channel for transmitting data from encoder to decoder. Turbo encoder produces an encoded output which is input to turbo decoder, that produces a decoded output by removing the errors and reducing the number of iterations by using MAP Algorithm and get back the original output.

1.3 TURBO ENCODER

Turbo encoder produces an encoded output which is an input to turbo decoder. A turbo code is formed from the parallel concatenation of two codes separated by an interleaver. The two encoders normally used are identical . Encoders are recursive systematic convolutional codes(RSC). The interleaver reads the bits ina psuedo-random order. The fundamental turbo code encoder is built using two recursive systematic convolutional (RSC) codes with parallel concatenation. LTE employs a 1/3 rate parallel concatenated turbo code. Each RSC works on two different data. Original data is provided to first encoder, while the second encoder receives the interleaved version of input data. A specified algorithm is used to scramble the data bits and the method is called interleaving [2].

a) Recursive Convolutional Encoder

Each RSC works on two different data. Original data is provided to the first encoder, while the second encoder receives the interleaved version of the input data. A specified algorithm is used to scramble the data bits and the method is called Interleaving. An appreciable impact on the performance of a decoder is seen with the interleaving algorithm when used. The RSC1 and RSC2 encoder outputs along with systematic input

comprise the output of turbo encoder, that is, a 24-bit output is generated. This will be transmitted through the channel to the Turbo decoder.

b) Interleaver

Here, pseudo-random interleaver is used, due to which the interleaved version of the code tends to be long and scrambled, that gives good performance of random codes. Interleavers scrambles the data in a pseudorandom order to lessen the resemblance between adjacent bits at the input of the encoder. The interleaver is used on both the encoder part and the decoder part. It produces a long block of data on the encoder side, while it compares two SISO decoders output in the decoder portion and helps to fix the error [3].

CHAPTER 2
LITERATURE SURVEY

A literature survey or a literature review in a project is a type of review articles. It is a scholarly paper, which includes the current knowledge including substantive findings, as well as theoretical and methodological contributions to a particular topic. Literatures reviews are secondary sources, and do not report new or original experimental work. It isa basis for research in nearly every academic field. Concentrate on the own field of expertise.

2.1 DETAILS OF LITERATURE

1. V. Kavinilavu1, S. Salivahanan, V. S. Kanchana Bhaaskaran2, Samiappa Sakthikumaran, B. Brindha and C. Vinoth "Implementation of Convolutional Encoder and Viterbi Decoder using Verilog HDL", IEEE 3rd International Conference on Electronics Computer Technology,2011

A Viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using Forward error correction based on a Convolutional code. Here they presenta Convolutional encoder and Viterbi decoder with a constraint length of 7 and code rate of1/2. Finally, the transmitted sequence is decoded by the Viterbi decoder and the estimatedoriginal sequence is produced. This is realized using Verilog HDL. It is simulated and synthesized using Modelsim PE 10.0e and Xilinx 12.4i.

2. Tepoju Vivek Vardhan, Bandi Neeraja, Boya Pradeep Kumar, Chandra Sekhar Paidimarry "Implementation of Turbo Codes Using Verilog HDL and Estimation ofIts Error Correction Capability", IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (Prime Asia),2015

This paper presents the implementation of Turbo codec for designing the Turbo encoder and decoder. The Decoder is developed based on Viterbi algorithm that incorporates hard-input and output values. The errors are purposefully introduced in the encoded data toestimate error correction capability. These encoded bits are transmitted to the Turbo Decoder through channel. At the Turbo Decoder, the received data may contain errors, which are decoded using Viterbi algorithm. In such case, developed Turbo decoder is able to correct two-bit error in the encoded data. The Encoderand Decoder of Turbo codes are implemented using Verilog-HDL. The code is ported in FPGA for real time verification.

3. Cagri Tanriover, Bahram Honary, Jun Xu, and Shu Lin, "Improving turbo code error performance by multifold coding", IEEE Communication letters, VOL. 6, NO.5, MAY 2002.

This letter presents a simple turbo coding technique to improve the error performance of a conventional rate-1/3 turbo code by shaping its weight spectrum closer to the binomial weight distribution of a random code. This technique can be applied to both symmetric andasymmetric rate 1/3 turbo codes to achieve additional coding gain.

4. Arash Ardakani, Mahdi Shabany, "An Efficient Max-Log MAP Algorithm For VLSIImplementation of Turbo Decoders", IEEE International Symposium on Circuits and Systems (ISCAS), 2015

In this paper, a novel form of computation of the max-log MAP core is proposed to highlyimprove the hardware implementation parameters of a turbo decoder

for the LTE and LTE-advanced standards. The proposed method can be applied to any max-log MAP architecture. In order to illustrate the impact of using the proposed method, a max-log MAP, as a case study, is implemented based on both the proposed form of computation andconventional one for a fair comparison. They came a conclusion that the max-log MAP based on the proposed method not only reduces the area and power consumption of each sub-blocks but also increases the throughput of the core without any performance (BER) degradation compared to the conventional method.

5. Claude Berrou, Ramesh Pyndiah, Patrick Adde, Catherine Douillard and Raphaël Bidan, "Application of turbo codes", IEEE 2005

Turbo Codes are now a mature technology that has been rapidly adopted for application in many commercial transmissions systems. This paper provides an overview of the basic concepts employed in Convolutional and Block Turbo Codes, and review the major evolutions in the field with an emphasis on practical issues such as implementation complexity and high-rate circuit architectures. We address the use of these technologies inexisting standards and also discuss future potential applications for this error-control coding technology.

6. Moeed Israr and Tad Kwasniewski, "Digital IC design of turbo codes", 9th International Database Engineering & Application Symposium (IDEAS'05) 2005 IEEE

This paper presents a Digital ASIC implementation of Turbo Encoder and simulation of the Encoder and the Decoder. The simulations determine the impact of decoder iterations,encoder transfer function and block size on latency, throughput and bit error rate. The paperproposes a design of Turbo Encoding hardware with dual-port on-chip memory targeting 0.18µm CMOS technology that reduces the memory requirements to half. Architectural and block level consideration are made to reduce

power and area requirements while achieving a latency of “packet size + 5” clock cycles. Estimated power and area are 54.19mW and 12.0 mm2 respectively.

7. Aswathy Narayanan; Senthil Murugan; Ramesh Bhakthavatchalu, “Low Latency Max Log MAP based Turbo Decoder”, International Conference on Communicationand Signal Processing (ICCSP),2019

The framework of convolutional coding persisting today incorporates decoder designs whose performance varies with the underlying algorithm’s efficiency. As process and technology advances from the basic fixed-point multiplier to the present Booth multiplier,the decoding performance varies. This paper focuses on bringing out the performance variations of a Max log MAP algorithm-based turbo decoder on implemented with fixed point, Vedic and Booth multipliers.Upon implementation, fixed point multiplier consumes a large amount of power, also since Max Log MAP algorithm must be power efficient, so it is not implemented. They reacheda conclusion such that for lesser delay, Vedic multiplier-based implementation can be preferred, which consumes more area. Whereas, in cases of highly scaled designs, where accommodation of high number of resources is not affordable, Booth algorithm-based implementation is preferred.

CHAPTER 3
EXISTING SYSTEM

Parallel Concatenated Convolutional Codes (PCCC): PCCC is a type of turbo code that involves the use of multiple convolutional codes in parallel, each with its own interleaver. The output of each convolutional encoder is then combined using a turbo decoder to produce the final encoded bitstream. This approach provides good error-correction performance and is relatively easy to implement in hardware.

Recursive Systematic Convolutional Codes (RSCC): RSCC is another type of turbo code that involves the use of a recursive encoder and a decoder. The recursive encoder produces the first set of encoded bits, which are then fed back into the encoder to produce a second set of encoded bits. This process continues recursively until the desired number of iterations is reached. RSCC provides excellent error-correction performance and is suitable for high-speed communication systems [4].

Punctured Turbo Codes (PTC): PTC is a variation of turbo codes that involves selectively removing some of the parity bits from the original code sequence. This approach reduces the complexity of the decoder, making it suitable for hardware implementation. However, the performance of PTC is slightly lower than that of other turbo codes [5].

Hybrid Turbo Codes (HTC): HTC is a combination of turbo codes and other error-correcting codes, such as Reed-Solomon codes. The approach provides excellent error-correction performance and is suitable for high-speed communication systems.

CHAPTER 4

PROPOSED SYSTEM

Our main objective is to implement the turbo coder. The objective is achieved by designing a Turbo Encoder and a Turbo Decoder using Verilog HDL. The decoder is developed based on SOVA algorithm. The SOVA algorithm identifies the most probable bit of information that was sent. The algorithm helps in reducing the number of iterations at the decoding process. The SOVAalgorithm is preferred, as it highly improves the hardware implementation parameters of a Turbo Decoders for LTE and LTE Advanced Standards also helps in reducing the area and power consumption of each block but also increases the throughput of the core. To Design Turbo Encoder it requires: Recursive Systematic Convolutional (RSC) Encoder, Interleave, Data Assembler.To implement a Turbo Decoder , the first criteria is to choose a suitable decoding algorithm.

4.1 SOFTWARE REQUIREMENTS

Tool : Xilinx ISE 14.7

Xilinx ISE (Integrated Synthesis Environment) is a discontinued software tool from Xilinx for synthesis and analysis of HDL designs, which primarily targets development of embedded firmware for Xilinx FPGA and CPLD integrated circuit (IC) product families. It was succeeded by Xilinx Vivado.

HDL: Verilog

Fig 4.1 Xilinx ISE 14.7 logo

4.2 HARDWARE REQUIREMENTS

a) Microsoft® Windows XP
b) Intel® Pentium® 4 processor or Pentium 4 equivalent with SSE support
c) 512 MB RAM
d) 100 MB of available disk space

CHAPTER 5
IMPLEMENTATION OF TURBO ENCODER

In a communication system, when data is transferred from the source system to a destination system, errors can be present in the received signal at the source end. So error correction is required to retrieve the original message. Turbo codes, which were first introduced in 1993, represent a quantum leap in channel coding techniques and a turning point for modern digital telecommunication. Turbo codes are one of existing powerful error correcting codes. A Turbo code has inspired the coding community with the possibility of using an iterative decoding technique that relies solely on simple constituent code to achieve close channel capacity. Turbo coder architecture comprises of turbo encoder and turbo decoder. Encoder consists of two Recursive Convolutional Encoders (RSC) and interleaver. In this paper, pseudo-random interleaver is used due to which the interleaved version of the code tends to be long and scrambled, that gives good performance of random codes. In turbo code implementation, RSC encoders are employed rather than conventional convolutional encoders since it generates low weight parity codes. MAP algorithm is used for the decoding of turbo encoded data in which errors are intentionally added and verified an error free decoded data after decoding [6].

ARCHITECTURE OF TURBO ENCODER

Architecture of Turbo Coder Turbo encoder and decoder together comprises the Turbo coder architecture(shown in figure 1.2).Two identical Recursive convolutional encoders(RSC) and a pseudorandom interleaver constitutes the turbo encoder .LTE employs a 1/3 rate parallel concatenated turbo code. Each RSC works on two different data. Original data is provided to the first encoder, while the second encoder receives the interleaved version of the input data. A specified algorithm is used to scramble the data

bits and the method is called Interleaving. An appreciable impact on the performance of a decoder is seen with the interleaving algorithm when used [7].

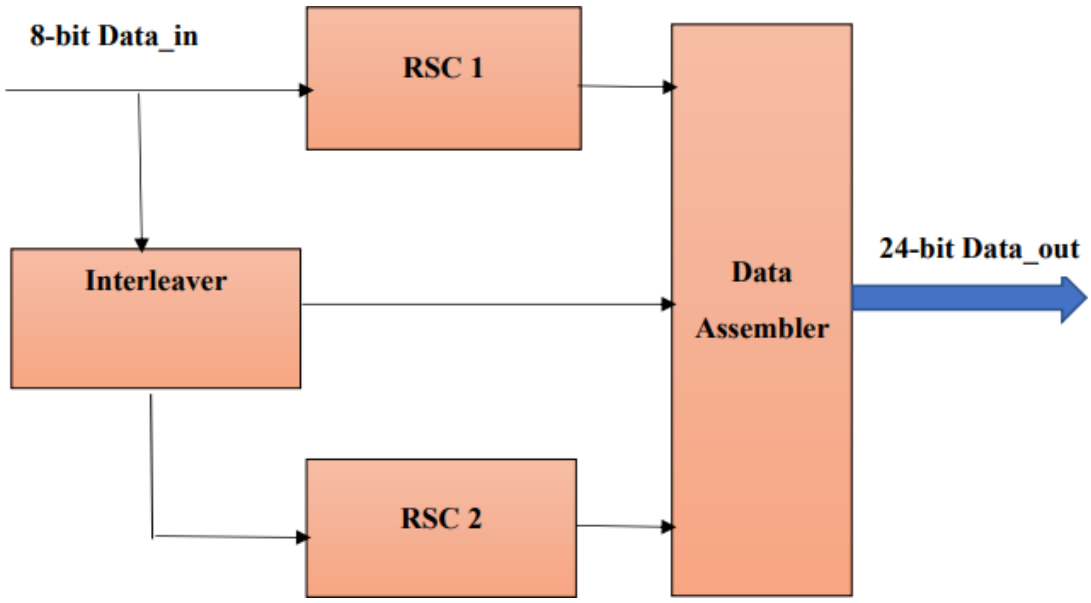

Fig 5.1 Block Diagram of Turbo Encoder

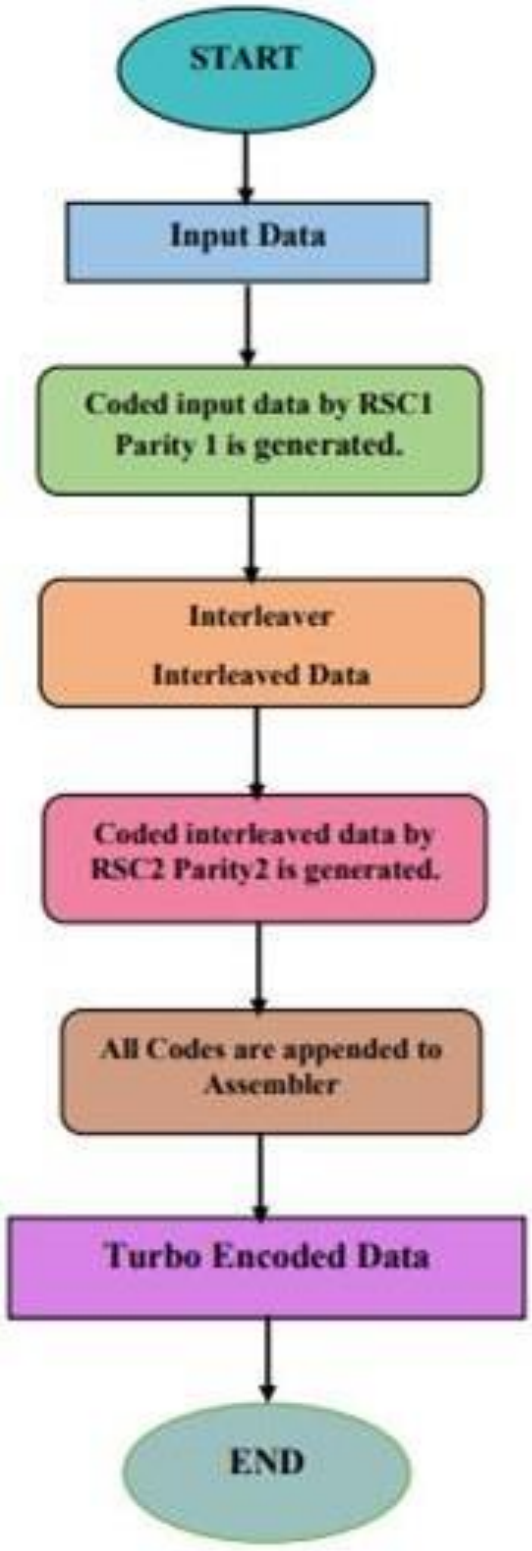

Fig 5.2 Flow chart of process of Turbo Encoder

CHAPTER 6
RESULTS AND DISCUSSION

The Turbo encoder and decoder simulations are done using Verilog HDL in Xilinx Vivado2020.2. Verilog Design Suite is a Xilinx based software suite. It may be used for HDL design synthesis and analysis. Recursive Convolutional encoders, Turbo encoder and decoder simulation outputs are performed using Xilinx ISE.

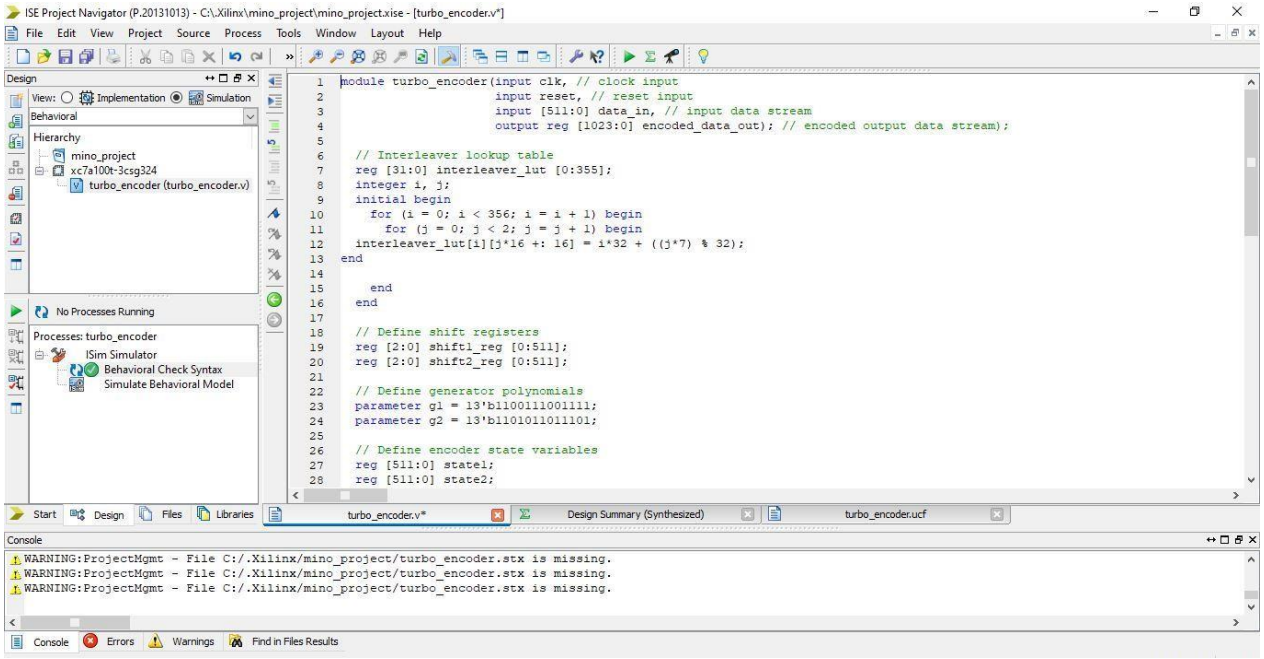

Fig 6.1 Implementation of Turbo Encoder

turbo_encoder Project Status (04/17/2023 - 18:03:18)			
Project File:	minor_project.xise	**Parser Errors:**	No Errors
Module Name:	turbo_encoder	**Implementation State:**	Synthesized
Target Device:	xc3s50a-4tq144	• **Errors:**	
Product Version:	ISE 14.7	• **Warnings:**	
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:		• **Final Timing Score:**	

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon 17. Apr 19:48:34 2023			
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	

Date Generated: 04/17/2023 - 19:54:30

Fig 6.2 Design Summary

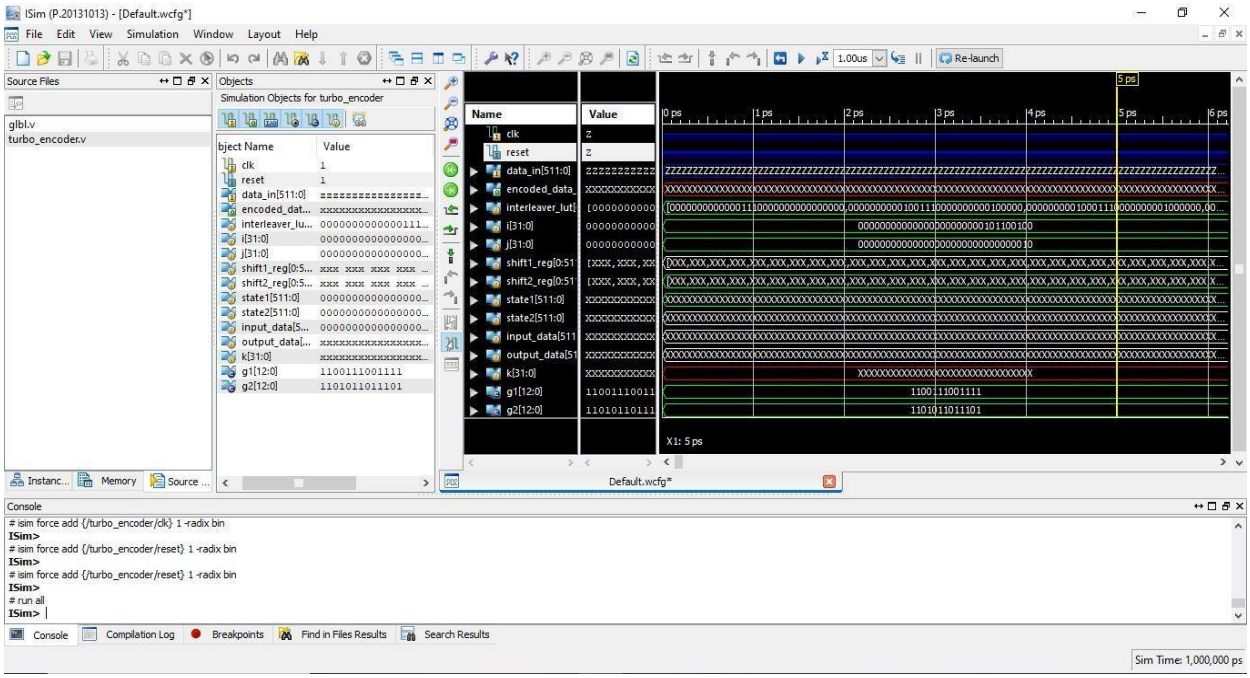

Fig 6.3 Simulation Output

CHAPTER 7
CONCLUSION

Turbo encoder and turbo decoder are components of the turbo coder architecture. In this Project we designed Turbo Encoder. Two Recursive Convolutional Encoders (RSC) and an interleaver make up the encoder. The Turbo encoder is simulated in Verilog HDL using Xilinx ISE 14.7 version. Input information bits are given to Turbo encoder that encodes data and then transmitted to Turbo Decoder through channel to obtain 24-bit output data. At decoder, the received data may contain errors, which are decoded using SOVA algorithm to obtain original information.

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[1] V. Kavinilavu1, S. Salivahanan, V. S. Kanchana Bhaaskaran2, Samiappa Sakthikumaran, B. Brindha and C. Vinoth **"Implementation of Convolutional Encoder and Viterbi Decoder using Verilog HDL"**, IEEE 3rd International Conference on Electronics Computer Technology,2011.

[2] Tepoju Vivek Vardhan, Bandi Neeraja, Boya Pradeep Kumar, Chandra Sekhar Paidimarry **"Implementation of Turbo Codes Using Verilog HDL and Estimation of Its Error Correction Capability",** IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (Prime Asia),2015.

[3] Cagri Tanriover, Bahram Honary, Jun Xu, and Shu Lin, **"Improving turbo code error performance by multifold coding"**, IEEE Communication letters, VOL. 6, NO. 5, MAY 2002.

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[6] Moeed Israr and Tad Kwasniewski, **"Digital IC design of turbo codes",** 9th International Database Engineering & Application Symposium (IDEAS'05) 2005 IEEE.

[7] Aswathy Narayanan; Senthil Murugan; Ramesh Bhakthavatchalu**, "Low Latency Max Log MAP based Turbo Decoder"**, International Conference on Communication and Signal Processing(ICCSP),2019.

OUTCOME

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CERTIFICATE OF PARTICIPATION

This is to certify that ~~Dr./~~Mr./Ms./~~Mrs.~~ K. RENUGA of II ECE, MKCE has presented a paper titled VLSI IMPLEMENTATION OF TURBO CODE FOR LTE USING VERILOG HDL in DST-SERB Sponsored Second International Conference on "Signal Processing and Communication Systems" Organized by the Department of Electronics and Communication Engineering on 07 th March 2023 of our Institution.

Organizing Chair

Dr.S.Palanivel Rajan
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