**Capstone Project – Introduction (PROJ2999), 7th Semester**

**Academic year: 2025-26**

**Project Title: Low power RTL design using clock gating**

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***Abstract:***

Clock gating is a fundamental low-power technique in digital design where the clock signal input to idle circuit blocks are disabled to reduce undesired switching activity and dynamic power consumption. While the fundamental approaches of clock gating exist in the literature, this project aims to introduce a smart, two-level power-saving system for digital circuits called a "unified adaptive clock gating methodology." Our design uses a single, unified controller that acts as a brain to manage two different energy-saving tools: clock gating, and dynamic frequency scaling.

The controller is "adaptive" because it intelligently watches the circuit to see how long it has been idle and adapts its strategy accordingly. Based on predefined time thresholds, it makes a smart decision: for short idle breaks, it saves power instantly by gating the clock, but for longer idle periods, it also switches the system to a slower, "eco-mode" clock frequency for even greater efficiency. We implemented our proposed algorithm on a full adder circuit for functional verification. The results proves that functionality of full adder circuit is not impacted by inclusion of the unified clock gating algorithm and the total power consumed is found out to be 0.5 W .

Based on the current advancements, this unified approach will be implemented in advanced computing blocks, to demonstrate the efficiency of the proposed technique.

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