LOW POWER RTL USING CLOCK GATING

Report submitted to GITAM (Deemed to be University) as a partial fulfillment of the requirements for the award of the Degree of Bachelor of Technology in (EECE -AIML)



DEPARTMENT OF ELECTRICAL, ELECTRONICS AND COMMUNICATION ENGINEERING

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**DECLARATION**

We declare that the project work contained in this report is original and it has been done by me under the guidance of my project guide.

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**CERTIFICATE**

This is to certify that Nukala Naga Jyoshika, Poojala Renuka, MD Sameena Thasleem bearing BU22EECE0100489, BU22EECE0100491, BU22EECE0100497 has satisfactorily completed Mini Project Entitled in partial fulfillment of the requirements as prescribed by University for VIIth semester, Bachelor of Technology in “Electrical, Electronics and Communication Engineering” and submitted this report during the academic year 2025-2026.

[Signature of the Guide] [Signature of HOD]

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**Chapter 1: Introduction**

* 1. Overview of the problem statement:

In our problem statement, we use modern VLSI and digital design. Power consumption has become a critical concern due to the increasing complexity and density of integrated circuits. In the clock network, the major contribution is to dynamic power consumption. When the clock runs continuously, even when parts of the circuit are idle, it results in unnecessary power wastage.

In this context, Clock Gating is used as an effective low-power technique. By selectively enabling or disabling the clock signal to certain modules, unnecessary switching activity is reduced. Our project focuses on designing a Low Power RTL architecture using Unified Adaptive Clock Gating combined with clock frequency scaling. This ensures power efficiency without sacrificing performance.

* 1. Objectives and goals:
* To design a Full Adder System in RTL using clock gating applied
* we can implement a Unified Adaptive Clock Gating Controller that combines gating and frequency scaling
* we can validate the design through simulation and observe reduced power consumption
* To compare the proposed design against a normal non gated using RTL design

**Chapter 2 : Literature Review**

**Power Reduction Through RTL Clock Gating**

* Validated a design methodology for reducing ASIC power using RTL clock gating.
* Proved that RTL clock gating can reduce dynamic current consumption by 72% (280mA to 78mA) on a real world 200K=gate ASIC.
* The technique was most effective at reducing power from flipflops, achieving an 80% reduction from that area.
* Found that RTL clock gating resulted in significant 6.75 cell area savings by eliminating multiplexers.

**Enhanced clock gating technique for power optimization in SRAM and Sequential circuit**

* This paper proposes enhanced clock gating technique using D latch and a buffer to reduce power consumption.
* It aims to solve common issues like glitching and clock triggering found in traditional clock gating.
* The proposed logic achieves a power consumption of 1.065W and a delay of 6ns on a sequential circuit.
* This is significant improvement over a traditional 4-bit counter without clock gating which has power of 22.96W and a delay of 72ns.

**Implementation of adaptive clock gating technique for Low power circuits - A Review**

* This paper reviews various clock gating methods and concludes that adaptive clock gating is the most robust technique.
* It compares latch based, flip flop based and gate based clock gating, finding the gate based method is most efficient.
* Case study showed that a power reduction of 21.5% in random flipflop design and 6% in 3-bit counter.
* It concludes that the amount of power reduction varies depending on system's specific activity and logic.

**Existing Implementations - Products | Opensource | GitHub etc**

1. Gate based clock gating:

This is one of the simplest and most efficient clock gating techniques, where a logic gate (such as an AND, OR, or NOR gate) is used to control the clock signal. The design is simple and has less area occupied

1. Latch-based clock gating:

This technique uses a level-sensitive latch as the controlling element for the clock. It avoids glitches and has a good performance, but it has a long sleep period and can cause a mismatch in delay.

1. Flip-flop based clock gating:

This method uses an edge-triggered flip-flop to control the clock enable pin. Flip-flop based gating is not highly preferred due to high power consumption, high switching activity, and large area usage.

1. Synthesis-based clock gating:

This is widely used method where EDA tools automatically insert clock gating to reduce clock pulses. It is easy to implement and has less timing constraints, but it can have a high redundant problem and consume more power compared to other techniques.

1. Data-driven based clock gating:

This technique blocks the clock signal in the next cycle by XOR-ing the current data output with the present data input. It consumes less power, avoids the redundant problem, and has moderate switching activity, but its implementation is difficult.

1. Auto-gated clock gating:

This method uses an auto-gated flip-flop for the design. It is easy to implementand has a less redundant problem, but it has high switching activity and high timing constraints. It only gates the slave latches and not the remaining clock loads.

1. Look-ahead based clock gating:

Similar to data-driven gating, this technique can stop most redundant clock pulses. It is preferred for its ability to avoid tight timing constraints and its easy circuit implementation. It also consumes less power and has less switching activity

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**Chapter 3 : Strategic Analysis and Problem Definition**

* 1. SWOT Analysis:
* **Strengths**: The Significant power reduction, easy RTL integration, scalable to larger systems.
* **Weaknesses**: It Adds minor control logic overhead, slight latency due to clock synchronization.
* **Opportunities**: The Applicable in portable devices, IoT, battery-powered systems.
* **Threats**: The Competing low-power techniques (multi-VDD, DVFS) may offer alternative solutions.
  1. Project Plan - GANTT Chart:

**Review 1: Project Proposal & Design**

* Define the project scope and propose the high-level design.
* Milestones:
* Research and summarize existing low-power design techniques, including clock gating and frequency scaling.
* Clearly define the issue of power consumption in RTL circuits.
* Outline the project's objectives, goals, and methodology.

**Review 2: Unified Controller on a Full Adder**

* combine multiple power-saving techniques under a single, advanced controller to achieve maximum energy efficiency.
* To Your controller now manages both clock gating (for light sleep) and frequency scaling (for deep sleep) based on the duration of inactivity. This is the unified adaptive system we've been working on.
* This is where you show your best results, including the significant power reduction numbers and the functional waveforms that validate your Light Sleep and Deep Sleep modes.
  1. Problem statement:

“To design and implement a Low Power RTL Full Adder system using Unified Adaptive Clock Gating and Clock Frequency Scaling to reduce dynamic power consumption while maintaining functionality.”

**Chapter 4 : Methodology**

* 1. Description of the approach:
* Design a **basic Full Adder** in Verilog.
* Introduce **clock gating** using enable signals.
* Develop a **unified controller** that manages both gating and frequency scaling.
* Integrate modules into a **top-level system.**
* Perform functional simulation and analyze waveforms.
  1. Tools and techniques utilized:
* **Vivado 2025.1**: RTL coding, synthesis, power analysis.
* **Vivado Simulator**: Testbench simulation.
* **Verilog HDL**: RTL implementation.
* **Clock Gating + Frequency Scaling**: Power optimization techniques.
  1. Design considerations:
* Minimize area overhead while introducing clock gating logic.
* Ensure synchronous design principles are followed (no glitches on gated clocks).
* Use **effective clock enable (CE) pulses** instead of generating separate clocks, for synthesis-friendliness.

**Chapter 5 : Implementation**

* 1. Description of how the project was executed:

The project consists of three main RTL modules:

* **Unified Controller** :It generates clk\_en and clk\_select.
* **CE Generator**: It produces enable pulses for fast/slow modes.
* **Full Adder System** :It operates only when clock enable is active.

Integration:

* The **Unified Controller** monitors data\_valid signal and decides when to gate or slow down the clock.
* The **CE Generator** ensures no additional clocks are created; instead, it creates enable pulses.
* The **Full Adder** updates its inputs/outputs only when the **effective\_ce** signal is high.
  1. Challenges faced and solutions implemented:

**1.** Delay in output due to sequential behavior.

**Solution**: Accepted as an inherent part of synchronous design. Registers update outputs only on the next clock edge.

**2.** Avoiding glitches from gated clocks.

**Solution**: Used **clock enable signals** instead of directly gating clocks.

**3.** Verifying power Decremented

**Solution**: Clock gating and frequency scaling

**Chapter 6: Results**

* 1. Outcomes:
* Advanced clock gating: **0.5 W**

6.2 Interpretation of results:

The results confirm that Clock gating + frequency scaling effectively reduces unnecessary switching activity in idle periods, leading to significant power savings without impacting functional correctness.

**Chapter 7: Conclusion**

In this project, we successfully introduced and implemented a smart, two-level power-saving system called a "unified adaptive clock gating methodology." Our design uses a single controller that intelligently manages two distinct energy-saving tools: clock gating and dynamic frequency scaling.

The results proved that the functionality of the full adder circuit was not impacted by this algorithm. The design successfully reduced the total power consumption to 0.5 W, demonstrating the efficiency of our approach. This project shows that a unified, adaptive strategy is a highly effective method for low-power RTL design.

**Chapter 8 : Future Work**

Implement in Advanced Computing Blocks: The unified approach can be applied to more complex computing blocks to further demonstrate the efficiency and scalability of the proposed technique.

Dynamic Voltage and Frequency Scaling (DVFS): Extend the controller to manage not only clock frequency but also the core voltage. This would lead to a quadratic reduction in power, achieving even greater energy savings.

Application to a Larger System: Apply the controller to a more extensive, multi-module system to verify its effectiveness and robustness in a real-world, System-on-Chip (SoC) environment.

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