Design & Implementation of FPGA based PID Controller

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***Abstract*— Proportional-Integral-Derivative controllers are universal control structures and have been widely used in Automation systems, they are usually implemented either in hardware using Analog components or in software using Computer-based systems. The purpose of this project is to implement PID controllers on Field Programmable Gate Arrays (FPGAs) which improve speed, accuracy, power, compactness, and cost effectiveness over other digital implementation techniques. Finally, the PID controller can be used for applications such as DC motor speed control or Temperature controller.**

***Index Terms*—Proportional-Integral-Derivative (PID) control, Field Programmable Gate Arrays (FPGA), DC Motor, Pulse Width Modulation (PWM)**

I. Introduction

Hardware Description Languages (HDLs) are used to describe hardware for the purpose of Simulation, Modeling, Testing, Design, and Documentation Hardware Description Languages (HDLs) are used to describe hardware for the purpose of Simulation, Modeling, Testing, Design, and Documentation of digital systems. The most popular HDLs are VHDL [(Very High Speed Integrated Circuit) Hardware Description Language], and Verilog. VHDL is used to describe hardware from the abstract to the concrete level.

The Proportional-Integral-Derivative (PID) controllers have been widely used over the past five decades due to their simplicity, robustness, effectiveness and applicability for a broad class of systems. Despite the numerous control design approaches that have appeared in the literature, it is estimated that, nowadays PID controllers are still employed in more than 95% of industrial processes [1]. For many decades, the digital PID controller has been used extensively in real time digital control. The PID is used extensively in the field of servo motor control, robotics, temperature control and power electronics. It has a long history of development and very mature tuning rules. Overall, the PID is an important tool for the embedded real time digital control designer. They are usually implemented either in hardware using analog components or in software using computer-based systems. The emergence of field programmable gate arrays and hardware description languages allows for added dimensions of digital PID controllers, Parallelism, Programmable bit widths and absolute determinism. Building PID controllers on Field Programmable Gate Arrays (FPGAs) improves speed, accuracy, power efficiency, compactness and cost effectiveness.

With the growing complexity of motor and motion control applications, it becomes apparent that a Field Programmable Gate Array (FPGA) offers significant advantage over the off shelf Application Specific Standard Product (ASSP) solutions in the areas of performance, flexibility and inventory control [2]. Custom motor drive interfaces such as Pulse Width Modulation (PWM) can be developed easily, quickly and at low cost. Additionally, because of full configurability, the same FPGA can be used in various product ranges, reducing the need to maintain inventory for multiple devices [3].

The organization of this paper is given as follows: In section II, the theory behind PID controllers and the discrete PID equation is explained. In section III, the proposed methodology is presented. In section IV, the design specifications are discussed. Simulation results and conclusions are presented in section V.

II. PID Controller and Discrete PID Equation

The PID algorithm consists of three basic modes, the Proportional mode, the Integral and the Derivative modes. When utilizing this algorithm it is necessary to decide which modes are to be used (P, I or D) and then specify the parameters (or settings) for each mode used. Generally, three basic algorithms are used P, PI or PID. The implementation of PID controllers using microprocessors and DSP chips is old and well known [2] [3], whereas very little works can be found in the literature on how to implement PID controllers using FPGAs [4]. Field Programmable Gate Arrays (FPGA) have become an alternative solution for the realization of digital control systems, previously dominated by the general purpose microprocessor systems.

The application of a PID controller in a feedback control system is shown in *Fig. 1*, where *ref* is the set point signal, *y* is the feedback signal, *e* is the error signal, and *u* is the control input.

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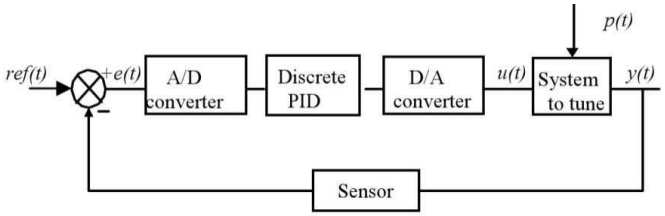


Fig. 1. A PID based feedback control system.

The simplest form of the PID control algorithm is given by:

$$U(t) = K_p\left(e(t) + \frac{1}{T_i}\int e(t)dt + T_d\frac{de(t)}{dt}\right) \quad (1)$$

Where K_p is the Proportional gain, T_i is the Integral time, T_d is the derivative time, $e(t)$ is the error signal and $U(t)$ is the output of the controller. The digitized PID equation can be written as:

$$U_n = K_p e_n + K_i\sum_{i=0}^{n} e_i + K_d(e_n - e_{n-1})$$

$$\Delta U_n = U_n - U_{n-1} = (K_p + K_i + K_d)e_n - (2k_d + K_i)e_{n-1} + K_d e_{n-2}$$

$$\therefore u_n = U_{n-1} + K_0 e_n + K_1 e_{n-1} + K_2 e_{n-2} \quad (2)$$

Where,

$$K_0 = K_p + K_i + K_d$$
$$K_1 = -(2k_d + K_i)$$
$$K_2 = K_d$$

Where K_p, K_i and K_d are proportional, integral and derivative constants which can be tuned according to the needs.

III. Proposed Methodology

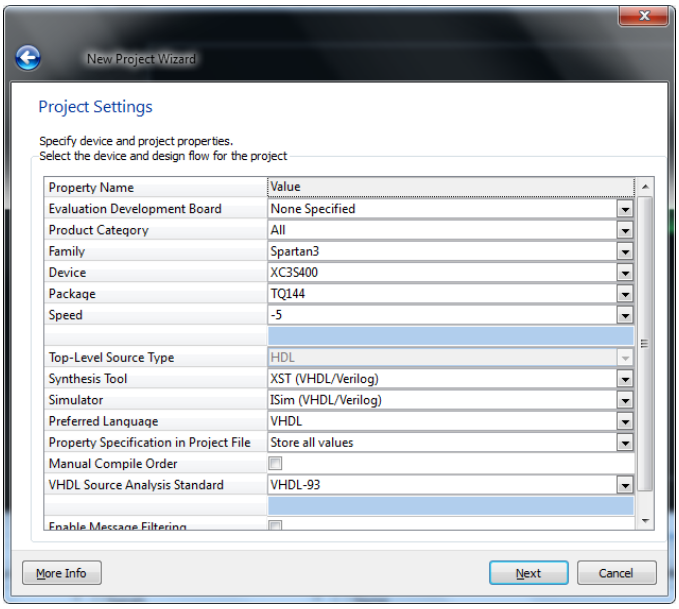
We take 16-bit feedback signal from an Analog-to-Digital converter (ADC) into the system at regular intervals of the clock. The binary value is then converted to decimal for easy operation. This value is then subtracted from the set point to calculate the error. The error is then used to evaluate the discrete PID equation and hence the control input *U(n)* is generated. It is then converted back to 16-bit binary and given to the Digital-to-Analog converter (DAC).

IV. Design

A. Target Platform

The targeted platform is Spartan 3 - XC3S400. Here is the target specifications:

Category	Integrated Circuits (ICs)
Family	Embedded - FPGAs (Field Programmable Gate Array)
Series	Spartan®-3
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	141
Number of Gates	400000
Voltage - Supply	1.14 V ~ 1.26 V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C
Package / Case	TQ144



B. Design Summary

pid Project Status			
Project File:	PIDusingVHDL.xise	**Parser Errors:**	No Errors
Module Name:	pid	**Implementation State:**	Synthesized
Target Device:	xc3s400-5tq144	**•Errors:**	No Errors
Product Version:	ISE 14.7	**•Warnings:**	51 Warnings (3 new)
Design Goal:	Balanced	**•Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	
Environment:	System Settings	**•Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	226	3584	6%
Number of Slice Flip Flops	187	7168	2%
Number of 4 input LUTs	312	7168	4%
Number of bonded IOBs	33	97	34%
Number of MULT18X18s	4	16	25%
Number of GCLKs	5	8	62%

C. Schematics

The inputs to the system are ADC_Data(15:0) and Clock, whereas the outputs are DAC_Data(15:0) as shown in *Fig. 2*. The top module technology schematic is shown in *Fig. 3*.

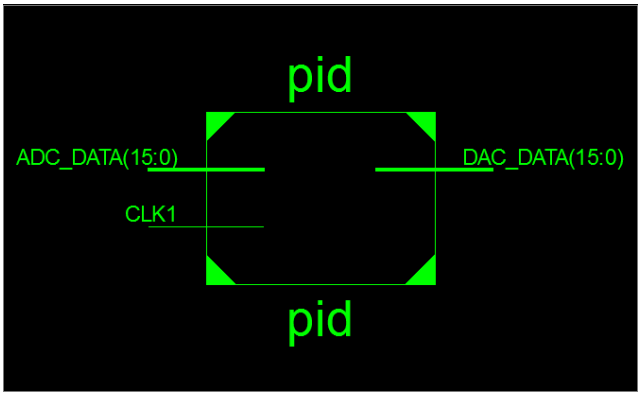


Fig. 2. Top-level Block Diagram

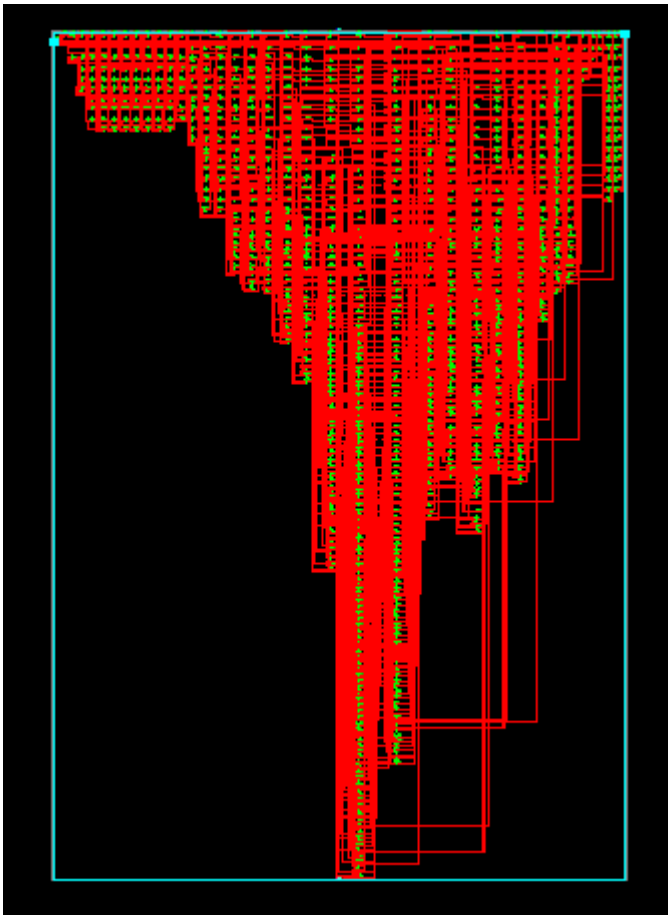
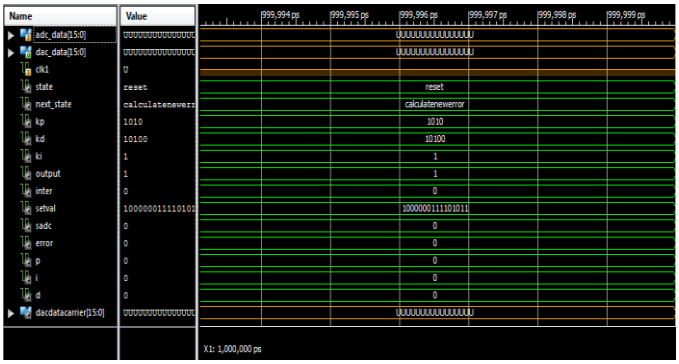


Fig. 3. Top Module Technology Schematic

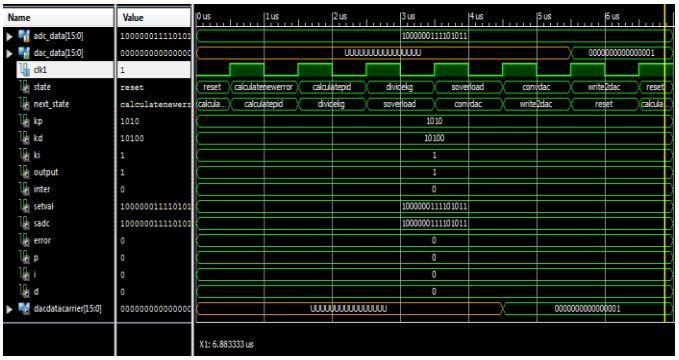
V. Result

A digital PID controller is successfully implemented using the FPGA and its performance is verified using the simulation results. A set point of decimal value 33,259 has been selected. For simulation, a 50% duty cycle clock with a period of 1µs is used. Since each complete cycle takes 7 clock cycles (according to the design), the simulation run time is set as 7µs.

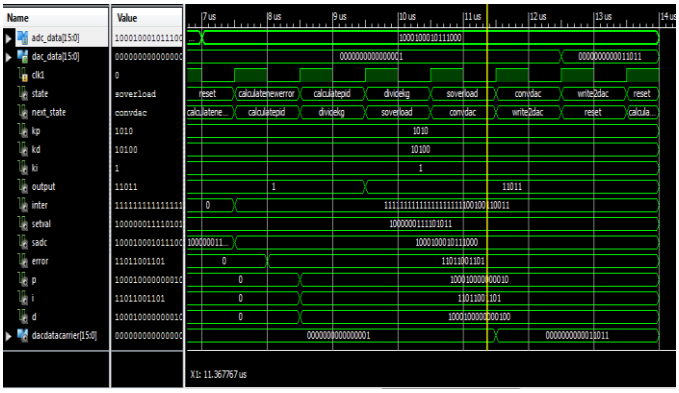
A. Initial Conditions



B. Cycle 1, ADC_Data = 0b 1000000111101011 (Decimal: 33259), No error



C. Cycle 2, ADC_Data = 0b 1000100010111000 (Decimal: 35000), Negative error



D. Cycle 3, ADC_Data = 0b 111100100011000 (Decimal: 31000), Positive error

In brief, the role of FPGA, in measurement and control point of view, is to acquire the data from sensor through analog-to-digital converter, do the processing on the acquired data and then generate control signals to the digital-to-analog, which in turn controls the parameter being measured. FPGAs ensure ease of design, lower development costs, more product revenue, and the opportunity to speed products to market. Building PID controllers on FPGAs improves speed, accuracy, power efficient, compactness and cost effectiveness over other digital implementation techniques.

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