Cascade Circuit Analyser Design report

*EE20084 - Structured Programming

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***Abstract*—This document outlines the design approach used to solve the terminal inputs and outputs to a generalised two-port cascade circuit by method of ABCD matrix analysis. The program is designed to be modular, flexible and robust, with a thorough testing process embedded.**

***Index Terms*—circuit analysis, Python, doctest, regex, software testing**

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I. Analysis of the Problem

The main objective of the assignment is to create a program that analyzes electrical circuits using two-port ABCD matrix analysis, with functionalities to read an input ".net" file, perform the analysis calculations, and output the results in the specified CSV format.

A. Sub-tasks Identification

- Parsing the input file to extract circuit components, terminations, and desired outputs.
- Malformed input file handling.
- Translating those components into a matrix representation for analysis.
- Calculatinng the ABCD matrix for the circuit.
- Applying the ABCD matrix to the input and output terminations to obtain the desired results.
- Logic error handling and exception raising.
- Generating output files with the analysis results.
- Extending the program to include additional features such as exponent prefixes and decibel calculations.

II. Module realisation and design decisions

This section breaks down the program into modules, classes and functions, and explains the design decisions made for each.
The program is divided into four modules, each with a specific role:

- `net_parser.py`: Parses the input file and extracts circuit information.
- `circuit.py`: Contains classes and functions for circuit analysis.
- `csv_writer.py`: Manages the creation and formatting of the output file with analysis results.
- `main.py`: The main driver script that utilizes the above modules.

From a broad view, due to the flexibale nature of the input file, the program is designed to be modular and flexible in kind. The circuit module is designed as a class and subclass structure, with the main Circuit class containing the component array, the source and load terminations, and the output array. The subclasses are instances of the components, terminations, and output variables which are then appended to their respective arrays to keep track of their order. The main class has the methods to add to and sort these arrays, and to recusively reduce and invert the component matricies to obtain the ABCD termination solutions.

The ordering of output array is then used to generate the output CSV, and it is formatted to match the provided example output files.

A. Data Structures

This section outlines the primary data structures utilized within the main module (`main.py`), the circuit analysis module (`circuit.py`), and other modules such as the net file parser (`net_parser.py`) and the CSV writer (`csv_writer.py`).

Main Module (`main.py`): The main module orchestrates the program's execution flow, leveraging the following data structures:

- **Circuit Object:** An instance of the `Circuit` class from `circuit.py`, encapsulating the entire circuit's structure, including components and terminations.

- **Results array:** A list for the circuit's subclass of solved terminations for CSV output.

Circuit Analysis Module (`circuit.py`): Central to circuit analysis, this module employs:

- **Circuit Class:** Contains the circuit's comprehensive data, with arrays for instances of the component, termination, and output subclasses.
  - **Component List:** A list of component objects (resistors, capacitors, etc.), detailing type, value, and connections (e.g. {"n1": 1, "n2": 2, "value": 100, "type": "R"}).
  - **Terminations Dictionary:** Stores the source and load terminations parameters (e.g., {"VT": 5, "RS": 50}).
  - **Output Requirements List:** Lists the output variables as defined in the input file's order (e.g. {"name": Vin, "unit": V, "magnitude": m, "is_db": true}).
- **NumPy Arrays:** Employed for constructing and manipulating ABCD matrices, facilitating the numerical analysis of the electrical circuits. These arrays provide efficient handling of complex numbers and matrix operations essential for ABCD matrix calculations.

Net File Parser Module (`net_parser.py`): Responsible for interpreting the circuit definition file, it utilizes:

- **Regular Expressions (Regex):** For identifying component definitions and extracting pertinent information. This is especially useful as it can allow for optional fields,flexible use of whitespace and has extremely robust pattern matching, this also lets us define the correct form of a line for each section in the input file, playing nicely into exception raising when a line doesn't get a match.
- **Lists and Dictionaries:** To organize components, terminations, and output specifications for subsequent processing.

CSV Writer Module (`csv_writer.py`): Manages output file creation, employing:

- **Lists:** To compile analysis results for output variables across specified frequencies.
- **File Handler:** A standard object for writing formatted results to a CSV file/tempfile.
- **Magnitude Lookup:** A dictionary of magnitude multipliers for converting results to the desired units (e.g., "m": 1e-3, "u": 1e-6).

B. Functions and methods overview

This section provides an overview of the primary functions and methods within the program's modules, detailing their purpose and functionality.

Input File Parsing

The parsing of the input file is a critical initial step for the circuit analysis program, involving several key tasks to correctly interpret or sanatise the provided data for circuit components, terminations, and desired outputs. The process is outlined as follows:

1) **Reading the File:** Open and read the contents of the '.net' file line-by-line, paying special attention to lines starting with the hash symbol (#) as comments and thus skipping them during processing.
2) **Identifying Blocks:** Systematically identify the three main blocks within the file: CIRCUIT, TERMS, and OUTPUT, each of which provides essential data for the circuit analysis.
3) **Extracting Component Data:** Within the CIRCUIT block, extract details of each component, including node connections and component values (resistance, inductance, capacitance, or conductance).
4) **Source and Load Termination:** From the TERMS block, determine the terminal connections provided for the source and load terminations, along with their respective values if available.
5) **Output Requirements:** In the OUTPUT block, capture the required output variables and formats, ensuring the program knows what results to calculate and how to format them.
6) **Error Handling:** Implement robust error handling to manage potential issues in the input file, such as missing/duplicate blocks, incorrect formatting, or unsupported component types/values.
7) **Pattern Matching:** Utilize regular expressions to identify and extract the required data from the input file, to help with resilience and flexibility in handling different input file formats.
   This requires that the cases where the output is in decibels or inputs/outputs with exponent prefixes are handled and stored for the extension tasks.
8) **Storing Data:** Efficiently store the extracted information in the Circuit class module, to the respective component, termination, and output sub-classes.

This structured approach ensures that the program can flexibly interpret and process the wide range of circuit definitions it may encounter.

Circuit Realization and Solving

To realize and solve the electrical circuit defined in the input file, a systematic approach towards constructing and analyzing the circuit using the ABCD matrix method is as follows:

1) **Circuit Representation:** Construct an internal representation of the circuit from the parsed data, an array of component objects, and the source and load terminations. This can then be sorted based on the node connections to facilitate the ABCD matrix construction.
2) **Matrix Construction:** Implement functions to calculate the ABCD matrices for individual circuit elements (resistors, inductors, capacitors, and any series or parallel combinations thereof).
3) **Cascade Handling:** A method to create a new array of 2x2 sub-ABCD matricies from the components object

array, allowing for the multiplication reduction down to an individual ABCD matrix to represent the entire circuit's behavior.
4) **Termination Analysis:** Apply the source and load terminations as defined in the TERMS block to the overall circuit matrix to determine input/output impedance and thus Vin, Iin, Vout, and Iout. This requires that there are different methods for if the source is of Thevenin or Norton type to determine Vin/Iin.
5) **Solving the Circuit:** Utilize the inversion of the ABCD matrix of the whole circuit to solve for the desired output variables such as input/output impedance, voltage gain, and power gain.
6) **Error and Exception Handling:** Implement comprehensive error checking and exception handling to print an empty output file with an error message if the circuit analysis fails at any stage.
7) **Result storage:** Repeat the above and store the results for each frequency iteration in an array, to be passed to the CSV writer for output file generation.

Output File Generation

The final step in the program is to generate the output file with the calculated results. This involves the following steps:

1) **CSV File Creation:** Create a new CSV file with the specified output filename and write the header row with the required output variables names and units.
   This also requires that the cases where the output is in decibels or with exponent prefixes are handled, and that the order of the headers matches the output array order.
2) **Data Writing:** Write the calculated results to the CSV file, ensuring the order (as specified in the OUTPUT block and stored in the output array), and the formatting (decibels, exponent prefixes) in scientific notation, are correctly applied.
3) **File formatting:** Improve the readability of the file by padding the columns to be equal widths and aligning the values to one side, matching the provided example output files.
   This function should be able to operate on any CSV file.
4) **Error Handling:** Implement error handling to write an empty output file with an error message if the output file generation fails at any stage.

Extension Tasks

All of the extension tasks rely on the input file parsing being versatile enough to encompass the additional features, the approach to if the output is in dB or has additional exponent prefixes will be to store that to the output array and then convert the results to dB + Phase in the CSV writer and/or apply the exponent prefix.

Similar to determining if the source is of Thevenin or Norton type, the program will need to differentiate between if the frequency sweep is linear or logarithmic, which can also be done with a simple check of which sufficient values were provided by the input.

As for input values, the exponent will be converted on the spot with the input parser, this means that internally, all calculations are standardised to the base unit for consistency.

For all the above tasks, the input parser will pick them all up with regular expressions, these parameters being optional and the program will be able to handle them if they are present or not.

III. Testing Methodology

Testing is an integral part of the development process, ensuring that each component of the program functions correctly and as expected. For this project, testing is focused on ensuring the accuracy and reliability of the electrical circuit analysis program, particularly in the calculation functions and input file parsing. The methodology employs a combination of Python doctests for function-level testing and manual testing with modified input files for regex and error handling validation.

A. Python Doctests

Doctests are a convenient way to embed tests in the documentation strings (docstrings) of Python functions. They are ideal for testing individual functions, especially those involved in calculations, data manipulation, and specific logic implementations. Important functions within modules like `circuit.py` and `net_parser.py` will be tested to confirm their correctness. For instance:

- In `circuit.py`, doctests will validate the ABCD matrix calculations for different circuit components, ensuring that the matrix operations produce the expected outcomes.
- In `net_parser.py`, doctests will test the component parsing logic, ensuring that circuit components are accurately extracted from input strings.

These tests are executed automatically as part of the documentation review process, offering a quick and integrated way to validate function outputs against expected results.

B. Regex and Error Handling Testing

For regex testing and error handling, a manual approach is adopted due to the complexity and variability of input files. This involves creating a set of modified example input files that specifically target edge cases, malformed inputs, and unusual component arrangements. The aim is to:

- Ensure that the regex patterns correctly match and extract component information, even in the presence of variations in spacing, line endings, and format deviations.
- Validate that the program can gracefully handle errors in the input file, such as missing blocks, unsupported component types, or incorrect formatting, by raising appropriate exceptions or producing meaningful error messages.

This manual testing approach is crucial for assessing the robustness and reliability of the input parsing and error

handling mechanisms of the program.

Besides the testing, edge cases will be handled with exception raising, and the program will be able to handle any input file that is in the correct format, and will raise an exception if it is not thanks to the regex, but also functions will have checks against invalid inputs, such as negative or zero frequencies, partially defined sources and will raise exceptions if these are encountered.

IV. Conclusion

The combination of doctests and manual testing provides a comprehensive testing strategy that covers both function-level correctness and the overall robustness of the program against malformed or unexpected inputs. By ensuring that each component functions as expected and that the program can handle errors gracefully, this testing methodology supports the development of a reliable and accurate electrical circuit analysis tool.