# Design and Implementation Report on Electrical Circuit Analysis Program

EE20084 - Structured Programming

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# Contents



# 1 Introduction

This report outlines the development process of an electrical circuit analysis program, as specified in the structured programming coursework. It aims to detail the problem analysis, design decisions, and testing strategies that align with the provided marking rubric.

# 2 Analysis of the Problem

The main objective of the assignment is to create a program that analyzes electrical circuits using two-port ABCD matrix analysis, with functionalities to read an input ".net" file, perform the analysis calculations, and output the results in the specified CSV format.

## 2.1 Sub-tasks Identification

- Parsing the input file to extract circuit components, terminations, and desired outputs.
- Malformed input file handling.
- Translating those components into a matrix representation for analysis.
- Calculatinng the ABCD matrix for the circuit.
- Applying the ABCD matrix to the input and output terminations to obtain the desired results.
- Logic error handling and exception raising.
- Generating output files with the analysis results.
- Extending the program to include additional features such as exponent prefixes and decibel calculations.

# 3 Module realisation and design decisions

This section breaks down the program into modules, classes and functions, and explains the design decisions made for each.
The program is divided into four modules, each with a specific role:

- `net_parser.py`: Parses the input file and extracts circuit information.
- `circuit.py`: Contains classes and functions for circuit analysis.
- `csv_writer.py`: Manages the creation and formatting of the output file with analysis results.
- `main.py`: The main driver script that utilizes the above modules.

From a broad view, due to the flexibale nature of the input file, the program is designed to be modular and flexible in kind. The circuit module is designed as a class and subclass structure, with the main Circuit class containing the component array, the source and load terminations, and the output array. The subclasses are instances of the components, terminations, and output variables which are then appended to their respective arrays to keep track of their order. The main class has the methods to add to and sort these arrays, and to recusively reduce and invert the component matricies to obtain the ABCD termination solutions.

The ordering of output array is then used to generate the output CSV, and it is formatted to match the provided example output files.

## 3.1 Data Structures

This section outlines the primary data structures utilized within the main module (`main.py`), the circuit analysis module (`circuit.py`), and other modules such as the net file parser (`net_parser.py`) and the CSV writer (`csv_writer.py`).

### Main Module (`main.py`)

The main module orchestrates the program's execution flow, leveraging the following data structures:

- **Circuit Object:** An instance of the `Circuit` class from `circuit.py`, encapsulating the entire circuit's structure, including components and terminations.
- **Results array:** A list for the circuit's subclass of solved terminations for CSV output.

### Circuit Analysis Module (`circuit.py`)

Central to circuit analysis, this module employs:

- **Circuit Class:** Contains the circuit's comprehensive data, with arrays for instances of the component, termination, and output subclasses.
  - **Component List:** A list of component objects (resistors, capacitors, etc.), detailing type, value, and connections (e.g. {`"n1"`: 1, `"n2"`: 2, `"value"`: 100, `"type"`: "R"}).
  - **Terminations Dictionary:** Stores the source and load terminations parameters (e.g., {`"VT"`: 5, `"RS"`: 50}).
  - **Output Requirements List:** Lists the output variables as defined in the input file's order (e.g. {`"name"`: Vin, `"unit"`: V, `"magnitude"`: m, `"is_db"`: true}).
- **NumPy Arrays:** Employed for constructing and manipulating ABCD matrices, facilitating the numerical analysis of the electrical circuits. These arrays provide efficient handling of complex numbers and matrix operations essential for ABCD matrix calculations.

### Net File Parser Module (`net_parser.py`)

Responsible for interpreting the circuit definition file, it utilizes:

- **Regular Expressions (Regex):** For identifying component definitions and extracting pertinent information.
- **Lists and Dictionaries:** To organize components, terminations, and output specifications for subsequent processing.

### CSV Writer Module (`csv_writer.py`)

Manages output file creation, employing:

- **Lists:** To compile analysis results for output variables across specified frequencies.
- **File Handler:** A standard object for writing formatted results to a CSV file/tempfile.
- **Magnitude Lookup:** A dictionary of magnitude multipliers for converting results to the desired units (e.g., `"m"`: 1e-3, `"u"`: 1e-6).

## 3.2 Functions and methods overview

## Input File Parsing

The parsing of the input file is a critical initial step for the circuit analysis program, involving several key tasks to correctly interpret or sanatise the provided data for circuit components, terminations, and desired outputs. The process is outlined as follows:

1. **Reading the File:** Open and read the contents of the '.net' file line-by-line, paying special attention to lines starting with the hash symbol (#) as comments and thus skipping them during processing.
2. **Identifying Blocks:** Systematically identify the three main blocks within the file: CIRCUIT, TERMS, and OUTPUT, each of which provides essential data for the circuit analysis.

3. **Extracting Component Data:** Within the CIRCUIT block, extract details of each component, including node connections and component values (resistance, inductance, capacitance, or conductance).

4. **Source and Load Termination:** From the TERMS block, determine the source and load characteristics, including type (Thevenin or Norton) and values.

5. **Output Requirements:** In the OUTPUT block, capture the required output variables and formats, ensuring the program knows what results to calculate and how to format them.

6. **Error Handling:** Implement robust error handling to manage potential issues in the input file, such as missing/duplicate blocks, incorrect formatting, or unsupported component types/values.

7. **Pattern Matching:** Utilize regular expressions to identify and extract the required data from the input file, to help with resilience and flexibility in handling different input file formats.
   This requires that the cases where the output is in decibels or inputs/outputs with exponent prefixes are handled and stored for the extension tasks.

8. **Storing Data:** Efficiently store the extracted information in the Circuit class module, to the respective component, termination, and output sub-classes.

This structured approach ensures that the program can flexibly interpret and process the wide range of circuit definitions it may encounter.

## Circuit Realization and Solving

To realize and solve the electrical circuit defined in the input file, a systematic approach towards constructing and analyzing the circuit using the ABCD matrix method is as follows:

1. **Circuit Representation:** Construct an internal representation of the circuit from the parsed data, an array of component objects, and the source and load terminations. This can then be sorted based on the node connections to facilitate the ABCD matrix construction.

2. **Matrix Construction:** Implement functions to calculate the ABCD matrices for individual circuit elements (resistors, inductors, capacitors, and any series or parallel combinations thereof).

3. **Cascade Handling:** A method to create a new array of 2x2 sub-ABCD matricies from the components object array, allowing for the multiplication reduction down to an individual ABCD matrix to represent the entire circuit's behavior.

4. **Termination Analysis:** Apply the source and load terminations as defined in the TERMS block to the overall circuit matrix to determine input/output impedance and thus Vin, Iin, Vout, and Iout.

5. **Solving the Circuit:** Utilize the inversion of the ABCD matrix of the whole circuit to solve for the desired output variables such as input/output impedance, voltage gain, and power gain.

6. **Error and Exception Handling:** Implement comprehensive error checking and exception handling to print an empty output file with an error message if the circuit analysis fails at any stage.

7. **Result storage:** Repeat the above and store the results for each frequency iteration in an array, to be passed to the CSV writer for output file generation.

## Output File Generation

The final step in the program is to generate the output file with the calculated results. This involves the following steps:

1. **CSV File Creation:** Create a new CSV file with the specified output filename and write the header row with the required output variables names and units.
   This also requires that the cases where the output is in decibels or with exponent prefixes are handled, and that the order of the headers matches the output array order.

2. **Data Writing:** Write the calculated results to the CSV file, ensuring the order (as specified in the OUTPUT block and stored in the output array), and the formatting (decibels, exponent prefixes) in scientific notation, are correctly applied.

3. **File formatting:** Improve the readability of the file by padding the columns to be equal widths and aligning the values to one side, matching the provided example output files.
   This function should be able to operate on any CSV file.

4. **Error Handling:** Implement error handling to write an empty output file with an error message if the output file generation fails at any stage.