Test case 1:
Memory blocks: 1024, 4567, 6484, 7894 ; 4 Simulations each
Sequential:

Simulation started with 1024 memory blocks and test case: Sequential Sequence
Simulation started with 4567 memory blocks and test case: Sequential Sequence
Simulation started with 6484 memory blocks and test case: Sequential Sequence
Simulation started with 7894 memory blocks and test case: Sequential Sequence

Memory Access Count: 64
Cache Hit Count: 16
Cache Miss Count: 48
Cache Hit Rate: 25.00%
Cache Miss Rate: 75.00%
Average Memory Access Time: 7.75 ns
Total Memory Access Time: 496.00 ns

Memory Access Count: 64
Cache Hit Count: 16
Cache Miss Count: 48
Cache Hit Rate: 25.00%
Cache Miss Rate: 75.00%
Average Memory Access Time: 7.75 ns
Total Memory Access Time: 496.00 ns

Memory Access Count: 64
Cache Hit Count: 16
Cache Miss Count: 48
Cache Hit Rate: 25.00%
Cache Miss Rate: 75.00%
Average Memory Access Time: 7.75 ns
Total Memory Access Time: 496.00 ns

Random:

Simulation started with 1024 memory blocks and test case: Random Sequence
Simulation started with 4567 memory blocks and test case: Random Sequence
Simulation started with 6484 memory blocks and test case: Random Sequence
Simulation started with 7894 memory blocks and test case: Random Sequence

Memory Access Count: 128
Cache Hit Count: 26
Cache Miss Count: 102
Cache Hit Rate: 20.31%
Cache Miss Rate: 79.69%
Average Memory Access Time: 8.17 ns
Total Memory Access Time: 1046.00 ns

Memory Access Count: 128
Cache Hit Count: 22
Cache Miss Count: 106
Cache Hit Rate: 17.19%
Cache Miss Rate: 82.81%
Average Memory Access Time: 8.45 ns
Total Memory Access Time: 1082.00 ns

Memory Access Count: 128
Cache Hit Count: 38
Cache Miss Count: 90
Cache Hit Rate: 29.69%
Cache Miss Rate: 70.31%
Average Memory Access Time: 7.33 ns
Total Memory Access Time: 938.00 ns

Memory Access Count: 128
Cache Hit Count: 35
Cache Miss Count: 93
Cache Hit Rate: 27.34%
Cache Miss Rate: 72.66%
Average Memory Access Time: 7.54 ns
Total Memory Access Time: 965.00 ns

Mid-Repeat:

Simulation started with 1024 memory blocks and test case: Mid-Repeat Blocks
Simulation started with 4567 memory blocks and test case: Mid-Repeat Blocks
Simulation started with 6484 memory blocks and test case: Mid-Repeat Blocks
Simulation started with 7894 memory blocks and test case: Mid-Repeat Blocks

Memory Access Count: 95
Cache Hit Count: 24
Cache Miss Count: 71
Cache Hit Rate: 25.26%
Cache Miss Rate: 74.74%
Average Memory Access Time: 7.73 ns
Total Memory Access Time: 734.00 ns

Memory Access Count: 95
Cache Hit Count: 24
Cache Miss Count: 71
Cache Hit Rate: 25.26%
Cache Miss Rate: 74.74%
Average Memory Access Time: 7.73 ns
Total Memory Access Time: 734.00 ns

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Memory Access Count: 95
Cache Hit Count: 24
Cache Miss Count: 71
Cache Hit Rate: 25.26%
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Average Memory Access Time: 7.73 ns
Total Memory Access Time: 734.00 ns
```


```
Memory Access Count: 95
Cache Hit Count: 24
Cache Miss Count: 71
Cache Hit Rate: 25.26%
Cache Miss Rate: 74.74%
Average Memory Access Time: 7.73 ns
Total Memory Access Time: 734.00 ns
```