Test cases:
Memory blocks: 1024, 4567, 6484, 7894 ; 4 Simulations each
Sequential Sequence:

Simulation started with 1024 memory blocks (Sequential Sequence)
Final cache memory snapshot.
Step 1: Accessed Block 0 (Cache Miss)
Step 2: Accessed Block 32 (Cache Miss)
Step 3: Accessed Block 64 (Cache Miss)
Step 4: Accessed Block 96 (Cache Miss)
Step 5: Accessed Block 128 (Cache Miss)
Step 6: Accessed Block 160 (Cache Miss)
Step 7: Accessed Block 192 (Cache Miss)

Block	Data
0	0
32	512
64	1024
96	1536
128	2048
160	2560
192	3072
224	3584
256	4096
288	4608
320	5120
352	5632
384	6144
416	6656
448	7168
480	7680
512	8192
544	8704
576	9216
608	9728
640	10240
672	10752
704	11264
736	11776
768	12288
800	12800
832	13312
864	13824
896	14336
928	14848
960	15360
992	15872

Memory Access Count: 128
Cache Hit Count: 96
Cache Miss Count: 32
Cache Hit Rate: 75.00%
Cache Miss Rate: 25.00%
Average Memory Access Time: 3.25 ns
Total Memory Access Time: 416.00 ns

Simulation started with 4567 memory blocks (Sequential Sequence)
Final cache memory snapshot.
Step 1: Accessed Block 0 (Cache Miss)
Step 2: Accessed Block 142 (Cache Miss)
Step 3: Accessed Block 284 (Cache Miss)
Step 4: Accessed Block 426 (Cache Miss)
Step 5: Accessed Block 568 (Cache Miss)
Step 6: Accessed Block 710 (Cache Miss)
Step 7: Accessed Block 852 (Cache Miss)

Block	Data
4498	71968
73	1168
215	3440
357	5712
499	7984
641	10256
783	12528
925	14800
1067	17072
1209	19344
1351	21616
1493	23888
1635	26160
1777	28432
1919	30704
2061	32976
2203	35248
2345	37520
2487	39792
2629	42064
2771	44336
2913	46608
3055	48880
3197	51152
3339	53424
3481	55696
3623	57968
3765	60240
3907	62512
4049	64784
4191	67056
4333	69328

Memory Access Count: 128
Cache Hit Count: 0
Cache Miss Count: 128
Cache Hit Rate: 0.00%
Cache Miss Rate: 100.00%
Average Memory Access Time: 10.00 ns
Total Memory Access Time: 1280.00 ns

Simulation started with 6484 memory blocks (Sequential Sequence)
Final cache memory snapshot.
Step 1: Accessed Block 0 (Cache Miss)
Step 2: Accessed Block 202 (Cache Miss)
Step 3: Accessed Block 404 (Cache Miss)
Step 4: Accessed Block 606 (Cache Miss)
Step 5: Accessed Block 808 (Cache Miss)
Step 6: Accessed Block 1010 (Cache Miss)
Step 7: Accessed Block 1212 (Cache Miss)

Block	Data
6424	102784
142	2272
344	5504
546	8736
748	11968
950	15200
1152	18432
1354	21664
1556	24896
1758	28128
1960	31360
2162	34592
2364	37824
2566	41056
2768	44288
2970	47520
3172	50752
3374	53984
3576	57216
3778	60448
3980	63680
4182	66912
4384	70144
4586	73376
4788	76608
4990	79840
5192	83072
5394	86304
5596	89536
5798	92768
6000	96000
6202	99232

Memory Access Count: 128
Cache Hit Count: 0
Cache Miss Count: 128
Cache Hit Rate: 0.00%
Cache Miss Rate: 100.00%
Average Memory Access Time: 10.00 ns
Total Memory Access Time: 1280.00 ns

Simulation started with 7894 memory blocks (Sequential Sequence)
Final cache memory snapshot.
Step 1: Accessed Block 0 (Cache Miss)
Step 2: Accessed Block 246 (Cache Miss)
Step 3: Accessed Block 492 (Cache Miss)
Step 4: Accessed Block 738 (Cache Miss)
Step 5: Accessed Block 984 (Cache Miss)
Step 6: Accessed Block 1230 (Cache Miss)
Step 7: Accessed Block 1476 (Cache Miss)

Block	Data
7828	125248
180	2880
426	6816
672	10752
918	14688
1164	18624
1410	22560
1656	26496
1902	30432
2148	34368
2394	38304
2640	42240
2886	46176
3132	50112
3378	54048
3624	57984
3870	61920
4116	65856
4362	69792
4608	73728
4854	77664
5100	81600
5346	85536
5592	89472
5838	93408
6084	97344
6330	101280
6576	105216
6822	109152
7068	113088
7314	117024
7560	120960

Memory Access Count: 128
Cache Hit Count: 0
Cache Miss Count: 128
Cache Hit Rate: 0.00%
Cache Miss Rate: 100.00%
Average Memory Access Time: 10.00 ns
Total Memory Access Time: 1280.00 ns

Random Sequence:

Simulation started with 1024 memory blocks (Random Sequence)
Final cache memory snapshot.
Step 1: Accessed Block 54 (Cache Miss)
Step 2: Accessed Block 321 (Cache Miss)
Step 3: Accessed Block 699 (Cache Miss)
Step 4: Accessed Block 783 (Cache Miss)
Step 5: Accessed Block 958 (Cache Miss)
Step 6: Accessed Block 193 (Cache Miss)
Step 7: Accessed Block 809 (Cache Miss)

Block	Data
967	15472
902	14432
230	3680
100	1600
487	7792
278	4448
124	1984
538	8608
665	10640
658	10528
348	5568
205	3280
985	15760
146	2336
0	0
763	12208
77	1232
777	12432
687	10992
133	2128
710	11360
545	8720
86	1376
514	8224
615	9840
326	5216
980	15680
415	6640
196	3136
549	8784
929	14864
64	1024

Memory Access Count: 128
Cache Hit Count: 3
Cache Miss Count: 125
Cache Hit Rate: 2.34%
Cache Miss Rate: 97.66%
Average Memory Access Time: 9.79 ns
Total Memory Access Time: 1253.00 ns

Simulation started with 4567 memory blocks (Random Sequence)
Final cache memory snapshot.
Step 1: Accessed Block 3738 (Cache Miss)
Step 2: Accessed Block 3812 (Cache Miss)
Step 3: Accessed Block 27 (Cache Miss)
Step 4: Accessed Block 291 (Cache Miss)
Step 5: Accessed Block 3026 (Cache Miss)
Step 6: Accessed Block 3162 (Cache Miss)
Step 7: Accessed Block 3905 (Cache Miss)

Block	Data
2125	34000
1525	24400
3616	57856
4416	70656
536	8576
656	10496
700	11200
949	15184
780	12480
2849	45584
2804	44864
1766	28256
907	14512
1418	22688
4342	69472
2660	42560
810	12960
1748	27968
2846	45536
2207	35312
214	3424
1148	18368
447	7152
3185	50960
4217	67472
1567	25072
705	11280
466	7456
1373	21968
3595	57520
3113	49808
3184	50944

Memory Access Count: 128
Cache Hit Count: 1
Cache Miss Count: 127
Cache Hit Rate: 0.78%
Cache Miss Rate: 99.22%
Average Memory Access Time: 9.93 ns
Total Memory Access Time: 1271.00 ns

Simulation started with 6484 memory blocks and test case: Random Sequence
Final cache memory snapshot.
Step 1: Accessed Block 4232 (Cache Hit)
Step 2: Accessed Block 2697 (Cache Hit)
Step 3: Accessed Block 5201 (Cache Hit)
Step 4: Accessed Block 4249 (Cache Hit)
Step 5: Accessed Block 3198 (Cache Hit)
Step 6: Accessed Block 3099 (Cache Hit)
Step 7: Accessed Block 1605 (Cache Hit)

Block	Data
4053	64848
1972	31552
5273	84368
3242	51872
5242	83872
3277	52432
4307	68912
3024	48384
4891	78256
4623	73968
4712	75392
5256	84096
1451	23216
723	11568
264	4224
5418	86688
3188	51008
2679	42864
2913	46608
1910	30560
1842	29472
2692	43072
1603	25648
4595	73520
4673	74768
1406	22496
4651	74416
3911	62576
3210	51360
1605	25680
843	13488
5684	90944

Memory Access Count: 128
Cache Hit Count: 1
Cache Miss Count: 127
Cache Hit Rate: 0.78%
Cache Miss Rate: 99.22%
Average Memory Access Time: 9.93 ns
Total Memory Access Time: 1271.00 ns

Simulation started with 7894 memory blocks (Random Sequence)
Final cache memory snapshot.
Step 1: Accessed Block 2612 (Cache Miss)
Step 2: Accessed Block 1501 (Cache Miss)
Step 3: Accessed Block 4807 (Cache Miss)
Step 4: Accessed Block 4791 (Cache Miss)
Step 5: Accessed Block 1646 (Cache Miss)
Step 6: Accessed Block 6903 (Cache Miss)
Step 7: Accessed Block 289 (Cache Miss)

Block	Data
6178	98848
969	15504
4987	79792
5827	93232
6121	97936
5002	80032
5246	83936
7095	113520
1977	31632
6407	102512
161	2576
7043	112688
534	8544
772	12352
2125	34000
1918	30688
6837	109392
1148	18368
6585	105360
1981	31696
2772	44352
2024	32384
3054	48864
6672	106752
1479	23664
2362	37792
7577	121232
6272	100352
7087	113392
2943	47088
2743	43888
2347	37552

Memory Access Count: 128
Cache Hit Count: 2
Cache Miss Count: 126
Cache Hit Rate: 1.56%
Cache Miss Rate: 98.44%
Average Memory Access Time: 9.86 ns
Total Memory Access Time: 1262.00 ns

Mid-Repeat Sequence:

Simulation started with 1024 memory blocks (Mid-Repeat Blocks)
Final cache memory snapshot.
Step 1: Accessed Block 0 (Cache Miss)
Step 2: Accessed Block 32 (Cache Miss)
Step 3: Accessed Block 64 (Cache Miss)
Step 4: Accessed Block 96 (Cache Miss)
Step 5: Accessed Block 128 (Cache Miss)
Step 6: Accessed Block 160 (Cache Miss)
Step 7: Accessed Block 192 (Cache Miss)

Block	Data
0	0
32	512
64	1024
96	1536
128	2048
160	2560
192	3072
224	3584
256	4096
288	4608
320	5120
352	5632
384	6144
416	6656
448	7168
480	7680
512	8192
544	8704
576	9216
608	9728
640	10240
672	10752
704	11264
736	11776
768	12288
800	12800
832	13312
864	13824
896	14336
928	14848
960	15360
992	15872

Memory Access Count: 160
Cache Hit Count: 65
Cache Miss Count: 95
Cache Hit Rate: 40.63%
Cache Miss Rate: 59.38%
Average Memory Access Time: 6.34 ns
Total Memory Access Time: 1015.00 ns

Simulation started with 4567 memory blocks (Mid-Repeat Blocks)
Final cache memory snapshot.
Step 1: Accessed Block 0 (Cache Miss)
Step 2: Accessed Block 142 (Cache Miss)
Step 3: Accessed Block 284 (Cache Miss)
Step 4: Accessed Block 426 (Cache Miss)
Step 5: Accessed Block 568 (Cache Miss)
Step 6: Accessed Block 710 (Cache Miss)
Step 7: Accessed Block 852 (Cache Miss)

Block	Data
4498	71968
73	1168
215	3440
357	5712
499	7984
641	10256
783	12528
925	14800
1067	17072
1209	19344
1351	21616
1493	23888
1635	26160
1777	28432
1919	30704
2061	32976
2203	35248
2345	37520
2487	39792
2629	42064
2771	44336
2913	46608
3055	48880
3197	51152
3339	53424
3481	55696
3623	57968
3765	60240
3907	62512
4049	64784
4191	67056
4333	69328

Memory Access Count: 160
Cache Hit Count: 32
Cache Miss Count: 128
Cache Hit Rate: 20.00%
Cache Miss Rate: 80.00%
Average Memory Access Time: 8.20 ns
Total Memory Access Time: 1312.00 ns

Simulation started with 6484 memory blocks (Mid-Repeat Blocks)
Final cache memory snapshot.
Step 1: Accessed Block 0 (Cache Miss)
Step 2: Accessed Block 202 (Cache Miss)
Step 3: Accessed Block 404 (Cache Miss)
Step 4: Accessed Block 606 (Cache Miss)
Step 5: Accessed Block 808 (Cache Miss)
Step 6: Accessed Block 1010 (Cache Miss)
Step 7: Accessed Block 1212 (Cache Miss)

Block	Data
6424	102784
142	2272
344	5504
546	8736
748	11968
950	15200
1152	18432
1354	21664
1556	24896
1758	28128
1960	31360
2162	34592
2364	37824
2566	41056
2768	44288
2970	47520
3172	50752
3374	53984
3576	57216
3778	60448
3980	63680
4182	66912
4384	70144
4586	73376
4788	76608
4990	79840
5192	83072
5394	86304
5596	89536
5798	92768
6000	96000
6202	99232

Memory Access Count: 160
Cache Hit Count: 32
Cache Miss Count: 128
Cache Hit Rate: 20.00%
Cache Miss Rate: 80.00%
Average Memory Access Time: 8.20 ns
Total Memory Access Time: 1312.00 ns

Simulation started with 7894 memory blocks (Mid-Repeat Blocks)
Final cache memory snapshot.
Step 1: Accessed Block 0 (Cache Miss)
Step 2: Accessed Block 246 (Cache Miss)
Step 3: Accessed Block 492 (Cache Miss)
Step 4: Accessed Block 738 (Cache Miss)
Step 5: Accessed Block 984 (Cache Miss)
Step 6: Accessed Block 1230 (Cache Miss)
Step 7: Accessed Block 1476 (Cache Miss)

Block	Data
7828	125248
180	2880
426	6816
672	10752
918	14688
1164	18624
1410	22560
1656	26496
1902	30432
2148	34368
2394	38304
2640	42240
2886	46176
3132	50112
3378	54048
3624	57984
3870	61920
4116	65856
4362	69792
4608	73728
4854	77664
5100	81600
5346	85536
5592	89472
5838	93408
6084	97344
6330	101280
6576	105216
6822	109152
7068	113088
7314	117024
7560	120960

Memory Access Count: 160
Cache Hit Count: 32
Cache Miss Count: 128
Cache Hit Rate: 20.00%
Cache Miss Rate: 80.00%
Average Memory Access Time: 8.20 ns
Total Memory Access Time: 1312.00 ns