DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
UNIVERSITY OF BARISHAL

Final EXAMINATION

Course Title: Digital Logic Design
Course Code: CSE-2103
2nd Year 1st Semester
Session: 2018-19

Time: 3 hour

Marks: 60

Answer any five Questions from the followings.

1. a) What are the advantages and disadvantages of Digital Technology? [3]

   b) Convert $35.65_{(10)}$ to Binary, Octal and Hex number system. [4]

   c) Explain parity bit method for error correction. [2]

   d) Consider a bit string, 1011. Using a parity bit generator and a parity bit checker circuit, show how even parity bit method works in a communication system. [3]

2. a) What do you understand by Universality of logic gate? Show that the NOR gate is a Universal gate. [4]

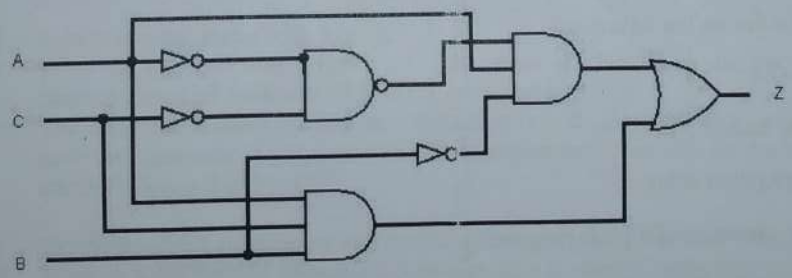
   b) Prove DeMorgan's Theorem. [2]

   c) What are different methods to write a logical expression from truth table? Explain with an example. [3]

   d) Explain K-Map method to simplify a logic circuit. [3]

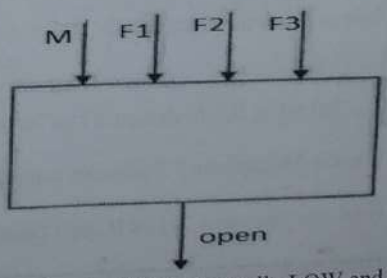
3. a) Design a logic circuit with inputs P, Q, R so that output S is HIGH whenever P is '0' or whenever Q=R=1. [3]

   b) Simply the logic circuit shown below: [2]



   c) Design a Full Adder. [4]

   d) Design a logic circuit that controls the elevator door in a three-story building. The circuit has four inputs. M is a logic signal that indicates when the elevator in moving (M=1) or stopped (M=0). F1, F2 and F3 are floor indicator signals that are normally LOW, and they go HIGH only when the elevator is positioned at the level of that particular floor. For example, when the elevator is lined up level with the second floor, F2=1 and F1=F3=0. The circuit output is the OPEN signal, which is normally LOW and will go to HIGH when the elevator door is to be opened. Find the simplified design and draw the circuit diagram of the elevator circuit. Because the elevator cannot be lined up with more [3]

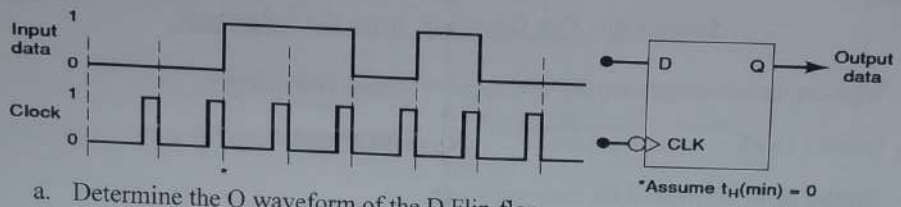


than one floor at a time, the cases when more than one floor inputs are high can be treated as don't care condition. When the elevator reaches at one floor and stops, the door opens.

4. a) What is a Flip Flop? Briefly explain the function of a JK-Flip Flop with suitable circuit diagram. [3]

b) What is the limitation of S-R FlipFlop? Explain how the limitation can be resolved. [3]

c) A D FF is sometimes used to delay a binary waveform so that the binary information appears at the output a certain amount of time after it appears at the D input. [6]



a. Determine the Q waveform of the D Flip-flop.
b. How can a delay of two clock periods can be obtained?

5. a) What is the limitation of a parallel adder? Using 74LS83 ICs, draw a 12 bit parallel Adder. [3]

b) Explain how 2's complement system can facilitate arithmetic operations in digital computing. [3]

c) Draw a parallel adder/subtractor using 2's-complement system. Using your designed circuit, explain steps to subtract 4 from -3. Consider that your designed circuit receives only positive input. [6]

6. a) What is Counter? What are the differences between Synchronous and Ripple counter? [2]

b) Draw a Mod-14 and a Decade ripple counter with their state transition diagram. [4]

c) Show how to wire the 74293 IC as a MOD-6 counter. [2]

d) Explain the operation of a Synchronous up/down MOD-8 counter with an appropriate diagram. [4]

7. a) Write short notes on the followings: [4]

I) Fan-Out

II) Noise Immunity

III) Propagation delay

IV) Characteristics of TTL logic gate.

b) Design and explain the working principle of a TTL NOR gate. [4]

c) Draw the circuit diagram of a CMOS NAND gate. [2]

d) A certain TTL IC output is rated at I_{OH}(max) = 800 μA and I_{OL} = 48 mA. Express the IC's fan-out in terms of unit loads. [consider 1UL = 40 μA in the HIGH state and 1.6 mA in the LOW state] [2]

8. a) Use 74LS138 ICs to design a 1 of 32 decoder. [4]

b) What is Multiplexer? Design an 8-input MUX and explain its operation. [4]

c) How can you use a 74138 IC as a DEMUX. [2]

d) Draw the logic diagram for the 7442 BCD to decimal decoder. [2]