DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
UNIVERSITY OF BARISHAL

FINAL EXAMINATION
2nd Year 1st Semester; Session 2018-19 Rahat Sir

Course Title: Digital Logic Design

Course Code: CSE-2103

Time: 3 hours **Marks:** 60

Answer any five Questions from the followings.

1. a) Implement the Boolean function: [3]

$$F = xy + x'y' + y'z$$

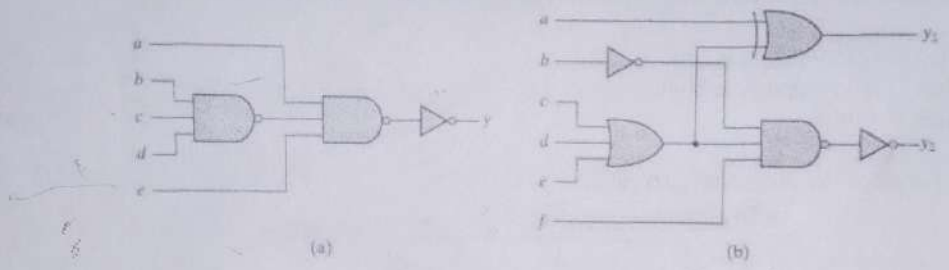
i. With AND, OR, and inverter gates ,

ii. With NOR and inverter gates,

iii. With NAND and inverter gates

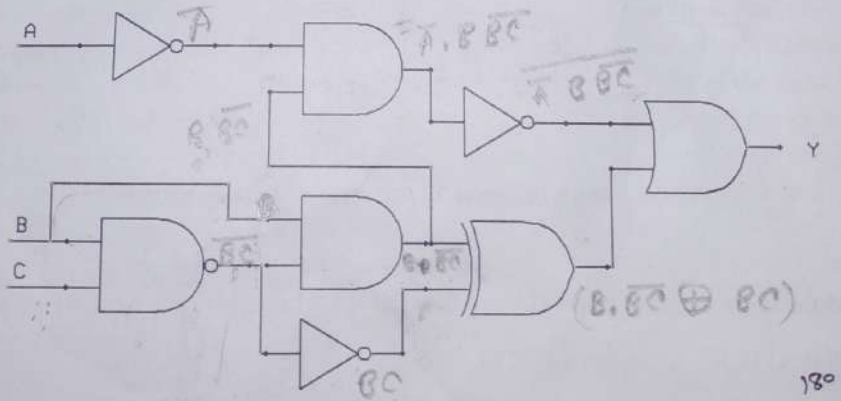
b) Show that a p that a positive logic NAND gate is a negative logic NOR gate and vice versa. [3]

c) Write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the following logic diagrams: [6]



2. a) Design a logic circuit with inputs P, Q, R so that output S is HIGH whenever P is '1' or whenever Q=R=0. [3]

b) Simply the logic circuit shown below: [2]



c) Design a Full Adder. [5]

d) Draw a Full Adder using two half adders. [2]

3. a) Explain how a S-R FlipFlop store a bit. [3]

b) What is the limitation of S-R FlipFlop? Explain how the limitation can be resolved. [4]

c) Define Race Around condition in J-K FlipFlop. How can you overcome the problem? Explain with an appropriate figure and waveforms. [5]

4. a) What is the limitation of a parallel adder? Using 74LS83 ICs, draw a 12 bit parallel Adder.

b) Explain how 2's complement system can facilitate arithmetic operations in digital computing. [3]

c) Draw a parallel adder/subtractor using 2's-complement system. Using your designed circuit, explain steps to subtract 4 from -3. Consider that your designed circuit receives only positive input. [6]

5. a) Explain the working principle of a Synchronous up/down MOD-16 counter with an appropriate diagram. [7]

b) Use two 74293 ICs to design a mod 50 counter. [5]

6. a) Show the circuit of a four-input NAND and NOR gates using CMOS transistors. [4]

b) Construct an exclusive-OR circuit with two inverters and two transmission gates. [4]

c) For the following conditions, list the transistors that are off and the transistors that are conducting in the three-state TTL gate of Fig (a). (for Q1 and Q6. it is necessary to list the states in the base-emitter and base--collector junctions separately): [4]

i) When C is low and A is low.
ii) When C is low and A is high.
iii) When C is high.

What is the state of the output in each case?

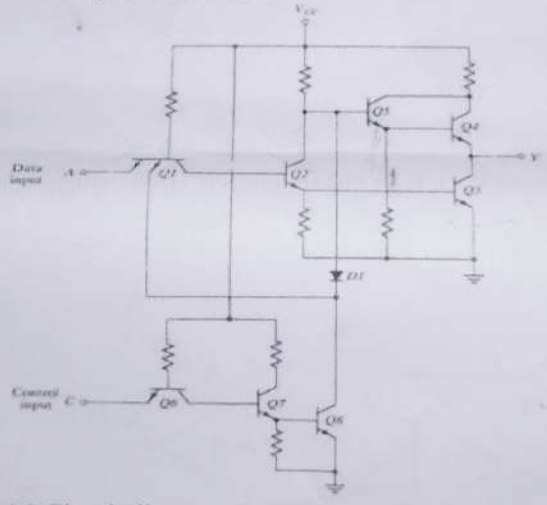


Fig (a) Circuit diagram for the three-stale Inverter gate

7. a) Draw the logic diagram of a 74LS138 decoder IC. Also explain its working principle. [5]

b) Use 74LS138 ICs to design a 1 of 24 decoder. [4]

c) How Liquid Crystal Display (LCD) works? [3]

8. a) Design a 16 input multiplexer using 74151 ICs. [4]

b) With appropriate diagram explain the working principle of a 1 line to 8 line demultiplexer. [5]

c) How can you use a 74LS138 IC as a DEMUX. [3]

Good Luck!!!