Avalon MM Master Interface Simulator Compiler User Guide

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1 I. Input arguments:
   - (1) *.av source to be compiled [by default: \"instruction.av\"]
    - (2) Verilog definition subfolder path [by default that is in the root] - Compiled file output: \"<source>.mem\" stored in the root directory.
3
4
5
    - Verilog definition file output: \"avsim_define.v\" stored in the root directory.
6 II. Acceptable Operating Codes (case-insensitive):
7
    - 1. nop: No operation for an Avalon cycle
    - 2. read: Reads the data from the specific address
8
9
    - 3. write: Writes the data to the specific address
10
    - 4. wait: Waiting until the specified cycles defined by the data
11
    - 5. load: Loading the timing parameters (see later)
12 III. Input Source Format:
    13
14
    - 2. Comment: ; <any comments>
15
    - 3. Operating code, address and data must be separated by non-alphanumeric character e.g.
     white space.
    - 4. Comment section is not mandatory at the end, use the ';' key if needed.
16
17
    - 5. It is valid to use single line comment without instruction
18 IV. Limits:
19
    - 1. Each line (including the comment) is limited to 100 character.
20
    - 2. 4 Byte address and data in hexadecimal format.
     - 3. Maximum value of program counter: 999.
21
22 V. Timing settings: 1 Byte format with the usage of LOAD operating code.
23
    - 1. data: <Hold><ReadLatency><WriteWait><ReadWait> (MSB --> LSB)
24
    -2. \text{ address: } 0 \times 0000000 < \text{Setup} > (MSB \longrightarrow LSB)
25
    - 3. Example: \"load 11 2233aa01; setting avalon timing parameters\"
26
    => Setup: 0x11, ReadWait: 0x01, WriteWait: 0xaa, ReadLatency: 0x33, Hold: 0x22
27 VI. Input Source Format Error Handling:
28
    - 1. The specific line of the compiled output will be commented out in case of any source
29
    - 2. Compiler is able to distinguish the 3 different type of errors: opcode, address, data.
    - There will be placed an 'X' key where the input error is occurred.
30
31 VII. Source Example:
32
    ; Initialization
33
    load 0 00020001; Timing parameters: ReadWait = 1, ReadLatency = 2
34
    read 5 0
                     ; get module status
35
36
    ; Setting the module I/O data
37
    write 0 1235fe; setting the dividend
                     ; setting the divisor
38
    write 1 a12
39
    write 2 1
                     ; starting the module
40
    write 2 0
41
    wait 0 5
                    ; waiting for completion
42
    nop 0 0
                     ; wait one more cycle
43
44
    ; Obtaining the results
45
    read 3 0
                     ; get quotient
    read 4 a12
46
                     ; get remainder
47
48
    ; Integer Division Module Address Mapping
49
        0x00: 32-bit dividend (cpu write)
50
        0x01: 32-bit divisor (cpu write)
51
        0x02: start operation (cpu write)
52
        0x03: 32-bit quotient (cpu read)
        0x04: 32-bit remainder (cpu read)
53
54
        0x05: bit 0: 1-bit ready (cpu read)
```

55

0x06: bit 0: 1-bit done_trg (cpu read/write)

Avalon Memory-Mapped Slave Timing Parameters

Setup:	* Iming Catua:
	Setup:
Read wait: 0	Read wait: 0
Write wait: 0	Write wait: 0
Hold: 0	Hold: 0
I ming units: Cycles	Timing units: Cycles V
▼ Pipelined Transfers	▼ Pipelined Transfers
Read latency: 0	Read latency: 0
Maximum pending read transactions: 0	Maximum pending read transactions: 0
Burst on burst boundaries only	
	Burst on burst boundaries only
Linewrap bursts	Linewrap bursts
▼ Read Waveforms	▼ Read Waveforms
	Note Water Stills
clk	clk
write	write
chipselect	chipselect
address A0	address A0
readdata D0	readdata X D0
* Write Waveforms	▼ Write Waveforms
clk	cik
write	write
chipselect	chipselect
address A0	addressX_A0
writedata	writedata D0
D - £14	0-1 1
Default	Setup = 1
* Timing	* Timing
Setup: 0	Setup: 0
Read wait: 1	Read wait: 0
Write wait: 0	Write wait:
Hold: 0	Hold: 0
	•
Timing units:	Timing units:
▼ Pipelined Transfers	▼ Pipelined Transfers
Read latency: 0	Read latency: 0
Maximum pending read transactions: 0	Maximum pending read transactions:
Burst on burst boundaries only	Burst on burst boundaries only
Linewrap bursts	Linewrap bursts
▼ Read Waveforms	▼ Read Waveforms
clk	clk
write	write
write	write
chipselect	
chipselect address A0	chipselect
chipselect address readdata A0 D0	chipselect address Paddata D0
chipselect address A0	chipselect address A0
chipselect address readdata A0 D0 Write Waveforms	chipselect address readdata D0 Write Waveforms
chipselect address readdata D0 D0 Write Waveforms	chipselect address readdata D0 Write Waveforms
chipselect address readdata Write Waveforms clk write	chipselect address readdata D0 Write Waveforms clk write
chipselect address readdata D0 D0 * Write Waveforms clk write chipselect	chipselect address readdata White Waveforms clk write chipselect
chipselect address readdata D0 D0 * Write Waveforms clk write chipselect address A0	chipselect address readdata Write Waveforms clk write chipselect address A0
chipselect address readdata D0 D0 *Write Waveforms clk write chipselect address A0 Writedata D0 D0	chipselect address readdata Write Waveforms CIK write chipselect address writedata D0 A0 Write Waveforms
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Chipselect address A0	Chipselect
Chipselect address A0	Chipselect
Chipselect address A0	chipselect address readdata
Chipselect address A0	Chipselect
Chipselect address A0	chipselect address readdata Write Waveforms clk write chipselect address writedata D0 Write wait = 1 Timing Setup: Read wait: Write wait: Hold: Timing units: Cycles
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Chipselect address A0	chipselect address readdata Write Waveforms clk write chipselect address writedata D0 Write wait = 1 Timing Setup: Read wait: Write wait: Urite w
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chipselect address readdata Write Waveforms clk write chipselect address writedata Read wait = 1 Timing Setup: Read wait: 0 Read wait: Urite wait: Hold: 1 Timing units: Cycles Pipelined Transfers Read latency: Maximum pending read transactions: Burst on burst boundaries only Linewrap bursts Read Waveforms clk write chipselect address A0 A0 A0 A0 A0 A0 A0 A0 A0	chipselect address readdata Write Waveforms clk write chipselect address writedata Do Write wait = 1 Timing Setup: Read wat: Write wait: Hold: Timing units: Cycles Pipelined Transfers Read latency: Maximum pending read transactions: Burst on burst boundaries only Linewrap bursts Read Waveforms clk write chipselect address A0 A0 A0 A0 A0 A0 A0 A0 A0
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Chipselect address A0	chipselect address readdata With Waveforms clk write chipselect address writedata Do Write wait = 1 Timing Setup: Read wait: Write wait: Hold: Timing units: Cycles Pipelined Transfers Read latency: Maximum pending read transactions: Burst on burst boundaries only Burst on burst boundaries only Linewrap bursts Read Waveforms clk write chipselect address readdata With Waveforms clk write chipselect address readdata A0 With Waveforms