SEMICONDUCTORS

Q1.What are indirect and direct band gap semiconductors?

(M.U. Dec 2019)[3 Marks]

Direct band gap semiconductors: The semiconductors in which the top of valence band and the bottom of conduction band **occur at the same momentum** ($\boldsymbol{p} = \hbar \boldsymbol{k}$) as shown in *Figure 1a* are known as direct band gap semiconductors. **Si** and **Ge** are examples of indirect band gap semiconductors.

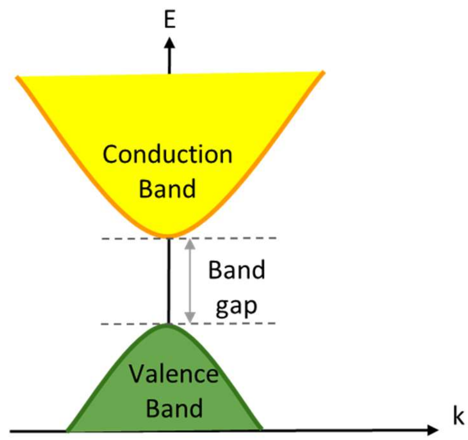

Figure 1a: Direct Band Gap

Indirect band gap semiconductors: The semiconductors in which the top of valence band and the bottom of conduction band **do not occur at the same momentum** ($\boldsymbol{p} = \hbar \boldsymbol{k}$) as shown in *Figure 1b* are known as indirect band gap semiconductors. **GaAs** and **InP** are examples of direct band gap semiconductors.

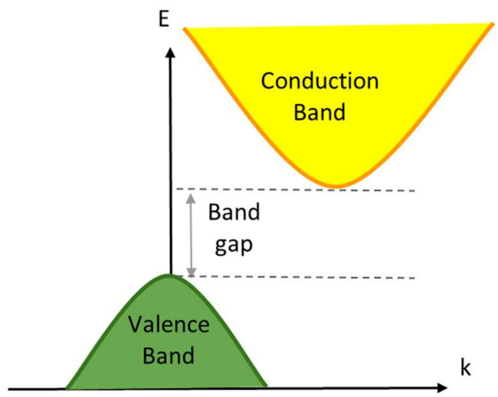

Figure 1b: Indirect Band Gap

Q2. Define drift velocity, mobility of charge, conductivity (σ), and resistivity (ρ) and state relation between them.

(M.U. May 2015, 2016; Dec 2013)[3 Marks]

Drift velocity (v_d): The net displacement of an electron's position per unit time in the steady state under the influence of electric field is called **drift velocity.**

Mobility of charge/electrons (μ): is defined as the magnitude of drift velocity obtained by the electron per unit electric field 'E'. It is given by $\mu = \frac{vd}{E}$. Mobility represents the ease with which an electron could drift in a material.

Conductivity (σ): Conductivity is the physical property that shows the conducting ability of a material. It is given by $\sigma = ne\mu$ where, n= charge carrier concentration and e= electronic charge =1.6×10^{-19} C.

Resistivity (ρ): Resistivity is the physical property of a material which shows the resistance 'R' of the material for given dimension (A= area of cross section, L length) of the wire. It is the inverse of conductivity. It is given by $\rho = \frac{1}{\sigma} = \frac{RA}{L}$.

Q3. Difference between intrinsic and extrinsic semiconductors.

Sr. No.	INTRINSIC SEMICONDUCTOR	EXTRINSIC SEMICONDUCTOR
1	They are **pure** semiconductors	They are **impure** or **doped** semiconductors
2	The charge carriers can be increased by **increasing the temperature**	The charge carriers can be increased by **increasing** the percentage of **impurities** or **doping**
3	**More energy** is required for electrons to cross band gap (E_g)	Less energy is required for electrons to cross (E_g)
4	**Pure** silicon or germanium are intrinsic semiconductors	When a semiconductor is doped by a **third group impurity** it forms a **P-type**

		extrinsic semiconductor and when doped by a **fifth group impurity** it forms an **N-type** extrinsic semiconductor.

Q4. What is Fermi level?

(M.U. May 2012, 2014; Dec 2013, 2015, 2019)[3-5 Marks]

Fermi level is defined as the **highest occupied energy level** of electrons at **absolute zero temperature.**

As shown in *Figure 4* 'E_F' denotes the Fermi level at 0^0K. All the energy levels above Fermi level are empty (white color) and those below Fermi level are filled (Blue shaded region).

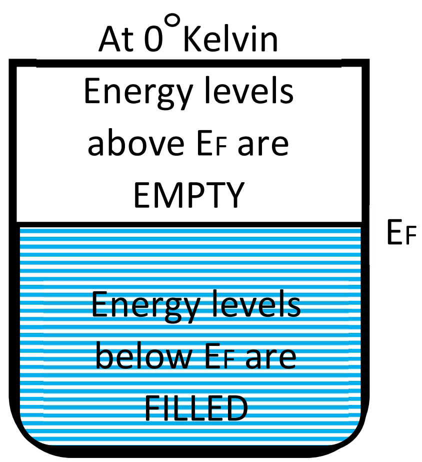

Figure 4: Fermi Level

It helps to assume that electrons in a semiconductor is like some water in a jar as shown in *Figure 4*. The level up to which the electrons (water) are (is) filled is the Fermi level. If concentration of electrons increases Fermi level rises and if concentration of electrons falls Fermi level drops.

Q5. Explain Fermi-Dirac distribution function.

Fermi-Dirac Distribution function F (E): The Fermi-Dirac distribution function F (E) represents the probability of an energy level with energy 'E' to be occupied by an electron. It is given by

$$\mathbf{F(E)} = \frac{\mathbf{1}}{\mathbf{1+e^{\frac{(E-E_F)}{KT}}}} \text{ ----- } (1)$$

Where,

F (E) = probability that a particular energy level 'E' is occupied

E_F = Fermi energy,

K = Boltzmann constant and

T = temperature

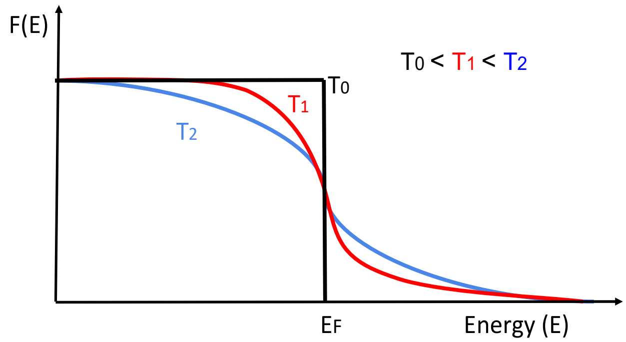

Figure 5: Fermi Dirac distribution

In *Figure 5* the black line shows that at '$T_0=0^0K$', for $E < E_F$ the $F(E)=1$ while for $E > E_F$ the $F(E)=0$. This can be mathematically shown as:

1. At $T = T_0=0^0K$
   a. Case A : F(E) for level at 'x' energy lower than fermi level ($E < E_F$)

      $$\therefore F\,(E) = \frac{1}{1+\exp\left(\frac{-x}{0}\right)} = \frac{1}{1+e^{-\infty}} = \frac{1}{1+\frac{1}{e^{\infty}}} = \frac{1}{1+e^{\infty}} = 1$$

      Conclusion A: At 0^0K all energy levels below fermi level are filled

      Mathematically: At 0^0K for $E < E_F$ the F (E) =1

   b. Case B : F(E) for level at 'x' energy higher than fermi level ($E > E_F$)

      $$\therefore F\,(E) = \frac{1}{1+\exp\left(\frac{x}{0}\right)} = \frac{1}{1+e^{\infty}} = \frac{1}{\infty} = 0$$

      Conclusion B: At 0^0K all energy levels above fermi level are empty

      Mathematically: At 0^0K for $E > E_F$ the F (E) = 0

In *Figure 5* the red line indicates that as temperature increases there is a slight probability that energy levels higher than E_F are occupied and ones lower than E_F are empty. The blue one at a higher temperature than red one indicates probability of energy levels higher than E_F being occupied and ones lower than E_F being empty increases as compared to the red line. The point to note is that for any temperature higher than 0^0K at $E = E_F$ the $F(E) = 1/2$. This can be mathematically shown as:

2. At $T = T_1$ or $T_2 > 0^0$K when $E = E_F$

$$\therefore F(E) = \frac{1}{1+ex\ \left(\frac{0}{KT}\right)} = \frac{1}{1+e^0} = \frac{1}{1+1} = \frac{1}{2}$$

Conclusion C: At $T > 0^0$K the fermi level is half filled

Mathematically: At $T > 0^0$K for $E = E_F$ the $F(E) = 1/2$.

Q6. Show that Fermi level for an intrinsic semiconductor lies in the middle of the forbidden energy gap.

(M.U. May 2015, 2017, 2019; Dec 2014, 2015, 2017, 2019) [3-8 Marks]

Pure semiconductors are called intrinsic semiconductors. For intrinsic semiconductors the concentration of electrons (n_e) is equal to the concentration of holes (n_h) which is also called the intrinsic concentration of charge carriers (n_i).

Concentration of charge carriers 'n' in a particular band is given as

$$\therefore n = N \exp(-\Delta E/KT) \text{ ---- } (1)$$

where,

N: maximum capacity or density of states of that band

ΔE: the difference between energy level of the band and fermi level

(KT): thermal energy (Boltzmann constant * temperature in ^{0}K)

Using (1) the concentration of electrons in the conduction band can be written as,

$$n_e = N_c \exp\left(\frac{-(\Delta Ee)}{KT}\right)$$

from *Figure 6* we get,

$$n_e = N_c \exp(\frac{-(E_C - E_F)}{KT}) \text{ -----(2)}$$

Using (1) the concentration of holes in the valence band can be written as,

$$n_e = N_c \exp(\frac{-(\Delta Eh)}{KT})$$

from *Figure 6* we get,

$$n_h = N_v \exp(\frac{-(E_F - E_V)}{KT}) \text{ -----(3)}$$

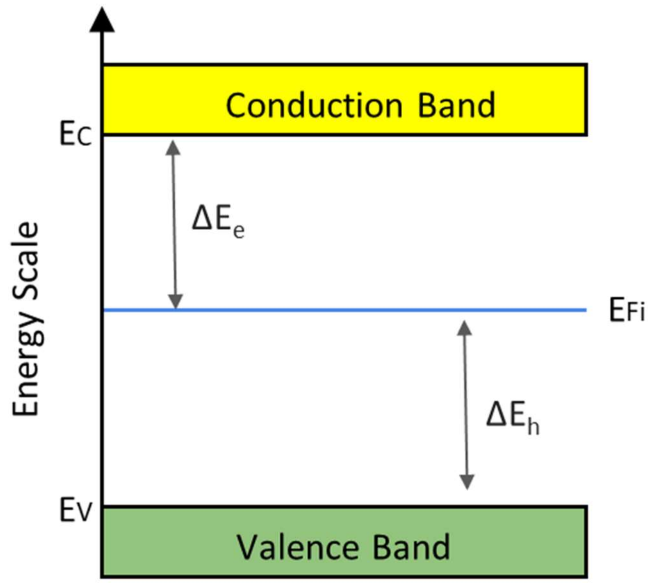

Figure 6: Energy band diagram of an intrinsic semiconductor

For an intrinsic semiconductor as the charge carrier concentrations are equal:

$$n_e = n_h \text{-----(4)}$$

Also, assuming that the density of states in the conduction and the valence bands are nearly same we get,

$$N_c \cong N_v \text{ ----- (4)}$$

Substituting equations (1), (2) and (4) in (3) we get,

$$\exp(\frac{-E_c + E_F}{KT}) = \exp(\frac{-E_F + E_F}{KT})$$

$$\therefore (\frac{-E_c + E_F}{KT}) = (\frac{-E_F + E_F}{KT})$$

$$\therefore -E_C + E_F = -E_F + E_V$$

$$\therefore 2E_F = E_C + E_F$$

$$\therefore E_F = \frac{E_C + E_F}{2}$$

Thus, we can say that the Fermi level in an intrinsic semiconductor lies in the middle of the forbidden energy gap.

Q7. With the help of diagram, explain the variation of Fermi level with temperature in N-type and P-type semiconductors.

(M.U. May 2017, 2018; Dec 2017)[3-5 Marks]

The Fermi level for a **N-type semiconductor** (E_{Fn}) lies close to the conduction band (at 0^0K $E_{Fn} = E_F$). Due to doping of the 5th group impurity donor levels (E_D) filled with electrons are created close to the conduction band just below E_F. As the temperature increases electrons from the E_D are excited to the conduction band. Thus, electrons in E_D get reduced and Fermi level (the indicator of level of electrons) falls with increase in temperature. The variation of E_{Fn} is shown with a curved black line in the *Figure 7a*. While transition from energy position 'E_F' (E_{Fn} at zero K temperature) to 'E_{Fi}' (E_{Fn} at Ti K temperature) in the *Figure 7a* 'T_D' shows the temperature at which the E_{Fn} coincides the E_D, while 'Ti' is the temperature at which E_{Fn} coincides the intrinsic Fermi level (E_{Fi}).

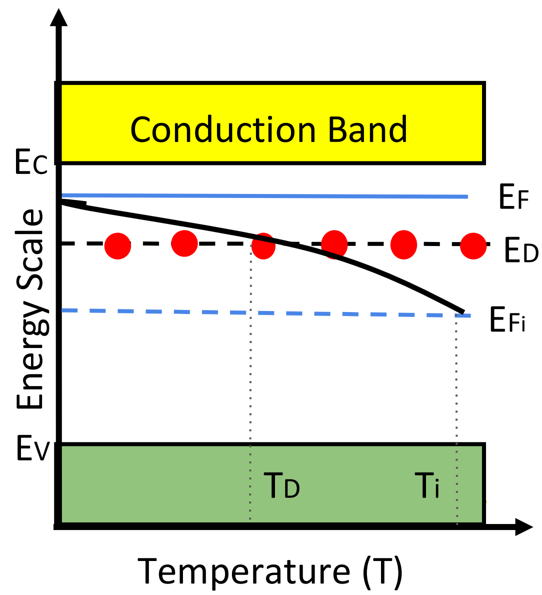

Figure 7a: Variation of EF with T in N-type

The Fermi level for a **P-type semiconductor** (E_{Fp}) lies close to the valence band (at 0^0K $E_{Fp} = E_F$). Due to doping of the 3rd group impurity Acceptor levels (E_A) filled with holes are created close to the valence band just above E_F. As the temperature increases electrons from valence band are excited to the E_A. Thus, there are electrons in E_A, hence Fermi level (the indicator of level of electrons) rises with increase in temperature. The variation of E_{Fp} is shown with a curved black line in the *Figure 7b*. While transition from energy position 'E_F' (E_{Fp} at zero K temperature) to 'E_{Fi}' (E_{Fp} at Ti K temperature) in the *Figure 7b* 'T_A' shows the temperature at which the E_{Fp} coincides the E_A, while 'Ti' is the temperature at which E_{Fp} coincides the intrinsic Fermi level (E_{Fi}).

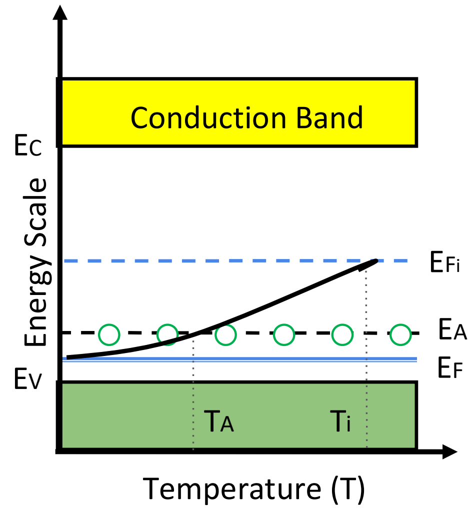

Figure 7b: Variation of EF with T in P-type

Q8. How does the position of Fermi level change with increasing doping concentration in P-type and N-type semiconductors?

(M.U. Dec 2015, 2016)[3-5 Marks]

In an **N-type semiconductor** as the doping concentration increases more electrons get added to the donor levels. Due to increase in the concentration of electrons **Fermi level in N-type (E_{Fn}) rises** indicating this increase.

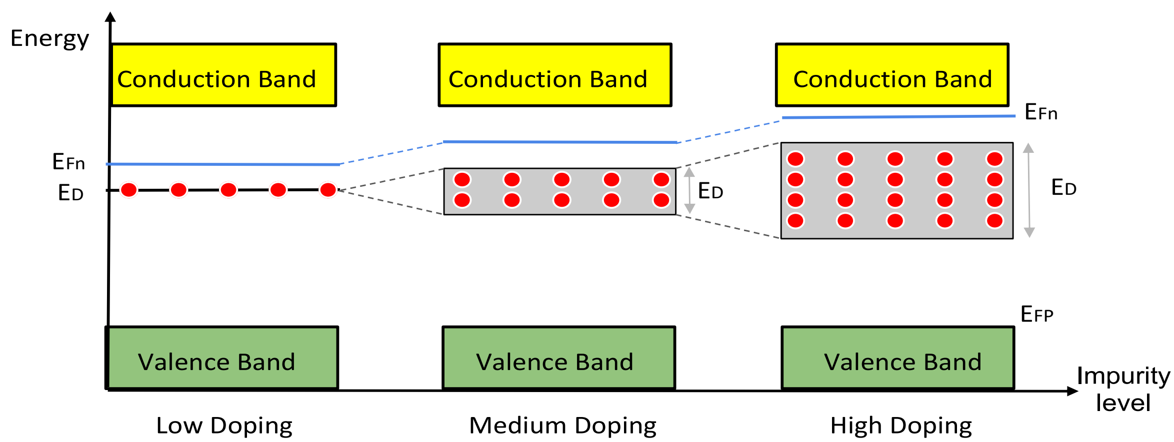

Figure 8a: Effect of Impurity on fermi level of N-type

In a **P-type semiconductor** as the doping concentration increases more holes get added to the acceptor levels. Due to increase in the concentration of holes

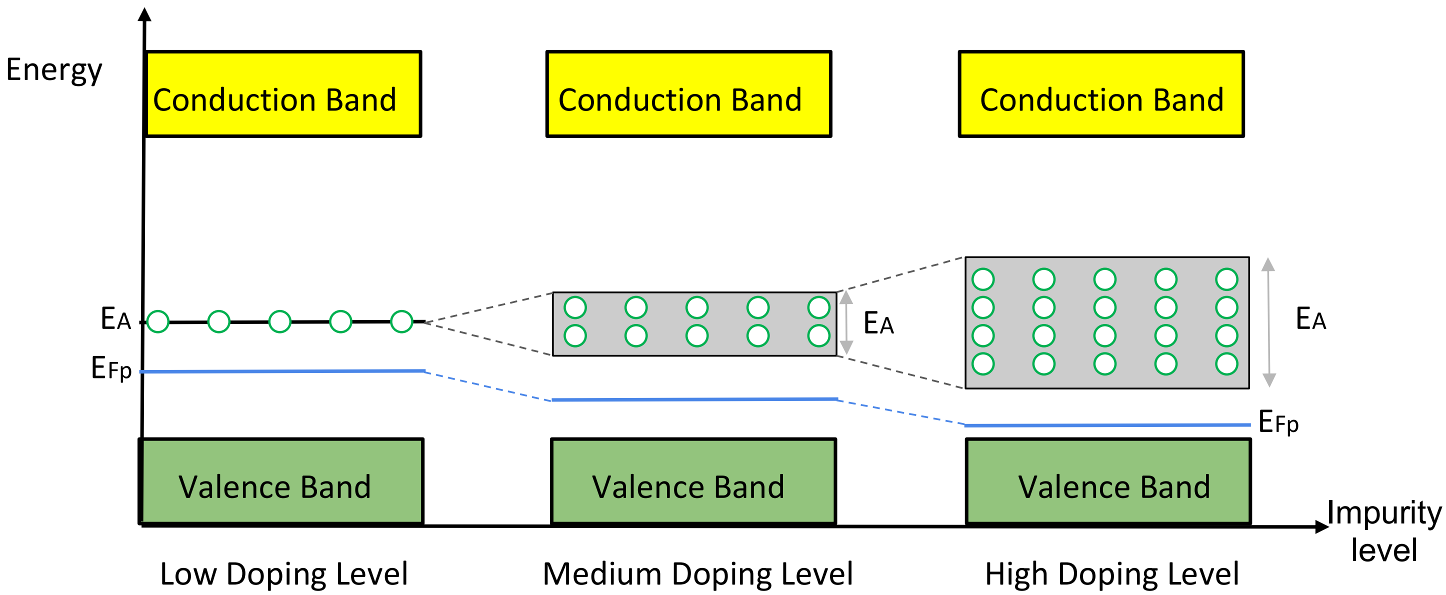

Figure 8b: Effect of Impurity on fermi level of P-type

(implies decrease in concentration of electrons comparatively) **Fermi level in P-type (E_{Fp}) falls** indicating this decrease of electrons relatively.

Q9. Define drift current, diffusion current and current density (J).

(M.U. May 2015, 2016; Dec 2013)[3 Marks]

Drift current (I_{Dr}): When there is a non-uniform distribution of electric field or potential is applied across the semiconducting material, there is a positive charge flow from the region of higher potential to the region of lower potential. Such a flow of charges is called **drift current.**

Diffusion current (I_{Df}): When there is a non-uniform concentration of charge carriers, there is a charge flow from the region of higher concentration to the region of lower concentration. Such a flow of charges is called **diffusion current.** This kind of non-uniform concentration of charge carriers can be formed by thermal or radiation excitation of a part of material or by adding carriers in the material through the surface.

Current density (J): Current density is defined as the current per unit area of cross-section of an imaginary plane held normal to the direction of current in current carrying conductor. It is given by $J = \frac{I}{A}$. Sometimes it is also expressed as J=nev, where n*e is the charge density and 'v' is the velocity of charge carriers giving thereby imparting the product 'nev' dimensions of current density.

Q10. What is Hall Effect? Derive an expression for Hall voltage with neat labelled diagram and give applications of Hall Effect.

(M.U. May 2015, 2016, 2018, 2019; Dec 2012, 2013, 2015, 2018, 2019)

[3-8 Marks]

Hall Effect : When a metal or semiconductor carrying a current 'I' is placed in a transverse magnetic field 'B', an electric emf 'E' is induced in the direction perpendicular to both 'I' and 'B' as shown in *Figure 10*.

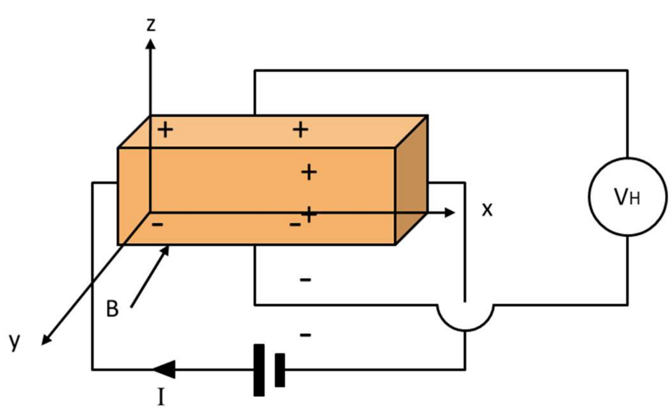

Figure 10: Hall's Effect

This phenomenon is known as Hall Effect and the voltage induced is Hall voltage (V_H).

Derivation for expression of Hall voltage (V_H):

At equilibrium condition in the semiconductor we should have:

Electric force = magnetic force i.e. $F_E = F_M$

$\therefore eE = e\,v\,B$ (here, 'v' is the velocity of charge carriers and 'e' is their charge)

$\therefore E = v\,B$ ----- (1)

Current density by definition is current per unit cross sectional area and it is also expressed as 'nev' so we can write that,

$J = \frac{I}{wd} = nev$ ----- (2)

The relationship between potential and electric field between two surfaces which are at 'd' distance from each other is

$V_H = E\,d$ ----- (3)

Substituting (1) in (3) we get,

$V_H = Bvd$ ----- (4)

Substituting 'v' from (2) in (4) we get,

$V_H = Bd\frac{I}{newd}$

$V_H = \frac{\boldsymbol{BI}}{\boldsymbol{new}}$ ----- (5)

This is the expression for the hall voltage and we find that it is directly proportional to the applied magnetic field and current flowing through the semiconductor and inversely proportional to the charge density and the width of the semiconducting wafer used for Hall Effect. (Sometimes hall voltage is also expressed in terms of hall coefficient $R_H = \frac{\boldsymbol{1}}{\boldsymbol{ne}}$ hence it is then $V_H = R_H\frac{\boldsymbol{BI}}{\boldsymbol{w}}$)

Applications of Hall Effect:

1. Used in magnetic field meter (gauss meter).
2. Charge carrier concentration can be determined.
3. Mobility of charge can be determined.
4. Nature (N-type/P-type) of semiconductor can be determined.

Q11. Write a brief note on a normal diode. Or Draw the energy band diagram of an unbiased p-n junction and mark the barrier potential and depletion region. Or Draw the energy band diagram of p-n junction diode in forward and reverse bias condition.

(M.U. May 2013, 2014; Dec 2013, 2014, 2015, 2016)[3-5 Marks]

A diode is a two-terminal device. The circuit symbol for a diode is a small triangle with a line at the end. The line represents the cathode and the other side of the triangle represents the anode. The most commonly used ordinary diode is a small black cylinder that has a silver-grey ruling at one edge indicating that side to be the cathode. *Figure 11a* and *Figure 11b* shows the circuit symbol of a diode and the cartoon representation of a real diode

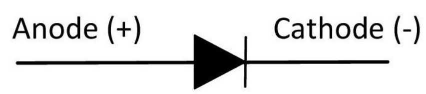

Figure 11a: circuit symbol of diode

Figure 11b: circuit symbol of diode

Construction:

1. The diode consists of a N-type substrate on which a P-Type layer is grown as shown in *Figure 11c*.
2. Metal contacts are provided for the P-side and N-side as anode and cathode connectors.

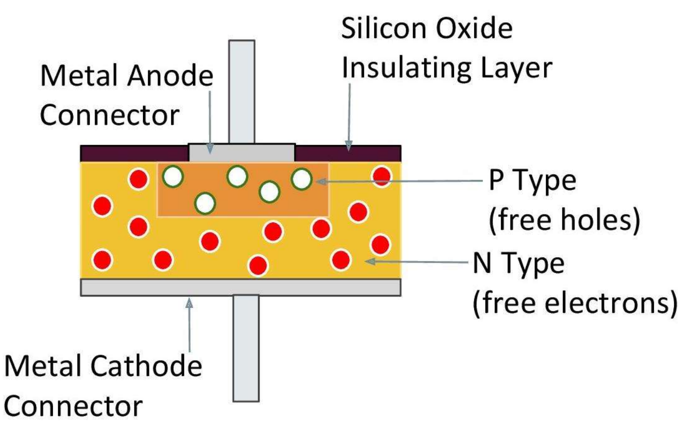

Figure 11c: construction of diode

3. The doping is covered by a thin layer of silicon oxide for insulation.
4. A common boundary between the P-type and N-type semiconductors is called a PN junction.

ZERO bias PN junction, *Figure 11d*:

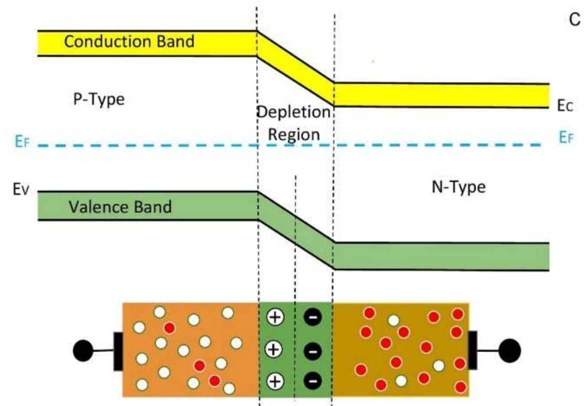

Figure 11d: Diode working in zero bias

1. As the PN junction comes to existence, the electrons from N-side diffuse to P-side and recombine with holes.
2. Electron hole pair recombination at the junction creates a region devoid of charge carriers left with immobile ions only is called the depletion region or the space charge region.
3. The immobile ions in the depletion region create an electric field which further opposes the diffusion of electrons to P-side. Thus, halting the electron hole pair recombination and thereby restricting the growth of depletion region width.
4. The width of the depletion region depends on the doping concentration. Higher the doping concentration, stronger is the field created in the space charge regions and hence thinner is the depletion region.

Forward bias PN junction, *Figure 11e:*

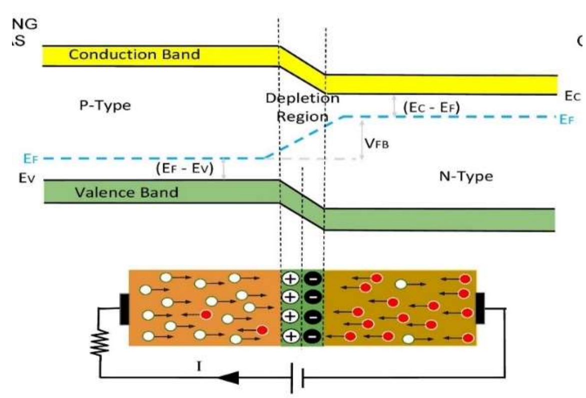

Figure 11e: Forward bias

1. The PN junction is forward biased when the P-side is connected to positive of the battery and the N-side is connected to the negative of the battery.
2. Electrons from the battery pour into the N-side raising the fermi level there wherein the electrons are drained from the P-side dropping the fermi level on this side. This is

indicated by the blue dotted line depicting fermi level for forward bias PN junction in *Figure 11e*.

Reverse bias PN junction, *Figure 11f:*

1. The PN junction is reverse biased when the N-side is connected to positive of the battery and the P-side is connected to the negative of the battery.

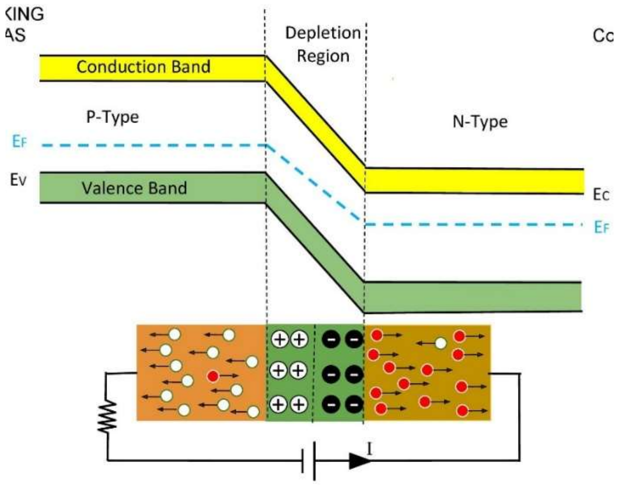

Figure 11f: Reverse bias

2. Electrons from the battery pour into the P-side raising the fermi level there wherein the electrons are drained from the N-side dropping the fermi level on this side. This is indicated by the blue dotted line depicting fermi level for Reverse bias PN junction in Figure 11f.

IV characteristics of diode, *Figure 11g*:

1. **Forward bias characteristics:** As the forward bias applied goes on increasing, initially no current is observed. Once the bias applied becomes greater than the barrier potential in the depletion region (also called knee voltage) the current starts increasing exponentially shown by the red curve.

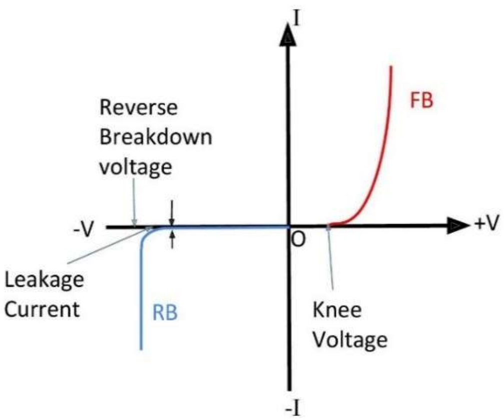

Figure 11g: IVcharacteristics of a diode

2. **Reverse bias characteristics:** As the reverse bias applied goes on increasing, initially very little almost negligible current due to minority

charge carriers is observed. As the bias reaches the breakdown voltage avalanche breakdown occurs and current increases without increasing the reverse voltage. After this stage the diode breaks down and is of no use further. Reverse characteristics is shown by the blue curve.

Q12. Explain the principle, construction and working of a LED.

(M.U. Dec 2015, 2018)[5 Marks]

LED or Light Emitting Diode is a two terminal device which emits light when supplied with electric potential. The circuit symbol of LED is shown in *Figure 12a* is just like the ordinary diode with additional two arrows pointing outward indicating emission of light as its main function. The real LED component looks like *Figure 12b* where the longer leg indicated the anode and the flat spot on the top capsule marks the cathode side.

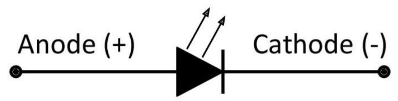

Figure 12a: circuit symbol of LED

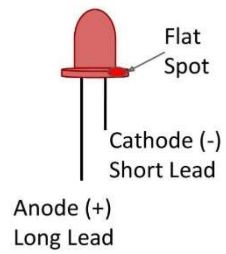

Figure 12b: real LED

An LED is a PN junction diode which functions only in forward bias mode.

Construction:

1. The most common method of constructing an LED is to stack two semiconducting layers on the substrate.
2. Indirect band gap semiconductors like silicon and germanium are used to make ordinary diodes whereas direct band gap materials like gallium arsenide (GaAs), gallium phosphide (GaP), gallium arsenide phosphide (GaAsP) etc. are used in LEDs.

3. The active region is the depletion region created between the p-type and n-type semiconductors as shown in *Figure 12c*.
4. The positive terminal (anode) is connected on top of the p region, while the negative terminal (cathode) is connected below the n region via metal contacts.

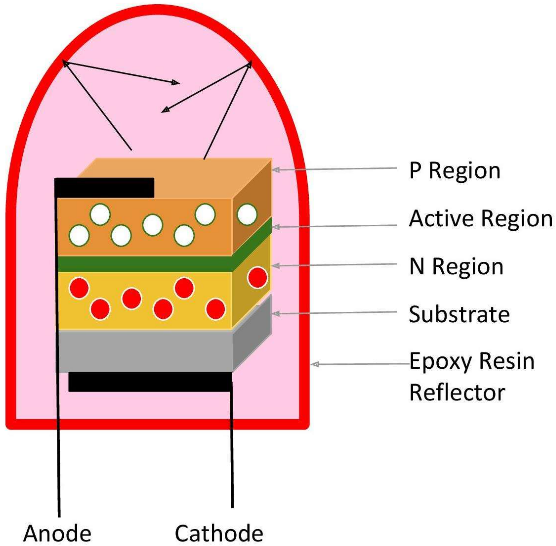

Figure 12c: LED construction

5. Light emerges from the active region when recombination takes place. Since recombination takes place when the electrons move into the holes, the p-layer containing holes is kept above the n-layer containing electrons.
6. Light thus emitted by an LED is spread in all directions. In order to prevent spreading, the structure is placed inside a small reflective hemispherical cup made from a transparent plastic of epoxy resin.
7. The unique shape of the cup helps focus all light in one direction (the top) through reflection because of its unique shape. This makes the device more efficient.

Principle of LED:

When LED is forward biased the electrons in the n-region cross the junction and recombine with the holes in the p-region releasing energy in the form of light.

Working of LED:

1. When a forward bias is applied to the LED, the energy levels of the p and n region become aligned thus allowing the electrons and holes to cross the energy gap as shown in *Figure 12d*.

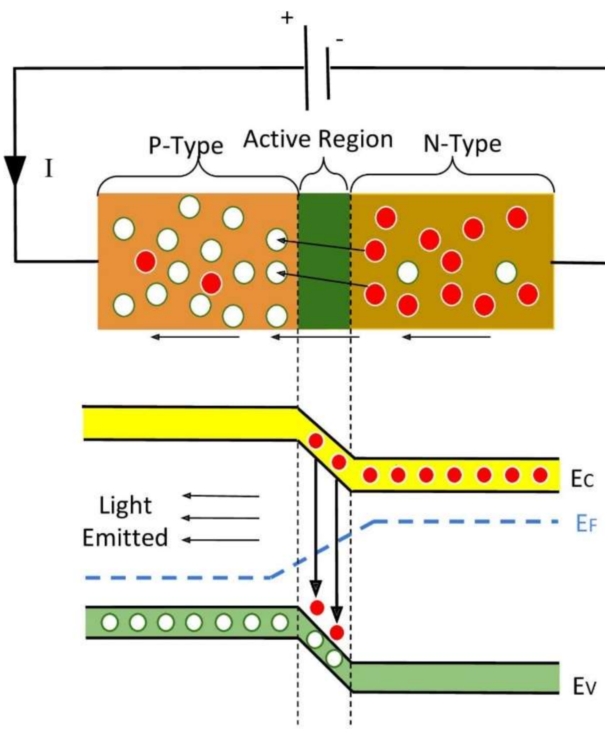

Figure 12d: LED working

2. This happens because the electrons are repulsed by the battery, which causes them to move from the conduction band into the valence band to recombine with the holes.
3. During this process, as the conduction band has a higher energy than valence band, the electrons move from a higher energy level, to a lower energy level to attain stability.
4. This causes them to emit some energy in the form of light. This is caused by the process of recombination.
5. This is how the energy emitted from LEDs is in the form of light.

This represents IV characteristics of an LED through a spectrum of light. As the wavelength of light decreases, the values of forward voltage increase for the same amount of current.

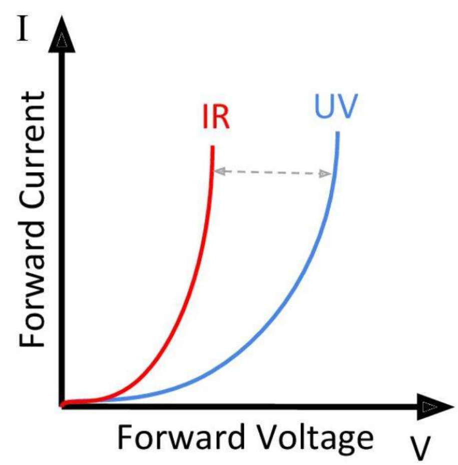

Figure 12e: IV Characteristic of LED

Q13. Explain Zener diode

It is a unique type of diode as shown in *Figure 13a* and *Figure 13b* which works in the breakdown region of the reverse bias mode. It is usually used for voltage regulation.

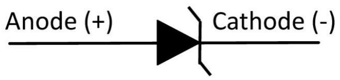

Figure 13a: circuit symbol

Figure 13b: symbol

Construction:

1. A Zener diode is, in essence, a silicon semiconductor which has been metalized to facilitate connections to the anode and cathode as shown in *Figure 13c*.
2. It consists of a heavily doped N-type and P-type substrate, such that the junction between the two is extremely thin.
3. It is insulated with a layer of silicon dioxide to stop the contamination of the junction.

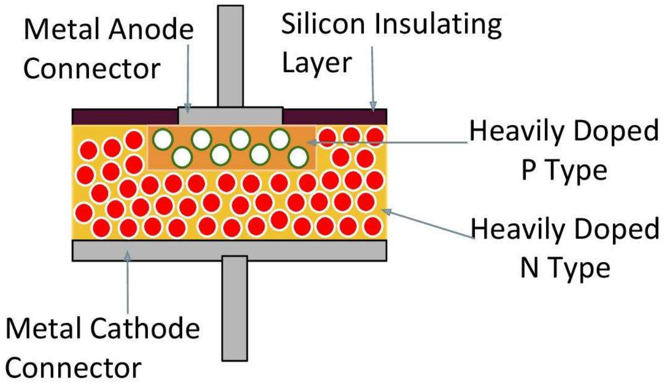

Figure 13c: Zener construction

Working:

1. A zener diode is heavily doped. Due to this the depletion region becomes extremely thin and hence breakdown can occur at a relatively low (reverse-biased) voltage.

2. In a normal diode, breakdown occurs through the avalanche effect. This effect takes place when the depletion region becomes wider due to reverse biased mode as shown in *Figure 13d*.
3. However in a zener diode, breakdown takes place because of an effect called quantum tunneling.
4. As the width of the depletion region in the zener diode is very narrow, when a reverse biased voltage is applied to it, there is a generation of a strong, electric field.

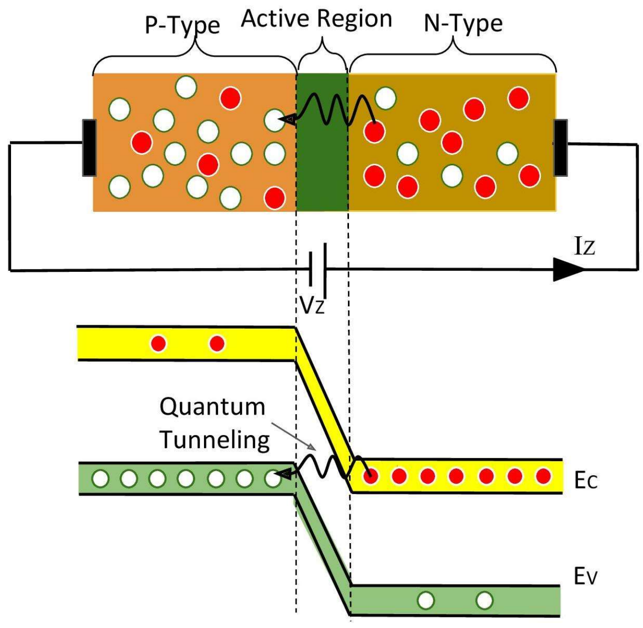

Figure 13d: Zener working

5. When the voltage reaches zener voltage, the energy of the p type conductor increases in such a manner that the energy level of the valence band of the P-type conductor is almost equal to the energy level of the conduction band of the N-type conductor.
6. Hence, as shown in the figure, it becomes difficult for the electrons to climb up to the conduction band on the P-type conductor, but because of the narrow width, they are simply able to "tunnel" through over to the valence band of the P-type conductor. This is the quantum tunneling effect.
7. During this process, because of the movement of free electrons across the junction, a sharp rise in current is obtained. This is Zener Breakdown.

This represents the I/V characteristics of a Zener diode. In reverse biased mode, on increasing the voltage, a sharp increase in the current is seen as shown in *Figure 13e*.

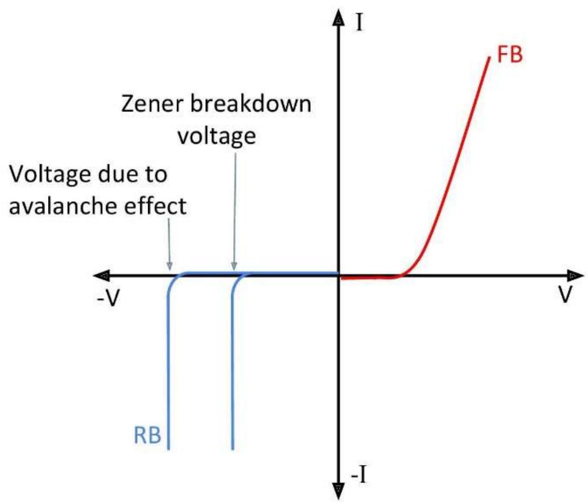

Figure 13e: Zener IV characteristics

1. A Zener diode in forward bias acts exactly like a normal diode.
2. The left half side of the curve is reverse biased.
3. In reverse biased mode, once it hits the breakdown voltage, the current drastically increases. This current which spikes drastically is the breakdown current.
4. The current remains constant after the breakdown voltage.

Q14. What is the photovoltaic effect? Explain the principle and working of solar cells.

(M.U. May 2013, 2014, 2015, 2017, 2018; Dec 2012, 2013 2014, 2017)

[5 Marks]

Photovoltaic effect –

1. When light energy falls on a p-n junction, a potential difference is formed across it.
2. This potential difference is capable of conducting a current through an external circuit.
3. This phenomenon is known as the photovoltaic effect.

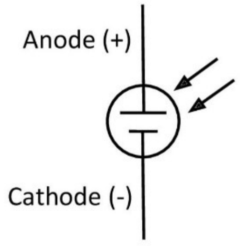

Figure 14a: Solar cell symbol

A solar cell as shown in *Figure 14a* and *Figure 14b* is a device which works on the principle of photovoltaic effect i.e. it converts incoming solar energy into electrical energy. A solar cell is made of semiconducting material. Mostly silicon, cadmium sulphide, gallium arsenide, etc. are used in making solar cells.

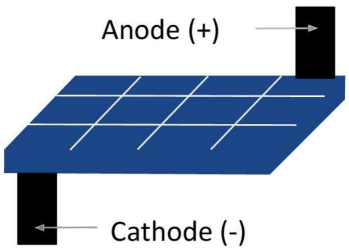

Figure 14b: symbol

Construction –

1. A solar cell is basically a p-n junction connected to an external circuit as shown in *Figure 14c*.
2. The p side of the cell is made thin as compared to the n side. This is to allow the solar energy, incident on the p side, to reach the junction.
3. The top of the solar cell is covered with glass to prevent heat (energy) loss.
4. Metallic grid contacts are fitted on the cell to connect the electrodes.
5. These solar cells are designed such that they are durable and weather resistant.

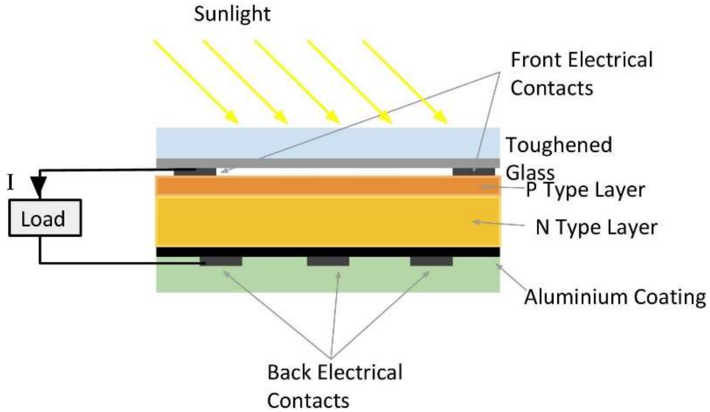

Figure 14c: Construction

Working –

1. In the equilibrium state the Fermi level lies near the conduction band of the n region and the valence band of the p region.

2. When energy in the form of solar radiation falls on the p-n junction, the electrons from the valence band get excited and reach the conduction band as shown in *Figure 14d*.
3. Subsequently, holes are formed in the valence band.
4. This process is known as electron-hole pair generation.

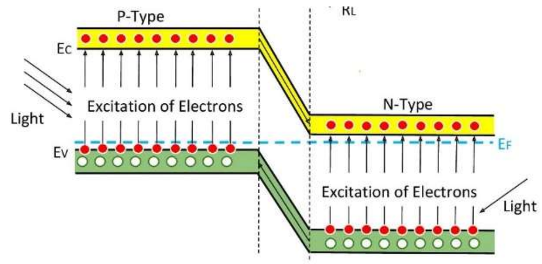

Figure 14d: Working

5. These electrons on the P side of conduction band, freely move to the N side while holes from the N side of the valence band, freely move to the P side.
6. The flow of these charge carriers results in the formation of current in solar cells.
7. This current produced is found to be directly proportional to the intensity of incident radiation.
8. With the solar cell open-circuited, the current will be at its minimum (zero) and the voltage across the cell is at its maximum, known as the solar cells open circuit voltage, or Voc.
9. At the other extreme, when the solar cell is short circuited, the voltage across the cell is at its minimum (zero),known as the solar cells short circuit current, or Isc.

The span of the solar cell I-V characteristics curve as shown in *Figure 14e* ranges from the short circuit current (Isc) at zero output volts, to zero current at the full open circuit voltage (Voc).

There is one particular combination of current and voltage for which the power reaches its maximum value, at Imp and Vmp. The point at which the cell generates maximum electrical power is called the "maximum power point" or MPP.

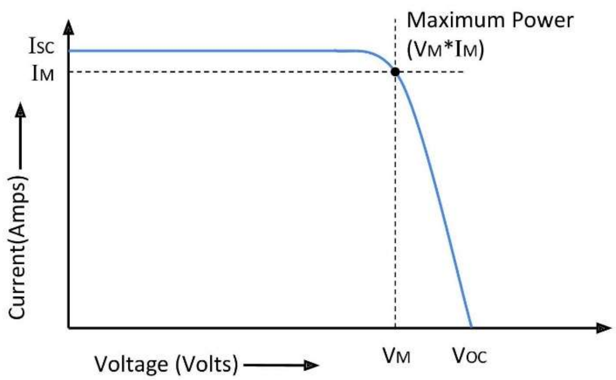

Figure 14e: IV characteristics of solar cell

Advantages-

1. It is pollution free.
2. Solar energy is abundant in nature.
3. They are used in areas where electrical transmission is difficult.

Disadvantages –

1. Initial cost is high.
2. It has low efficiency of energy conversion.
3. Operation at night is not possible.