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Synaptic behaviors and modeling of a metal oxide memristive device

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Abstract Nanoscale memristive devices using tungsten oxide as the switching layer have been fabricated and characterized. The devices show the characteristics of a flux-controlled memristor such that the conductance change is governed by the history of the applied voltage signals, leading to synaptic behaviors including long-term potentiation and depression. The memristive behavior is attributed to the migration of oxygen vacancies upon bias which modulates the interplay between Schottky barrier emission and tunneling at the WO_X/electrode interface. A physical model incorporating ion drift and diffusion effects using an internal state variable representing the area of the conductive region has been proposed to explain the observed memristive behaviors. A SPICE model has been further developed that can be directly incorporated into existing circuit simulators. This type of device can be fabricated with low-temperature processes and has potential applications in synaptic computations and as analog circuit components.

1 Introduction

A memristor or memristive device [1, 2] is essentially a two-terminal electronic device whose conductance can be modulated by controlling the charge or flux through it. This type of device exhibits a "pinched-hysteresis" in the I–V characteristics and has been proposed in a broad range of applications including, but not limited to, resistive random access memory (RRAM) [3], synaptic computation [4], neuromorphic systems [5], Boolean logic implementation [6], signal processing, and circuit design [7]. Here, we show analog memristive effects can be achieved in a nanoscale tungsten oxide-based device with inert electrodes and can be fabricated using CMOS compatible, low-temperature processes. These devices exhibit reliable synaptic behaviors and the memristive effects can be explained using a model involving an internal state variable representing the area of the conducting region.

2 Experimental

2.1 Device fabrication

The device consists of a top palladium electrode, a tungsten oxide switching layer and a bottom tungsten electrode as shown in Fig. 1(a). The fabrication process begins with a thermally oxidized silicon substrate, followed by 60 nm thick tungsten deposition by sputtering at room temperature. Then the tungsten film was patterned by e-beam lithography and reactive ion etching (RIE) to form the nanowire (130 nm wide) bottom electrodes and contact pads. To form the tungsten oxide layer, rapid thermal annealing (RTA) in pure oxygen or plasma oxidation in O_2 plasma was performed at 400°C. During the oxidation, a part of tungsten was consumed (15 ∼ 20 nm) and 40 ∼ 50 nm tungsten oxide (WO_3) film was formed. The thickness of tungsten oxide film saturates after a certain thickness (∼50 nm) during the annealing or plasma oxidation process due to finite oxygen diffusion at 400°C. Finally, the top palladium (Pd) nanowire elec-

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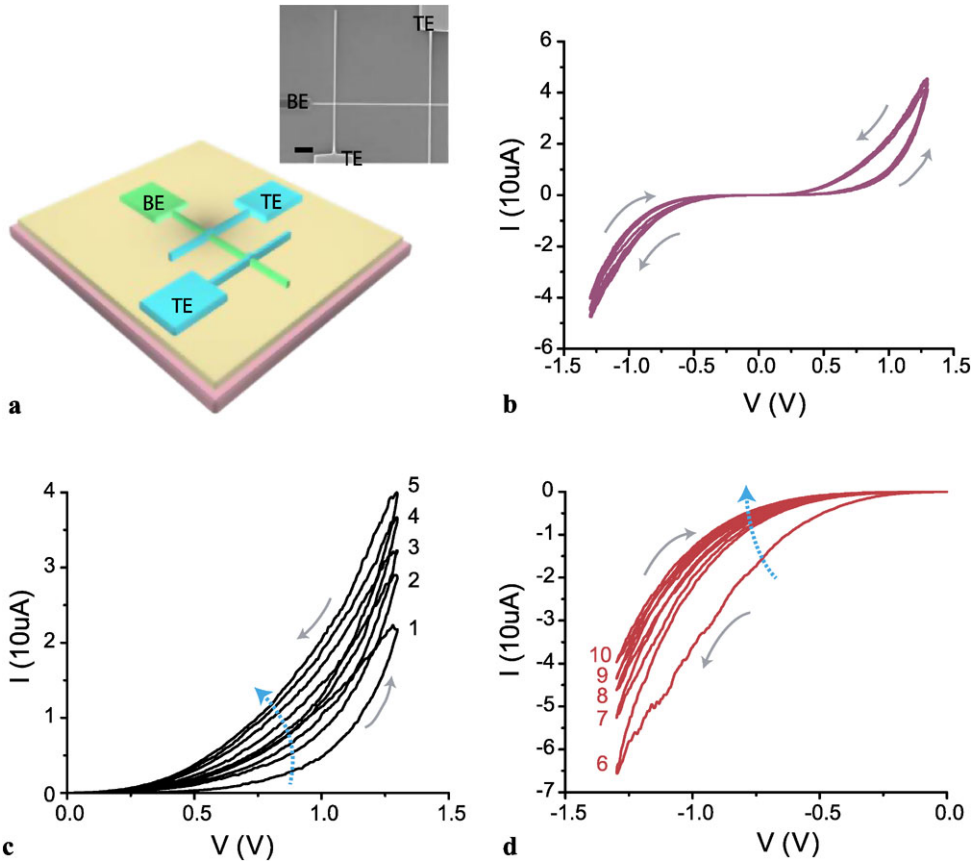

Fig. 1 (**a**) Schematic of a tungsten oxide-based resistance switching device. *Inset*—SEM image of a 1×2 crossbar structure (Scale bar: 2 μm). (**b**)–(**d**) Typical resistance switching characteristics of $Pd/WO_3/W$ devices. Tungsten oxide was formed by RTA in pure O_2 for 3 min at 400°C. (**b**) I–V from five alternating positive and negative voltage sweeping cycles. Overlapping of curves shows stable and reproducible switching. (**c**) I–V from five consecutive positive voltage sweeps (1–5) showing a continuous increase in conductance, and (**d**) five consecutive negative voltage sweeps (6–10) showing a continuous decrease in conductance. The *arrows* indicate switching polarity

trodes were formed by e-beam lithography and lift-off, followed by tungsten oxide etch outside the cross-points using RIE to confine the active area to the crosspoints and to expose the bottom contacts. The final device has a $Pd/WO_3/W$ structure with the device size of 130 nm ×130 nm (inset of Fig. 1(a)).

2.2 DC characteristics

Typical resistance switching behaviors observed in a $Pd/WO_3/W$ device are presented in Fig. 1(b). The as-fabricated device is highly resistive, and can be programmed without the high voltage electroforming process normally needed in other devices. If only positive (or negative) voltages are applied to the top electrodes (TE) with the bottom electrodes (BE) grounded, the device shows continuous increase (or decrease) in conductance, as shown in Fig. 1(c) (or Fig. 1(d)). The "pinched hysteresis" I–V characteristic is a signature of memristive effects. Note that the switching behavior is quite different from those observed in Cu (or Ag)/WO_3/W (or Pt) structures [8, 9] where the resistance switching effects rely on chemical redox processes involving Cu (or Ag) metal ions and exhibit an abrupt on-to-off (or off-to-on) resistance change.

2.3 Memristive and synaptic behaviors

The incremental increase (or decrease) of the device conductance is analogous to potentiation (or depression) of synapses in neuromorphic systems. In addition, potentiation and depression operations can be achieved by voltage pulses. As shown in Fig. 2, conductance modulation in an analog manner is observed when short pulses are applied. Specifically, two effects can be observed: the memristor conductance can be changed quasi-continuously, and the overall memristor conductance is determined by the history of the applied voltages (the time interval between the applied voltage pulses, e.g., flux in this case). For example, by applying a train of positive (negative) voltage pulses the memristor conductance is gradually strengthened (weakened), leading to long-term potentiation (depression). Further insight into the relationship of the memristor conductance change and the flux can be obtained by comparing the behaviors in Figs. 2(a) and (b). A train of fifty 1.4 V/400 μs potentiating pulses are followed by a train of fifty −1.4 V/400 μs depressing pulses so that the net flux through the memristor is zero after a complete potentiating/depressing cycle, and the average conductance of the memristor indeed returns to its starting value (Fig. 2(a)). On the other hand, when the depressing pulses are reduced to −1.2 V/400 μs the overall conductance

increases due to the net positive flux through the device after the potentiating/depressing cycle (Fig. 2(b)), as expected from the flux-controlled memristor [1, 10]. We further show in Fig. 3 that the devices can endure through at least 10^5 potentiating/depressing pulses without degradation, a necessary characteristic for practical applications in electronic circuits and neuromorphic systems.

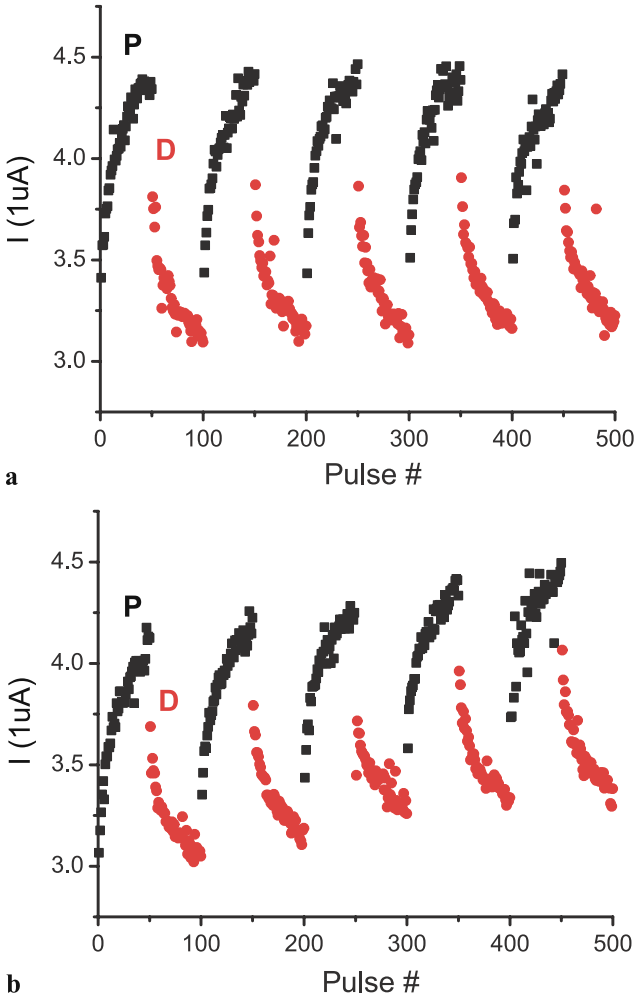

Fig. 2 Pulse response of a tungsten oxide resistive device of which tungsten oxide was formed by RTA in O_2 for 3 min at 400°C. The data show the read current measured with a read pulse of 0.5 V/3 ms after each potentiation (P: *black*-quadrangle) or depression (D: *red*-circle) pulse. Conductance of the device changes incrementally after each pulse. (**a**) P: 1.4 V/400 μs, D: −1.4 V/400 μs. (**b**) P: 1.4 V/400 μs, D: −1.2 V/400 μs. Decreasing the magnitude of the depression pulses in (**b**) results in an overall conductance increase of the device

3 Model and simulation

The behavior of a general memristive device can be described by a pair of coupled equations [1],

$$i = G(w, v)v \tag{1}$$

and

$$\dot{w} = f(w, v) \tag{2}$$

Here, (1) is the normal I–V equation for a resistive device, where w is an (or a group of) internal state variable(s). However, unlike normal devices where the internal state variable w is determined by the present control signals, in a memristive device, only (dw/dt), i.e., the rate of the state variable change, is explicitly determined. Equation (2) thus implies that the state of the device depends on the history of the device. By choosing different internal state variables and modifying the rate equation, a broad range of devices can be shown to fall in the general category of memristive devices.

In several recent publications, the state variable w has been proposed as a length index which specifies the boundary separating the doped (conductive) and undoped (resistive) regions along the thickness of a thin film [2, 11, 12], schematically illustrated in Fig. 4(a). This model works well if the rate of w is roughly a linear function of the voltage (or current), as assumed in [2]. However in real devices (dw/dt) is determined by the drift of charged mobile ions such as oxygen vacancies and it has been shown that at relatively high fields that causes the resistance switching the ions move at a speed exponentially dependent on the electric field

$$\frac{dw}{dt} \propto \sinh\left(\frac{V/E_0}{d-w}\right) \tag{3}$$

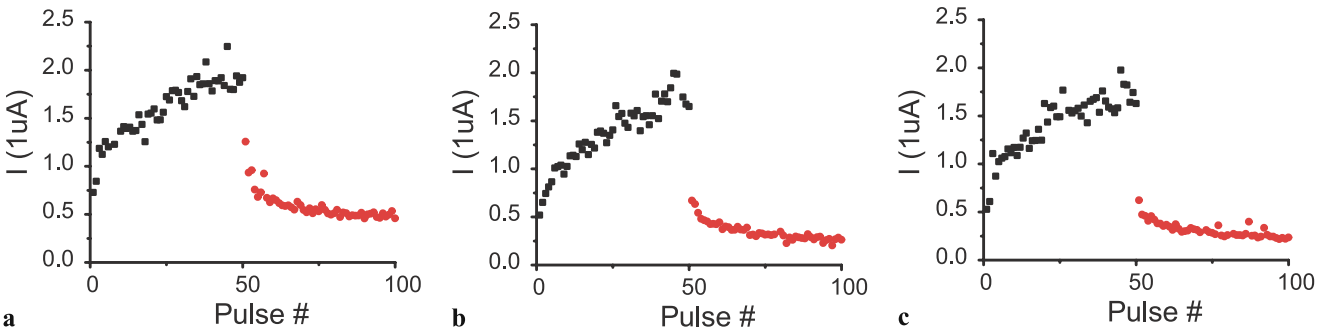

Fig. 3 Endurance characteristics with P: 1.7 V/80 μs, D: −1.7 V/80 μs, and Read: 0.5 V/3 ms pulses. P/D responses were measured at (**a**) fresh, (**b**) after 30K cycles, and (**c**) after 100K cycles

(where d is the total thickness of the film and E_0 a characteristic field), neglecting higher-order effects [13, 14]. As the length of the resistive region $(d - w)$ decreases, the effective electric field is enhanced and the rate (dw/dt) will increase in a significantly nonlinear fashion. As shown in the simulation results in Fig. S1 of the Electronic Supplementary Material (ESM), the nonlinear growth of the length w will lead to very small hysteresis loops in the first a few voltage cycles and much larger resistance changes in later cycles. These results are, however, in contrast to the observed memristive effects observed for TiO_x-based devices [15] and our WO_X-based devices (Fig. 1(c)), where the conductance change in each voltage cycle is roughly constant.

Here, we propose that for analog memristor devices such as the one discussed here, the internal state variable w is better described as an area index (e.g., the number of filaments in filamentary resistive devices or the area of the conductive region in ionic devices). Specifically for the WO_X-based device discussed here, the resistive switching is attributed to the motion of oxygen vacancies upon bias [16]. A schematic of the cross-section is shown in Fig. 4(b) with small particles representing oxygen vacancies (V_{OX}). The as-fabricated film

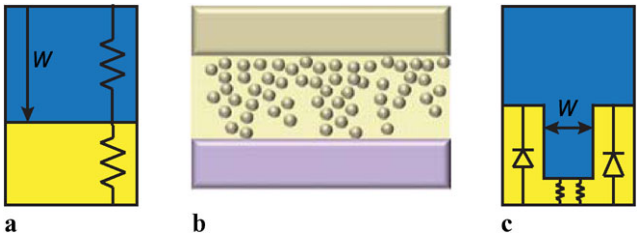

Fig. 4 (**a**) Schematic of the approach of defining w as filament length. (**b**) Cross-section view of a WO_X device. (**c**) Schematic of the approach of defining w as the conductive region area

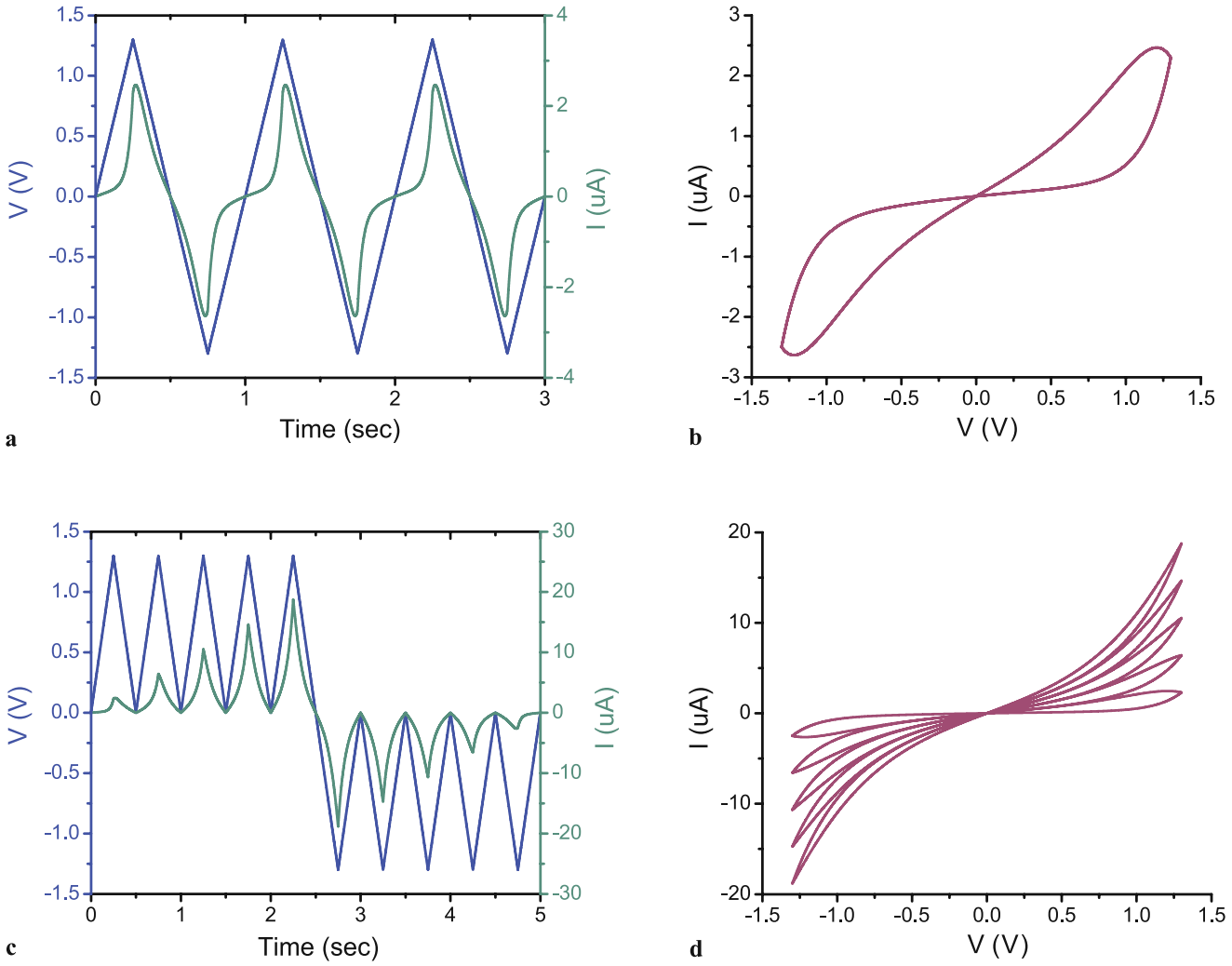

Fig. 5 Simulation results using (4) and (5) using w as an area index showing applied voltage and measured current plotted against time when applied with (**a**) alternating ± voltage sweeps, and (**c**) consecutive ± voltage sweeps. (**b**) and (**d**) are I–V curves extracted from (**a**) and (**c**), respectively

Table 1 LTspice code of the memristor model

```
****************** LTspice code for metal oxide memristors*****************
*Parameters:
*alpha is prefactor for Schottky barrier
*beta is exponent for Schottky barrier
*gamma is prefactor for tunneling
*delta is exponent for tunneling
********************************************************************************
.SUBCKT memristor 1 2 params:
+ alpha=0.5e-6 beta=0.5 gamma=4e-6 delta=2 wmax=1 wmin=0
*State variable:
.param lambda=4.5 eta1=0.004 eta2=4 tau=10
.param cp={1}
Cpvar l 0 {cp}
*rate equation considering the diffusion effect
Gx 0 l value={trunc(V(1,2),cp*V(l))*lambda*(eta1*sinh(eta2*V(1,2))-cp*V(l)/tau)}
*rate equation without the diffusion effect
*Gx 0 l value={trunc(V(1,2),cp*V(l))*lambda*(eta1*sinh(eta2*V(1,2)))}
.ic V(l) = 0.0
********************************************************************************
*auxiliary functions to limit the range of w
.func sign2(var) {(sgn(var)+1)/2}
.func trunc(var1,var2) {sign2(var1)*sign2(wmax-var2)+sign2(-var1)*sign2(var2-wmin)}
********************************************************************************
*Output:
Gw 1 2 value={(1-cp*V(l))*alpha*(1-exp(-beta*V(1,2)))+(cp*V(l))*gamma*sinh(delta*V(1,2))}
.ENDS memristor
```

is semiconducting hence a Schottky barrier is formed between the WO_X film and the W bottom electrode [17]. Upon the application of a positive voltage, oxygen vacancies drift toward the BE and the oxygen vacancy concentration will be increased, resulting in an Ohmic-like contact dominated by a tunneling current [2, 11]. Compared with models using w as a length index, here the growth of w is in parallel with existing conducting paths instead of in series, as schematically shown in Fig. 4(c).

The memristor equations can now be described as:

$$I = (1 - w)\alpha[1 - \exp(-\beta V)] + w\gamma \sinh(\delta V) \tag{4}$$

$$\frac{dw}{dt} = \lambda[\exp(\eta_1 V) - \exp(-\eta_2 V)] \tag{5}$$

where (4) is the I–V equation which includes the Schottky term (1st term) and the tunneling term (2nd term). The two conduction channels are in parallel and their relative weight is determined by the internal state variable w, which is the normalized area index representing the conductive region, i.e., $w = 0$ indicates fully Schottky-dominated conduction while $w = 1$ indicates fully tunneling-dominated conduction. α, β, γ, δ, η_1, and η_2 are all positive-valued parameters determined by material properties such as the barrier height for Schottky barrier and for tunneling, the depletion width in the Schottky barrier region, the effective tunneling distance in the conducting region, and interface effects. In practice, they can be treated as fitting parameters and are independent of w. Equation (5) is the memristor equation which describes the rate of change of the state variable with respect to the applied voltage. It originates from (3) but is no longer explicitly dependent on w since the existing conductive regions in this model do not affect the formation of new conductive regions. The expression is further chosen such that (dw/dt) can be different at positive and negative biases ($\eta_1 \neq \eta_2$) to account for potential differences in the activation energies for forward and backward ion hopping, e.g., in the presence of a build-in field. Having asymmetric activation energies ($\eta_1 \neq \eta_2$), however, is not essential in modeling. In the following simulations we keep $\eta_1 = \eta_2 = \eta$, Equation (5) thus reduces to the usual simpler form of sinh function.

Simulation results based on the model of (4) and (5) are shown in Fig. 5 with alternating and consecutive positive/negative bias. This model captures most of the observed experimental results and more importantly, is based on the

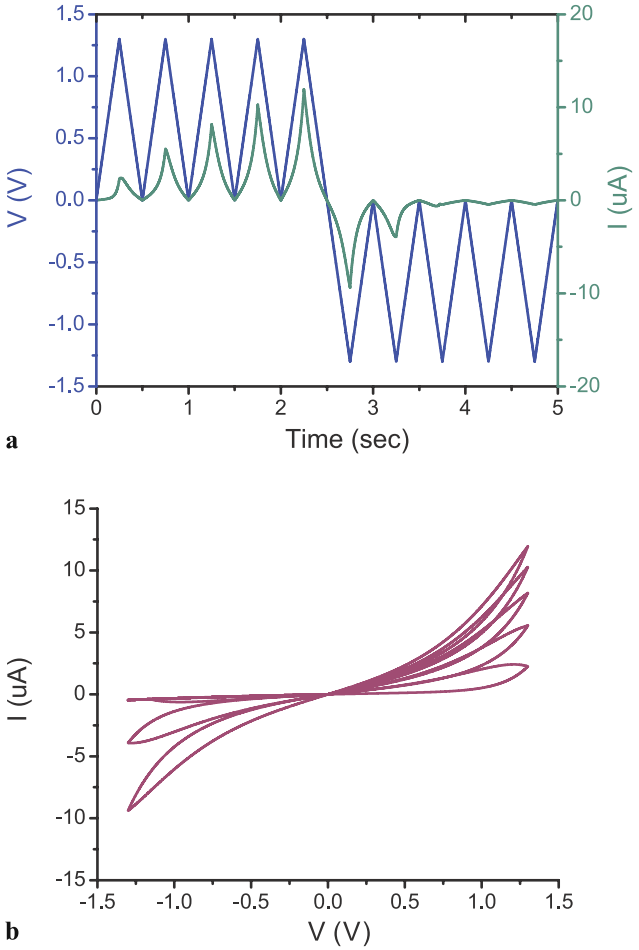

Fig. 6 Simulation results using (4) and (6) after considering diffusion of oxygen vacancies. (**a**) Applied voltage and measured current plotted against time upon consecutive ± voltage sweeps. (**b**) I–V curves extracted from (**a**)

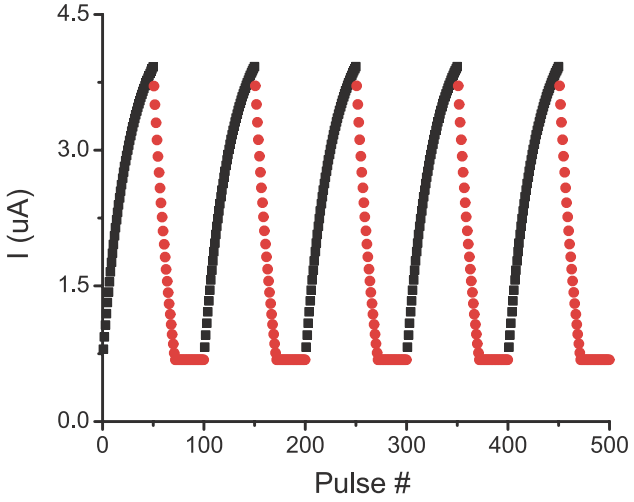

Fig. 7 Simulation results using (4) and (6) and identical conditions used in Fig. 2(a), showing the expected LTP/LTD pulse responses

more accurate ion drift equation, and hence, it will be more accurate in modeling the dynamic device behavior. However, differences between Fig. 1(c)–(d) and Fig. 5(d) can also be found. Notably, there is a significant overlapping of neighboring hysteresis loops in real devices during the potentiation process that is not captured by the model. This phenomenon can be explained by the fact that in addition to drift of V_{OX} under electric field, diffusion of V_{OX} may also be considered due to the high mobility of oxygen vacancies in metal oxide materials. Specifically, the more resistive state is the thermodynamically ground state [15] and diffusion of ions will lead to a natural decay to that state. By adding a diffusion term, $(-w/\tau)$, where τ is a diffusion time constant, the rate equation (5) can be rewritten as

$$\frac{dw}{dt} = \lambda \sinh(\eta V) - \frac{w}{\tau} \tag{6}$$

I–V curves based on the new model using (4) and (6) are shown in Fig. 6(a)–(b). The improved model including the diffusion term clearly captures the overlap of the hysteresis curves in Fig. 1(c) and the lack of such overlap in Fig. 1(d). In addition, results of the pulse-based LTP/LTD operations are reliably captured by the model shown in Fig. 7 using the same pulsing condition as in Fig. 2(a), further proving the validity of the model.

In the next step, we implemented the device physics based memristor model into the library of a circuit simulator (LTspice) and the code are provided in Table 1. A similar scheme as in [12] was used in which the value of w is stored in a floating capacitor and Eqs. (4)–(6) were solved self-consistently in the subcircuit. The SPICE model is very compact and can be directly embedded in commercial simulators, and will likely be useful for various proposed applications of memristors [18, 19] for circuit-level simulations.

4 Role of oxygen vacancy

As discussed earlier, the resistance change is thought to be due to the motion of oxygen vacancies in the WO_X layer. It is well known that the stoichiometry of tungsten oxide films depends on the fabrication process. For example, it has been reported that longer oxidation of tungsten at temperatures of 300°C or higher yields larger W^{5+} to W^{6+} ratios [20]. In other words, the tungsten oxide formed at higher temperature (or longer oxidation time) is not stoichiometric but highly oxygen-deficient. The increased W^{5+} to W^{6+} ratio (hence increased oxygen deficiency) with oxidation time or temperature may be explained by the fact that the as-grown amorphous phase of tungsten oxide is changed to a (poly-) crystalline phase in which V_{OX} segregate at the grain boundaries [21]. Drift and diffusion of V_{OX} at grain boundaries is also enhanced compared to the amorphous phase.

During the tungsten oxidation at a temperature above 300°C, the density of V_{OX} in grain boundaries near the surface of WO_3 is increased for several reasons. First, the surface of tungsten oxide experiences the longest annealing time, since the surface of tungsten oxide is the part that grown first and the inner part of the tungsten oxide layer is close to its as-grown state. Second, bombardment from Pd evaporation followed by possible oxygen diffusion through Pd grain boundaries [22] also generates V_{OX} near the top surface. Hence the density of dopants (oxygen vacancies) in grain boundaries at the surface will likely be higher than that of the bulk, generating an oxygen vacancy gradient distribution along the tungsten oxide depth direction (Fig. 4(b)). This results in a nearly Ohmic contact at the top electrode interface and a Schottky contact at the bottom electrode interface.

When the top electrode is positively biased, oxygen vacancies move toward the bottom electrode. If V_{OX} moves close enough to the bottom electrode, direct tunneling can occur, increasing the overall conductance. As a result, conduction in some regions of the bottom interface experiences a transition from a Schottky junction to a tunneling junction, and the overall device conductance depends on the areal proportion of the two types of junctions. Similarly, a negative bias would cause the oxygen vacancies to move back toward the surface region, resulting in a decrease in conductance.

5 Conclusion

A tungsten oxide-based memristive device has been fabricated and characterized, showing reliable synaptic operations with good endurance. Furthermore, a memristor model incorporating both drift and diffusion effects using a normalized state variable w as an area index has been developed and demonstrated to reasonably explain the resistive switching. The device model has been successfully implemented into SPICE and will be valuable for future circuit evaluations in memristor-based applications.

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