Team Details

Team Name: EdgeInnovators

SR. NO	ROLE	NAME	ACADEMIC YEAR
1	**Team Leader**	*Bibaswan Sarkar*	*2025-29*
2	Member 1	*Pranavi Pathak*	*2025-29*
3	Member 2	*Dipali*	*2025-29*
4	Member 3	*Shiwani Anand*	*2025-29*

COLLEGE NAME

Indian Institute of Information and Technology Senapati, Manipur

TEAM LEADER CONTACT NUMBER

+91 94330 65609

TEAM LEADER EMAIL ADDRESS

bibaswansarkar11@gmail.com

Problem Statement Addressed: Edge-AI Defect Classification for semiconductor images

The problem statement our idea addresses :

DESCRIPTION / DETAILS

Semiconductor manufacturing produces large volumes of wafer and die inspection images. Defects in these images can reduce yield and cause failures, but traditional centralized/manual inspection creates latency, bandwidth bottlenecks, and high infrastructure cost, making it difficult to scale to real-time production needs.

Task is to build an Edge-AI capable system that can detect and classify defects in semiconductor wafer/die images using AI/ML, while balancing accuracy, latency, and compute efficiency to reflect real fab constraints.

Proposed Solution - AI-Based Wafer/Die Defect Detection with Edge AI.

Our idea in detail. Including the methodology, technologies involved, and how it addresses the chosen problem statement.

SOLUTION DETAILS

We propose an AI-driven wafer and die defect classification system designed for semiconductor manufacturing inspection. The solution utilizes a lightweight deep learning architecture optimized for real-time defect detection and classification on Edge AI devices. The system processes wafer map images or optical defect images, automatically identifies defect patterns, and outputs classification results with confidence scores. The model is specifically optimized to operate under low latency, limited computational resources, and high accuracy requirements, making it suitable for deployment directly on manufacturing inspection systems.

Innovation and Uniquenes s

What makes our idea unique or innovative compared to existing solutions.

KEY INNOVATION

Supervised learning–based defect classification aligned with fab inspection workflows.
AI + Edge Computing–driven semiconductor quality inspection.

COMPETITIVE ADVANTAGE

Our solution uses defect-aware localization and relocation to generate physics-consistent SEM datasets from minimal real data, avoiding black-box GAN hallucinations. This enables explainable, supervised CNN training with full traceability, making the pipeline data-efficient, reliable, and model-agnostic.

Impact and Benefits

How the solution will make an impact.

Primary Impact

Low-latency, scalable, and industry-ready solution.
Software-centric architecture suitable for semiconductor manufacturing integration.

Quantifiable Outcomes

We scaled from 1–2 real SEM images per defect to hundreds of labeled samples per class and trained a supervised CNN with measurable Accuracy, Precision, Recall, and F1-score. The system provides per-image classification outputs with filenames, ensuring 100% test-sample traceability and reproducibility.

Technology & Feasibility/Methodology Used

The technologies, methodologies, or tools we plan to use to implement our idea.

IMPLEMENTATION STRATEGY

Data Acquisition & Preprocessing:
The system accepts wafer/die defect images or wafer maps.
Preprocessing includes resizing, normalization, and data augmentation to improve model generalization and robustness.

Model Training:
A Convolutional Neural Network (CNN) is trained using supervised learning, where labeled defect images are used to learn discriminative features for classification .The system classifies semiconductor defect types including:
Bridge, LER (Line Edge Roughness) , CMP (Chemical Mechanical Planarization defects), Crack, Vias, Opens.
Model Optimization & Export
The trained model is converted into ONNX format. Quantization techniques such as INT8 optimization are applied to reduce memory footprint and increase inference speed.

Edge AI Deployment:
The optimized model is deployed using NXP eIQ runtime or equivalent edge inference frameworks. Enables real-time classification directly on inspection hardware without requiring cloud connectivity.

Inference & Output:
The system performs real-time defect classification.Outputs include defect class and confidence score for quality control and yield analysis.
Technologies Involved : AI / ML Stack, Python, TensorFlow / PyTorch, OpenCV, NumPy, Matplotlib, Model Stack, Convolutional Neural Networks (CNN), MobileNet / EfficientNet-Lite, Quantized edge-optimized models, Edge AI Stack, ONNX model conversion, NXP eIQ Toolkit, Embedded inference runtime.

Hardware Components:
Targeted Chip: NXP 32-BIT ARM BASED MCU LMX RT1170

Development Tools: NXP eIQ Toolkit

GitHub & Video Link
Research and References

GitHub Repository

https://github.com/RespectedBibaswanSarkar/iesa

Prototype / Simulation Video

https://drive.google.com/file/d/1Fr8VPR_thV54JiJqD7hHcRYxec1edNC1/view?usp=sharing

Research Background & Methodology

https://scholar.google.com/scholar?q=Convolutional+Neural+Network+for+Wafer+Surface+Defect+Classification+and+the+Detection+of+Unknown+Defect+Class https://scholar.google.com/scholar?q=Semiconductor+SEM+Image+Defect+Classification+Using+Supervised+and+Semi-Supervised+Learning+with+Vision+Transformers

References & Citations

List key papers, articles, or data sources.

Semiconductor Inspection: ITRS Yield Enhancement Reports; SEM-based defect analysis (SPIE, IEEE Transactions on Semiconductor Manufacturing).
Deep Learning & CNNs: LeCun et al., *Deep Learning* (MIT Press); CNN-based wafer defect classification (IEEE, CVPR).
Edge AI Deployment: TensorFlow Lite Optimization Docs; NXP eIQ Toolkit and i.MX 8M Plus Edge AI documentation.

1. https://arxiv.org/abs/2506.03345: Semiconductor SEM Image Defect ClassificationUsing Supervised and Semi-Supervised Learning withVision Transformers.
2. https://arxiv.org/abs/2308.08376:Automated Semiconductor Defect Inspection inScanning Electron Microscope Images:a Systematic Review