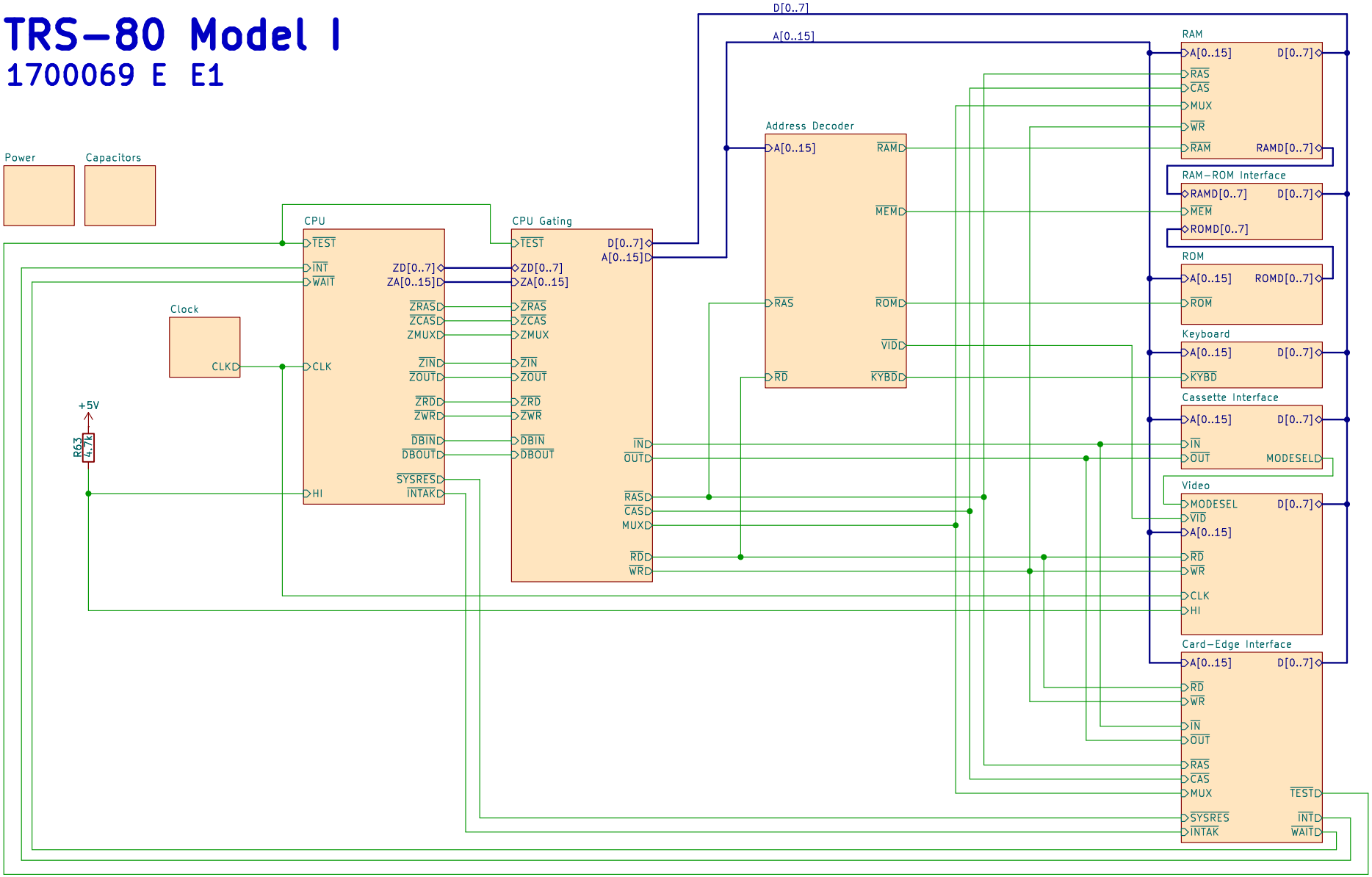
# TRS-80 Model I

## 1700069 E E1




System Overview

Full overview of the system

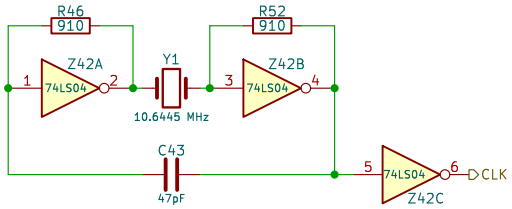
**RetroStack – Marcel Erz**

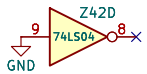
Sheet: /

File: TRS80_Model_I_E_E1.kicad_sch

***Title: TRS-80 Model I Rev E***

| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
|---|---|---|
| KiCad E.D.A. 8.0.3 | | Id: 1/21 |



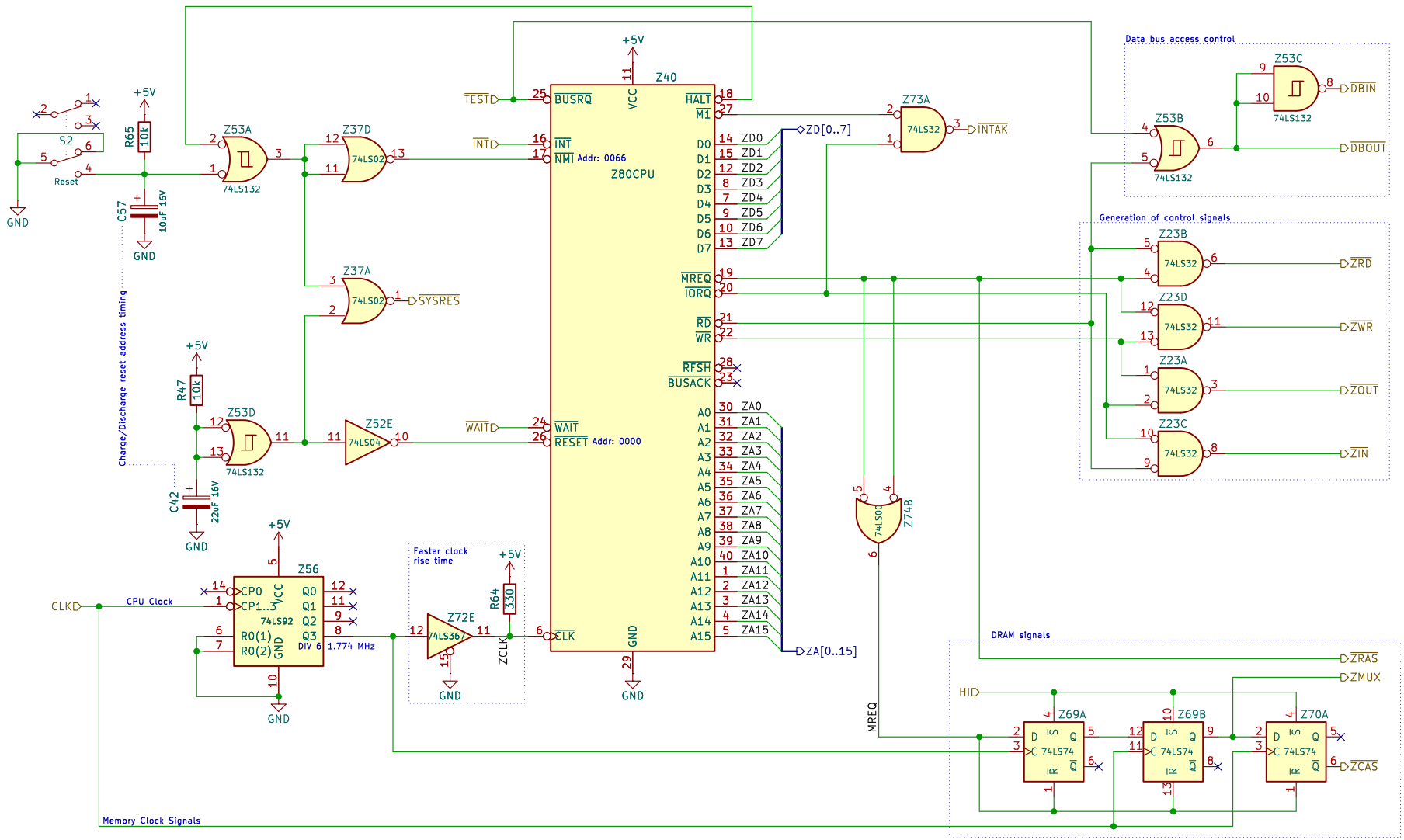

System Clock

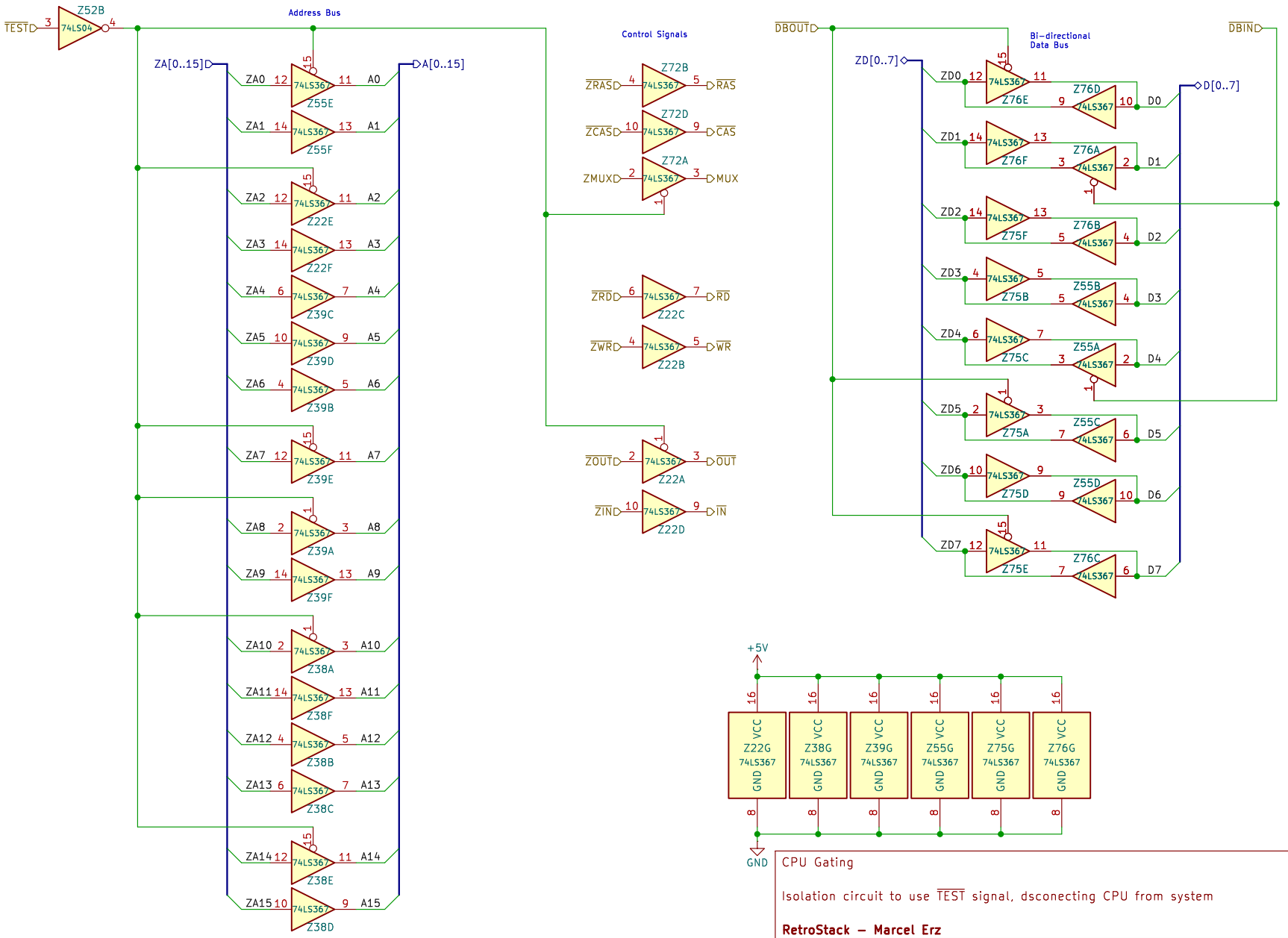
**RetroStack – Marcel Erz**

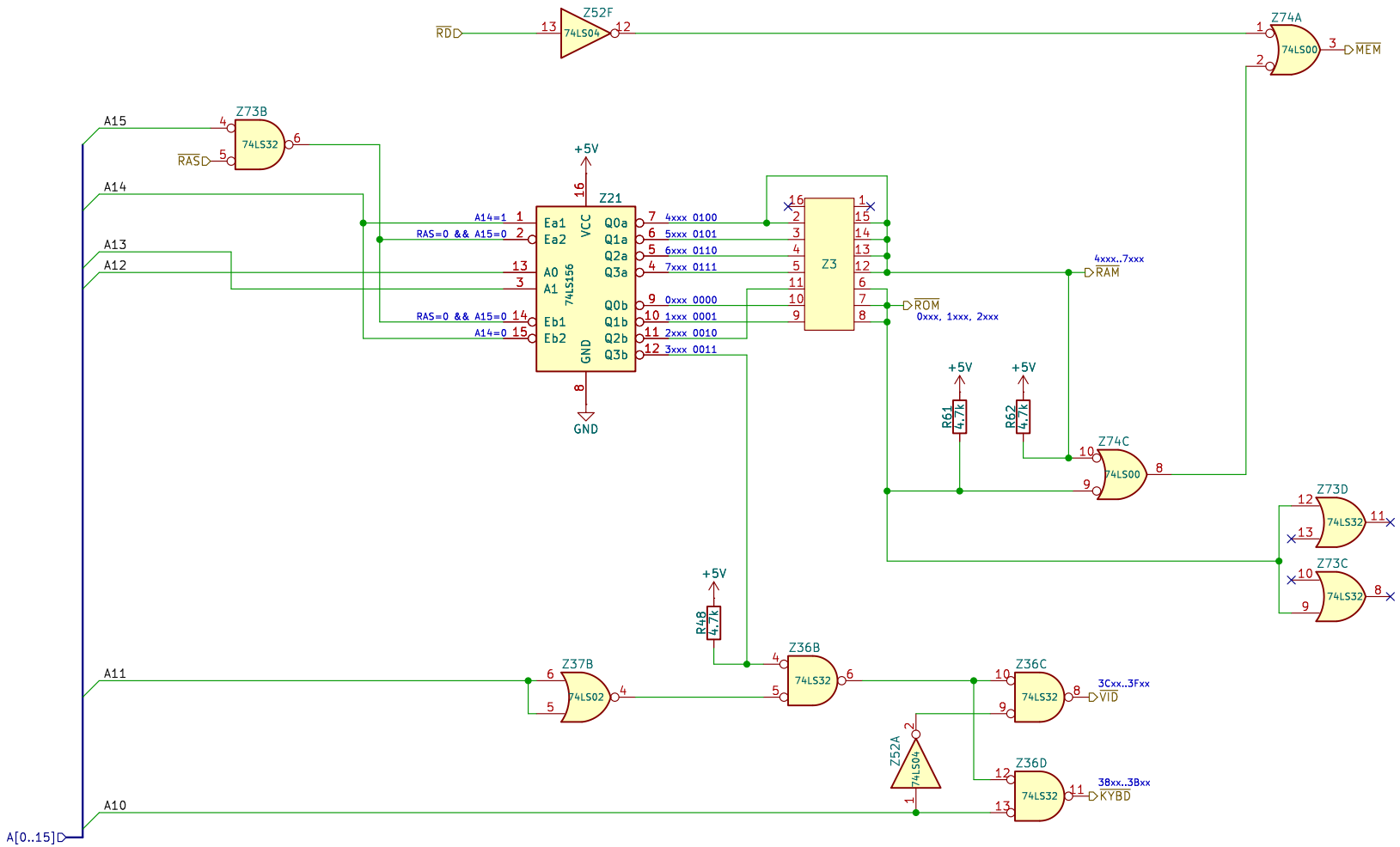
Sheet: /Clock/
File: Clock.kicad_sch

***Title: TRS-80 Model I Rev E***

| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
|---|---|---|
| KiCad E.D.A. 8.0.3 | | Id: 2/21 |


Data bus access control
Generation of control signals
DRAM signals
Charge/Discharge reset address timing
Faster clock rise time
Memory Clock Signals
Z40
Z80CPU
Z56
Z53A
Z37D
Z37A
Z53D
Z52E
Z72E
Z73A
Z53C
Z53B
Z23B
Z23D
Z23A
Z23C
Z74B
Z69A
Z69B
Z70A
Z69C
Z53E
Z23E
S2
Reset
R65
R47
R64
C57
C42
CPU Clock
1.774 MHz
DIV 6
ZD[0..7]
ZA[0..15]
INTAK
DBIN
DBOUT
ZRD
ZWR
ZOUT
ZIN
ZRAS
ZMUX
ZCAS
SYSRES
MREQ
HID
ZCLK
CPU & Signals
CPU with reset circuits (button and power-up), clock divider, RAS & CAS divider, signals
RetroStack – Marcel Erz
Sheet: /CPU/
File: CPU.kicad_sch
Title: TRS-80 Model I Rev E
Size: USLetter
Date: 2024-11-23
Rev: E1A-E
KiCad E.D.A. 8.0.3
Id: 3/21


Address Bus
Control Signals
Bi-directional
Data Bus
TEST
DBOUT
DBIN
ZA[0..15]
A[0..15]
ZD[0..7]
D[0..7]
Z52B
74LS04
ZRAS
ZCAS
ZMUX
ZRD
ZWR
ZOUT
ZIN
RAS
CAS
MUX
RD
WR
OUT
IN
+5V
GND
VCC
CPU Gating
Isolation circuit to use TEST signal, dsconecting CPU from system
RetroStack – Marcel Erz
Sheet: /CPU Gating/
File: CPUGating.kicad_sch
Title: TRS-80 Model I Rev E
Size: USLetter
Date: 2024-11-23
Rev: E1A-E
KiCad E.D.A. 8.0.3
Id: 4/21




Address Decoder

Address decoder circuit for main board components (except IO)

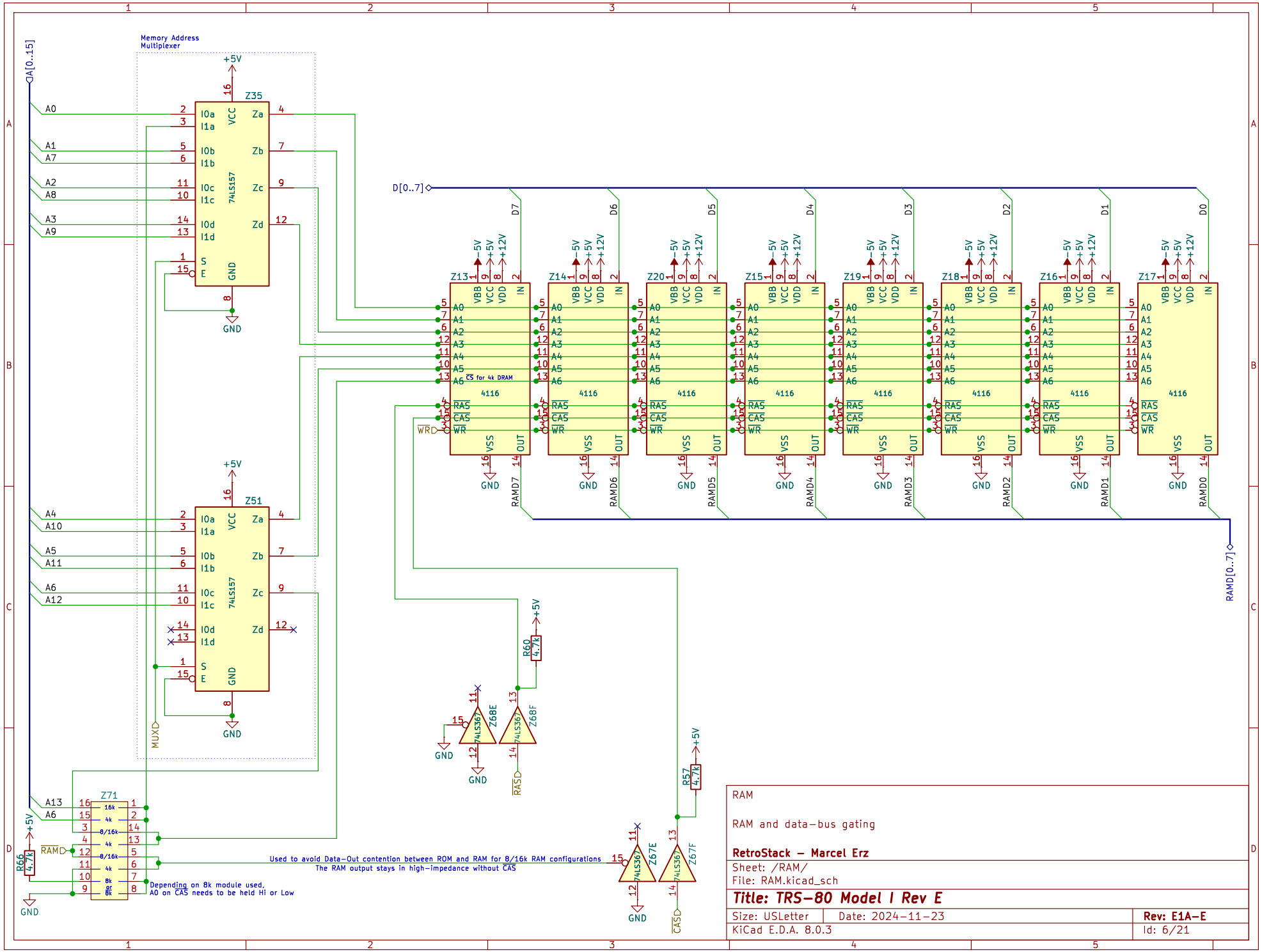
**RetroStack – Marcel Erz**

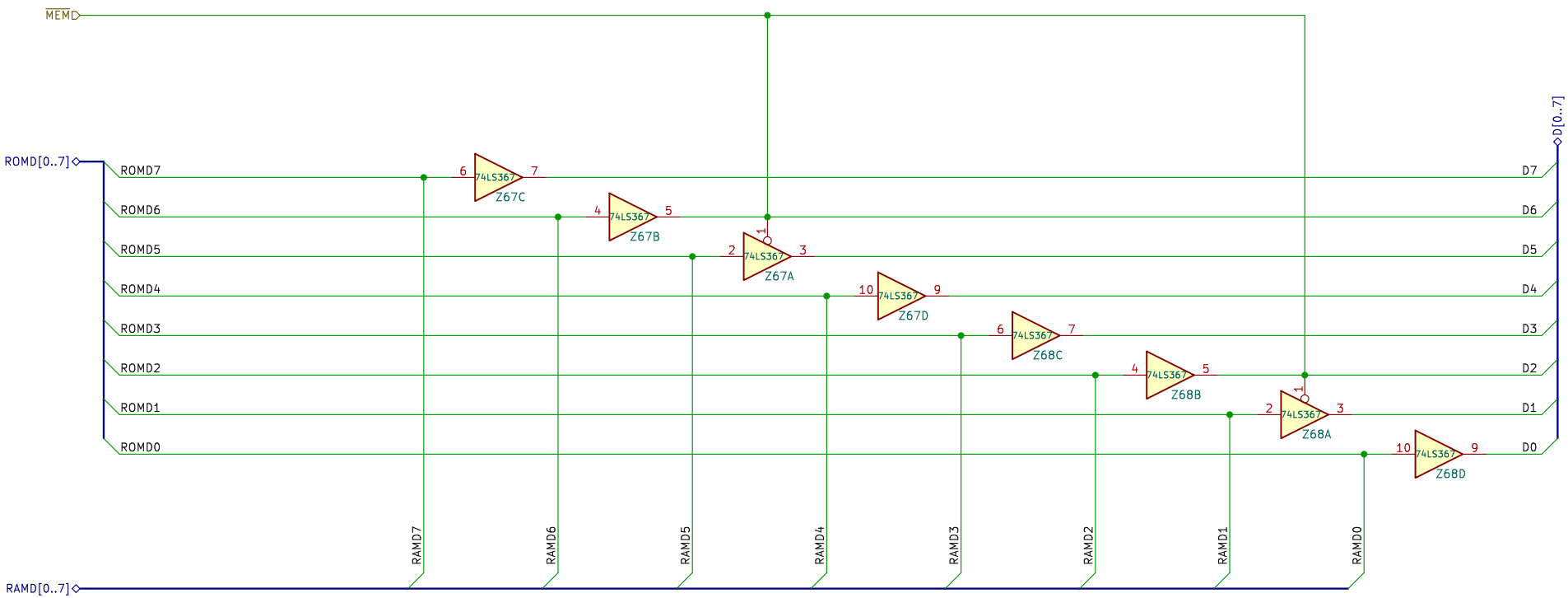
Sheet: /Address Decoder/

File: AddressDecoder.kicad_sch

***Title: TRS-80 Model I Rev E***

| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
|---|---|---|
| KiCad E.D.A. 8.0.3 | | Id: 5/21 |


Memory Address Multiplexer
A[0..15]
D[0..7]
RAMD[0..7]
Z35
Z51
74LS157
Z13
Z14
Z20
Z15
Z19
Z18
Z16
Z17
4116
CS for 4k DRAM
WR
RAMD7
RAMD6
RAMD5
RAMD4
RAMD3
RAMD2
RAMD1
RAMD0
MUXD
Z68E
Z68F
74LS367
R60
4.7k
RAS
Z71
RAM
R66
Used to avoid Data-Out contention between ROM and RAM for 8/16k RAM configurations
The RAM output stays in high-impedance without CAS
Depending on 8k module used,
A0 on CAS needs to be held Hi or Low
Z67E
Z67F
R57
CAS
RAM
RAM and data-bus gating
RetroStack – Marcel Erz
Sheet: /RAM/
File: RAM.kicad_sch
Title: TRS-80 Model I Rev E
Size: USLetter
Date: 2024-11-23
Rev: E1A-E
KiCad E.D.A. 8.0.3
Id: 6/21




RAM–ROM Interface

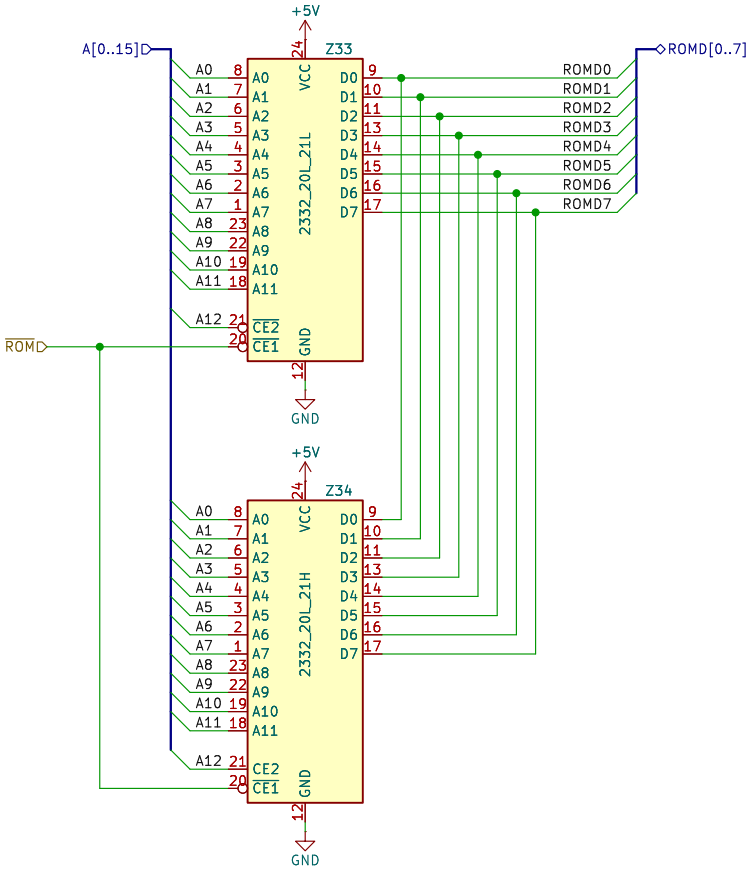
Connects RAM & ROM to the data bus

**RetroStack – Marcel Erz**

Sheet: /RAM–ROM Interface/
File: RAM_ROM_Interface.kicad_sch

***Title: TRS–80 Model I Rev E***

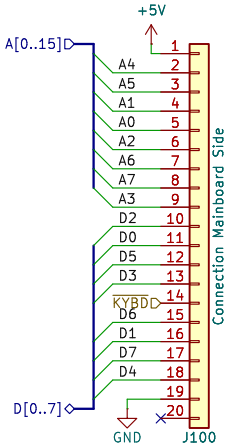
| Size: USLetter | Date: 2024–11–23 | **Rev: E1A–E** |
|---|---|---|
| KiCad E.D.A. 8.0.3 | | Id: 7/21 |




Level I ROMs:
- Intel 2616 EPROM (White Crystal Window)
- National MM2316 ROM (Colored Ceramic) (R/D=ROM A, S/D=ROM B)
- Motorola 7800 Series ROMs (7807=ROM A, 7804=ROM B)
- Motorola 7800 Series ROMs (7809=ROM A & B)

Level II ROMs:
- Generic 3 ROMs on separate board with logic chip (each 32kbit/4kb)
- NEC 8043364 & 8043732 (64kbit/8kb & 32kbit/4kb) (early 1979)
- NEC 8044364 & 8044732 (64kbit/8kb & 32kbit/4kb) (early 1980)

| | | |
|---|---|---|
| ROM | | |
| ROM circuit | | |
| **RetroStack – Marcel Erz** | | |
| Sheet: /ROM/ | | |
| File: ROM.kicad_sch | | |
| ***Title: TRS-80 Model I Rev E*** | | |
| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
| KiCad E.D.A. 8.0.3 | | Id: 8/21 |




Keyboard & Interface

Keyboard interface circuit

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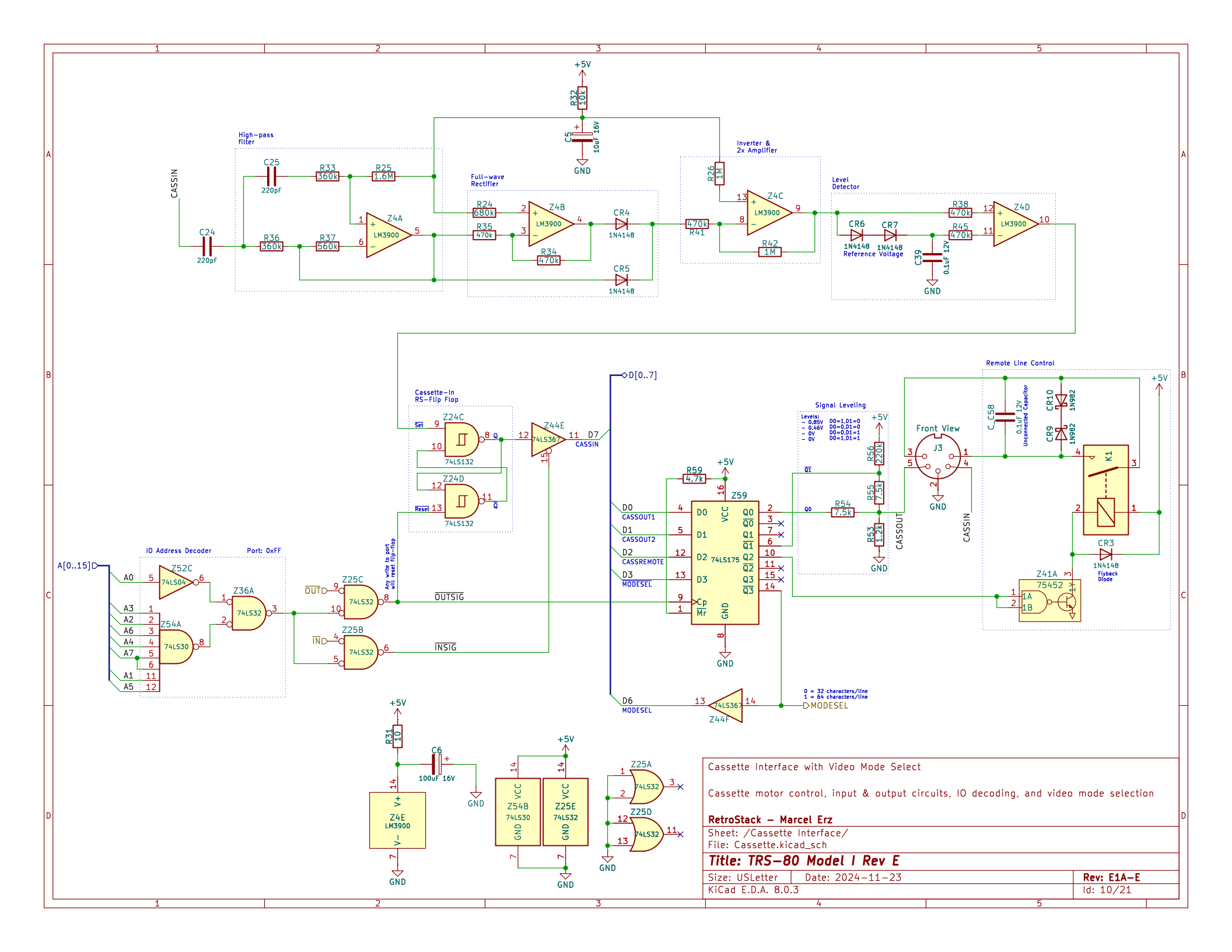
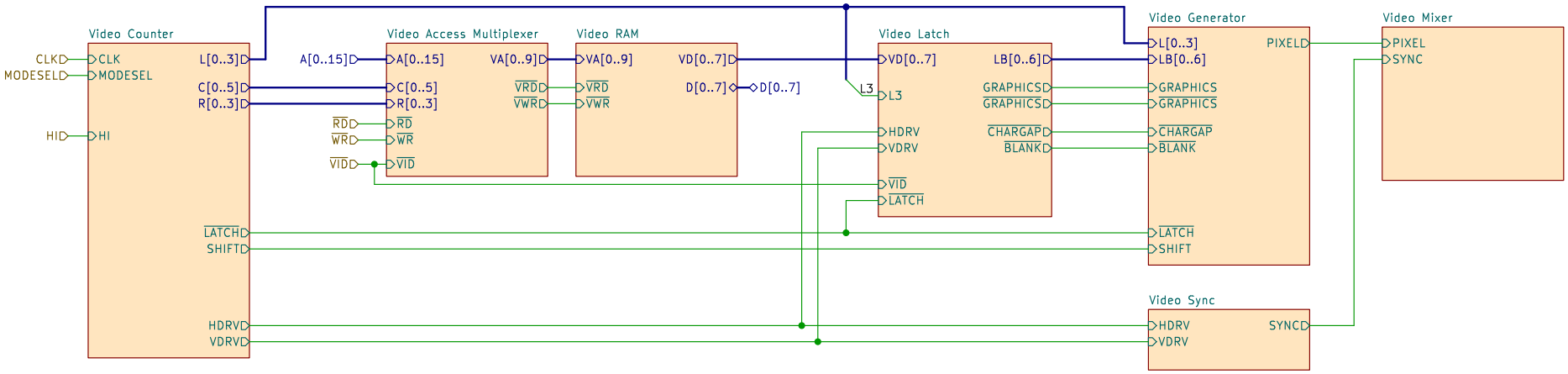
Sheet: /Keyboard/
File: Keyboard.kicad_sch

***Title: TRS-80 Model I Rev E***

| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
|---|---|---|
| KiCad E.D.A. 8.0.3 | | Id: 9/21 |


High-pass filter
Full-wave Rectifier
Inverter & 2x Amplifier
Level Detector
Cassette-In RS-Flip Flop
Signal Leveling
Remote Line Control
IO Address Decoder
Port: 0xFF
Front View
Reference Voltage
Flyback Diode
Unconnected Capacitor
Any write to port will reset flip-flop
0 = 32 characters/line
1 = 64 characters/line
Cassette Interface with Video Mode Select
Cassette motor control, input & output circuits, IO decoding, and video mode selection
RetroStack – Marcel Erz
Sheet: /Cassette Interface/
File: Cassette.kicad_sch
Title: TRS-80 Model I Rev E
Size: USLetter
Date: 2024-11-23
Rev: E1A-E
KiCad E.D.A. 8.0.3
Id: 10/21




Video Overview

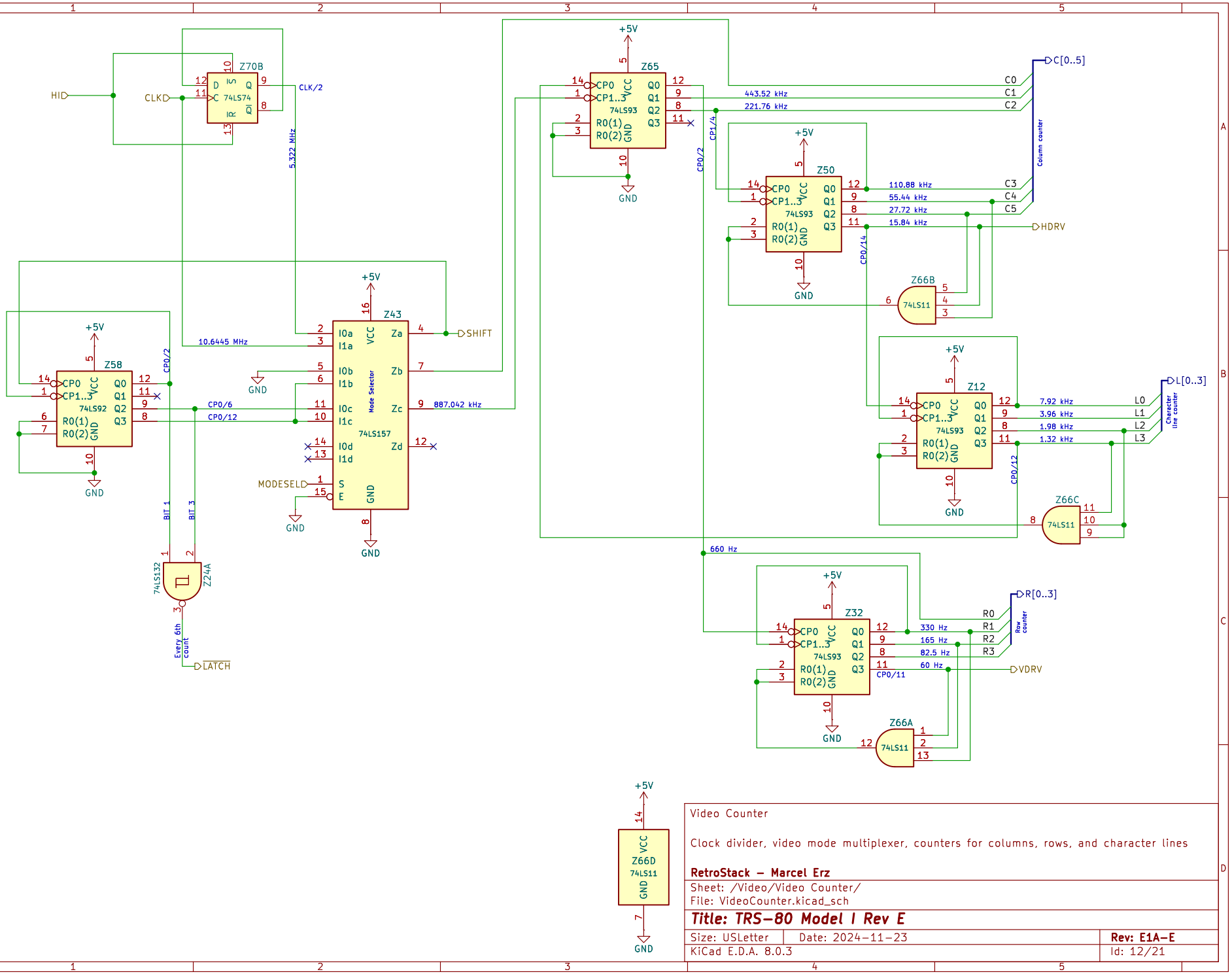
All video components of system

**RetroStack – Marcel Erz**

Sheet: /Video/
File: Video.kicad_sch

***Title: TRS-80 Model I Rev E***

| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
|---|---|---|
| KiCad E.D.A. 8.0.3 | | Id: 11/21 |




Video Counter

Clock divider, video mode multiplexer, counters for columns, rows, and character lines

**RetroStack – Marcel Erz**

Sheet: /Video/Video Counter/
File: VideoCounter.kicad_sch

***Title: TRS-80 Model I Rev E***

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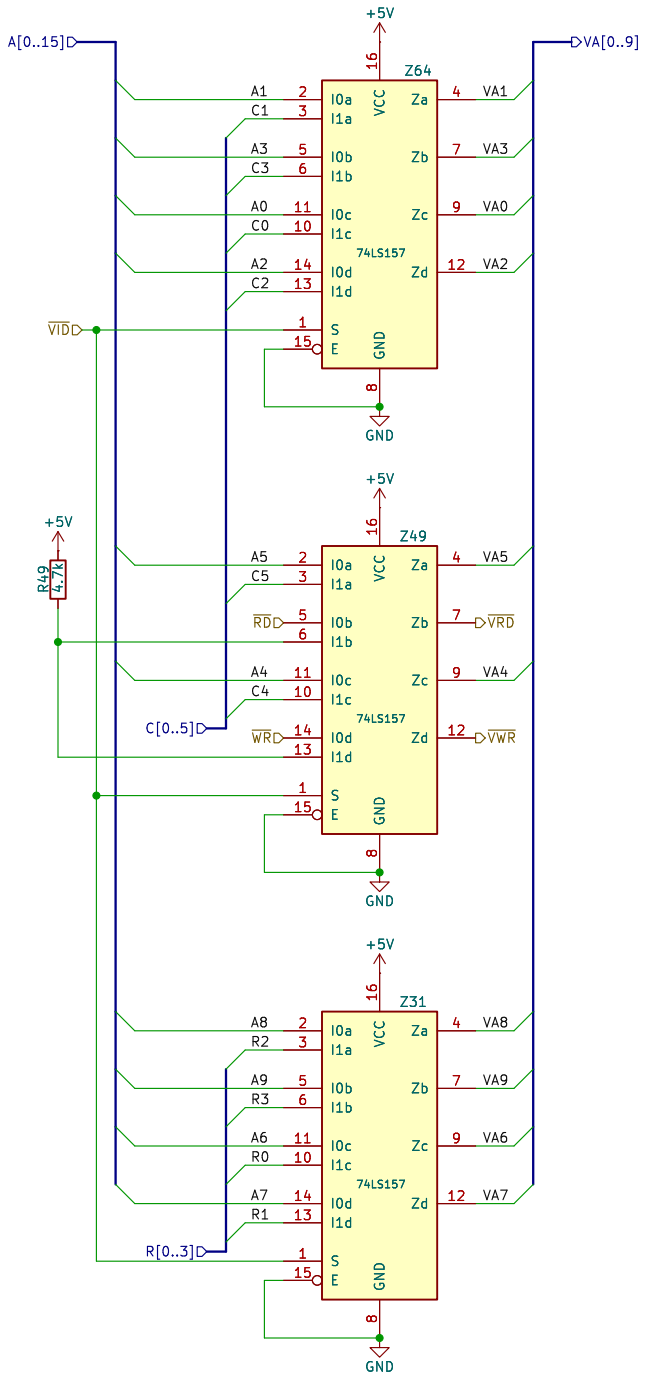


Video Access Multiplexer

Multiplexer for video RAM access of CPU or video circuit

**RetroStack – Marcel Erz**

Sheet: /Video/Video Access Multiplexer/
File: VideoAccessMultiplexer.kicad_sch

***Title: TRS-80 Model I Rev E***

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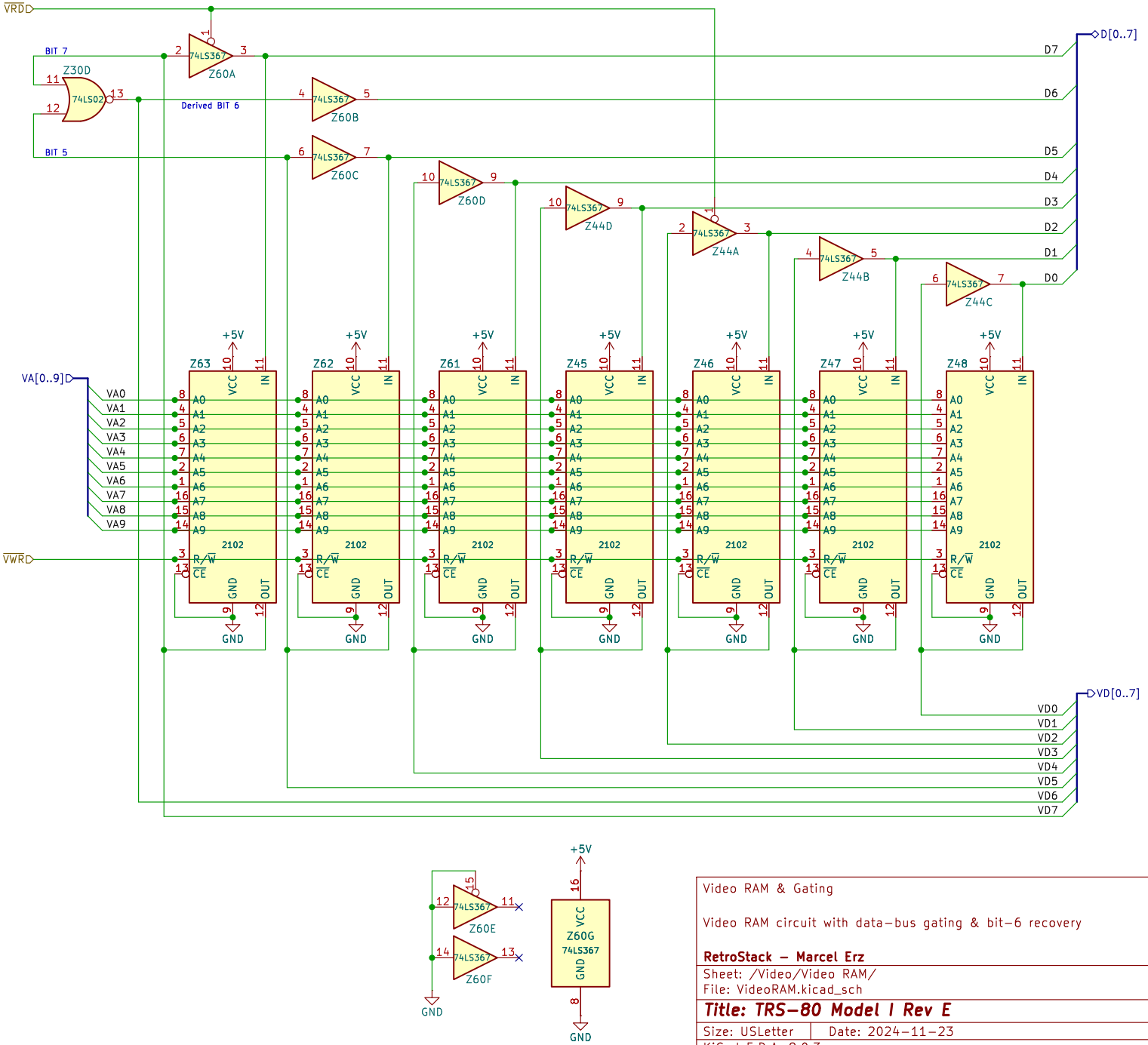


Video RAM & Gating

Video RAM circuit with data-bus gating & bit-6 recovery

**RetroStack – Marcel Erz**

Sheet: /Video/Video RAM/
File: VideoRAM.kicad_sch

***Title: TRS-80 Model I Rev E***

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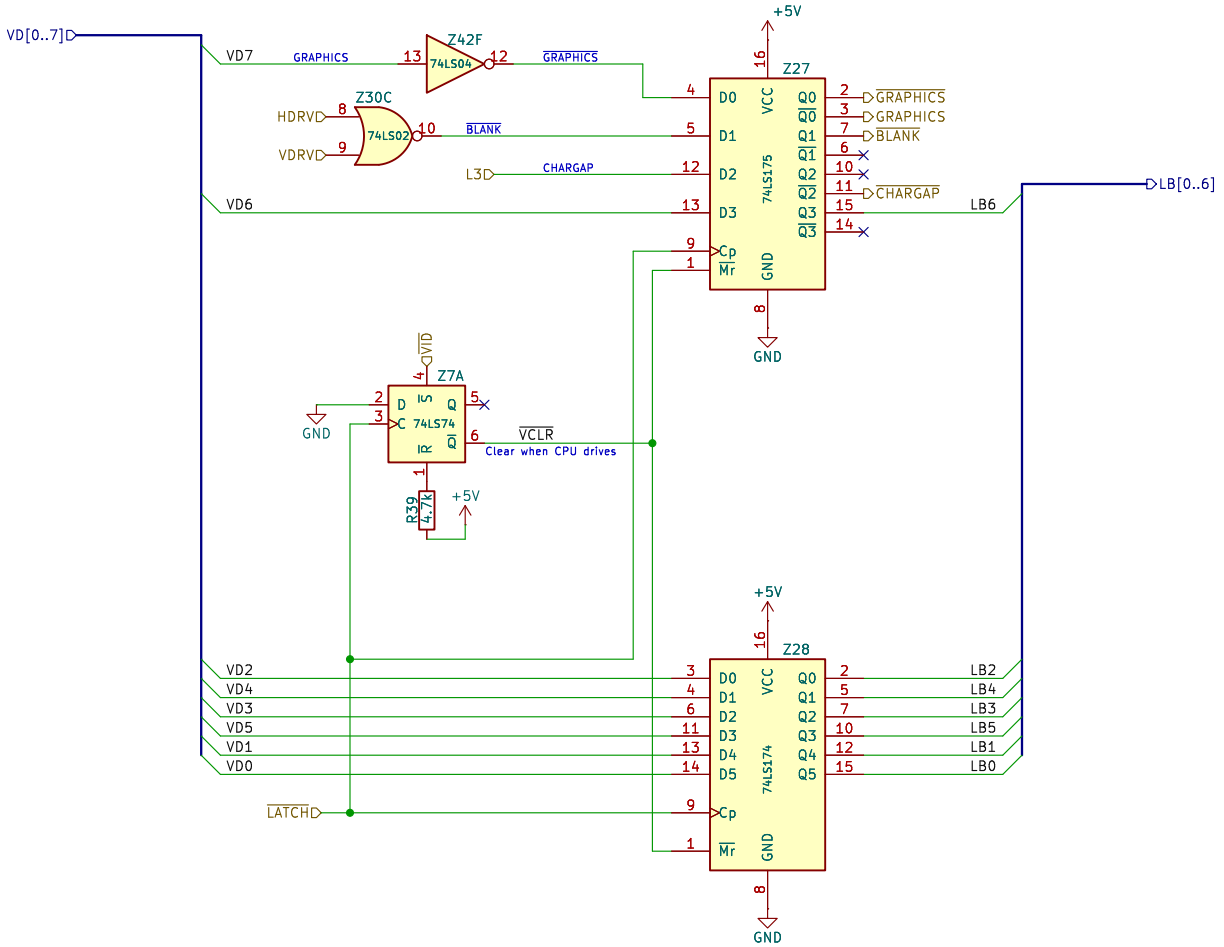


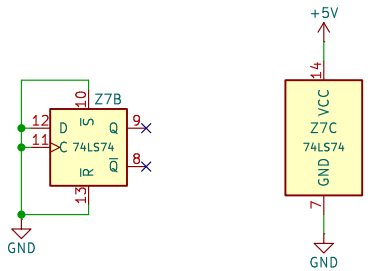


Video Latch

Circuit to latch video content addressed in video RAM

**RetroStack – Marcel Erz**

Sheet: /Video/Video Latch/

File: Video Latch.kicad_sch

***Title: TRS-80 Model I Rev E***

| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
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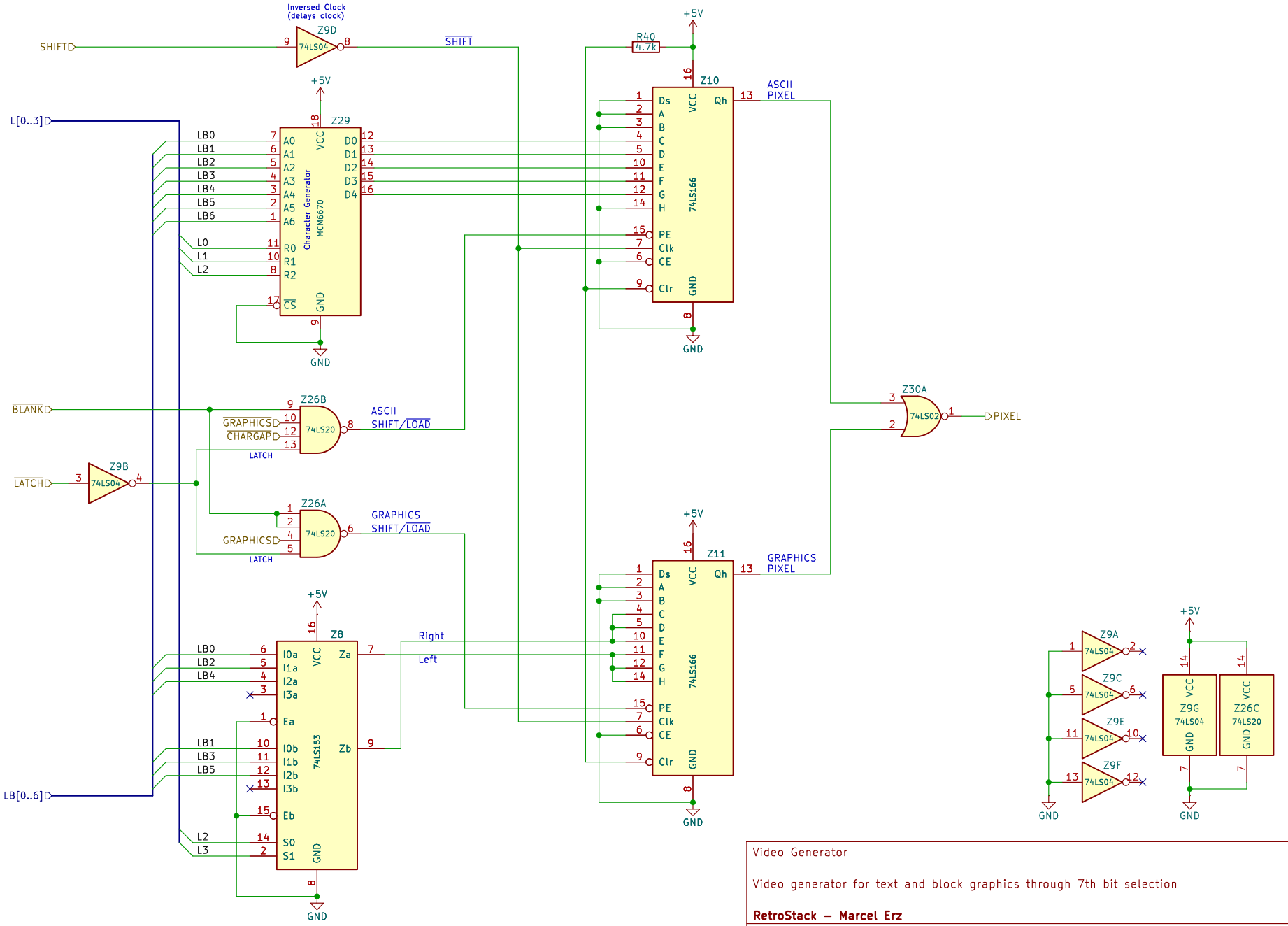


Video Generator

Video generator for text and block graphics through 7th bit selection

**RetroStack – Marcel Erz**

Sheet: /Video/Video Generator/
File: VideoGen.kicad_sch

***Title: TRS-80 Model I Rev E***

| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
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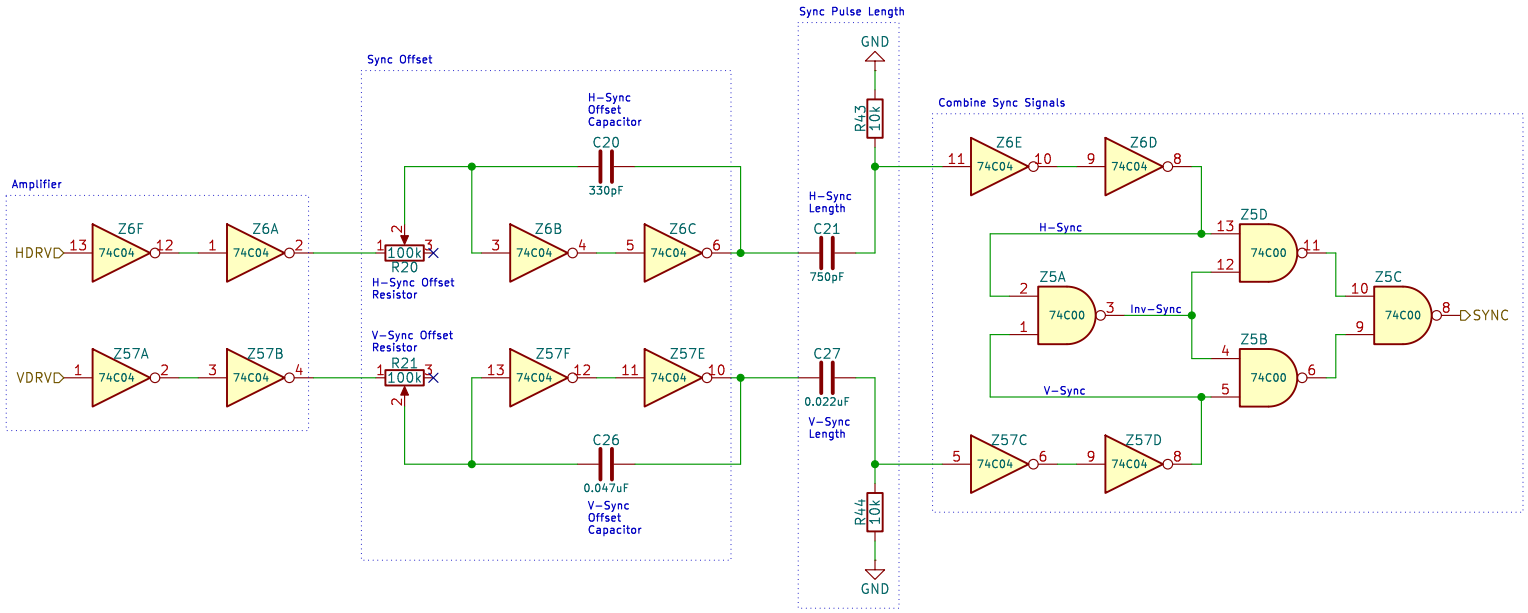


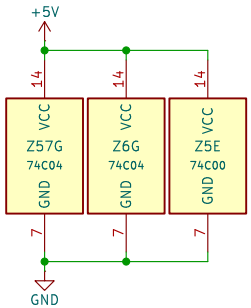


Video Sync

Circuit to combine sync signals and defining front- and back-porches in video signal

**RetroStack - Marcel Erz**

Sheet: /Video/Video Sync/

File: VideoSync.kicad_sch

***Title: TRS-80 Model I Rev E***

| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
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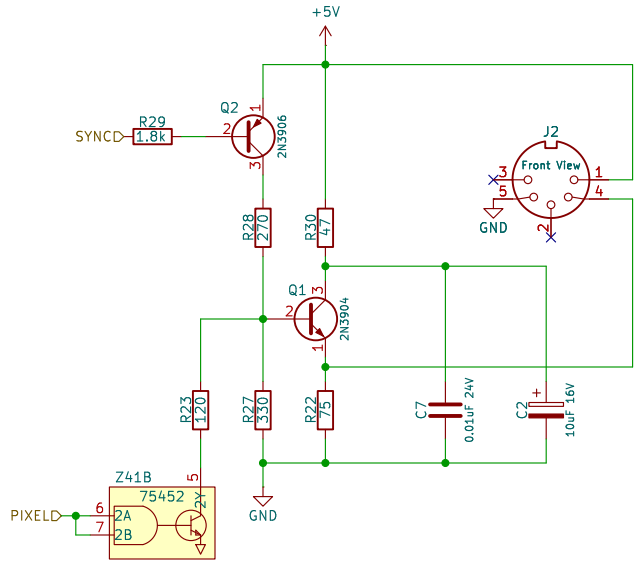


Q2 open, Z41 any => 0V (sync level)
Q2 closed, Z41 closed => 1.23V (black level) – R28 with series resistors R23 & R27
Q2 closed, Z41 open => 2.75V (white level) – Only R27 & R28

| | | |
|---|---|---|
| Video Mixer | | |
| Mixing circuit for sync and pixel data | | |
| **RetroStack – Marcel Erz** | | |
| Sheet: /Video/Video Mixer/ | | |
| File: VideoMixer.kicad_sch | | |
| ***Title: TRS-80 Model I Rev E*** | | |
| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
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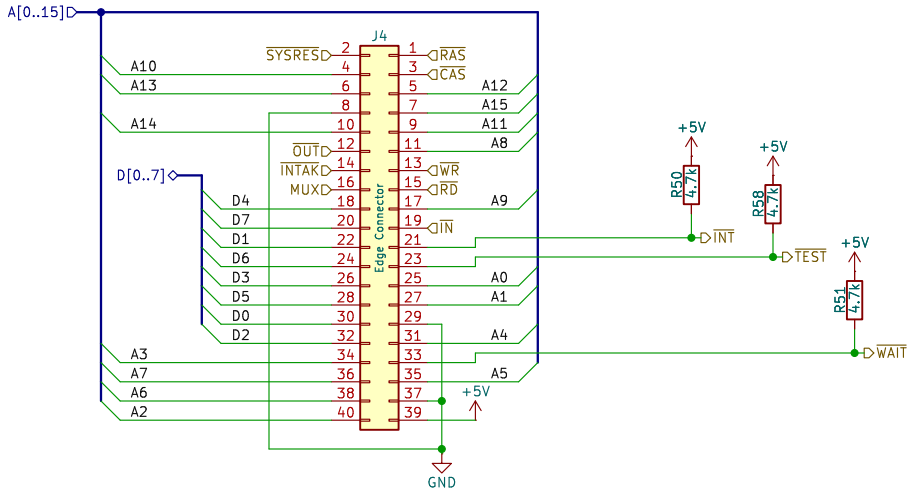


Card–Edge Interface

Unbuffered system interface with pull–up circuity for inputs

**RetroStack – Marcel Erz**

Sheet: /Card–Edge Interface/
File: CardEdgeInterface.kicad_sch

***Title: TRS–80 Model I Rev E***

| Size: USLetter | Date: 2024–11–23 | **Rev: E1A–E** |
|---|---|---|
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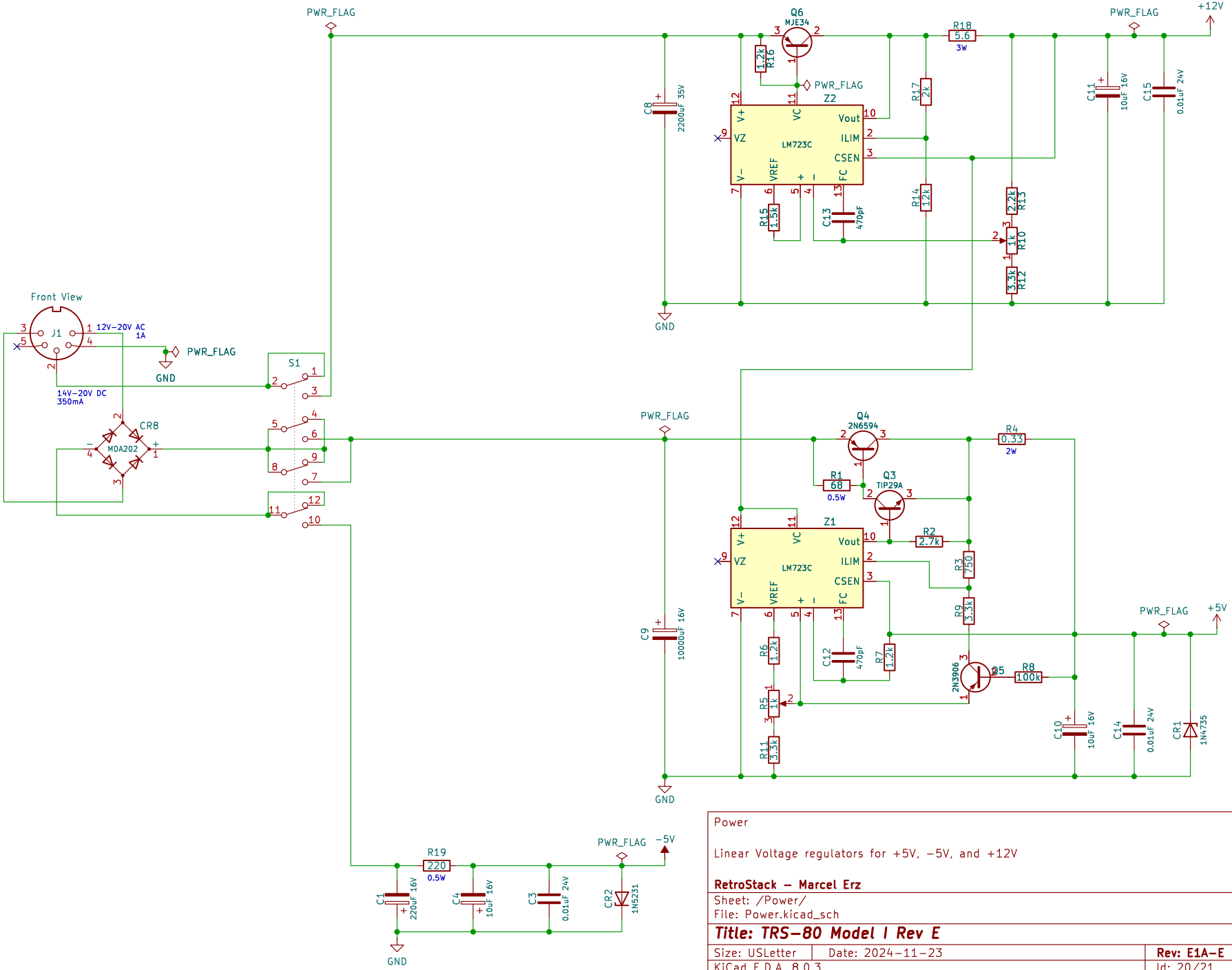



Power

Linear Voltage regulators for +5V, −5V, and +12V

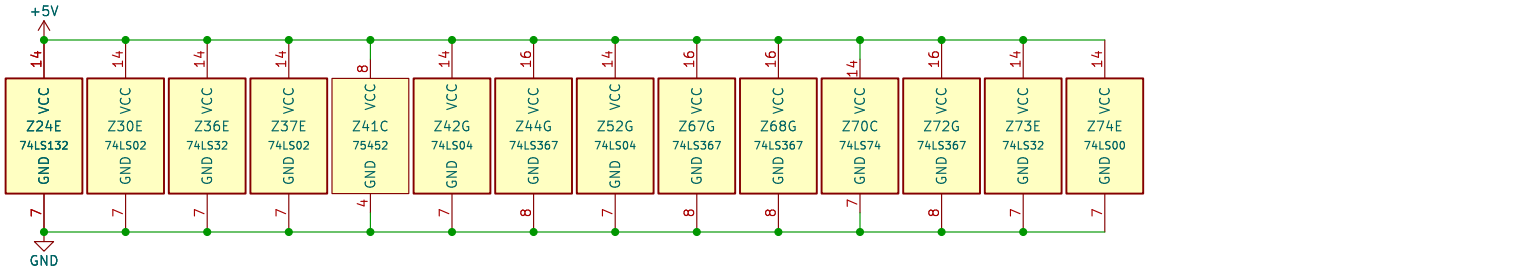
**RetroStack – Marcel Erz**

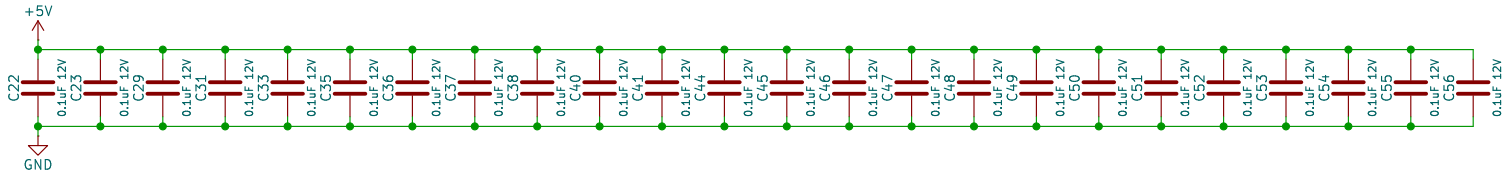
Sheet: /Power/

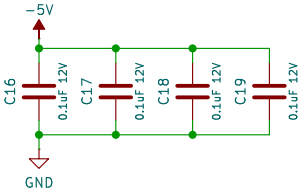
File: Power.kicad_sch

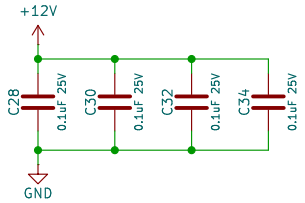
***Title: TRS–80 Model I Rev E***

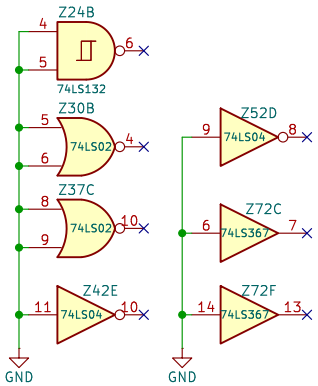
| | | |
|---|---|---|
| Size: USLetter | Date: 2024–11–23 | **Rev: E1A–E** |
| KiCad E.D.A. 8.0.3 | | Id: 20/21 |




Capacitors & Others

Main Units, Capacitors, and unused units

**RetroStack – Marcel Erz**

Sheet: /Capacitors/

File: Capacitors.kicad_sch

***Title: TRS-80 Model I Rev E***

| Size: USLetter | Date: 2024-11-23 | **Rev: E1A-E** |
|---|---|---|
| KiCad E.D.A. 8.0.3 | | Id: 21/21 |