

Intro To Processor Architecture

Assignment 1

Team 33 : Snapdragon

Macharla Harish : 2020102062

Revanth Sai : 2020102068

ALU Functionality:

1. Control [00] 0:

The first control we implemented is Full Adder(64bits)

The module takes A , B as inputs which are 64 bits respectively and returns SUM and CARRY_OVERFLOW as outputs. Overflow but returns 1 if overflow occurs else it returns 0.

```
module Add(A,B,SUM,CARRY_OVERFLOW);
```

Approach:

- We will take two 64 bits inputs $A = A_{64}A_{63}.....A_1A_0$,
 $B = B_{64}B_{63}.....B_1B_0$.
- Now for getting sum part we calculate $SUM_i = A_i \text{ XOR } B_i \text{ XOR } C_i$.
(We assumed $C_i = 0$).
- Now for getting the carry part $C_{i+1} = (A_i \text{ XOR } B_i) \text{ AND } C_i \text{ OR } A_i$
and B_i .
- In this manner we calculate the sum for all 64 bits and the XOR value of C_{63} and C_{64} will tell us whether an overflow has occurred or not.

2. Control [01] 1:

The next control we implemented is Subtractor(64bits)

This module also uses the full adder to accomplish subtraction. We take 2's complement of the Number that is getting subtracted and add it to the other digit.

```
module Sub(A,B,result,carry_overflow);
```

Here also A,B are the 64 bit inputs and result returns the subtracted output and carry overflow bit returns if an overflow has occurred.

Approach:

- Here suppose $A - B$ is the operation then we just take the 2's complement of B and add it to A.
- The approach for addition part is same as previous Sum control.
- For getting the 2's complement we just negate $\sim B$ and add 1 to it.

3. Control[10] 2:

The next control we implemented is the AND(64bits)

This module takes in two 64 bits inputs and returns the And result of them.

```
module And(A,B,OUT);
```

Approach:

- We will take two 64 bits inputs $A = A_{64}A_{63} \dots A_1A_0$,
 $B = B_{64}B_{63} \dots B_1B_0$.
- Now we will find the AND of A and B using simple & i.e.
 $OUT_i = A_i \text{ and } B_i$, for example $OUT_1 = A_1 \text{ and } B_1$,
 $OUT_{63} = A_{63} \text{ and } B_{63}$.

4. Control[11] 3:

The final control implemented is the XOR(64bits)

This module takes in two 64 bit inputs and returns the Xor result of them.

```
module Xor(A,B,OUT);
```

Approach:

- We will take two 64 bits inputs $A = A_{64}A_{63}\dots\dots A_1A_0$,
 $B = B_{64}B_{63}\dots\dots B_1B_0$.
- Now we will find the XOR of A and B using simple XOR i.e.
 $OUT_i = A_i \text{ XOR } B_i$, for example $OUT_1 = A_1 \text{ XOR } B_1$,
 $OUT_{63} = A_{63} \text{ XOR } B_{63}$.

ALU Unit:

| Control Input | Function |
|---------------|----------|
| 00 | ADD |
| 01 | SUB |
| 10 | AND |
| 11 | XOR |

We implemented the above sequence of instructions using case statements in verilog.

[illegible]

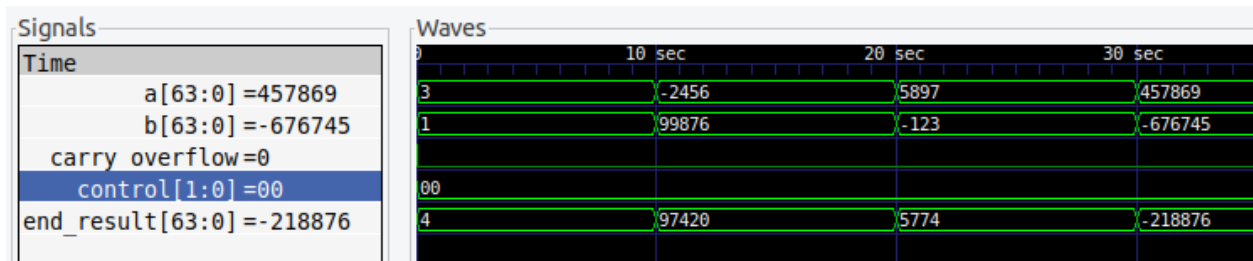
| Time | Control | Value | Overflow |
|------|---------|--------|----------|
| 80 | 10 | 3 | 0 |
| 90 | 10 | -2456 | 0 |
| 100 | 10 | 5897 | 0 |
| 110 | 10 | 457869 | 0 |

[illegible]

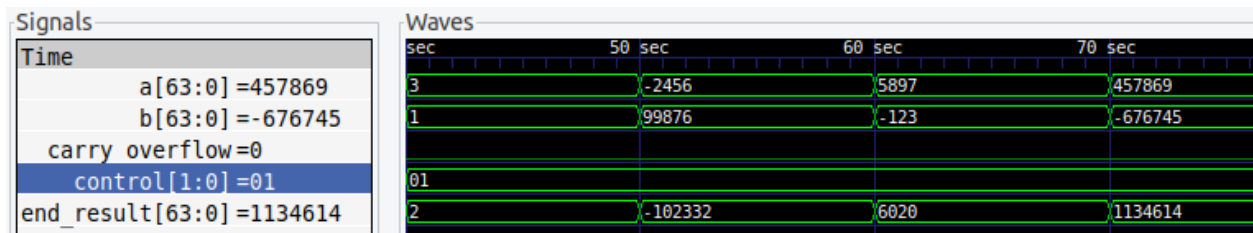
Results:

The following are the GTKWave Outputs

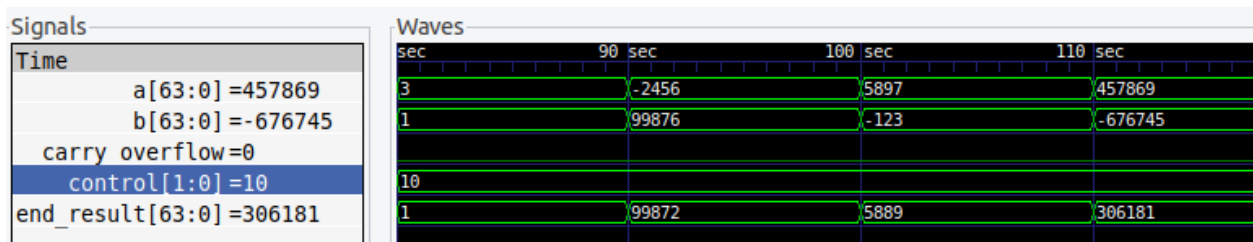
1. Sum



2. Subtraction



3. AND



4. XOR

