

REVANTH SAI NANDAMURI

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Seeking entry level full-time opportunities in the field of Pre-Si Validation

B-Tech (School of Electronics and Communication Engineer)

CGPA : 8.41

(2022)

Vellore Institute of Technology-AP University, Amaravati, Andhra Pradesh, India

Course Work:

Problem Solving using Python
Embedded Programming

Data Structures and Algorithms
Microcontrollers and interfacing

Sensor Systems
VLSI System Design

Digital Logic Design
Digital System Design using FPGAs

HDL Verification and Methodology
SoC Design

SKILLS

✓	Hardware Descriptive Languages	:	Verilog, SystemVerilog
✓	Methodologies	:	Universal Verification Methodology (UVM)
✓	Embedded Programming Languages	:	Embedded C, Python (Raspberry), LPC1768, LPC2148
✓	Embedded Systems	:	Arduino, NodeMCU, Raspberry Pi
✓	Programming Languages	:	C, Python
✓	Editors/Tools	:	Arduino IDE, LabVIEW, VSCode, Xilinx Vivado, ModelSim, QuestaSim

SystemVerilog and UVM Projects

1. Development of SystemVerilog and UVM of verification environment for Memory model (2021)

- **Domain:** SystemVerilog and UVM
- **Description:** Developed SV and UVM Verification Environment for Synchronous read/write Memory model.
 - Developed Master and Slave Agents
 - Developed Slave Sequencer, driver, and monitor.
 - Developed Out-Of-Order scoreboard.
 - Developed Functional Coverage component.
 - Developed Callbacks to implement error injection mechanism.
 - Developed RAL Environment to configure CSR's.
 - Developed backdoor RAL classes to configure CSR's.
 - Developed master Sequences with Test Cases.
 - Developed Slave sequence.
 - Running/Debugging Test Cases.

2. Development of SystemVerilog and UVM of verification environment for Router 4x4 Design (2021)

- **Domain:** SystemVerilog and UVM
- **Description:** Developed SV and UVM Verification Environment for Router 4x4 DUT.
 - Developed Master and Slave Agents.
 - Developed Out-Of-Order scoreboard.
 - Developed Functional Coverage component.
 - Developed Callbacks to implement error injection mechanism.
 - Developed RAL Environment to configure CSR's.
 - Developed backdoor RAL classes to configure CSR's.
 - Developed Sequences and Test Cases.
 - Running/Debugging Test Cases

3. Development of UVM of verification environment for ALU Design (2021)

- **Domain:** UVM
- **Description:** Developed UVM Verification Environment for ALU DUT.
 - Developed Master and Slave Agents.
 - Developed DPI-C reference model.
 - Developed Predictor component with DPI reference model.
 - Developed In-Order scoreboard.
 - Developed Functional Coverage component.
 - Developed Sequences and Test Cases.
 - Running/Debugging Test Cases.

INNOVATIONS

- ✓ Self-initiated idea titled "Portable UV-C Sanitizer" has been accepted and published as an 'Indian Patent' with an application number 202041033151.
- ✓ Self-initiated idea titled "Smart Electrical Measurement System" has been accepted and published as an 'Indian Patent' with an application number 202141026739.
- ✓ Self-initiated idea titled "Multimeter on Gloves" has been accepted and published as an 'Indian Patent' with an application number 202141030637.
- ✓ Secured 3rd place, in ARM wrestling competition of coding on LPC2148, target achieved within 6 hours.

Academic Projects

1. HOME+ 2.0 (2019)

- **Domain:** Embedded Systems and IoT.
- **Description:** A simple home automation system developed for Controlling Electrical Utilities using BLYNK. This is developed by interfacing utility switches with BLYNK via NodeMCU, which is programmed in Embedded C Language.

2. HOME+ 3.0 (2021)

- **Domain:** Embedded Systems and IoT.
- **Description:** A better and upgraded version of HOME+2.0 which is developed for Controlling Domestic Electrical Utilities using ALEXA. This is developed by interfacing utility switches with ALEXA via NodeMCU, which is programmed in Embedded C Language.

3. Class Attending bot using Python (2021)

- **Domain:** Python.
- **Description:** Developed a bot Using Python that attends the Online classes in the Microsoft Teams Platform As per Users' schedule at pinpointed time, to reduce the issue of not been able to attend on time.