

Revanth Sai Nandamuri

Hyderabad, Telangana

E-mail: revanthsai.nandamuri@gmail.com

Portfolio: https://revanthnandamuri1341b0.github.io GitHub: https://github.com/RevanthNandamuri1341b0 LinkedIn: https://www.linkedin.com/in/revanth-nandamuri

Mobile: +919581262000

Objective: Responsible and ambitious student with excellent time management, seeking to apply my technical skills in the field of VLSI and Embedded Systems. Possess proven communication skills, technical expertise and strong work ethics.

Educational Qualifications

Class	Institute	Board/University	Marks/ CGPA
10th Std	P. Obul Reddy Public School, Hyderabad(TS)	CBSE	8.0 CGPA
12 th Std	VelocIITy Jr College, Hyderabad (TS)	State Board of Intermediate Education,Telangana	756/1000
B. Tech (Studying)	Vellore Institute of Technology, Amaravati (AP) - 500049	VIT UNIVERSITY-AP	*8.41 CGPA

^{*}Up to 6th semester.

SKILLS:

Hardware Descriptive Languages

Methodologies

Embedded Programming

Programming Languages

Embedded Systems

: Embedded C, Python(Raspberry pi), LPC1728, LPC2148

: Arduino, NodeMCU, Raspberry Pi

: Universal Verification Methodology (UVM)

: Arduino IDE, LabVIEW, VSCode, Xilinx Vivado, ModelSim, QuestaSim, Kiel **Editors/Tools**

: Verilog, SystemVerilog

Workshop/Trainings Attended:

- Advanced Optimization Techniques and Hands-on with MATLAB conducted by Ministry of Electronics & Information Technology through MNIT, Jaipur.
- Achieved Certificate in **Python Data Structures** from University of Michigan.
- Achieved Certificate in Introduction to FPGA Design for Embedded Systems from University of Colorado
- Successfully completed 8 weeks training on "Advanced digital design using Verilog" from LUCID VLSI.
- Successfully Completed training on "System Verilog and Universal Verification Methodology" form LUCIDVLSI.

Academic Projects

1. Agni-PATH (2018)

- **Domain**: Embedded Systems
- **Description:** This project is based on its auto-sensing capability, by the use of various sensors positioned at specified positions, it can detect fire and navigate in the direction and when it reaches near fire it puts off the flame by spraying water in that direction.

2. HOME+ (2019)

- Domain: IoT & Programming in Raspberry pi
- **Description:** Developed for Controlling Home Electrical Utilities using Mobile application. This is developed by interfacing utility switches with Raspberry pi, which is programmed in Embedded Python Language.

3. HOME+ 2.0 (2020)

- Domain: IoT & Embedded Systems
- Description: A better version of HOME+ which is developed for Controlling Electrical Utilities using BLYNK. This
 is developed by interfacing utility switches with BLYNK via NodeMCU, which is programmed in Embedded C
 Language.

4. HOME+ 3.0 (2021)

- Domain: IoT & Embedded Systems
- Description: A better and upgraded version of HOME+2.0 which is developed for Controlling Domestic Electrical Utilities using ALEXA. This is developed by interfacing utility switches with ALEXA via NodeMCU, which is programmed in Embedded C Language.

5. Class Attending bot using Python

(2021)

- Domain: Python
- **Description:** Developed a bot Using Python that attends the Online classes in the Microsoft Teams Platform As per Users' schedule at pinpointed time, to reduce the issue of not been able to attend on time.

SystemVerilog and UVM Projects:

1. Development of SystemVerilog and UVM of verification environment for Memory model (2021)

- Domain: SystemVerilog and UVM
- Description: Developed SV and UVM Verification Environment for Synchronous read/write Memory model.
 - > Developed Master and Slave Agents
 - Developed Slave Sequencer, driver, and monitor.
 - > Developed Out-Of-Order scoreboard.
 - > Developed Functional Coverage component.
 - Developed Callbacks to implement error injection mechanism.
 - Developed RAL Environment to configure CSR's.
 - > Developed backdoor RAL classes to configure CSR's.
 - Developed master Sequences with Test Cases.
 - Developed Slave sequence.
 - Created Test Plan and implemented Test Cases.
 - Running/Debugging Test Cases.

2. Development of SystemVerilog and UVM of verification environment for Router 4x4 Design (2021)

- Domain: SystemVerilog and UVM
- Description: Developed SV and UVM Verification Environment for Router 4x4 DUT.
 - > Developed Master and Slave Agents.
 - > Developed Out-Of-Order scoreboard.
 - > Developed Functional Coverage component.
 - > Developed Callbacks to implement error injection mechanism.
 - Developed RAL Environment to configure CSR's.
 - > Developed backdoor RAL classes to configure CSR's.
 - Developed Sequences and Test Cases.
 - Created Test Plan and implemented Test Cases.
 - Running/Debugging Test Cases

3. Development of UVM of verification environment for ALU Design (2021)

- **Domain**: UVM
- Description: Developed UVM Verification Environment for ALU DUT.
 - > Developed Master and Slave Agents.
 - > Developed **DPI-C** reference model.
 - > Developed Predictor component with DPI reference model.
 - > Developed In-Order scoreboard.
 - > Developed Functional Coverage component.
 - Developed Sequences and Test Cases.
 - Created Test Plan and implemented Test Cases.
 - Running/Debugging Test Cases.

INNOVATIONS & ACHIEVEMENTS:

- Self-initiated idea titled "Portable UV-C Sanitizer" has been accepted and published as an Indian Patent' with an application number 202041033151.
- Self-initiated idea titled "Smart Electrical Measurement System" has been accepted and published as an 'Indian Patent' with an application number 202141026739.
- Self-initiated idea titled "Multimeter on Gloves" has been accepted and published as an 'Indian Patent' with an application number 202141030637.
- Secured 3rd place, in ARM wrestling competition of coding on LPC2148, target achieved in 6
 Hour

Areas of interest:

- Design Verification
- Home Automation
- Microcontroller And Interfacing
- Interfacing With Raspberry Pi.

Subject of interest:

- HDL-Verification
- Embedded Programming
- Machine Learning

Personal Attires:

- Strengths
 - ✓ Adaptability
 - ✓ Self-learner
 - ✓ Leadership skills
 - ✓ Reverse Engineering

- Hobbies
 - ✓ Watching Football
 - ✓ Playing Football
 - ✓ Experimenting new cuisine
 - ✓ Making Daily routine efficient

Personal Details:

1. Father's Name : Nandamuri Prasad

2. Date of Birth : 12th June 2000

3. Languages Known : English, Hindi & Telugu.

4. Address : Flat no.-305, Block

No:01, SMR Vinay Fountain Head, Near Calvery Temple, HyderNagar,

Hyderabad - 500049

Declaration

I hereby declare that the above information is true to my knowledge.

Place: Hyderabad, India.

Date: 25th November 2021 Revanth Sai Nandamuri