PROJECT REPORT

BTECH 3rd Year

ANALOG CIRCUITS

Course: EE301

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Submitted By:-

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AIM: To design beta multiplier, cascode current mirror and cascode amplifier in ltspice and magic.

CALCULATIONS:

➔ For 180nm:

Let the assumed current, I_d= 10µA and unity gain frequency, f_u = 3MHz

Required gain = 20V/V

$$f_u = \frac{1}{2\times\pi\times R_{out}\times C}$$

$$R_{out} = \frac{1}{2\times\pi\times f_u\times C}$$

$$R_{out} = \frac{1}{2\times\pi\times 3M\times 1p}$$

$$R_{out} = 53051.6476\Omega$$

$$A_v = g_m \times R_{out} \quad \Rightarrow g_m = \frac{A_v}{R_{out}} = \frac{20}{53051.6476} \quad \Rightarrow g_m = 3.14 \times 10^{-4}$$

$$g_m = \sqrt{2 \times I_d \times u_n \times C_{ox} \times \frac{W}{L}} = \sqrt{2 \times 10\mu \times 270\mu \times \frac{W}{L}}$$

$$314.159 = 18.277\sqrt{\frac{W}{L}}$$

- $(\frac{W}{L})_n = 18.277$

V_g ,V_s, V_{thp} be the gate voltage of 1st pmos in cascode amplifier,

$\Rightarrow V_g = V_{bias1}$

From cascode current mirror, $V_{bias1} = 1.08V$

$V_s = 1.8V$, $V_{thp} = 0.3906$

$$I_d = 0.5 \times u_p \times C_{ox} \times \frac{W}{L} \times (V_{gs} - V_{thp})^2$$

$10\mu = 0.5 \times 45\mu \times \frac{W}{L} \times 0.1085 \quad \Rightarrow \frac{W}{L} = 4.096$

- $(\frac{W}{L})_p = 4.096$

➔ For 22nm:

Let the assumed current, I_d= 8μA and unity gain frequency, f_u = 1MHz

Required gain = 20V/V

$f_u = \frac{1}{2\times\pi\times R_{out}\times C}$

$R_{out} = \frac{1}{2\times\pi\times f_u\times C}$

$R_{out} = \frac{1}{2\times\pi\times 1M\times 1p}$

R_{out} =159154.94Ω

$A_v = g_m \times R_{out} \quad \Rightarrow g_m = \frac{A_v}{R_{out}} = \frac{20}{159154.94} \quad \Rightarrow g_m = 12 \times 10^{-5}$

$g_m = \sqrt{2 \times I_d \times u_n \times C_{ox} \times \frac{W}{L}} \Rightarrow 12 \times 10^{-5} = \sqrt{2 \times 8\mu \times 120\mu \times \frac{W}{L}}$

$120 = 43.8178\sqrt{\frac{W}{L}}$

- $(\frac{W}{L})_n = 7.5$

V_g ,V_s, V_{thp} be the gate voltage of 1st pmos in cascode amplifier,

$\Rightarrow V_g = V_{bias1}$

From cascode current mirror, $V_{bias1} = 0.2481V$

$V_s = 0.8V$, $V_{thp} = 0.44$

I_d =$0.5 \times u_p \times C_{ox} \times \frac{W}{L} \times (V_{gs} - V_{thp})^2$

$4\mu = 0.5 \times 55\mu \times \frac{W}{L} \times 0.012544 \quad \Rightarrow \frac{W}{L} = 11.59554$

- $(\frac{W}{L})_p = 11.59554$

INPUTS OF CASCODE AMPLIFIER

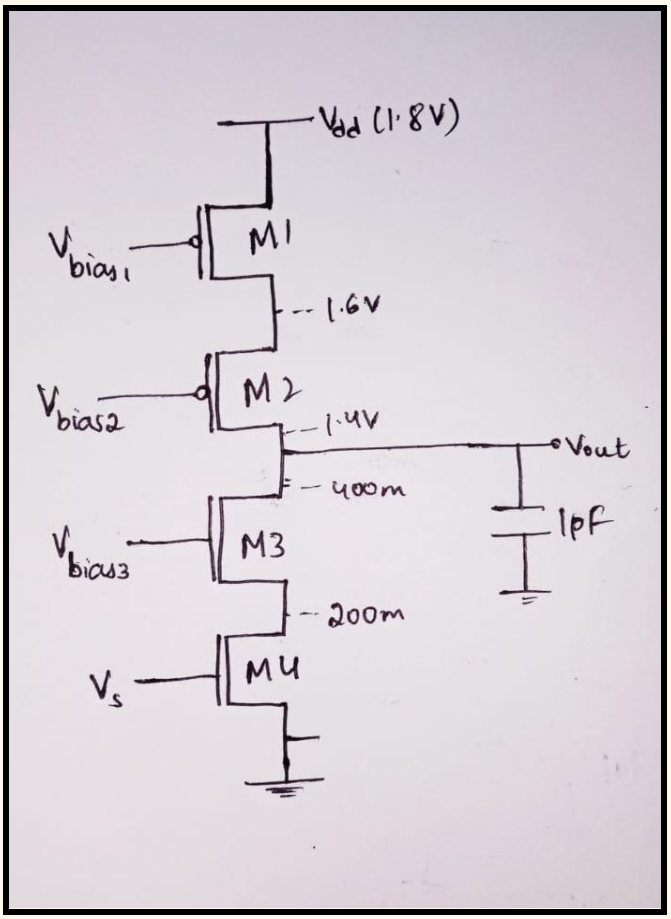
➔ **For 180nm**

For nmos to be in saturation region,

$V_{ds} \geq V_{gs} - V_{thn}$

Let us assume $V_{dsat} = 200m$

- For M4,
  $200m \geq V_s - 0.5, \Rightarrow V_s \leq 0.7$
- For M3,
  $200m \geq V_{bias3} - 0.2 - 0.5$
  $V_{bias3} \leq 0.7$



For pmos to be in saturation region,

$V_{ds} \leq V_{gs} - V_{thp}$

- For M2,
  $-200m \leq V_{bias2} - 1.6 + 0.3906$
  $V_{bias2} \geq 1.0094$
- For M1,
  $-200m \leq V_{bias1} - 1.8 + 0.3906$
  $V_{bias1} \geq 1.2094$

Spice Values:

- V_{bias1} = 1.08V

- V_{bias2} = 941.2mV
- V_{bias3} = 649.62mV
- V_s taken is 500m

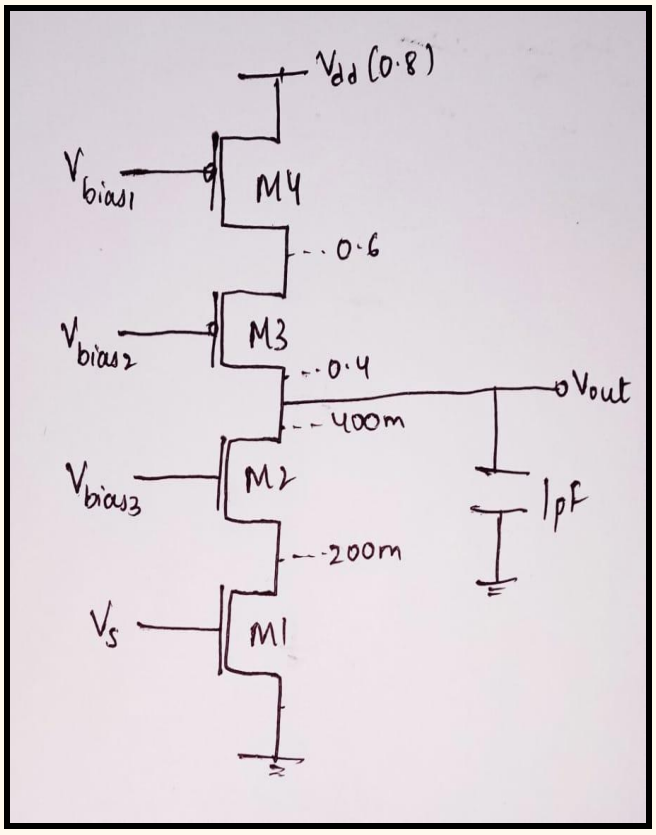
➔ **For 22nm**

For nmos to be in saturation region,

$V_{ds} \geq V_{gs} - V_{thn}$

Let us assume $V_{dsat} = 200m$

- For M4,
  $200m \geq V_s - 0.5, \Rightarrow V_s \leq 0.7$
- For M3,
  $200m \geq V_{bias3} - 0.2 - 0.5$
  $V_{bias3} \leq 0.7$



For pmos to be in saturation region,

$V_{ds} \leq V_{gs} - V_{thp}$

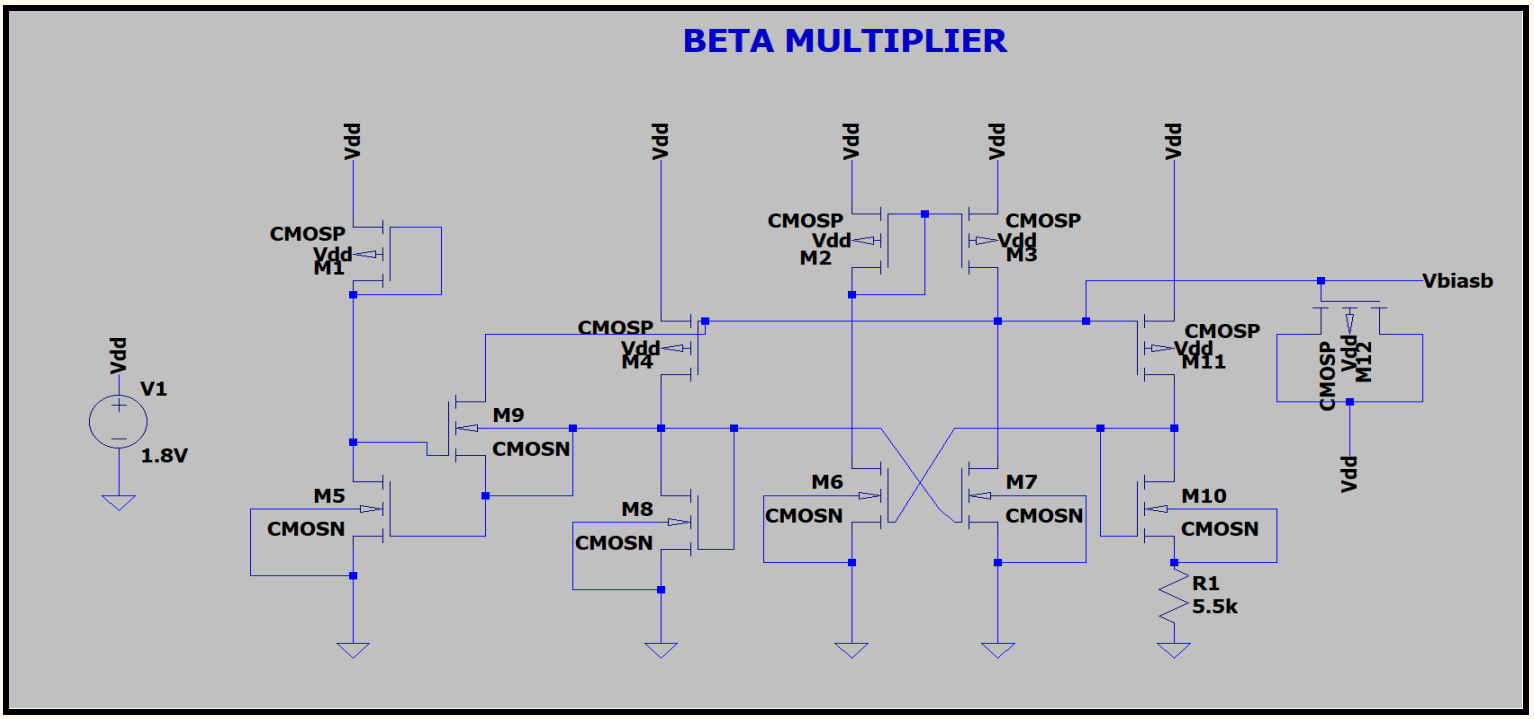
- For M2,
  $-200m \leq V_{bias2} - 0.6 + 0.46$
  $V_{bias2} \geq -0.06$
- For M1,
  $-200m \leq V_{bias1} - 0.8 + 0.3906$
  $V_{bias1} \geq 0.14$

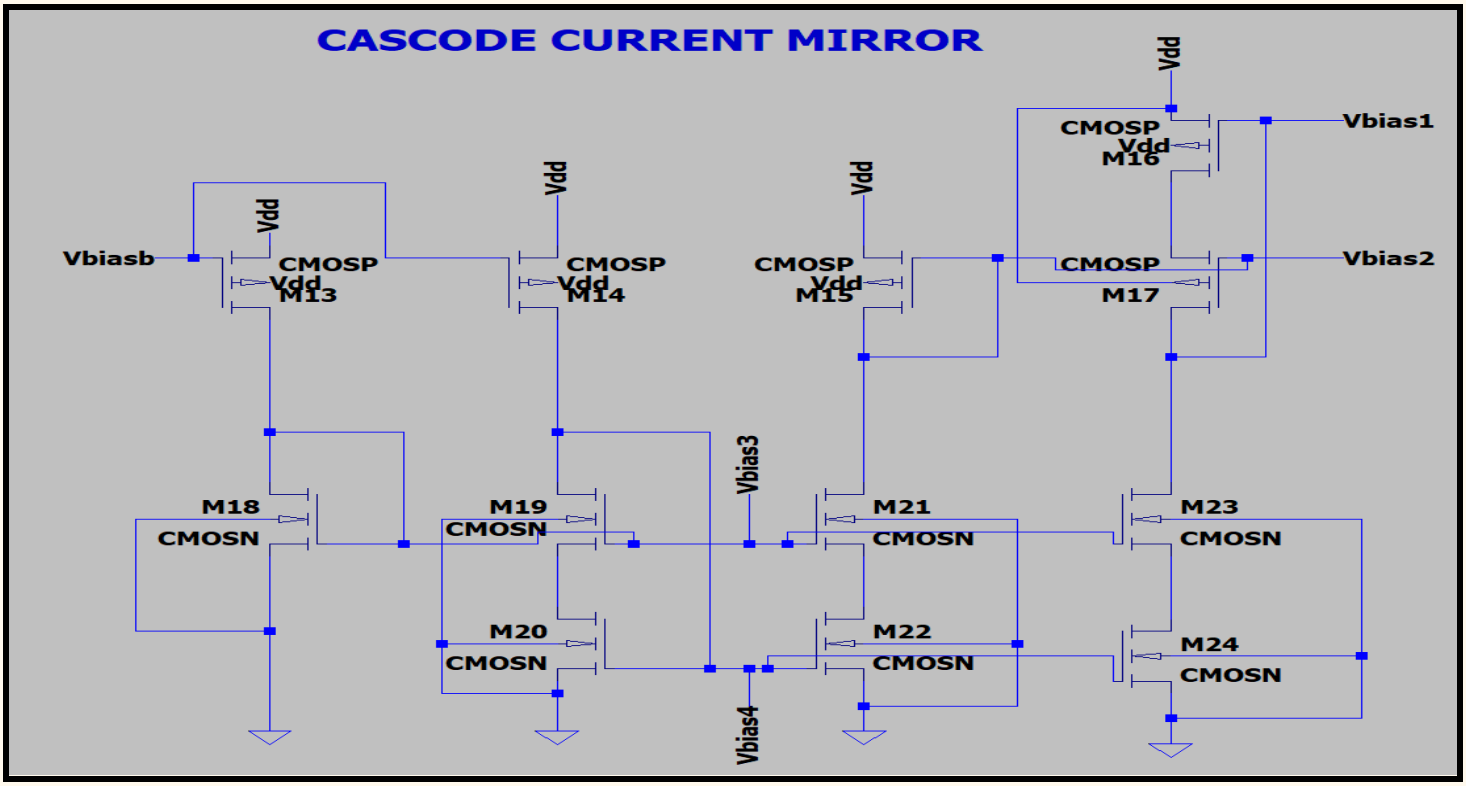
Spice Values:

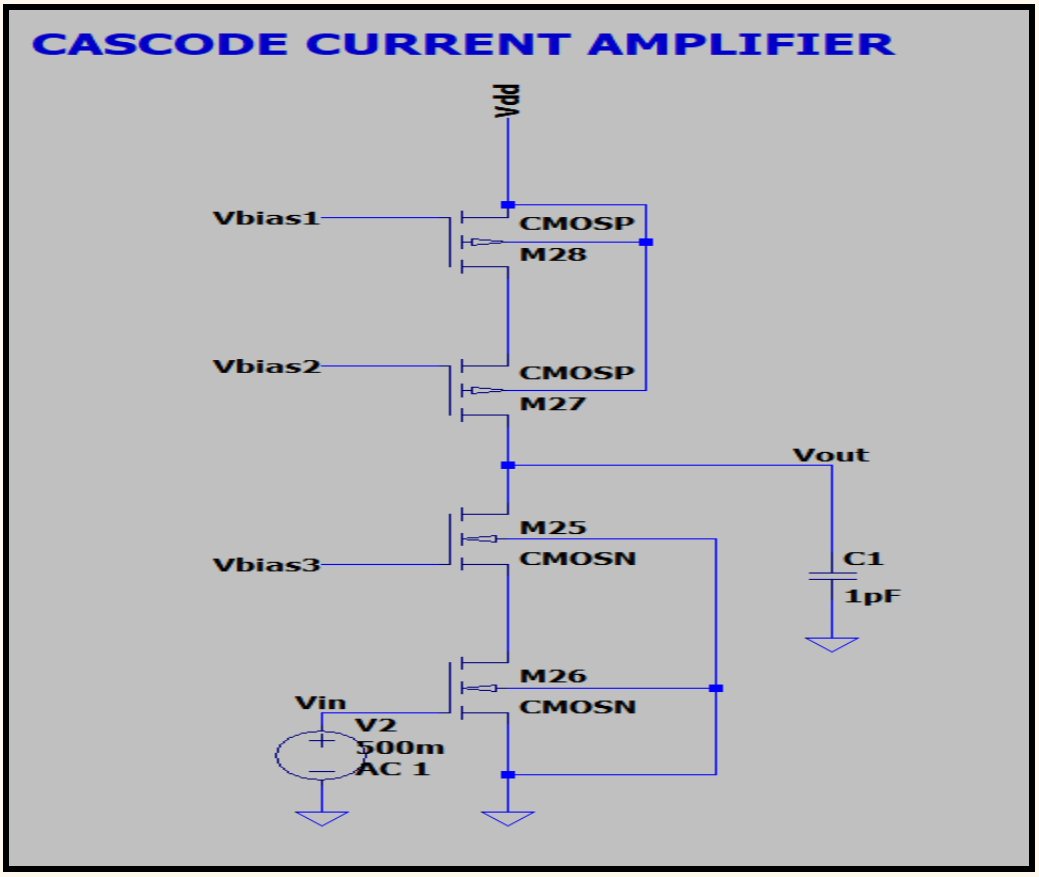
- V_{bias1} = 248.126mV

- V_{bias2} = 150.5mV
- V_{bias3} = 556.60mV
- V_s taken is 600m

SCHEMATIC




CASCODE CURRENT MIRROR
Vdd
Vbiasb
CMOSP
M13
M14
M15
M16
M17
Vbias1
Vbias2
Vbias3
Vbias4
M18
M19
M20
M21
M22
M23
M24
CMOSN


CASCODE CURRENT AMPLIFIER
Vdd
Vbias1
CMOSP
M28
Vbias2
M27
Vout
M25
Vbias3
CMOSN
C1
1pF
M26
Vin
V2
500m
AC 1

LAYOUT

Cascode Current Mirror

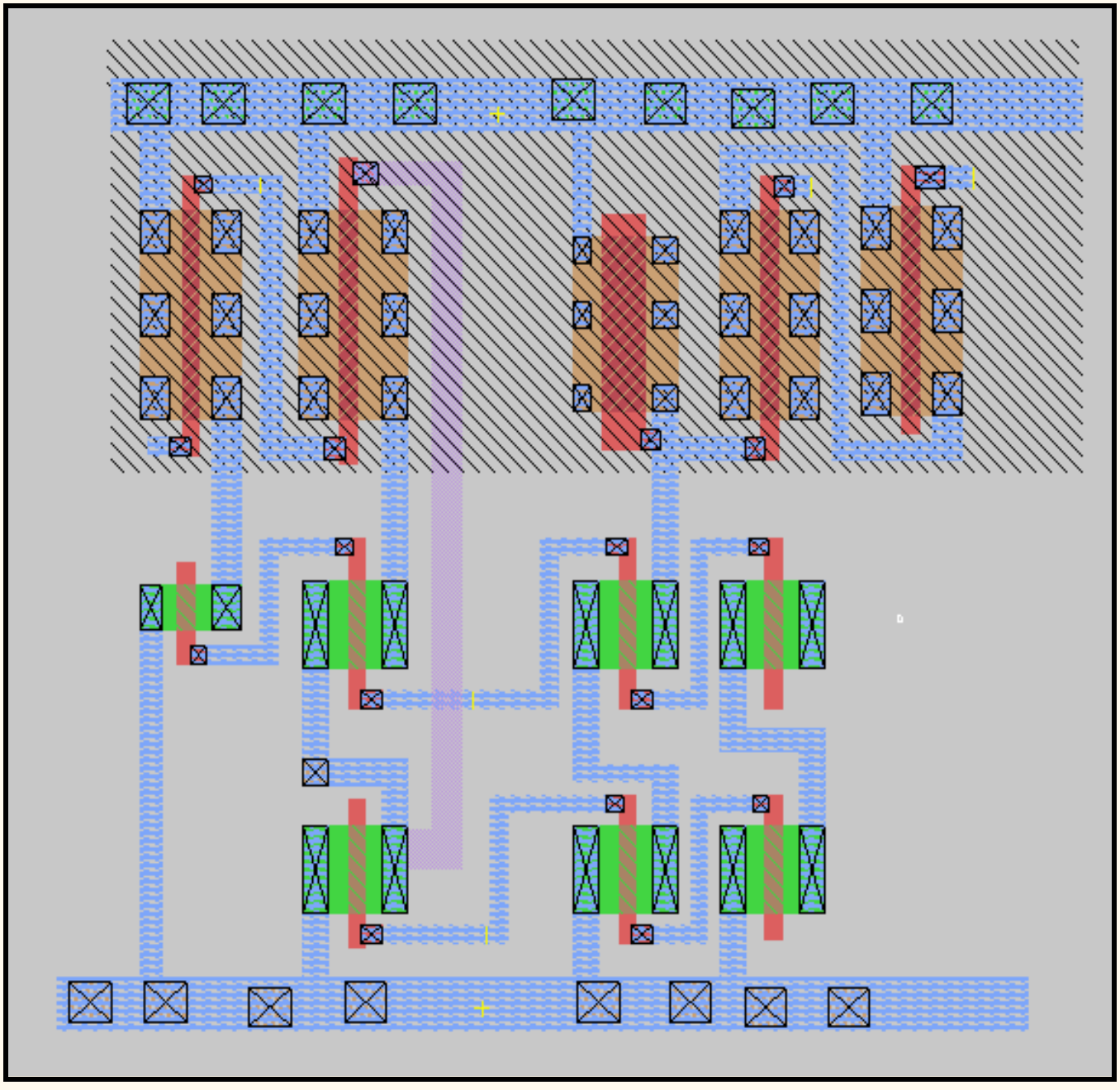


Fig: Cascode Current Mirror Layout

Cascode Amplifier

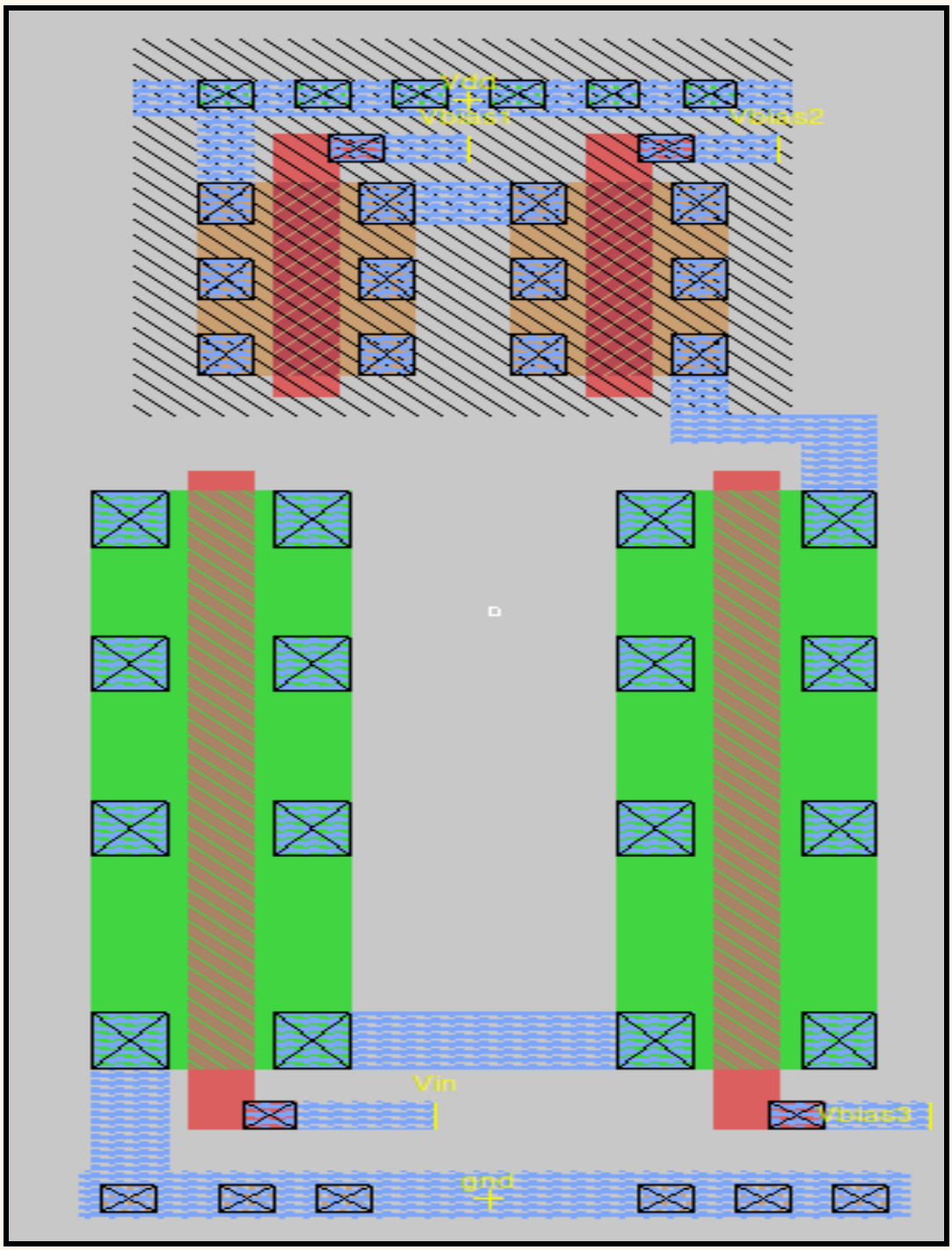


Fig: Cascode Amplifier

OBSERVATIONS:

Ltspice Plots:-

For180nm:

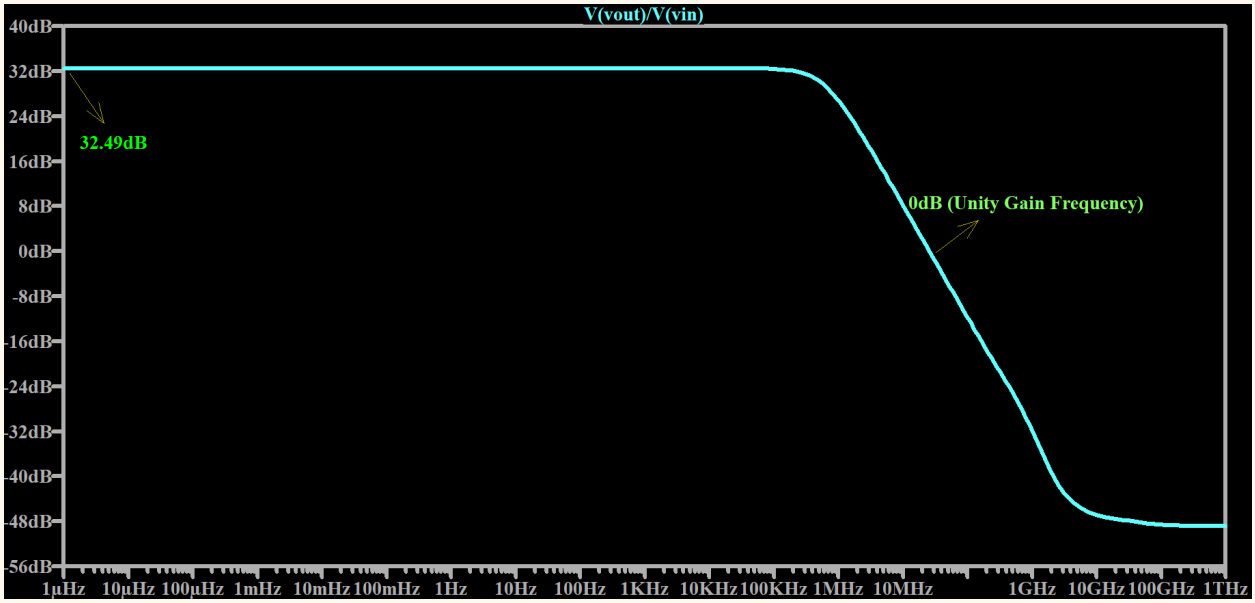


Fig: Frequency Response

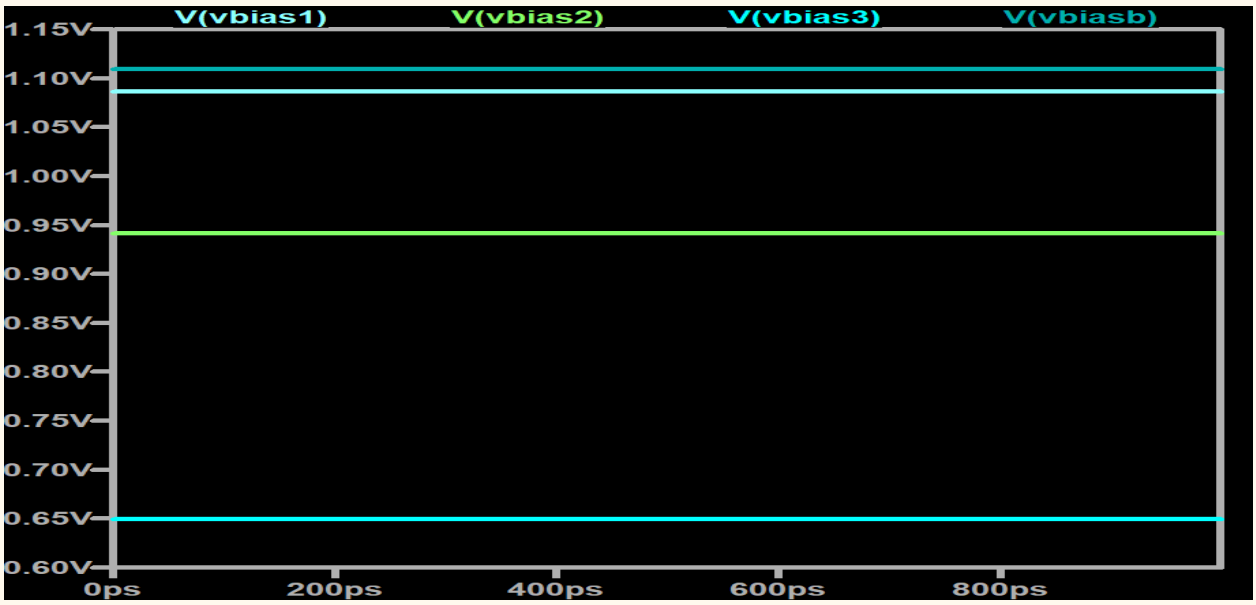


Fig: Vbias Values

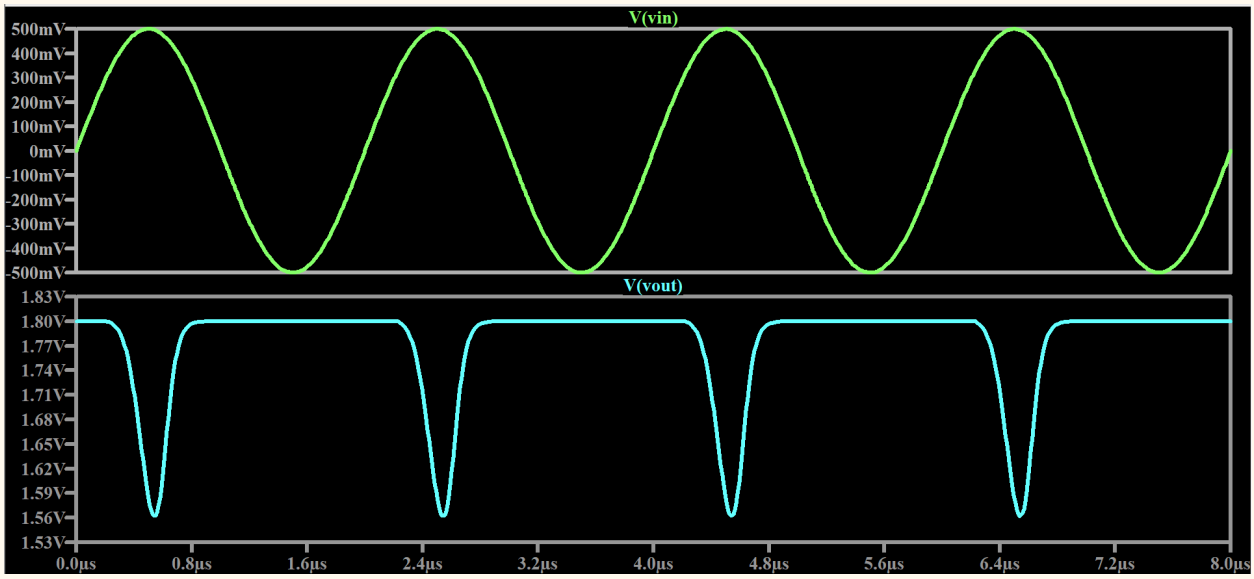


Fig: Sine Input

For 22nm:

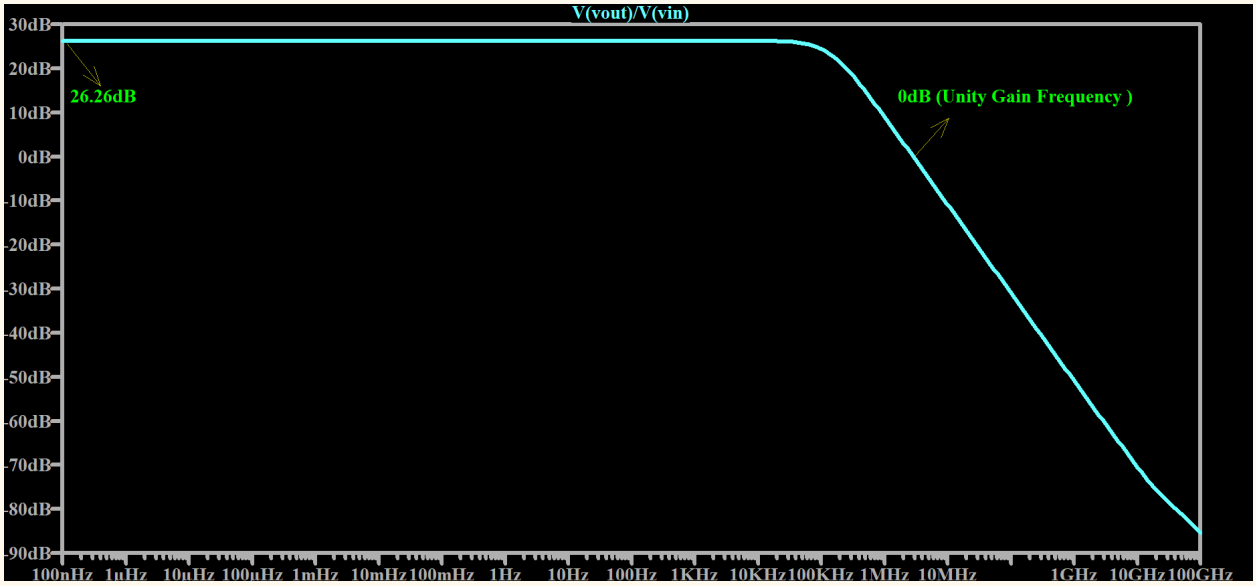


Fig: Frequency Response

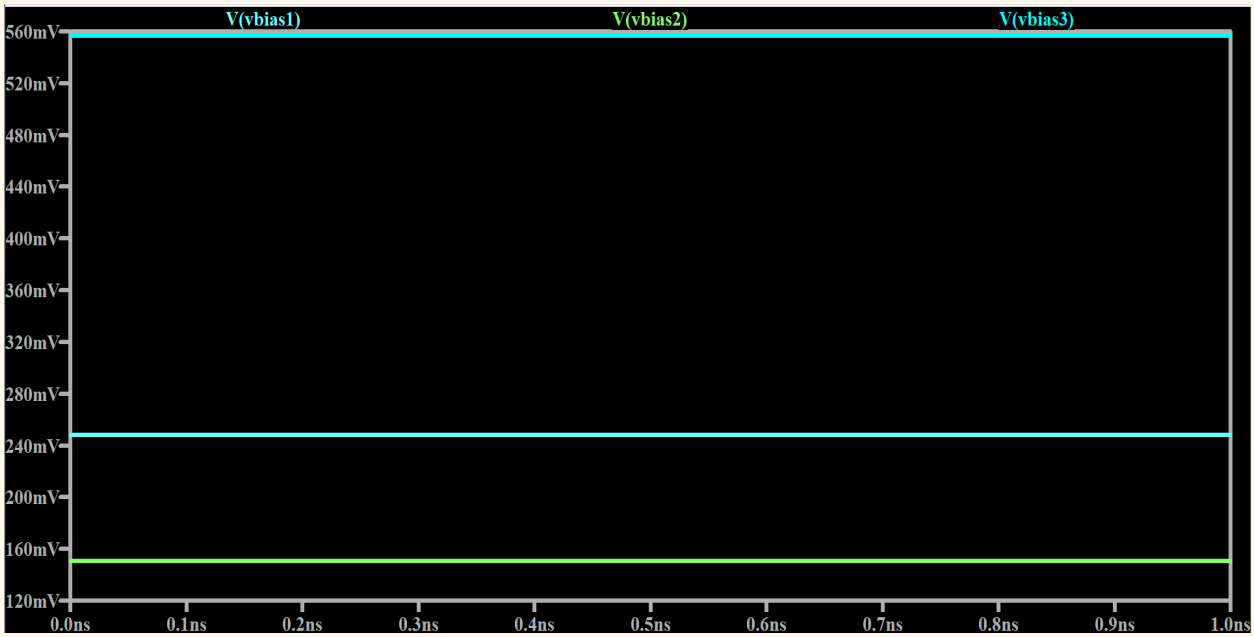


Fig: Vbias Values

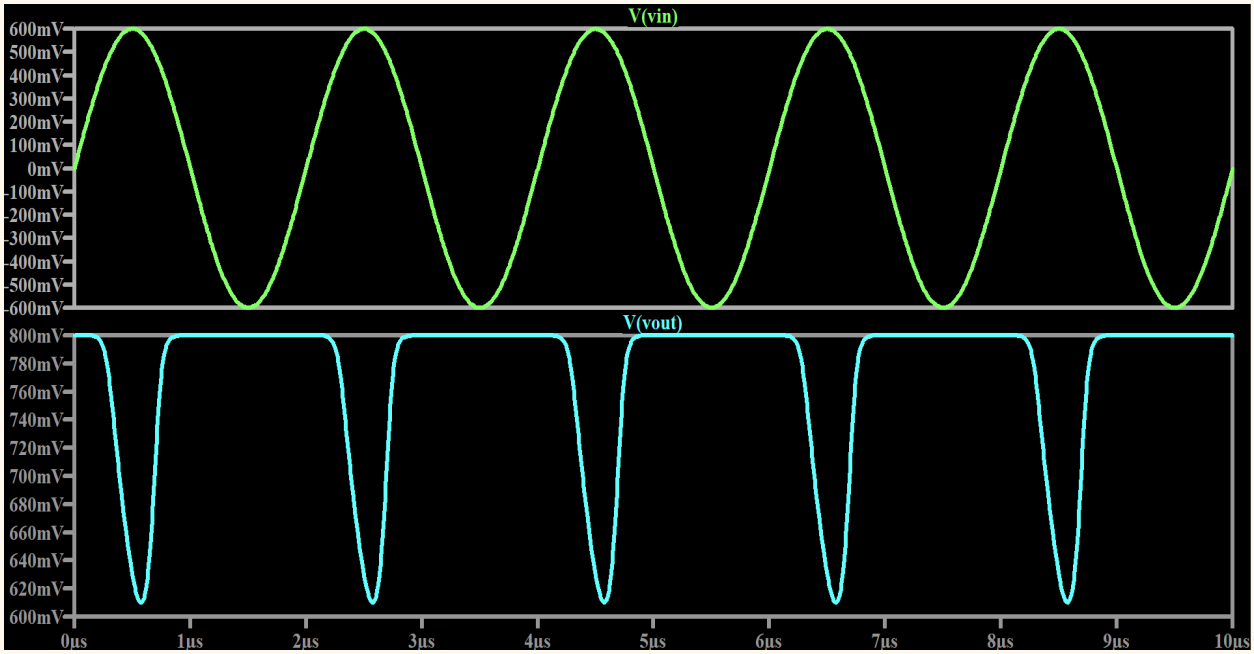


Fig: Sine Input

TABLES:

Technology File	Assumed Values		Spice Values		
	Unity Gain Frequency	Current (microamps)	Unity Gain Frequency	Current (microamps)	Gain (dB)
180nm	10MHz	10	25MHz	8.92	32.49
22nm	1MHz	4	2.78MHz	5.84	26.26

Technology File	Calculated Values			Spice Values		
	gm	$\frac{W}{L}_{nmos}$	$\frac{W}{L}_{pmos}$	gm	$\frac{W}{L}_{nmos}$	$\frac{W}{L}_{pmos}$
180nm	3.14e-04	18.277	4.096	1.7e-04	15	5
22nm	12e-05	7.5	11.59	4.59e-05	5	9.39

REQUIRED SPECIFICATIONS:

- Required gain is 20V/V = 20log(20) = 26.02dB, hence simulated gain should be atleast 26.02dB. Gain is 32.49dB and 26.26dB for 180nm and 22nm respectively.
- Power dissipation ≤ 5mW. From simulated data 16µW and 4µW for 180nm and 22nm respectively.
- Unity Gain Frequency must be greater than 500KHz. It is 25MHz and 2.78MHz for 180nm and 22nm respectively.
- Frequency response must be a low pass filter.

  Hence required specifications are satisfied.

CONCLUSION: Beta Multiplier, Cascode Current Mirror and Cascode Amplifier are simulated in ltspice and magic software. Practical calculations are almost appropriate to ltspice values. Different analyses are made and understood. It's also visible from the observation tables that the assumed, calculated and spice values of different parameters are approximately in the same ranges, which verifies that the simulations and practical calculations are almost matched with each other.