STUDY AND DESIGN OF PHASE INTERPOLATOR FOR CLOCK AND DATA RECOVERY CIRCUITS

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by

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2023

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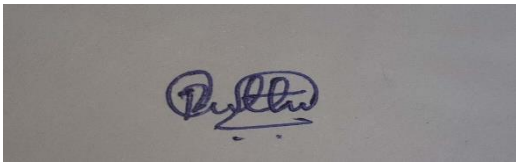

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Abstract

The Phase Interpolator (PI) circuit designed herein, generates an intermediate phase between two known phases to accurately estimate the phase of the input signal. The phase interpolator circuit provides a fast and accurate response to changes in the input signal's phase and frequency, ensuring reliable clock recovery. It is also highly scalable and can be easily adapted to different input signal frequencies and data rates by providing an efficient and effective solution for clock recovery in CDR networks, ensuring high-quality data transmission and improved system performance. The phase interpolator circuit designed herein is specifically tailored for CDR networks and provides accurate and reliable clock recovery.

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Chapter 1

Introduction

Signaling at high speeds in inter chips is a crucial area of development in a currently growing electronics system. The communication standards have two areas of interest: i) low-speed parallel links, ii) high speed serial links. Some examples of low speed parallel links are, processor interconnection buses, memory buses etc. Some examples of high speed serial links are backplane connectors used in larger systems.

Being the very basic architectures for data transportation, parallel links are used to convey data at the same time across many channels, and they have a slower transfer rate, which lead to rise of serial links. These serial connections can communicate data in a sequential order along a single channel.

Parallel links have separate clock which is sent in parallel along with the data stream. As a result, the receiver's key difficulty is to use the clock signal to sample the incomingdata at the most appropriate point. In contrast, the clock signal in serial-links is generally contained in the data stream, necessitating the usage of a joint clock and data recovery (CDR) circuit to extract the clock from the input stream and use it to sample the data.

Phase-interpolating circuits are increasingly being employed as independent circuits or integrated inside a phase locked loop (PLL) or delay locked loop (DLL) design to overcome timing difficulties that emerge in high-speed signaling. As a result, phase interpolators have become essential components in a wide range of systems. This research investigates the required functionality of phase interpolators, as well as their current architectures, strengths, and limits, to provide a full understanding of their application in minimizing timing difficulties in high-speed signaling.

The demand in recent years for high speed communication in chips has increased very rapidly. For these purposes transmission line has been setup, which can reach speeds of about 1Gbs , later from the year 2000. When a signal is sampled at these high frequencies, this make transmission line to become noisy, which is result of several causes like dispersion in channel, attenuation in channel, etc. This can lead to skew of data in high speed transmission lines. Hence transmitting information through these channels has been a challenging task.

In order to overcomes these limitations, it became important to have some high latency interconnections, so as to achieve high speeds of processing and also to increase performance of system. However, the input signals frequency, may change or vary due to factors like variations in load, voltage, and temperature. This can lead to inappropriate transmission of data, and also lead to control loss in some systems.

This lead to need of some clock alignment circuits like clock and data recovery circuits (CDR). There are different architectures of CDR, one of which is phase interpolator based CDR. With the help of phase interpolator in a circuit , we can generate a phase locked input reference signal of an output signal. This can be done even in presence of some phase variations and frequencies. Hence by adjusting the output signal's phase and finely tune it, in very fine increments or steps, so as to ensure the synchronization of an output signal along with the input signal. Hence, this reduces the errors in transmission line which is transmitting data and thereby increasing the performance of a system.

In this way, phase interpolator acts as a crucial component in data acquisition and high speed communication systems, as these systems require tracking of frequency and phase. Phase interpolator ensures accurate data recovery in a data stream, by ensuring synchronization between signals of input and output and has an ability to work or operate across a wide range of frequencies. This makes PI an essential tool for control and high speed communication systems.

Chapter 2

Literature survey

The idea of phase interpolation is there around for some long time, dating back to the signal processing's early days. Due to the huge spread uses of a phase interpolator, has been made possible, as a result of advancement in processing technique of digital signal , later 20th century.

In the initial days of communication systems, especially in analog, one of the clock data recovery architectures used were phase locked loop (PLL). The PLL can be used in order to retrieve the frequency of a carrier signal and modulated signal's phase. With the help of PLL we were able to trace the changes in these phases and frequencies, with a voltage controlled oscillator (VCO). It synchronizes the input signal by generating phase and frequency. This made the initial use of phase interpolation technique.

Digital control in networks of communication can be utilized to tune or adjust the framework of a phase interpolator, in order to achieve required phase of an output signal resulting in a phase creation. There are different types of phase generators, which are also called as digital to phase converters (DPCs) [5] and this is divided into three groups, namely digital controlled delay lines (DCDLs), digital to time converters (DTCs) and phase interpolator (PI).

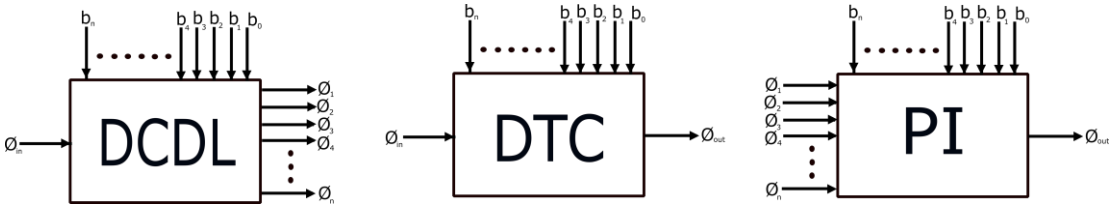


Figure 2.1: Types of digital to phase converters(DPC's)

With the development of digital signal processing techniques in the 1970s, the analog PLLs were replaced by digital phase-locked loops (DPLLs). [1] The DPLL is compared with analog PLL designs, and the advantages of the digital approach are discussed. These DPLLs used digital circuits to perform the same function as an analog PLL, to recover the carrier

frequency and phase of a digital modulated signal and to synchronize the receiver's clock to the transmitter's clock.

Phase interpolators were used to improve the performance of digital communication systems and to increase the data transmission rates in wireless communication systems. This was a significant advancement in signal processing technology, leading to more efficient and reliable communication systems.

In the 1990s, high-speed digital signal processing techniques paved the way for the use of phase interpolators to generate intermediate phases between two known phases. [2] Long wave encoders, despite having extremely long wavelengths, can achieve a high pitch accuracy. However, to obtain a high-accuracy and high-resolution pulse, high-accuracy and high-resolution interpolators are generally required.

In recent years phase interpolators are moving towards higher precision, faster operation, and lower power consumption. [3] Twin-phase interpolators are made up of two identical routes, each with its own delta quadrature delay-locked loop (DLL), current-mode logic (CML) phase detector, and capacitor array digital-to-analog converter (DAC). The twin-phase interpolator delivers outstanding jitter performance and strong linearity, making it suited for high-speed data link cloaking applications.

Today, phase interpolators are widely used in various digital signal processing applications and are an essential component of modern communication systems. Their development and refinement over the years have led to significant improvements in signal processing and communication technology, enabling faster and more reliable data transmission rates, and ensuring high-quality audio and video output in digital audio and video processing applications. The concept of phase interpolation has come a long way, and it continues to play a crucial role in the development of new technologies that shape the way we communicate and process information.

Chapter 3

Phase Interpolator

A phase interpolator (PI) is a circuit in electronics, that generates a set of output clock signals withphases that are intermediate between two or more input clock signals. The PI circuit is used in high speed digital communication systems, such as data transmission and clock recovery circuits, where precise timing synchronization is essential.

This section describes the overall working and operation of phase interpolator as follows:

3.1 Basic Phase Interpolator

A phase interpolator (PI) consists of two input clock signals ϑ_1 and ϑ_2 that are periodic and have the same period of oscillation. The desired interpolated phase is decided by the control bits or inputs of phase interpolator and is typically a signal that indicates the weighing factor for phase interpolation. The phase interpolator then generates an interpolated output signal , based on the specified phase mixing requirement. 3.1 shows the schematic of a phase interpolator adapted from [4] .

The circuit illustrated above includes inputs that have an absolute phase, along with a weighting factor, represented by “w”, which can range from 0 to W. If the control valueof w is set to 0, the output signal will have a phase of ϕ, while a value of W will result in an output signal with a phase of ψ. This is a basic representation of a phase interpolator, and 3.2 displays the corresponding waveforms.

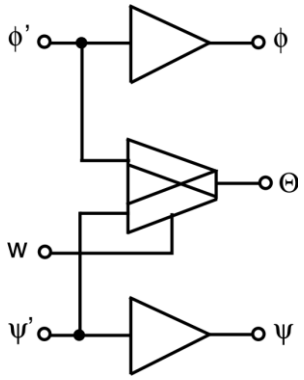


Figure 3.1: Block diagram of a basic phase interpolator

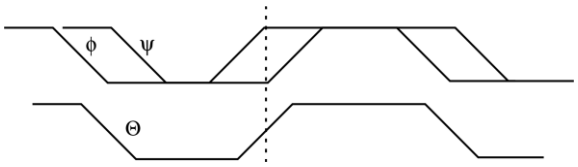


Figure 3.2: Phase interpolator output waveforms

3.2 Characteristics of Phase Interpolator

Phase interpolating circuits need to exhibit certain favorable characteristics such as a monotonic and linear transfer characteristic, maximum rejection at minimum or maximum control input, insensitivity to input waveform rise time and fall time, delay between inputs, process, temperature, and variations in supply voltage. The significance of properties differs depending on the intended uses. In addition, the seamless boundary requirement, as mentioned in [4], demands that only one input waveform should impact the output.

In a phase interpolator, **resolution** refers to the smallest step size in which the output signal phase is adjusted. The resolution of a phase interpolator is determined by the number of bits used in the digital-to-analog converter (DAC) that controls the phase adjustment.For example, a phase interpolator with a 10-bit DAC will have a resolution of 360/1024 degreesper step.

Jitter, on the other hand, refers to the deviation of the output signal from its expected position in time. In a phase interpolator, jitter can occur due to several factors such as noise, interference, and timing errors in the input signal and can be reduced by using techniques such

as jitter filters and delay-locked loops (DLLs).

Bandwidth is often referred to as the frequencies range, and in reference of phase interpolator , it refers to frequency range, to operate it efficiently and effectively. In phase interpolator, bandwidth can be known by various factors, like interpolator circuitry design, resolution of the interpolator and the input signal's speed.

There been a complex interdependence and tradeoff between resolution, jitter and bandwidth in a phase interpolator. In order to achieve a very high resolution, high sampling rates were used, and this increases the complexity in the circuit, thereby increasing the jitter of PI. Even higher bandwidths include complex circuits, which is also responsible in increasing the jitter of phase interpolator, this increases power consumption. This lead to need to settle for some optimal values, which satisfies the design specifications.

3.3 Types of Phase Interpolators

There are various categories of a phase interpolator, some of them are:

1. **Variable Slope PI:** A variable slope phase interpolator uses current mode logic (CML), which uses tail currents in order to adjust or control the weights of the input signals which is responsible in deciding the phase of output signal [5]. As the tail current has a variable slope, this lead to non linearity in the circuit, which increases power consumption. These variable PIs use analog circuits and delay elements, like phase detectors, charge pumps etc. Some of the applications of variable slope PI include spread spectrum communication system.

2. **Constant Slope PI:** Constant slope phase interpolators, on the other hand, generate clock signals with a constant phase slope. They use a series of delay elements with precisely matched delays to create output clock signals that are interpolated between two or more input clock signals. There is a relation between input signal, output signal and constant phase slope, making them useful in applications where precise timing synchronization is required, such as in high-speed data communication systems.

3. **Digital PI:** Digital phase interpolators generate a phase output using digital signal processing techniques. They are widely employed in digital communication systems because

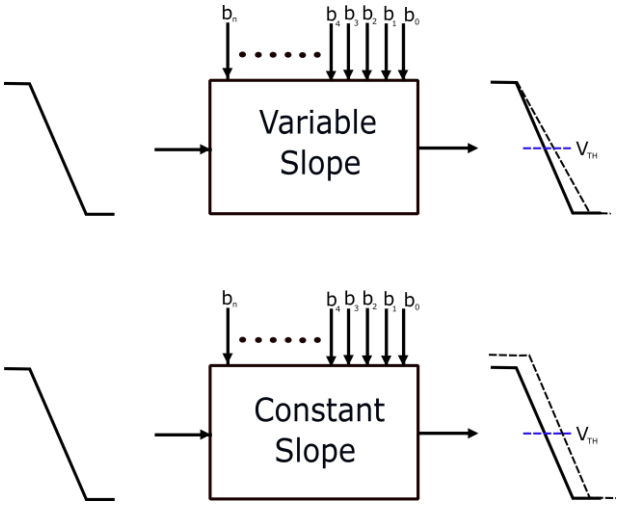


Figure 3.3: Variable vs constant slope operation

of their great accuracy and stability in phase generation. Digital phase interpolators are also simple to implement in DSPs and FPGAs.

4. **Analog PI:** Analogue phase interpolators generate a phase output using analogue circuits. They are widely employed in analogue communication systems because of their great accuracy and stability in phase generation. Analogue phase interpolators are also simple to incorporate into analogue circuits.

3.4 Implementation of Phase Interpolator

This report presents a phase interpolator that operates on a constant-slope basis [5]. As a result, a linear operation and low power consumption can be achieved with a large dynamic range. With a 1.2V supply and a 0.5GHz frequency, it is implemented in 65nm CMOS technology. Phase Interpolator design consists of some subsystems.

3.4.1 PI Half Cell

PI half-cell schematic is illustrated in Fig5, wherein M_S serves as a source that provides constant current, C_0 represents the capacitance across which output is taken. M_1 regulates the timing of discharge of C_0, while M_2 serves as a switch that 'reset', i.e it discharges C_0 to ground. Meanwhile, M_3 and M_4 function as switches that 'set', i.e charge Co from 0 to V_{dd}.

The corresponding schematic and waveforms with modes can be seen in 3.4 and 3.5 re-

spectively.

- In mode 1, the transition of clk0 from low to high occurs, while clk60 remains low. As a result, the capacitor charges slowly until clk0 becomes high.
- In mode 2, clk0 is high, and clk60 is low, leading to a slow discharge of the capacitor.
- In mode 3, clk0 is low, and clk60 is high, causing the voltage across the capacitor to be zero as it discharges rapidly to the ground via M_2 .

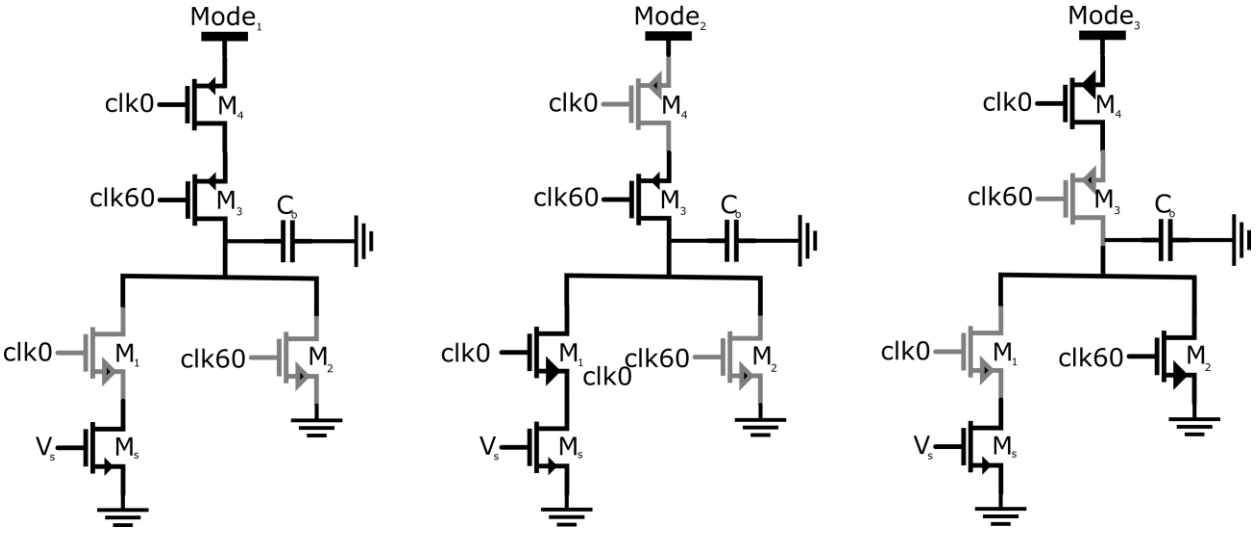


Figure 3.4: Schematic and operation of a PI half cell

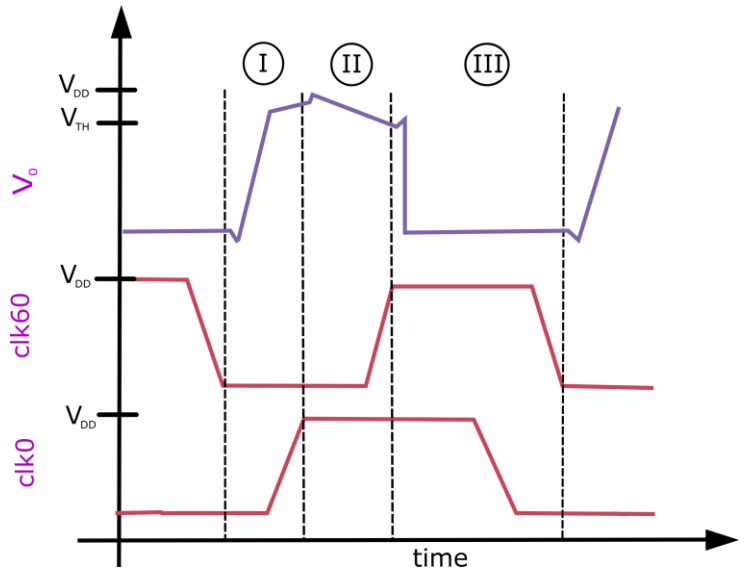


Figure 3.5: Waveforms from a PI half cell

The output voltage slope, during mode2 operation is: $\frac{dV_O}{dt} = -\frac{I_C}{C_O}$

If we consider the current through M1 as Ic, then for constant-slope operation, we need to keep Ic constant because Co is constant. To achieve this, a source Ms that provides constant current is utilized. By doing so, we can control the output voltage slope, exclusively with Co. We can also adjust Co to facilitate multi-rate operation.

3.4.2 PI Unit Cel

In order to construct a PI unit cell, the PI half-cell's output is linked to a toggle flip-flop (TFF) as depicted in 3.6. The PI half-cell is powered by the clk0 and clk60 inputs, and the TFF is set to the high state. An edge-triggered TFF that responds to positive edges is used, resulting in an output clock signal that runs at half the rate of input. The waveforms were illustrated in 3.7.

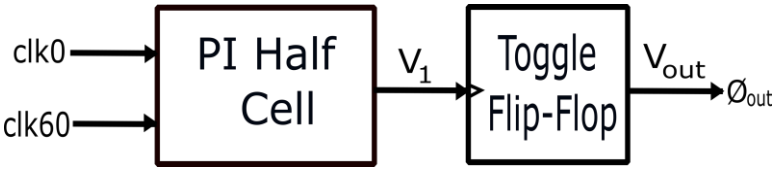


Figure 3.6: Phase Interpolator unit cell

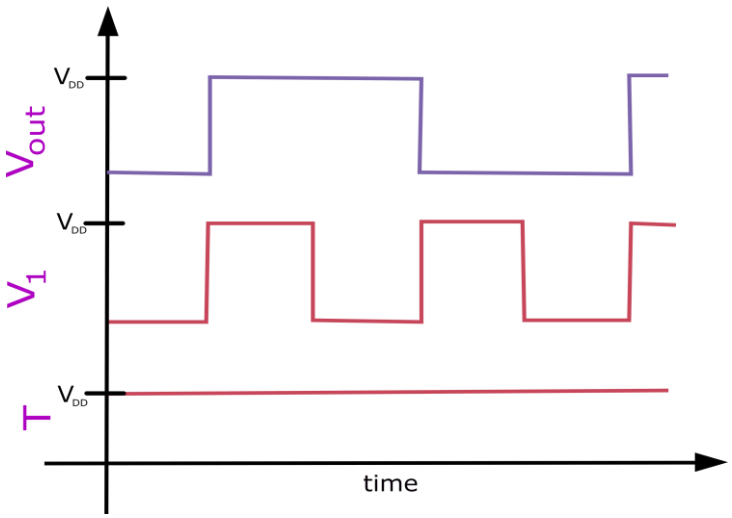


Figure 3.7: Waveforms from a PI unit cell

3.4.3 PI Cell

Fig3.8 depicts the complete structure of the PI cell, which comprises six PI half cells that utilize the input clocks of clk0, clk60, clk120, clk180, clk240, and clk300 to divide the phas

space into 60-degree sextants. The output from each half cell is conveyed to a TFF to yield the ultimate output clock.

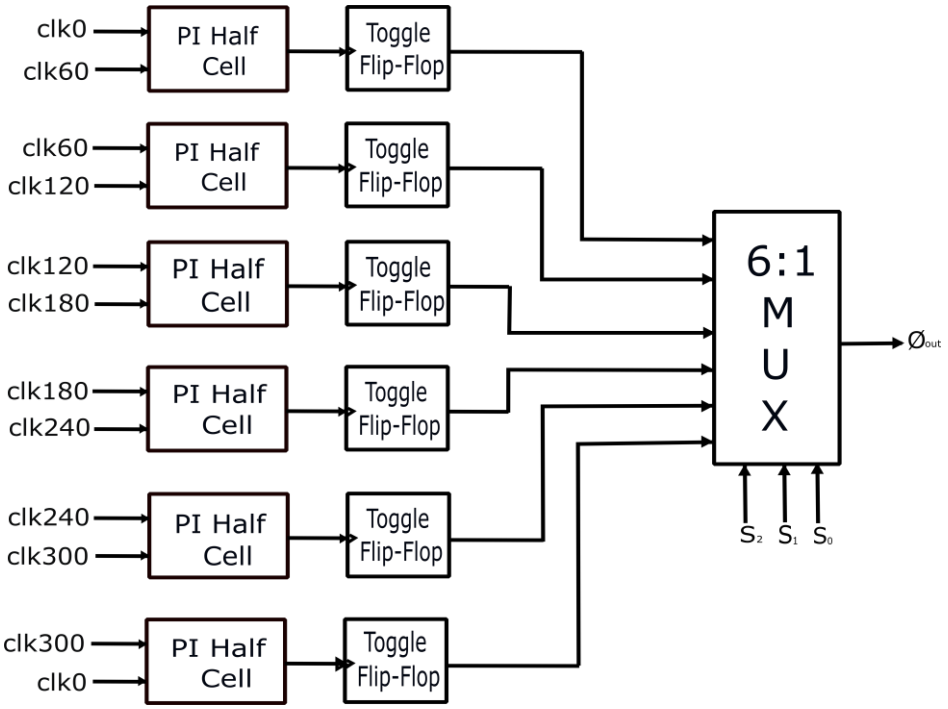


Figure 3.8: Schematic of a PI cell

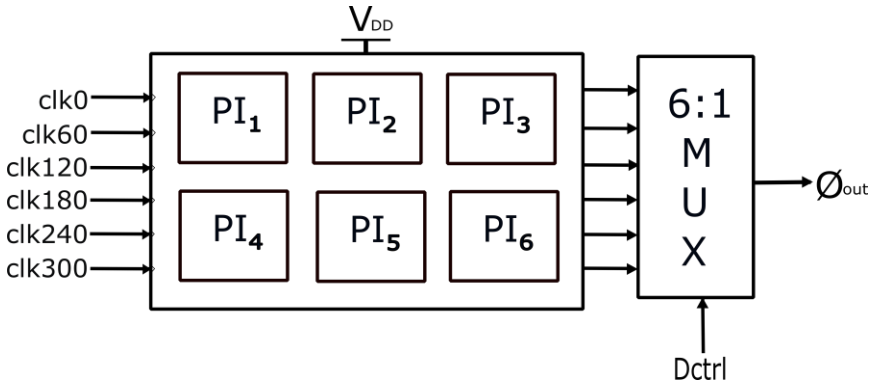


Figure 3.9: Block diagram of full phase interpolator architecture.

To enable coarse control, a 6:1 multiplexer is employed to select the sextant based on the control bits. The detailed schematic is presented in , while 3.8 illustrates the entire suggested phase interpolator architecture.

3.4.4 Challenges and limitations in design

A constant slope phase interpolator is a type of phase interpolator that generates output clock signals with a constant phase slope. This type of phase interpolator is commonly used in high-speed digital communication systems, where precise timing synchronization between the transmitter and receiver is critical.

Designing a constant slope phase interpolator can present several challenges and limitations. Some of these include:

- **Circuit complexity:** A constant slope phase interpolator requires a significant number of delay stages to achieve a constant phase slope, which can increase the circuit complexity.
- **Power consumption:** The increased circuit complexity can also lead to higher power consumption, which can be a limitation in low-power applications.
- **Nonlinearity:** Nonlinearity in a circuit is due to varying slope of output voltage. When there are delay elements in a circuit, nonlinearity causes distortion in output signals, which leads to timing synchronization's errors.
- **Jitter:** Jitter refers to the dissimilarity in the timing of a clock signal. This can be caused due to interferences, complex circuitry, noise, etc. Jitter is a necessary limitation when high speed communication systems are considered. Hence it important and challenging to minimize jitter.
- **Operating frequency:** In a constant phase interpolator, parasitic capacitances, intrinsic delay due to delay elements, limit the operating frequency of a phase interpolator.
- **Interpolation range:** In a constant phase interpolator, delay line's number of stages, minimum delay of the delay elements, limits the interpolation range of PI.

To achieve high-performance, low-power, and accurate timing synchronization in high-speed communication systems, it is necessary to carefully design and optimize a constant slope phase interpolator while also using compensation techniques and hybrid interpolation strategies. Overcoming the challenges involved in designing a constant slope phase interpolator requires a thoughtful approach that addresses each of the aforementioned design considerations.

3.5 Phase Interpolation Applications

Phase interpolator applications are becoming increasingly important in various fields such as telecommunications, digital signal processing, and frequency synthesis. The ability to generate high-frequency signals with precise phase control is critical for many applications, including wireless communication systems, radar systems, and satellite communications. In this section, we will explore its various applications, and provide examples of how it is used in real-world scenarios.

- High-speed signaling circuits require phase interpolating circuits to produce accurately synchronized clocks [6], especially in channels where no additional clock signal is transmitted. A common approach is to use a PLL-based clock data recovery (CDR) system, which em- ploys a voltage-controlled oscillator (VCO) in order to generate clock signals with some phases of about four or eight in number. However, a PI is employed for interpolation in between the VCO clock phases. Generating phases of greater than eight in number from VCO is usually not practical, as this requires a ring oscillator which has a limited frequency of oscillation. The design of PLL, that uses phase interpolator is discussed in [7].

- Even in parallel standard links, in which the clock is sent through the channel along with the data, it is important to produces clock signals from the primary clock which is provided by the source, for the alignment of precise data sampling. In such cases, the clock of input signal is sent across buffers, which are responsible for generating several phases. This accurately synchronized clock signal is thereafter used in sampling received data. Such a network is often realized with a delay- locked loop and a voltage-controlled line (VCDL) as the delay chain. In [8] a designing of DLL which also includes phase interpolator is illustrated.

- Phase interpolators are used in clock data recovery (CDR) circuits to recover the signal of clock, from incoming signals. [9] Phase interpolator is used to generate a clocksignal that is aligned with the data signal, ensuring accurate data sampling.

3.6 Results

The output waveform of each PI cell is designed to exhibit a specific phase shift with respect to the input signal. This phase shift is necessary to ensures that the retrieved clock signal will be in phase to data stream, and is achieved by changes the input phases of PI unit cell. The output waveform from the designed phase interpolator is as shown in Fig 3.10 and full architecture of PI cell in Fig 3.11.

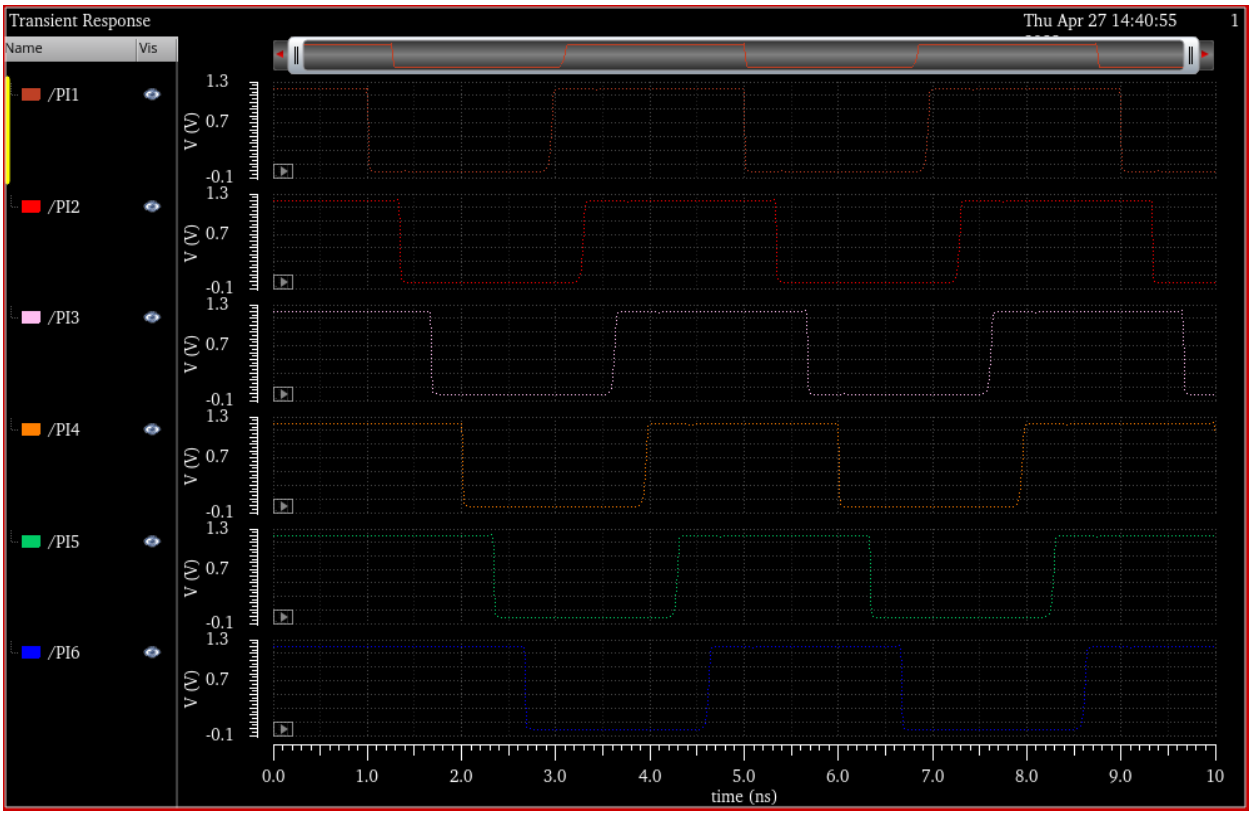
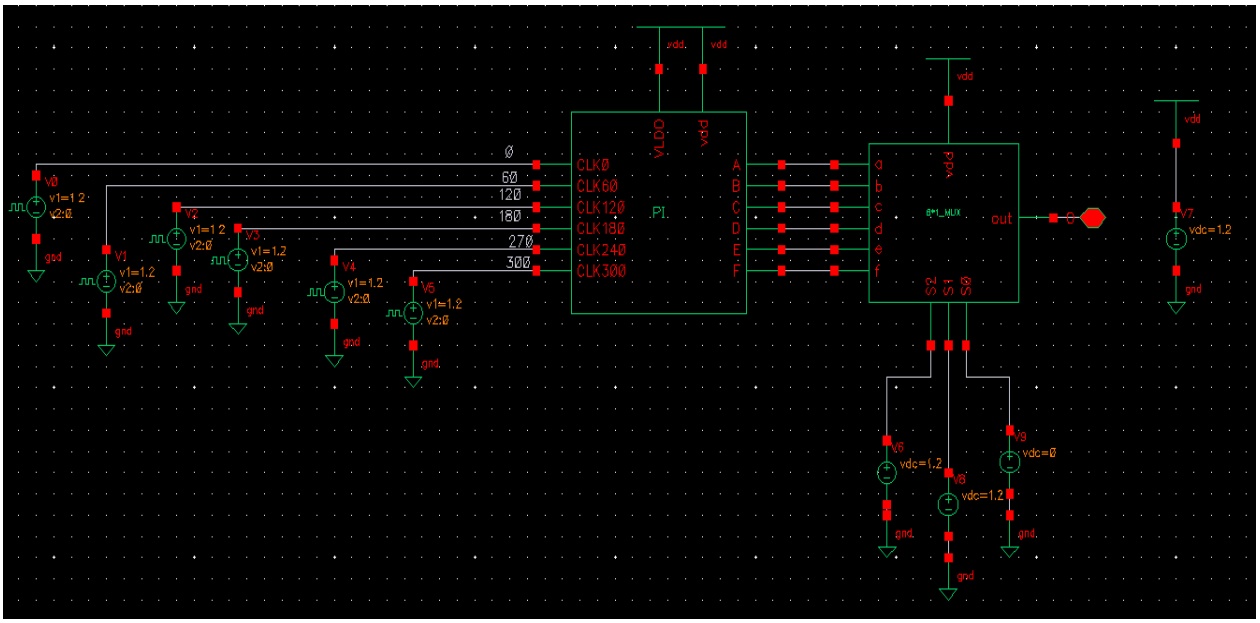


Figure 3.10: Output waveforms from each PI unit cell.

The output waves of each Phase interpolator cell are designed to produce a half-rate pulse of that of input clock signal. This means, the output is produced at half the frequency of the input, which has a duty of 50%. Purpose of this design is to facilitate clock recovery by allowing the circuit to generate a clock signal that is synchronized with the input data stream.

Figure 3.11: Schematic of complete architecture of PI cell.



Therefore, by synchronizing the output and input signals, the phase interpolator can accurately retrieve data in an incoming data stream. This shows the reliability and accuracy, efficiency and improved system performance of the phase interpolator, resulting in wide applications of it in communication networks.

Chapter 4

Conclusion

This report deals with characteristics, implementation, applications, limitations and challenges faced in designing a phase interpolator. It is a very crucial element in communication systems. This report also includes inclusive analysis of phase interpolator and also highlights the future work or extensions which can be done. Overall, the report consists of a thorough study of design of phase interpolator for clock and data recovery.

Chapter 5

Future Work

5.1 LDO Powered PI

An LDO [5] stands for low dropout voltage regulator, can provide a stable and precise voltage reference for a phase interpolator circuit. It also consists of delay elements like resistors, capacitances in its feedback path, which is responsible in tuning the phase of output signal in fine increments or steps.

The need for an LDO-powered PI arises when the power supply voltage available for the PI is low and the required output voltage needs to be stable over a wide range of operating conditions. In such scenarios, traditional PI circuits may not be able to maintain the required output voltage stability and accuracy.

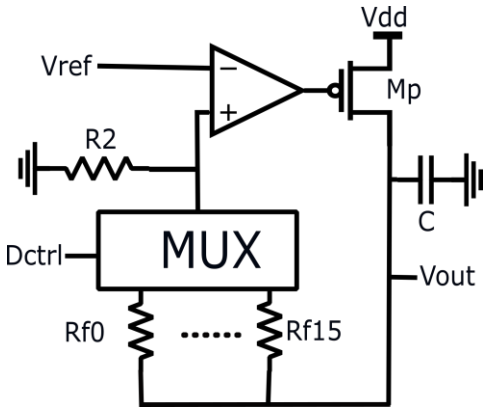


Figure 5.1: Schematic of a LDO

The LDO circuit in the LDO-powered PI typically consists of a voltage reference, a feedback amplifier, and a pass element such as a MOSFET or BJT transistor as shown in 5.1 and taken from [5]. This reference is used to create a precise reference which can be compared to

the voltage of output by the amplifier feedback. The pass element regulates its impedance to main- tain the output voltage at the desired level, based on the error signal generated by the feedbackamplifier. The lines in LDO that are responsible for delay, includes cascaded delay elements that introducea fixed delay between adjacent stages. The delay between adjacent stages determines the reso-lution of the phase interpolation.

5.2 PI based CDR

A phase interpolator-based Clock Data Recovery [10] is a circuit which can be utilized to retrieve the clock waveform, from incoming signals by interpolating between the phases of a reference signal.The CDR compares, incoming signal with the reference clock signal and produces a fault or error signal which can be used in tuning the output's phase.

The output signals of clock are produced by delaying the reference clock signal by fraction of its period using a delay line. This line typically consists of a cascaded delay elements, such as delay cells or inverters, that introduce a fixed delay between adjacent stages. The delay between adjacent stages determines the granularity of the phase interpolation. The fully proposed CDR architecture is shown in 5.2.

The phase interpolator selects two adjacent clock signals with the closest phases to the incoming data signal and generates an interpolated clock with a phase difference between two clock signals. The phase interpolator is implemented using a linear or nonlinear function that maps the incoming data signal to the interpolated phase. The nonlinear function can be implemented using a lookup table or a polynomial approximation.

The output clock signal from the phase interpolator is fed back to the CDR and associated to the incoming data. The error signal which is produced by a phase detector is directly proportional to the difference in phase of the input incoming signal and output signal. This signal can be filtered using a lowpass filter which removes the noise and jitter caused due to high frequency signals.

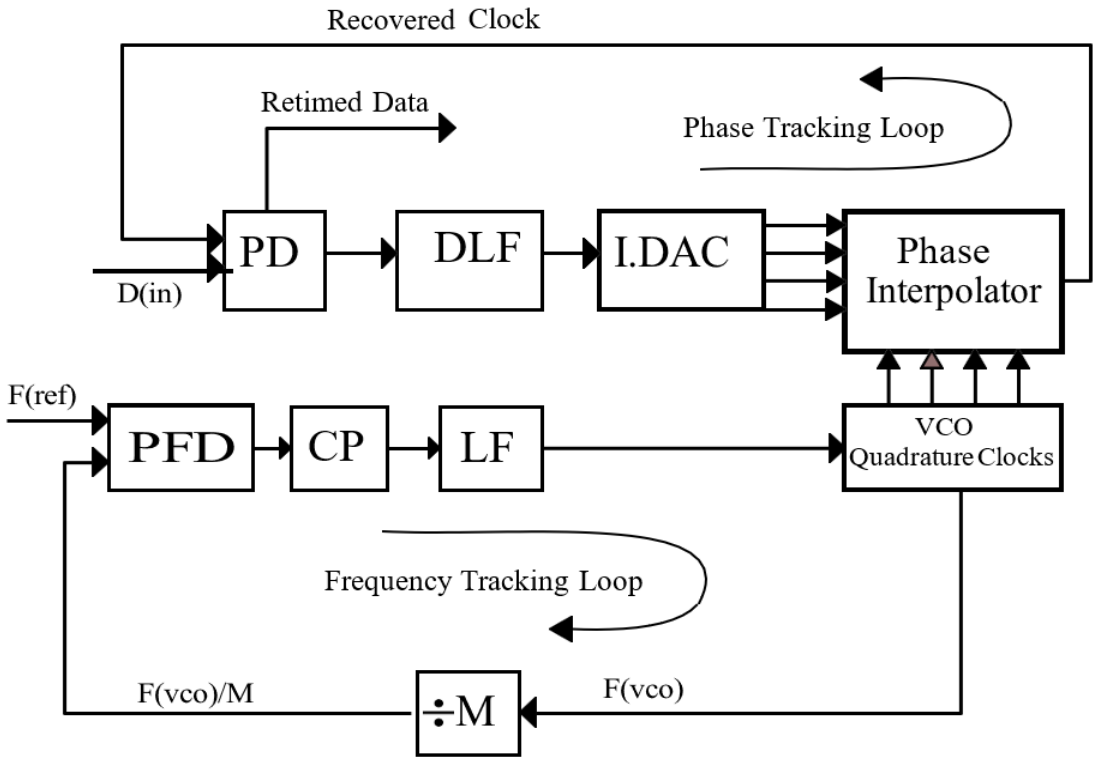


Figure 5.2: PI based CDR architecture (from [11])

The phase interpolator-based CDR can recover the clock signal from a huge variety of data rates and frequencies without requiring a high-quality reference clock signal. It also provides a higher resolution for phase interpolation, which improves the accuracy of the recovered clock signal. However, it requiresa more complex circuit design and consumes more power than traditional CDR circuits

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