ECTION NAME			G RULE TEXT		RULE FULL TEXT
ADL Specification  ADL Specification	_	0	0 Identifiers in specification namespace must be unique.	Checked when processing package and property set nodesBUT: predeclared pack	(N1) An AADL specification has one global namespace. The package and property set identifiers reside in (N2) These package and property set identifiers qualify the names of individual elements contained in the
OL Specification		0			(N3) Package declarations represent labeled namespaces for component type, component implementation
L Specification		0			(N4) Property set declarations represent labeled namespaces for component type, component implementation.
OL Specification		0			(N5) Packages and property sets may be separately stored. Those packages and property sets are consi
DL Specification			0	Provided by parser	(N6) Defining identifiers in AADL must not be one of the reserved words of the language (see Section 15.
DL Specification		0		Provided by parser  Provided by realization of AADLIdentifer class	(N7) The AADL identifiers and reserved words can be in upper or lower case (or a mixture of the two) (se
DL Specification		0	<u> </u>		
ADE Specification	p4 IIIo	U	U CONTRACTOR OF THE CONTRACTOR		(N8) The AADL does not require that an identifier be declared before it is referenced.
kages	p42n1	0	A defining package name must be unique in the global namespace.	Checked by counting private and public package declarations	(N1) A defining package name consists of a sequence of one or more package identifiers separated by a
ckages	p42n2	0		3 5 1 1 5	(N2) The public and private section of a package may be declared in separate package declarations; thes
ckages	p42n3	0			(N3) Associated with every package is a package may be declared in separate package declarations, ties
ckages	p42n4	0			(N4) The package namespace is divided into a public section and a private section. Items declared in the
	p42n4			Can be checked after all possible references are known	
ckages		0			(N5) The reference to an item declared in another package must be an item name qualified with a packag
ckages	p42n6 p42n7	0	O The applications is a installed declaration and evidence that the detail accesses	Can be checked after all possible references are known	(N6). The reference to a property other than predeclared properties must be an property name qualified w
ckages		U	0 The package name in a import_declaration must exist in the global namespace.	Checked when processing package imports	(N7) The package name in a import_declaration must exist in the global name space.
ickages	p42n8	U		Checked when processing package imports	(N8) The property set identifier in a import_declaration must exist in the global name space.
ckages	p42n9	0		Can be checked after all possible references are known	(N9) Items declared in the private section of the package can only be referenced from within the private s
ckages	p42n10	0		0	(N10) If the qualifying package identifier of a qualified reference is missing, the referenced component class
ckages	p42n11global		The package name referenced in an alias_declaration must exist in the global namespace.		(N11) The package name referenced in an alias_declaration must exist in the global namespace and mus
ckages	p42n11import		The package name referenced in an alias_declaration must be listed in the import_declaration.	Checked when processing package aliases	(N11) The package name referenced in an alias_declaration must exist in the global namespace and mus
ckages	p42n12		0 Classifier referenced is not found in public package section.	Checked when processing classifier aliases	(N12) The classifier referenced by the alias_declaration must exist in the name space of the public section
ckages	p42n12other		0 Wrong reference structure, no package is referenced	Checked when processing classifier aliases	(N12) The classifier referenced by the alias_declaration must exist in the name space of the public section
ckages	p42n13	0	0	Provided by parser	(N13) The classifier referenced by the alias declaration must refer to a component type or a feature group
ckages	p42n14package	e 0	0 Conflict of alias name of the package with imported package.	Checked when processing package and classifier aliases	(N14) The defining identifier of an alias_declaration must be unique in the namespace of the package con
ckages	p42n14defining	0	0 Conflict of alias name of the package with package name where it is defined.	Checked when processing package and classifier aliases	(N14) The defining identifier of an alias_declaration must be unique in the namespace of the package con
ckages	p42n14other	0	0 The defining identifier of an alias_declaration is not unique in package namespace.	Checked when processing package and classifier aliases	(N14) The defining identifier of an alias_declaration must be unique in the namespace of the package con
ckages	p42n15		0 The defining identifier of an alias_declaration is not unique in package namespace. (identifier not specified)	Checked when processing classifier aliases	(N15) The alias_declaration makes the publicly visible identifier of classifiers declared in another package
ckages	p42n16		0 The defining identifier of an alias_declaration is not unique in package namespace. ("all" alias declaration)	Checked when processing all aliases by intersection of two namespaces	(N16) If the alias declaration renames all publicly visible identifiers of component types and feature group
ckages	p42n17	0	0		(N17) The identifiers introduced by the alias declaration are only accessible within the package. When de
ckages		0	0		(N18) The alias declared for a component type can be used instead of a qualified component type in a reference.
ckages	p42l1	0		Provided by parser	(L1) The defining package name following the reserved word end must be identical to the defining package
ickages	p42l2	0			(L2) For each package there may be at most one public section declaration and one private section decla
ckages	p42l3		0 Public part of component implementation can contain only properties and modes if it is declared in both public and		(L3) A component implementation may be declared in both the public and private part of a package. In the
ckages	p42l4		The component category does not match the category of referenced component type.	Checked when processing component implementations  Checked when processing classifier aliases	(L4) The component category in an alias declaration must match the category of the referenced compone
			2 miles and subject of the materials and subject of telefolious component type.	The state of the s	tery and compositing category in an alias declaration must match the category of the releitenced compone
mponent Type:	0.04204	0	0 The defining identifier for a component type is not unique in the namespace of the package.	Charled when greating level namespaces of the packages BLIT: autrently no phosp	(N1) The defining identifier for a component type must be unique in the namespace of the package within
mponent Type:					
			0 Identifier is not unique in component type local namespace.		(N2) Each component type has a local namespace for defining identifiers of prototypes, features, modes,
mponent Type:			Ancestor in a component type extension must exist.	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	(N3) The component type identifier of the ancestor in a component type extension, i.e., that appears after
mponent Type:			0 Identifier is not unique in component type namespace because of it's ancestors.	Checked by recursive creating ancestors namespace when processing component	
mponent Type:		0			(N5) A component type that extends another component type does not include the identifiers of the imple
mponent Type		0		Same as p43n2?	(N6) The defining identifier of a feature, flow specification, mode, mode transition, or prototype must be ur
mponent Type:		0	0	0	(N7) The refinement identifier of a feature, flow specification, or prototype refinement refers to the closest
mponent Type:		0		0	(N8) The prototypes referenced by prototype binding declarations must exist in the local namespace of the
mponent Type:	s p43n9	0			(N9) Mode transitions declared in the component type may not refer to event or event data ports of subco
mponent Type:	s p43l1	0	0	Provided by parser	(L1) The defining identifier following the reserved word end must be identical to the defining identifier that
mponent Type:	s p43l2	0	0	Provided by parser(kinda, error is - "No viable alternative")	(L2) The prototypes, features, flows, modes, and properties subclauses are optional. If a subclause is pre
mponent Type:	s p43l3	0	0 The category of the component type being extended must match the category of the extending component type.	Checked when processing component type declarations	(L3) The category of the component type being extended must match the category of the extending comp
mponent Type:	s p43l4	0	0	0	(L4) The classifier being extended in a component type extension may include prototype bindings. There
mponent Type:	s p43l5	0	0	Provided by parser(kinda, error is - extraneous input 'requires' expecting {'ANNEX'	
nponent Type:		0	0 Component type and it's ancestor should have both modes or requires modes subclauses.		(L6) If the extended component type and an ancestor component type in the extends hierarchy contain mo
mponent Type:		0			The defining identifier for a component type cannot contain '.'
, , , , , ,					
nponent Imple	er p44n1	n	Component type of component implementation is not declared.	1 - Provided by parser(kinda, error is - mismatched input 'end' expecting ' ') 2 - che	(N1) A component implementation name consists of a component type identifier and a component implem
mponent Imple			The defining identifier for a component implementation is not unique in the local namespace of the component type		
mponent Imple			0 Identifier is not unique in component implementation local namespace.		(N3) Every component implementation defines a local namespace for all defining identifiers of prototypes.
mponent Imple		0	Component implementation contains identifier which intersects with component type local namespace.	Checked by intersection of local namespaces of type and impl.Problem: error mark	
mponent Imple		0		0	(N5) Refinement identifiers of features must exist in the namespace of the associated component type or
omponent Imple	err p44n6	0	0	0	(N6) In a component implementation extension, the component type identifier of the component implementation
					(N7). When a component implementation extends another component implementation, the local namespa

mponent Impler p44n8	0	0	0	(N8) Within the scope of the component implementation, subcomponent declarations, connections, subpr	
mponent Implen p44I1	0	0	0	(L1) The pair of identifiers separated by a dot (вЪњ.вЪк) following the reserved word end must be identified.	
mponent Impler p44l2	0		0	(L2) The prototypes, subcomponents, connections, calls, flows, modes, and properties subclauses are op	
mponent Implen p44l3			Checked when processing classifier implementations	(L3) The category of the component implementation must be identical to the category of the component to	1
nponent Implen p44l4		0 The category of the component implementation being extended must match the category of the extending component		(L4) If the component implementation extends another component implementation, the category of both n	í .
ponent Implen p44l5	0	0	0	(L5) The classifier being extended in a component implementation extension may include prototype binding	(
ponent Impler p44l6	0	0 Component implementation must not contain mode subclause because component type contains requires modes s	Checked when processing classifier implementations, BUT: not watching at ancest	(L6) If the component type of the component implementation contains a requires_modes_subclause then	
ponent Impler p44I7	0	0 If modes are declared in the component type, then modes cannot be declared in component implementations.	Checked when processing classifier implementations, BUT: not watching at ancest	(L7) If modes are declared in the component type, then modes cannot be declared in component impleme	i -
ponent Implen p44l8	0		0	(L8) If modes or mode transitions are declared in the component type, then mode transitions can be adde	1
ponent Impler p44I9	0	0	0	(L9) The category of a subcomponent being refined must match the category of the refining subcompone	i .
ponent Impler p44I10	0	0	0	(L10) For all other refinement declarations the categories must match (see the respective sections).	i -
ponent Impler p44I11	0	0	0	(L11) Component implementations and component implementation extensions must not refine prototypes	i
omponents p45n1	0		0	(N1) The defining identifier of a subcomponent declaration placed in a component implementation must b	i .
omponents p45n2	0	0	0	(N2) The defining identifier of a subcomponent refinement must exist as a defining subcomponent identifier	i .
omponents p45n3	0	0	0	(N3) The component type identifier or the component implementation name of a component classifier refe	
omponents p45n4	0	0	0	(N4) The prototype identifier of a prototype reference must exist in the local name space of the componer	1
omponents p45n5	0	0	0	(N5) The prototype referenced by the prototype binding declarations must exist in the local namespace of	
omponents p45n6	0	0	0	(N6) The modes named in the in modes statement of a subcomponent must refer to modes in the compo	1
omponents p45l1	0	0	0	(L1) The category of the subcomponent declaration must match the category of its corresponding component	1
omponents p45l2	0	0	0	(L2) The component classifier reference of a subcomponent declaration may include prototype bindings for	1
omponents p45l3	0	0	0	(L3) In a subcomponent refinement declaration the component category may be refined from abstract to c	
omponents p45l4	0	0	0	(L4) The Classifier_Substitution_Rule property specifies the rule to be applied when a refinement supplier	1
mponents p45l5	0		0	(L5) In the case of a signature match, the component type of the subcomponent being refined must have	i i
omponents p45l6	0	0	0	(L6) The component category and optional component classifier or prototype reference can be followed b	i .
mponents p45l7	0		0	(L7) The array size specification for the dimensions is optional. In this case the array declaration is consid	i i
mponents p45l8	0	0	0	(L8) When refining a subcomponent array the number of dimensions of the array cannot be changed, but	ı .
omponents p45l9	0	0	0	(L9) When the subcomponent is declared as an array with array dimension sizes then a list of component	ı
omponents p45l10	0	0	0	(L10) Selecting index ranges in one or more dimensions of an array is only possible if the size of the array	i
omponents p45l11	0	0	0	(L11) An array element implementation list is valid only if (a) the subcomponent classifier is a component t	i
omponents p45c1	0	0	0	(C1) The classifier of a subcomponent cannot recursively contain subcomponents with the same compone	ı
ract Componei p46l1	0	0	0	(L1) An abstract component type declaration can contain feature declarations (including abstract feature (	i .
act Componei p46l2	0	0	0	(L2) An abstract component implementation can contain subcomponent declarations of any category. Cer	i .
act Componer p46l3	0		0	(L3) An abstract component implementation can contain a modes subclause, a connections subclause, a	i i
act Componei p46l4	0	0	0	(L4) An abstract subcomponent can be contained in the implementation of any component category.	i i
act Componei p46l5	0	0	0	(L5) If an abstract subcomponent is refined to a concrete category, the concrete category must be accept	i i
act Componei p46l6	0		0	(L6) An abstract subcomponent can be declared as an array of subcomponents.	i i
act Componei p46l7	0		0	(L7) If an abstract component type is refined to a concrete category, the features, modes, and flow specifi	i .
act Componei p46l8	0		0	(L8) If an abstract component implementation is refined to a concrete category, the subcomponents, call :	i .
types p47n1	0	0	0	(N1) The prototype identifier on the left-hand side of a prototype binding must exist in the local namespace	1
types p47n2	0	0	0	(N2) The prototype identifier on the right-hand side of a prototype binding, if present, must exist in the loc	1
ypes p47n3	0	0	0	(N3) Unique component classifier references must exist in the public section of the package being identifi	1
ypes p47n4	0	0	0	(N4) Unique feature group type references must exist in the public section of the package being identified	1
ypes p47l1	0	0	0	(L1) The component category declared in the component prototype binding must match the component c	1
ypes p47l2	0		0	(L2) The component category of the optional component classifier reference in the prototype declaration	
ypes p47l3	0		0	(L3) If the component prototype only specifies a component category, then any component type and com	1
ypes p47l4	0		0	(L4) If the component prototype declaration includes a component classifier reference, then the classifier	
/pes p47l5	0		0	(L5) The category of the component implementation that contains the prototype declaration places restric	
vpes p47l6	0		0	(L6) If the direction is declared for feature prototypes, then the prototype actual satisfies the direction acc	
/pes p47I7	0	0	0	(L7) In the case of feature group prototypes, the supplied feature group types must match the declared fe	
vpes p47l8	0	0	0	(L8) A classifier supplied in a feature prototype binding must match the classifier of the prototype declarat	1
ypes p47l9	0		0	(L9) Component prototypes declared with square brackets specify that they expect a list of component cla	1
ypes p47l10	0	0	0	(L10) The component category of the classifier reference or prototype reference in a prototype binding dec	
types p47l11	0	0	0	(L11) If a direction is specified for an abstract feature in a prototype declaration, then the direction of the p	1
types p47l12	0	0	0	(L12) Component prototype bindings must only bind component prototypes, feature group prototype binding	
types p47l13	0	0	0	(L13) Component prototype refinements must only refine component prototypes, feature group prototype i	
Subclauses p48n1	0		0	(N1) The annex identifier must be the name of an approved annex or a project-specific identifier different	1

Company   Comp			
Test Services (Control of Control	Annex Subclauses p48n2		0 (N2) The mode identifiers in the in_modes statement must refer to modes in the component type or comp
Test Services (Control of Control	Annex Subclauses p48l1	0 0	(I.1) Appex subclauses can only be declared in component types component implementations, and feature
Process   Proc			
Process   Proc			
Company of the Comp	Annex Subclauses p48l3		0 (L3) Annex libraries must be declared in packages.
Company of the Comp	Annex Subclauses p48l4		(L4) A package declaration may contain at most one annex library declaration for each annex.
Section   Sect			
Dec.   10   10   10   10   10   10   10   1			
See   ASS   2   5   6   6   7   7   7   7   7   7   7   7	Data p51l1		0 (L1) A data type declaration can contain provides subprogram access declarations as well as property as
Mary   1	Data p51 2	0 0	(L2) A data type declaration must not contain a flow specification or modes subclause
Property of the Company of the Com			
Experiment of 1922 of			U (L3) A data implementation can contain abstract, data and subprogram subcomponents, access connecting
According to an infinite of the company of the co	Data p51l4		0 (L4) A data implementation must not contain a flow implementation, an end-to-end flow specification, or a
Description of ICCS   Comment   Co			
Description of ICCS   Comment   Co	Cubarages and (append		
Experiment of 1504 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			U (N1) The defining identifier of a subprogram call sequence declaration must be unique within the local nation
Subsequence and 1,554	Subprograms and (p52n2		0 (N2) The defining identifier of a subprogram call declaration must be unique within the local namespace of
Adequage and Infall 6	Subprograms and (n52n3		(N3) If the called subprogram name is a subprogram classifier reference, its component type identifier or i
Resignant met (phb)  Lagranger and (phb)  Lagranger			
Address and Life Market and Address and Ad	Subprograms and 1 p52n4		U (N4) The subprogram classifier reference of a subprogram call may be a subprogram type reference.
Addressment of pAST   0   0   0   0   0   0   0   0   0	Subprograms and (p52n5		(N5) If the called subprogram name is a subprogram subcomponent reference, the subprogram subcomp
Degrey part of [521]  Degrey part of [522]  Degrey part of [523]	Subprograms and (n52n6		(NE) If the collect outbrookers come is a required experience the required subspaces of
Regregation and [453] 0 C C C C C C C C C C C C C C C C C C			
Appropries of \$25.0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			(L1) A subprogram type declaration can contain parameter, out event port, out event data port, and feature
Applying man of \$253   0   0   0   0   0   0   0   0   0	Subprograms and (p52l2	0 0	0 (L2) A subprogram implementation can contain abstract, subprogram, and data subcomponents, a subprogram
Editoring minor (1985) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		0 0	
Educación Cox. (Section 1997)  Color (Sectio			
Expregnent Conce p\$20-1			(C1) The reference to a provides subprogram access of a processor in a subprogram call (processor, pro
Designation Concept 2011   0   0   0   0   0   0   0   0   0	Subprograms and (p52c2	0 0	0 (C2) A subprogram call may reference a subprogram classifier. A project may enforce a consistency rule of
Depression Company Charge (Charge Schold)  O			
Adjungment Come p Ch2-C  Adjungment Come p Ch2			
Subgroupes Courty (2-1-4)  Appropriate Courty (2-1-4)  App	Subprogram Group p53n1		(N1) The defining identifier of a subprogram group type must be unique within the package namespace of
Subgroupes Courty (2-1-4)  Appropriate Courty (2-1-4)  App	Subprogram Group p53n2	0 0	(N2) Each subprogram group provides a local namespace. The defining subprogram identifiers of subprogram
Degregate Orace p 53x4			
Subgrouped Group (20-16)  Debugging of Class (20-16)  Debu			U (N3) The local namespace of a subprogram group type extension includes the defining identifiers in the id
Dubylooging Group (531 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Subprogram Group p53n4		0 (N4) The defining subprogram identifiers of subprogram access feature declarations in feature group refin
Dubylooging Group (531 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Subprogram Group p53n5	0 0	(NS). The package name of the unique subprogram group type reference must refer to a package name in
Distriction Cross p503 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			
December (1924) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			U (L1) A subprogram group type can contain provides and requires subprogram access, and provides and r
Procedit   Policy	Subprogram Group p53l2		0 (L2) A subprogram group implementation can contain abstract, data, subprogram group, and subprogram
Proceding   Policy	Subprogram Group p53l3	0 0	(I 3) A subcrogram group type or implementation may contain zero or more subcomponent declarations.
Preside (PASE) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			( <del></del>
Preside (PASE) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			
Preads pALO 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			
Preads pALO 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Threads p54l1	0 0	0 (L1) A thread type declaration can contain port, feature group, requires data access declarations, as well
Pread   PAC   PA			
Company   Comp	Threads p54l2	0 0	0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group
Thread Groups p551 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads p54l2 Threads p54l3	0 0 0 0 0 0	0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group
Thread Groups p552 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads p54l2 Threads p54l3	0 0 0 0 0 0	0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identify
Thread Groups p592 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads         p54l2           Threads         p54l3           Threads         p54c3		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ
Thread Groups p551 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads         p54l2           Threads         p54l3           Threads         p54c3		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ
Thread Groups p552 0 0 0 0 0 0 0.1.3 A tread group component implementation can cortain abstract, data, subprogram spring p553 0 0 0 0 0 0.1.3 A tread group picture final contains a control and subdiscute, in models in Thread Groups p553 0 0 0 0 0 0 0.1.4 A tread group contains a contains a subdiscute in flower group provides and requires data accesses. Processes p564 0 0 0 0 0.1.4 A processor component type can contain port, flower group provides and requires data accesses, part processes p564 0 0 0 0 0.1.4 A processor component type can contain port, flower group provides and requires data accesses, part p565 0 0 0 0 0.1.4 A processor component type can contain port, flower group provides and requires data accesses part p565 0 0 0 0 0 0.1.4 A processor p565 0 0 0 0 0 0.1.4 A processor component type can contain port, flower group provides and requires data accesses part p565 0 0 0 0 0 0 0.1.4 A processor component type can contain port, flower group provides actively processor p565 0 0 0 0 0 0 0 0 0 0 0 0.1.4 A processor component type can contain port, flower group provides and legal processor p565 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads         p54l2           Threads         p54l3           Threads         p54c3		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ
Thread Groups   5513   0   0   0   0   0   0   0   0   0	Threads p54l2 Threads p54l3 Threads p54c3 Threads p54c4		0 (L2) A thread component implementation can contain abstract, date, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic.
Processes p661 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic, 0 (L1) A thread group component type can contain provides and requires data access, as well as port, feat
Processes p5611 0 0 0 (1.1) A process component type can cortain port, feature group, provider and requires data access, power processes p5613 0 0 0 (1.2) A process component implementation can cortain a content subclause, a modes subclause p5613 0 0 0 (1.3) A process implementation can cortain a content subclause, a modes subclause p7605-sesses p5614 0 0 0 (1.4) A process implementation can cortain a content subclause, a modes subclause p7605-sesses p5614 0 0 0 (1.4) A processor p6615 0 0 0 (1.5) The complete source text associated with a process component must form a complete and legal properties p5605	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1           Thread Groups         p55l2		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text.Compute_Entrypoint_Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic. 0 (L1) A thread group component type can contain provides and requires data access, as well as port, feating 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group.
Processes p5611 0 0 0 (1.1) A process component type can contain port, feature group, provider and requires data access, power processes p5613 0 0 0 (1.2) A process component implementation can contain a content subclause, a modes subclause processes p5613 0 0 0 (1.3) A process implementation can contain a content subclause, a modes subclause processes p5614 0 0 0 (1.4) A thread group must not dorstain a subclause, a modes subclause processes p5614 0 0 0 (1.5) The complete source text associated with a process component must form a complete and legal properties p5614 processors p5611 0 0 0 (1.5) A processor promoter type can contain port, feature group, provides authorized and legal properties p5614 processors p5611 0 0 0 (1.5) A processor promoter type can contain port feature group provides subprogram access, provides p5611 0 0 0 (1.5) A processor promoter type can contain port feature group provides subprogram access, provides p5611 0 0 0 (1.5) A processor p5612 0 0 0 (1.5) A virtual p56000000000000000000000000000000000000	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1           Thread Groups         p55l2		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text.Compute_Entrypoint_Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic. 0 (L1) A thread group component type can contain provides and requires data access, as well as port, feating 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group.
Processes p6612 0 0 0 (L2) A process component implementation can contain abstract, data, subprogram, subprogram group, the Processes p6643 0 0 0 (L3) A process implementation can contain a comment on contain a comment of subclause, a modes subclause. Processes p6644 0 0 0 (L4) A trivial processor component must form a complete and logal program processor p6645 0 0 0 (L4) A trivial processor component must form a complete and logal program processor p6645 0 0 0 (L5) A processor component must form a complete and logal program processor p6645 0 0 0 (L5) A processor component must form a complete and logal program processor p6645 0 0 0 (L5) A processor component implementation can contain declarations of memory, but, virtual but, virtual processors p6445 0 0 0 (L5) A processor component implementation can contain declarations of memory, but, virtual but, virtual processors p6445 0 0 0 (L5) A processor implementation can contain a modes subclause, and a properties such processors p6445 0 0 0 (L5) A processor implementation can contain a modes subclause, and a properties such processors p6445 0 0 0 (L5) A processor implementation can contain a modes subclause. Processors p6455 0 0 0 (L5) A virtual processor component must not contain a subclause.  Virtual Processors p6455 0 0 0 (L5) A virtual processor component myber can contain port, feature group, provides utgroup an access, as a propertie virtual processor p6455 0 0 0 (L5) A virtual processor implementation can contain declarations of virtual but, virtual processors p6455 0 0 0 (L5) A virtual processor implementation can contain a subgroup an access, port virtual processor p6455 0 0 0 (L5) A virtual processor implementation can contain a subgroup and cases, subgroup and cases, port virtual processor p6455 0 0 0 (L5) A virtual processor implementation can contain a subgroup and cases, port virtual processor p6455 0 0 0 (L5) A virtual processor implementation can contain a subgroup and cases, port virtual processor p6455 0 0 0 (L5) A virtual processor implementat	Threads         p5412           Threads         p5413           Threads         p54c3           Threads         p54c4           Thread Groups         p5511           Thread Groups         p5512           Thread Groups         p5513		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint, Source_Text Compute_Entrypoint, Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic.  (L1) A thread group component type can contain provides and requires data access, as well as port, feati 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group 0 (L3) A thread group implementation can contain a connections subclause, a modes su
Frocesses p5612 0 0 0 (L2) A process component implementation can contain abstract, data, subprogram, subprogram group, the Processes p5613 0 0 0 (L3) A process implementation can contain an content and content	Threads         p5412           Threads         p5413           Threads         p54c3           Threads         p54c4           Thread Groups         p5511           Thread Groups         p5512           Thread Groups         p5513		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint, Source_Text Compute_Entrypoint, Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic.  (L1) A thread group component type can contain provides and requires data access, as well as port, feati 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group 0 (L3) A thread group implementation can contain a connections subclause, a modes su
Processes p563 0 0 0 (L3) A process implementation can contain a connections subclause, a flows subclause, a flows subclause, a flows subclause, a flow subclause, a flow subclause, a flow subclause, processes p564 0 0 0 (L4) A trained group must not contain a subgroup an acids subclause.  Processes p561 0 0 0 (C1) The complete source text associated with a process component must form a complete and legal propriate processors p611 0 0 0 (L1) A processor component implementation can contain port, feature group, provides subgroup an access, provides processors p612 0 0 0 (L2) A processor implementation can contain an anotes subclause, flows subcla	Threads         p5412           Threads         p6413           Threads         p54c3           Threads         p64c4           Thread Groups         p5511           Thread Groups         p5512           Thread Groups         p5513           Thread Groups         p5514		0 (L2) A thread group component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event to port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic, 0 (L1) A thread group component type can contain provides and requires data access, as well as port, feats 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram gro 0 (L3) A thread group implementation can contain a connections subclause, a modes s. 0 (L4) A thread group must not contain a subprogram calls subclause.
Processes p6i3 0 0 0 (L5) A process implementation can contain a connections subclause, a flows subclause, a flows subclause, a flows subclause.  Processes p6i4 0 0 0 (L1) A thread group must not contain a subprogram access and subclause.  Processes p6i5 0 0 0 (C1) The complete source text associated with a processor possible and logal program access, provides and program access, provides and program access, provides processors p6i1 0 0 0 (L1) A processor component implementation can contain port, feature group, provides subprogram access, provides processors p6i1 0 0 0 (L2) A processor implementation can contain an anotes subclause, flows subclause.  Processors p6i1 0 0 0 (L1) A processor implementation can contain but access, subprogram acces	Threads         p5412           Threads         p6413           Threads         p54c3           Threads         p64c4           Thread Groups         p5511           Thread Groups         p5512           Thread Groups         p5513           Thread Groups         p5514		0 (L2) A thread group component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event to port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic, 0 (L1) A thread group component type can contain provides and requires data access, as well as port, feats 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram gro 0 (L3) A thread group implementation can contain a connections subclause, a modes s. 0 (L4) A thread group must not contain a subprogram calls subclause.
Processes p5614 0 0 0 (4.) A thread group must not contain a subprogram cats subclause.  Processes p5611 0 0 0 (1.1) he complete source text associated with a process component must form a complete and legal processors p5112 0 0 (1.1) A processor component type can contain port, feature group, provides subprogram access, provides processors p5112 0 0 (1.2) A processor component type can contain a declarations of memory, bus, virtual processors p5112 0 0 (1.2) A processor component type can contain a modes subclosus, substance, while processors p5114 0 0 (1.3) A processor implementation can contain a modes subclosus, substance, and provides subprogram access, substance, subs	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic, 0 (L1) A thread group component type can contain provides and requires data access, as well as port, feat 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram gro 0 (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes as 0 (L4) A thread group must not contain a subprogram calls subclause
Processors p611 0 0 0 (C1) The complete source text associated with a process component must form a complete and legal processors p611 0 0 0 (L1) A processor component type can contain port, feature group, provides subprogram access, provide processors p612 0 0 (L2) A processor implementation can contain declarations of memory, bus, virtual processors p613 0 0 (L3) A processor implementation can contain a modes subclause, and a properties subclasses p614 0 0 (L3) A processor implementation can contain a modes subclause, and a properties subclasses p614 0 0 (L4) A processor implementation can contain bus access, subprogram group access p7 p615 0 0 (L5) A processor implementation must not contain a subprogram cacess, subclause.  Virtual Processors p621 0 0 (L1) A virtual processor component type can contain port, feature group, provides subclause.  Virtual Processors p622 0 0 (L2) A virtual processor component implementation can contain subprogram access, subviving processor virtual Processors p623 0 0 0 (L2) A virtual processor implementation can contain subclause, and a properties virtual Processors p624 0 0 (L3) A virtual processor implementation must not contain a subprogram group access, portification processor implementation must not contain a subprogram group access, portification processor implementation must not contain a subprogram group access, portification processor implementation can contain subprogram	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1           Processes         p56l2		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text.Compute_Entrypoint_Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic.  0 (L1) A thread group component type can contain provides and requires data access, as well as port, feats 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group 0 (L3) A thread group implementation can contain a connections subclause, a modes second (L4) A thread group must not contain a subprogram calls subclause.  0 (L1) A process component type can contain port, feature group, provides and requires data access, provides of the process component implementation can contain abstract, data, subprogram, subprogram group, the process component implementation can contain abstract, data, subprogram, subprogram group, the
Processors p6112 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads p5412 Threads p543 Threads p5463 Threads p5464 Thread Groups p5511 Thread Groups p5512 Thread Groups p5513 Thread Groups p5514 Processes p5611 Processes p5612 Processes p5612 Processes p5613		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text.Compute_Entrypoint_Call_Sequ 0 (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic.  0 (L1) A thread group component type can contain provides and requires data access, as well as port, feats 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group 0 (L3) A thread group implementation can contain a connections subclause, a modes second (L4) A thread group must not contain a subprogram calls subclause.  0 (L1) A process component type can contain port, feature group, provides and requires data access, provides of the process component implementation can contain abstract, data, subprogram, subprogram group, the process component implementation can contain abstract, data, subprogram, subprogram group, the
Processors p6112 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads p5412 Threads p543 Threads p5463 Threads p5464 Thread Groups p5511 Thread Groups p5512 Thread Groups p5513 Thread Groups p5514 Processes p5611 Processes p5612 Processes p5612 Processes p5613		0 (L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group 0 (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif 0 (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text.Compute_Entrypoint_Call_Sequ 0 (C4) The Period properly must have a value if the Dispatch_Protocol property value is periodic, sporadic 0 (L1) A thread group component type can contain provides and requires data access, as well as port, feats 0 (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group 0 (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes stated to the contain a connection of the contain a con
Processors p6112 0 0 0 (L1) A processor component type can contain port, feature group, provides subprogram access, provides processors p6112 0 0 0 (L2) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual processors p6113 0 0 (L3) A processor implementation can contain an bus access, subprogram access, subprogram access, provides subcompanies and processors p6114 0 0 0 (L3) A processor implementation can contain an bus access, subprogram access, subprogram access, p6115 0 0 0 (L5) A processor implementation must not contain an bus access, subprogram access, subprogram access, p6115 0 0 (L5) A processor implementation must not contain an bus access, subprogram access, accessors p6115 0 0 0 (L5) A processor implementation must not contain access, subprogram access, accessors p6115 0 0 0 (L5) A virtual processor implementation must not contain access, accessors access, accessors p6115 0 0 0 (L5) A virtual processor implementation can contain declarations of which subprogram access, accessors p6115 0 0 0 (L5) A virtual processor implementation must not contain access, subprogram access, accessors p6115 0 0 0 (L5) A virtual processor implementation can contain access, accessors accessors p612 0 0 (L5) A virtual processor implementation must not contain an authorized access, accessors p612 0 0 (L5) A virtual processor implementation must not contain a subprogram access, access, accessors p612 0 0 (L5) A virtual processor implementation can contain access, access, access, accessors p612 0 0 (L5) A virtual processor implementation can contain access, access	Threads         p54I2           Threads         p64I3           Threads         p54c3           Threads         p54c4           Thread Groups         p55I1           Thread Groups         p55I2           Thread Groups         p55I3           Thread Groups         p55I4           Processes         p56I2           Processes         p56I3           Processes         p56I3           Processes         p56I4		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclared, i.e. are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ (C4) The Penod property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (L1) A thread group component type can contain provides and requires data access, as well as port, feath (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes as (L4) A thread group must not contain a subprogram calls subclause. (L1) A process component type can contain a connection and requires data access, provided to the contain a connection and call of the contain a connection and call of the contain and contain and contain and call of the contain and contain a
Processors p612 0 0 0 (L2) A processor component implementation can contain dectarations of memory, bus, virtual bus, virtual processors p613 0 0 (L3) A processor implementation can contain a must access, subgrogram access, subgrogram group access processors p614 0 0 (L4) A processor implementation can contain a must access, subgrogram group access processors p615 0 0 (L5) A virtual processor component type can contain port, feature group, provides subgrogram access, access	Threads         p54I2           Threads         p64I3           Threads         p54c3           Threads         p54c4           Thread Groups         p55I1           Thread Groups         p55I2           Thread Groups         p55I3           Thread Groups         p55I4           Processes         p56I2           Processes         p56I3           Processes         p56I3           Processes         p56I4		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclared, i.e. are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ (C4) The Penod property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (L1) A thread group component type can contain provides and requires data access, as well as port, feath (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes as (L4) A thread group must not contain a subprogram calls subclause. (L1) A process component type can contain a connection and requires data access, provided to the contain a connection and call of the contain a connection and call of the contain and contain and contain and call of the contain and contain a
Processors p5112 0 0 0 (L2) A processor component implementation can contain dectarations of memory, bus, virtual bus, virtual Processors p5113 0 0 (L3) A processor implementation can contain a must access, subgroup as subclause, and properties subclause. Processors p5114 0 0 (L4) A processor implementation can contain a must access, subgroup and group access p5115 0 0 (L5) A processor implementation can contain port, feature group, provides subgroup access p5115 0 0 0 (L5) A virtual processor component type can contain port, feature group, provides subgroup access, at Virtual Processors p5212 0 0 (L2) A virtual processor component implementation can contain access, and subgroup access p5213 0 0 (L2) A virtual processor implementation can contain access and subgroup access p5214 0 0 (L3) A virtual processor implementation can contain access and a properties virtual Processors p5214 0 0 (L3) A virtual processor implementation can contain access, and a properties virtual Processors p5215 0 0 (L3) A virtual processor implementation can contain access, and a properties virtual Processors p5214 0 0 (L3) A virtual processor implementation can contain access, and a properties virtual Processors p5215 0 0 (L5) A virtual processor implementation can contain access, subgroup access, porticular processor implementation can contain access, subgroup access, porticular processor p5215 0 0 0 (L5) A virtual processor implementation can contain subgroup access, porticular processor p5215 0 0 0 (L5) A virtual processor implementation can contain subgroup access, porticular processor p5215 0 0 0 (L5) A virtual processor implementation can contain subgroup access, porticular processor p5215 0 0 0 (L5) A virtual processor implementation can contain subgroup access, porticular processor p5215 0 0 0 0 (L5) A virtual processor p5215 0 0 0 0 (L5) A virtual processor p5215 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1           Processes         p56l2           Processes         p56l4           Processes         p56l4           Processes         p56c1		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclared, i.e. are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ (C4) The Penod property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (L1) A thread group component type can contain provides and requires data access, as well as port, feath (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes as (L4) A thread group must not contain a subprogram calls subclause. (L1) A process component type can contain a connection and requires data access, provided to the contain a connection and call of the contain a connection and call of the contain and contain and contain and call of the contain and contain a
Processors p6113 0 0 0 (L3) A processor implementation can contain a modes subclause, flows subclause, and a properties subclause, p614 0 0 (L4) A processor implementation can contain bus access, subprogram group access p615 0 0 (L5) A processor implementation must not contain a subprogram carbs subclause.  Virtual Processors p621 0 0 (L1) A virtual processor component type can contain port, feature group, provides subprogram access, at Virtual Processors p6212 0 0 (L2) A virtual processor component inplementation and contain accidance of virtual processor p6212 0 0 (L3) A virtual processor p6213 0 0 (L3) A virtual processor implementation can contain accidance of virtual bus, virtual processor y p6214 0 0 (L3) A virtual processor implementation can be clause, flows subclause, and a propertie virtual Processors y p6214 0 0 (L3) A virtual processor implementation must not contain accidance of virtual bus, and a propertie virtual Processors y p6215 0 0 (L5) A virtual processor implementation can contain subprogram access, subprogram group access, portificial Processors y p6215 0 0 (L5) A virtual processor implementation can contain subprogram group access, portificial Processors y p6215 0 0 (L5) A virtual processor implementation can contain subprogram group access, portificial processor implementation can contain subprogram group access, portificial processor implementation can contain subprogram group access, portificial processor implementation can contain subprogram access, subprogram group access, portificial processor implementation can contain subprogram access, subprogram group access, portificial processor implementation can contain subprogram access, subprogram group access, portificial processor implementation can contain subprogram access, subprogram group access, portificial processor implementation can contain subprogram access, subprogram group access, portificial processor implementation can contain subprogram access, subprogram group access, portificial processor implementation can contain subpro	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1           Processes         p56l2           Processes         p56l4           Processes         p56l4           Processes         p56c1		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text.Compute_Entrypoint_Call_Sequ (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic,  (L1) A thread group component trype can contain provides and requires data access, as well as port, feat (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram gro (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes as (L4) A thread group must not contain a subprogram calls subclause.  (L1) A process component trype can contain port, feature group, provides and requires data access, provided and contain a connection subclause, a flows subclause, a flows subclause, and contain a connection subclause, and constain a connection subclause.  (L3) A thread group must not contain a connection subclause, and constain a connection subclause, and constain a connection subclause.
Processors p6114 0 0 (L1) A processor implementation can contain bus access, subprogram group access processors p6115 0 0 (L5) A processor implementation must not contain a subprogram access, subprogram group access p6115 0 0 (L5) A processor implementation must not contain a subprogram access, access p6115 0 0 (L1) A virtual processor component type can contain port, feature group, provides subprogram access, access p6115 0 0 (L1) A virtual processor component implementation or virtual access, access p6115 0 0 (L2) A virtual processor component implementation can contain declarations of virtual access, and a property processor p6115 0 0 (L3) A virtual processor implementation can contain access, and a property processor p6115 0 0 (L4) A virtual processor implementation must not contain a subprogram access, and a property processor p6115 0 0 (L5) A virtual processor implementation can contain subprogram access, subprogram group access, port	Threads p5412 Threads p543 Threads p5463 Threads p5463 Thread p5464  Thread Groups p5512 Thread Groups p5512 Thread Groups p5513 Thread Groups p5514  Processes p5611 Processes p5612 Processes p5614 Processes p5614 Processes p5617 Processes p5617 Processes p5618 Processes p5619 Processes p5611		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclared, 1a, are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ (C4) The Penod property must have a value if the Diepatch_Protocol property value is periodic, sporadic, (C4) The Penod group component type can contain provides and requires data access, as well as port, feat (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes su (L4) A thread group must not contain a connections subclause, a flows subclause, a modes su (L4) A process component type can contain port, feature group, provides and requires data access, provide (L3) A process component implementation can contain abstract, data, subprogram, subprogram group, the (L3) A process component implementation can contain a subprogram, subprogram, subclause, a modes subclause (L4) A thread group must not contain a connections subclause, a flows subclause, a modes subclause (L4) A thread group must not contain a subprogram calls subclause, a flows subclause, a modes subclause (L4) A thread group must not contain a subprogram calls subclause, a flows subclause, a modes subclause. (C5) The complete source text associated with a process component must form a complete and legal provides of the process component must form a complete and legal provides subcroups and contain a connection port, feature group, provides subprogram access, provides
Processors p6115 0 0 (L5) A processor implementation must not contain a subprogram calls subclause.  Virtual Processors p6211 0 0 0 (L1) A virtual processor component type can contain port, feature group, provides subprogram access, as Virtual Processors p6212 0 0 0 (L2) A virtual processor component implementation or virtual bus, virtual processor virtual Processors p6213 0 0 0 (L2) A virtual processor implementation can contain a subprogram access, as Virtual Processors p6213 0 0 0 (L2) A virtual processor implementation can contain a subprogram calls subclause.  Virtual Processors p6214 0 0 (L3) A virtual processor implementation must not contain a subprogram calls subclause.  Virtual Processors p6215 0 0 0 (L5) A virtual processor implementation can contain a subprogram group access, port	Threads         p5412           Threads         p5413           Threads         p5403           Threads         p5404           Thread Groups         p5511           Thread Groups         p5512           Thread Groups         p5513           Thread Groups         p5514           Processes         p5612           Processes         p5612           Processes         p5613           Processes         p5614           Processes         p5614           Processes         p5617           Processes         p5618           Processes         p5619           Processes         p5611           Processors         p5611           Processors         p6112		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Cata_Sequ. (C4) The Pened property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (C4) The Pened property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (C4) A thread group component type can contain provides and requires data access, as well as port, feath (C2) A thread group implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group must not contain a connections subclause, a flows subclause, a modes su (L4) A thread group must not contain a subprogram calls subclause. (L5) A process component type can contain a port, feature group, provides and requires data access, provide (L6) A process component implementation can contain abstract, data, subprogram, subprogram group, the (L6) A process component implementation can contain abstract, data, subprogram, subprogram group, the (L6) A process component implementation can contain a subprogram access, provides (L7) A process implementation can contain a connections subclause, a flows subclause, a modes subclause (L7) A process implementation can contain a subprogram calls subclause. (L8) A process implementation can contain a subprogram calls subclause. (L9) A process component type can contain port, feature group, provides subprogram access, provides (L1) A processor component type can contain port, feature group, provides subprogram access, provides (L9) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual
Processors p6115 0 0 (L5) A processor implementation must not contain a subgrogram calls subclause.  Virtual Processors p6211 0 0 0 (L1) A virtual processor component type can contain port, feature group, provides subgrogram access, as virtual Processors p6212 0 0 0 (L2) A virtual processor component implementation or contain dedurations of virtual bus, virtual processor p6213 0 0 (L2) A virtual processor implementation can contain a subgrogram access, as virtual processors p6213 0 0 (L2) A virtual processor implementation can contain a subgrogram calls subclause.  Virtual Processors p6214 0 0 (L3) A virtual processor implementation must not contain a subgrogram calls subclause.  Virtual Processors p6215 0 0 (L5) A virtual processor implementation can contain a subgrogram group access, port	Threads         p5412           Threads         p5413           Threads         p5403           Threads         p5404           Thread Groups         p5511           Thread Groups         p5512           Thread Groups         p5513           Thread Groups         p5514           Processes         p5612           Processes         p5612           Processes         p5613           Processes         p5614           Processes         p5614           Processes         p5617           Processes         p5618           Processes         p5619           Processes         p5611           Processors         p5611           Processors         p6112		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Cata_Sequ. (C4) The Pened property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (C4) The Pened property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (C4) A thread group component type can contain provides and requires data access, as well as port, feath (C2) A thread group implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group must not contain a connections subclause, a flows subclause, a modes su (L4) A thread group must not contain a subprogram calls subclause. (L5) A process component type can contain a port, feature group, provides and requires data access, provide (L6) A process component implementation can contain abstract, data, subprogram, subprogram group, the (L6) A process component implementation can contain abstract, data, subprogram, subprogram group, the (L6) A process component implementation can contain a subprogram access, provides (L7) A process implementation can contain a connections subclause, a flows subclause, a modes subclause (L7) A process implementation can contain a subprogram calls subclause. (L8) A process implementation can contain a subprogram calls subclause. (L9) A process component type can contain port, feature group, provides subprogram access, provides (L1) A processor component type can contain port, feature group, provides subprogram access, provides (L9) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual
Virtual Processors p6211 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1           Processes         p56l2           Processes         p56l3           Processes         p56l4           Processes         p56c1           Processors         p61l1           Processors         p61l2           Processors         p61l3		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequ (C4) The Period proporty must have a value if the Dispatch_Protocol property value is periodic, sporadic, (L1) A thread group component type can contain provides and requires data access, as well as port, feats (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group must not contain a connections subclause, a flows subclause, a modes subclause, a flows subclause, a flows subclause, a flow subclause, a flow subclause, a flow subclause, and cut in the component type can contain port, feature group, provides and requires data access, provided (L2) A process component implementation can contain abstract, data, subprogram, subprogram group. It (L3) A process component implementation can contain abstract, data, subprogram, subprogram group. It (L3) A process component implementation can contain abstract, data, subprogram, subprogram group. It (L3) A process component implementation can contain abstract, data, subprogram, subprogram group. It (L3) A process component implementation can contain a subprogram access, provides (L4) A thread group must not contain a subprogram calls subclause. (C1) The complete source text associated with a process component must form a complete and legal program of the contain a subprogram access, provides (L2) A processor component type can contain port, feature group, provides subprogram access, provides (L2) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual
Virtual Processors p6212 0 0 0 (L2) A virtual processor component implementation can contain dediarations of virtual bus, virtual processor p6213 0 0 (L3) A virtual processor implementation can contain a modes subclause, flows subclause, and a propertie virtual Processors p6214 0 0 (L4) A virtual processor implementation must not contain a subprogram calls subclause.  Virtual Processors p6215 0 0 0 (L5) A virtual processor implementation can contain subprogram group access, subprogram group access, port.	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread p54c4         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1           Processes         p56l2           Processes         p56l4           Processes         p56l4           Processors         p56l1           Processors         p61l1           Processors         p61l2           Processors         p61l3           Processors         p61l4		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclated, i.e., are implicitly identif (C3) Eliner the Compute_Entrypoint, Compute_Entrypoint, Compute_Text Compute_Entrypoint_Call_Sequ (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic,  (L1) A thread group component type can contain provides and requires data access, as well as port, feast (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group must not contain a connections subclause, a flows subclause, a modes su (L4) A thread group must not contain a subprogram calls subclause.  (L1) A process component type can contain port, feature group, provides and requires data access, provides (L2) A process component implementation can contain abstract, data, subprogram, subprogram group, the (L3) A process component implementation can contain assubclause, a flows subclause, a modes subclause (L4) A thread group must not contain a connections subclause, a flows subclause, a modes subclause (L4) A thread group must not contain a connections subclause, a flows subclause, a modes subclause (L4) A thread group must not contain a subprogram calls subclause, a flows subclause, a modes subclause (L5) A process or component type can contain port, feature group, provides subprogram access, provides (L5) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual (L5) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual (L6) A processor implementation can contain a modes subclause, flows subclause, and a properties subclause.
Virtual Processors p6212 0 0 0 (L2) A virtual processor component implementation can contain dediarations of virtual bus, virtual processor p6213 0 0 (L3) A virtual processor implementation can contain a modes subclause, flows subclause, and a propertie virtual Processors p6214 0 0 (L4) A virtual processor implementation must not contain a subprogram calls subclause.  Virtual Processors p6215 0 0 0 (L5) A virtual processor implementation can contain subprogram group access, subprogram group access, port.	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread p54c4         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1           Processes         p56l2           Processes         p56l4           Processes         p56l4           Processors         p56l1           Processors         p61l1           Processors         p61l2           Processors         p61l3           Processors         p61l4		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclated, i.e., are implicitly identif (C3) Eliner the Compute_Entrypoint, Compute_Entrypoint, Compute_Text Compute_Entrypoint_Call_Sequ (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic,  (L1) A thread group component type can contain provides and requires data access, as well as port, feast (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group must not contain a connections subclause, a flows subclause, a modes su (L4) A thread group must not contain a subprogram calls subclause.  (L1) A process component type can contain port, feature group, provides and requires data access, provides (L2) A process component implementation can contain abstract, data, subprogram, subprogram group, the (L3) A process component implementation can contain assubclause, a flows subclause, a modes subclause (L4) A thread group must not contain a connections subclause, a flows subclause, a modes subclause (L4) A thread group must not contain a connections subclause, a flows subclause, a modes subclause (L4) A thread group must not contain a subprogram calls subclause, a flows subclause, a modes subclause (L5) A process or component type can contain port, feature group, provides subprogram access, provides (L5) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual (L5) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual (L6) A processor implementation can contain a modes subclause, flows subclause, and a properties subclause.
Virtual Processors p6212 0 0 0 (L2) A virtual processor component implementation can contain dediarations of virtual bus, virtual processor p6213 0 0 (L3) A virtual processor implementation can contain a modes subclause, flows subclause, and a propertie virtual Processors p6214 0 0 (L4) A virtual processor implementation must not contain a subprogram calls subclause.  Virtual Processors p6215 0 0 0 (L5) A virtual processor implementation can contain subprogram group access, subprogram group access, port.	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread p54c4         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1           Processes         p56l2           Processes         p56l4           Processes         p56l4           Processors         p56l1           Processors         p61l1           Processors         p61l2           Processors         p61l3           Processors         p61l4		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclated, i.e., are implicitly identif (C3) Eliner the Compute_Entrypoint, Compute_Entrypoint, Compute_Text Compute_Entrypoint_Call_Sequ (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic,  (L1) A thread group component type can contain provides and requires data access, as well as port, feast (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group must not contain a connections subclause, a flows subclause, a modes su (L4) A thread group must not contain a subprogram calls subclause.  (L1) A process component type can contain port, feature group, provides and requires data access, provides (L2) A process component implementation can contain abstract, data, subprogram, subprogram group, the (L3) A process component implementation can contain assubclause, a flows subclause, a modes subclause (L4) A thread group must not contain a connections subclause, a flows subclause, a modes subclause (L4) A thread group must not contain a connections subclause, a flows subclause, a modes subclause (L4) A thread group must not contain a subprogram calls subclause, a flows subclause, a modes subclause (L5) A process or component type can contain port, feature group, provides subprogram access, provides (L5) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual (L5) A processor component implementation can contain declarations of memory, bus, virtual bus, virtual (L6) A processor implementation can contain a modes subclause, flows subclause, and a properties subclause.
Virtual Processors p6213 0 0 (L3) A virtual processor implementation can contain a modes subclause, flows subclause, and a propertie Virtual Processors p6214 0 0 (L4) A virtual processor implementation must not contain a subprogram calls subclause.  Virtual Processors p6215 0 0 (L5) A virtual processor implementation can contain subprogram group access, subprogram group access, subprogram group access, port.	Threads         p5412           Threads         p5413           Threads         p5463           Threads         p5464           Thread Groups         p5512           Thread Groups         p5513           Thread Groups         p5513           Thread Groups         p5514           Processes         p5612           Processes         p5612           Processes         p5614           Processes         p5614           Processes         p5614           Processors         p6114           Processors         p6112           Processors         p613           Processors         p614           Processors         p615		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predeclared, i.e., are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Cata_Dource_Text Compute_Entrypoint_Cata_Sequ (C4) The Pendd property make a value if the Dispatch_Protocol property value is periodic, sporadic.  (L1) A thread group component type can contain provides and requires data access, as well as port, feath (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes su (L4) A thread group must not contain a connections subclause, a flows subclause, a modes su (L4) A process component type can contain port, feature group, provides and requires data access, provided and program group. If (L3) A process component implementation can contain abstract, data, subprogram, subprogram group, the catalogue of the contain a subprogram group, provides and requires data access, provided and contain a connections subclause, a flows subclause, a modes subclause.  (L4) A process component implementation can contain a connections subclause, a modes subclause.  (L4) A thread group must not contain a subprogram calls subclause, a modes subclause.  (L4) A thread group must not contain a subprogram calls subclause.  (L5) A processor component type can contain port, feature group, provides subprogram access, provides (L2) A processor implementation can contain declarations of memory, bus, virtual bus, virtual (L3) A processor implementation can contain an imades subclause, flows subclause, and a properties subclause.  (L4) A processor implementation can contain a subprogram access, subprogram group access, and properties subclause.
Virtual Processors p6214 0 0 (L4) A virtual processor implementation must not contain a subprogram calls subdause.  Virtual Processors p6215 0 0 (L5) A virtual processor implementation can contain subprogram group access, subprogram group access, port	Threads         p5412           Threads         p543           Threads         p54c3           Threads         p54c4           Thread Groups         p5511           Thread Groups         p5512           Thread Groups         p5513           Thread Groups         p5514           Processes         p5612           Processes         p5612           Processes         p5613           Processes         p5644           Processes         p5651           Processes         p5612           Processes         p5614           Processors         p6111           Processors         p6112           Processors         p6114           Processors         p6115           Virtual Processors         p6211		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event bort, and Error out event data port are predeclared, i.e. are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Cat_Sequ (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (L1) A thread group component type can contain provides and requires data access, as well as port, feath (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes subclause and contain a connections subclause, a flow subclause, a modes subclause and catally a process component type can contain port, feature group, provides and requires data access, provided (L1) A process component implementation can contain abstract, data, subprogram, subprogram group, the catally of the catally and catally subprogram group, the catally of the catally subprogram group, the catally subprogram group, the catally subprogram group, the catally subprogram group, the catally subprogram group is catally subprogram group, the catally subprogram group is catally subprogram group, the catally subprogram group is catally subprogram access, provides (L4) A thread group must not contain a subprogram calls subclause, a modes subclause and legal program calls subclause.  (C1) The complete source text associated with a process component must form a complete and legal program calls subclause, and a properties subclause and subprogram access, provides (L2) A processor implementation can contain and subprogram access, subprogram group access (L5) A processor implementation must not contain a subprogram calls subclause, and a properties subclause in program access, subprogram group access (L5) A processor implementation must not contain a subprogram calls subclause.
Virtual Processors p62/5 0 0 (L5) A virtual processor implementation can contain subprogram access, subprogram group access, port	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1           Processes         p56l2           Processes         p56l3           Processes         p56l4           Processes         p56l4           Processes         p56l1           Processors         p6l11           Processors         p6l12           Processors         p6l13           Processors         p6l14           Processors         p6l15           Virtual Processors         p62l1           Virtual Processors         p62l2		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event bort, and Error out event data port are predeclared, i.e. are implicitly identif (C3) Either the Compute_Entrypoint, Compute_Entrypoint_Source_Text Compute_Entrypoint_Cat_Sequ (C4) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (L1) A thread group component type can contain provides and requires data access, as well as port, feath (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram group (L3) A thread group implementation can contain a connections subclause, a flows subclause, a modes subclause and contain a connections subclause, a flow subclause, a modes subclause and catally a process component type can contain port, feature group, provides and requires data access, provided (L1) A process component implementation can contain abstract, data, subprogram, subprogram group, the catally of the catally and catally subprogram group, the catally of the catally subprogram group, the catally subprogram group, the catally subprogram group, the catally subprogram group, the catally subprogram group is catally subprogram group, the catally subprogram group is catally subprogram group, the catally subprogram group is catally subprogram access, provides (L4) A thread group must not contain a subprogram calls subclause, a modes subclause and legal program calls subclause.  (C1) The complete source text associated with a process component must form a complete and legal program calls subclause, and a properties subclause and subprogram access, provides (L2) A processor implementation can contain and subprogram access, subprogram group access (L5) A processor implementation must not contain a subprogram calls subclause, and a properties subclause in program access, subprogram group access (L5) A processor implementation must not contain a subprogram calls subclause.
Virtual Processors p6215 0 0 (L5) A virtual processor implementation can contain subprogram access, subprogram group access, port	Threads         p54l2           Threads         p54l3           Threads         p54c3           Threads         p54c4           Thread Groups         p55l1           Thread Groups         p55l2           Thread Groups         p55l3           Thread Groups         p55l4           Processes         p56l1           Processes         p56l2           Processes         p56l3           Processes         p56l4           Processes         p56l4           Processes         p56l1           Processors         p6l11           Processors         p6l12           Processors         p6l13           Processors         p6l14           Processors         p6l15           Virtual Processors         p62l1           Virtual Processors         p62l2		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Complete out event port, and Error out event data port are predectared, i.e., are implicitly identif (C3) Either the Compute_Entrypoint_Entrypoint_Compute_Entrypoint_Entrypoint_Compute_Entrypoint_Compute_Entrypoint_Compute_Entrypoint_Entrypoin
	Threads p5412 Threads p543 Threads p543 Threads p5463 Threads p5464 Thread p5464 Thread Groups p5512 Thread Groups p5512 Thread Groups p5513 Thread Groups p5514  Processes p5611 Processes p5612 Processes p5613 Processes p5614 Processors p6117 Processors p6117 Processors p6118 Processors p6118 Processors p6119 Thread Groups p5514 Thread Groups p5611 Thread Groups p5612 Thread Groups p		(2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (3) The Compite out event port, and Error out event data port are predeclared, i.e., are implicitly identify (3) Either the Compute, Eintrypoint, Compute, Eintrypoint, Course, Ext Compute, Entrypoint, Call, Sequipoint, Sequip
Virtual Processors p62c1 0 0 (C1) In a fully bound system every virtual processor must be directly or indirectly bound to, or directly or in	Threads p5412 Threads p5413 Threads p5413 Threads p5423 Threads p5424 Thread Groups p5512 Thread Groups p5512 Thread Groups p5513 Thread Groups p5514 Processes p5612 Processes p5612 Processes p5614 Processes p5614 Processors p6117 Processors p6117 Processors p6118 Processors p6118 Processors p6119 Processors p6119 Processors p6111 Processors p6111 Processors p6111 Processors p6112 Processors p6113 Processors p6114 Processors p6115 Virtual Processors p6211 Virtual Processors p6212 Virtual Processors p6213 Virtual Processors p6213		(12) A thread component implementation can contain abstract, data, subprogram, and subprogram group (13) The Compite out event port, and Error out event data port are predictaned, i.e., are implicitly identify (13) Either the Compute_Entrypoint, Compute_Entrypoint_Course_Text Compute_Entrypoint_Call_Sequ (14) The Period property must have a value if the Dispatch_Protocol property value is periodic, sporadic, (14) A thread group component type can contain provides and requires data access, as well as port, feat. (14) A thread group more mentation can contain abstract, data, subprogram, subprogram group (13) A thread group must not contain a connections subclause, a flows subclause, a modes subclause. (14) A thread group must not contain a subprogram calls subclause. (14) A thread group must not contain a subprogram calls subclause. (14) A process component implementation can contain abstract, data, subprogram, subprogram group, the call of the contain a subprogram calls subclause, a flows subclause, a modes subclause. (14) A thread group must not contain a subprogram access, and the contain a subprogram calls subclause. (15) The complete source text associated with a process component must form a complete and legal program access, provides (15) A processor component type can contain port, feature group, provides subprogram access, provides (15) A processor implementation can contain a contain declarations of memory, bus, virtual bus, virtual (15) A processor implementation can contain a contain declarations of memory, bus, virtual bus, virtual (16) A processor implementation can contain port, feature group, provides subprogram access, are (17) A virtual processor implementation can contain port, feature group, provides subprogram access, are (17) A virtual processor implementation can contain a subprogram calls subclause.
	Threads p5412 Threads p543 Threads p543 Threads p54c3 Threads p54c4 Thread p54c4  Thread Groups p5512 Thread Groups p5512 Thread Groups p5513 Thread Groups p5514 Processes p5614 Processes p5612 Processes p5614 Processes p5614 Processors p6112 Processors p6112 Processors p6114 Processors p6114 Processors p6115 Virtual Processors p6115 Virtual Processors p6212 Virtual Processors p6212 Virtual Processors p6213 Virtual Processors p6214 Virtual Processors p6215		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Compilete out event port, and Error out event data port are predeclared, i.e., are implicitly identify (C3) Errier the Compute_Entrypoint_Source_Text Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequil (C4) The Period procept must have a value if the Dispatch_Protocol property value is periodic, sponadic.  (L1) A thread group component type can contain provides and requires data access, as well as port, feat (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram provides (L3) A thread group implementation can contain a connection subclause, a flows subclause, a modes su (L4) A thread group implementation can contain a connection subclause, a flows subclause, a modes su (L4) A thread group must not contain a subprogram calls subclause.  (L5) A process component type can contain port, feature group, provides and requires data access, provided and call thread can be contained to the contained to the contained can be contained to the contained to the contained can be contained to the contain
	Threads p5412 Threads p543 Threads p543 Threads p54c3 Threads p54c4 Thread p54c4  Thread Groups p5512 Thread Groups p5512 Thread Groups p5513 Thread Groups p5514 Processes p5614 Processes p5612 Processes p5614 Processes p5614 Processors p6112 Processors p6112 Processors p6114 Processors p6114 Processors p6115 Virtual Processors p6115 Virtual Processors p6212 Virtual Processors p6212 Virtual Processors p6213 Virtual Processors p6214 Virtual Processors p6215		(L2) A thread component implementation can contain abstract, data, subprogram, and subprogram group (L3) The Compilete out event port, and Error out event data port are predeclared, i.e., are implicitly identify (C3) Errier the Compute_Entrypoint_Source_Text Compute_Entrypoint_Source_Text Compute_Entrypoint_Call_Sequil (C4) The Period procept must have a value if the Dispatch_Protocol property value is periodic, sponadic.  (L1) A thread group component type can contain provides and requires data access, as well as port, feat (L2) A thread group component implementation can contain abstract, data, subprogram, subprogram provides (L3) A thread group implementation can contain a connection subclause, a flows subclause, a modes su (L4) A thread group implementation can contain a connection subclause, a flows subclause, a modes su (L4) A thread group must not contain a subprogram calls subclause.  (L5) A process component type can contain port, feature group, provides and requires data access, provided and call thread can be contained to the contained to the contained can be contained to the contained to the contained can be contained to the contain

Virtual Processors p62c2	0 0	0 (C2) In a fully deployed system a requires virtual bus binding of a virtual processor specified t	,
Memory p63I1	0 0	0 (L1) A memory type can contain bus access declarations, feature groups, a modes subclaus	e, and prope
Memory p63l2	0 0	0 ((2) A memory implementation can contain abstract, memory, and bus subcomponent declar	ations.
Memory p63l3	0 0	0 (L3) A memory implementation can contain a modes subdause and properly associations.	
Memory p63l4	0 0	0 (LALA memory implementation can contain hus access connection declarations. Bus access	
Memory p63I5	0 0	0 (5.5 A manage implementation must not contain flower substitutes or substitutes as substitutes	iuse.
incinory pools	0 0	(CO) A manual important must not contain their action and the contain the action and the contain the c	luoc.
Buses p64I1	0 0		
	0 0	0 (L1) A bus type can have requires bus access declarations, a modes subclause, and propert	
Buses p64l2	0 0	0 (L2) A bus type must not contain any flow specifications.	
Buses p64l3	0 0	0 (L3) A bus implementation can contain virtual bus and abstract subcomponent declarations.	
Buses p64l4	0 0	0 (L4) A bus implementation can contain a modes subclause and property associations.	
Buses p64l5	0 0	0 (L5) A bus implementation must not contain flows subclause, or subprogram calls subclause	
/irtual Buses p65l1	0 0	0 (L1) A virtual bus type can have property associations.	
Virtual Buses p65l2	0 0	0 (L2) A Virtual bus type must not contain flow specifications.	
Virtual Buses p65l3	0 0	0 (L3) A virtual bus implementation can contain virtual bus subcomponent declarations.	
/irtual Buses p65l4	0 0	0 (L1 A virtual bus implementation can contain a modes subclause and properly associations.	
/irtual Buses p65l5	0 0	(c) A vitual bus implementation can contain a more social and projectly associated by a containing the containing a connection such data for the containing a connection subclaims (final subclaims) and containing a containin	
/irtual Buses p65c1	0 0	(L.3) A virtual bus implementation must not contain a connection's subclause, how subclause.	s or buses th
ritual buses pood 1	0 0	U (C1) In a Tully deployed system virtual buses must be directly found to processor	
Devices p66l1	0 0	0 (L1) A device type can contain port, feature group, provides subprogram access, provides su	
Devices p66l2	0 0	0 (L2) A device component implementation must not contain a subprogram calls subclause.	s, bus acces:
Devices p66l3	0 0	0 (L3) A device implementation can contain abstract, data, virtual bus, and bus subcomponent	, bus acces
Systems p71I1	0 0	0 (L1) A system component type can contain subprogram, subprogram group, data and bus ac	cess declara
Systems p71l2	0 0	0 (L2) A system component implementation can contain abstract, data, subprogram, subprogram, subprogram	ım group, pre
Systems p71l3	0 0	0 (L3) A system implementation can contain a modes subclause, a connections subclause, a fi	
Systems p71l4	0 0	0 (L4) A thread group must not contain a subprogram calls subclause.	
Systems p71n1	0 0	0 (41) The defining identifier of a feature must be unique within the namespace of the associated (12) and the control of the	
Systems p71n2	0 0		
		(NE) Throad roughest or a straight of the stra	
Systems p71n3	0 0	(11)	
Systems p71n4	0 0	0 (N4) A feature is referenced in one of two ways. Within the component implementations for a	
Systems p71n5	0 0	0 (N5) The path of a contained property association for a feature must refer to an element of a	feature grou
Systems p71I1	0 0	0 (L1) Each feature can be refined at most once in the same type extension.	
Systems p71l2	0 0	0 (L2) A feature refinement declaration of a feature and the original feature must both be declar	ed as port, r
Systems p71I3	0 0	0 (L3) Feature arrays must only be declared for threads, devices, and processors.	
systems p71l4	0 0	0 (L4) If the feature refinement specifies an array dimension, then the feature being refined mu	st have an a
Systems p71l5	0 0	0 (L5) If the refinement specifies an array dimension size, then the feature being refined must t	
Systems p71l6	0 0	0 (L6) A contained property association must only be used when the feature is a feature group	
Systems p7117	0 0	(L7) In the case of a feature with a classifier ofference, the classifier of the refined feature de	
,,o.o pr 117	0 0	(Lr) in the case of a feature with a classifier reletence, the classifier of the feature de	iarauori III d
Abstract Features p81I1	0 0	0 (L1) The feature direction in a refined feature declaration must be identical to the feature direction.	-41 !- 41 6
Abstract Features p81I2	0 0	0 (L2) If the direction of an abstract feature is specified, then the direction must be satisfied by	
bstract Features p81l3	0 0	0 (L3) An abstract feature with a feature prototype identifier and the prototype being referenced	
bstract Features p81l4	0 0	0 (L4) An abstract feature refinement declaration of a feature with a feature prototype reference	must only a
eature Groups an p82n1	0 0	0 (N1) The defining identifier of a feature group type must be unique within the package names	pace of the
eature Groups an p82n2	0 0	0 (N2) Each feature group type provides a local namespace. The defining identifiers of prototy	
eature Groups an p82n3	0 0	0 (N3) The local namespace of a feature group type extension includes the defining identifiers	
eature Groups an p82n4	0 0	0 (N4) The defining feature identifiers of feature group declarations must be unique in the local	
eature Groups an p82n5	0 0	0 (KIS) The defining feature group identifier of feature_refinement declarations in component by	
eature Groups an p82n6	0 0	· · · · · · · · · · · · · · · · · · ·	
		( · · · · · · · · · · · · · · · · · · ·	
eature Groups an p82n7		v., mp. and p. a	
eature Groups an p82l1	0 0	0 (L1) A feature group type may contain zero or more elements, i.e., feature or feature groups.	
eature Groups an p82l2	0 0	0 (L2) A feature group type can be declared to be the inverse of another feature group type, as	indicated by
eature Groups an p82l3	0 0	0 (L3) Only feature group types without inverse of or feature group types with features and inve	rse of can b
eature Groups an p82l4	0 0	0 (L4) A feature group type that is an extension of another feature group type without an invers	a of cannot (
eature Groups an p82l5	0 0	0 (L5) The feature group type that is an extension of another feature group type with features a	
eature Groups an p82l6	0 0	0 (L6) A feature group declaration with an inverse of statement must only reference feature gro	
eature Groups an p8217	0 0	0 (LT) A feature group refinement may be refined to only add property associations. In this case	
0.00pc un pozn	5 0	(LET / in leasure group remaining may be fellined to thing add properly associations, in this case	

Feature Groups an p82		0		
Feature Groups an p82			0 (L9) Each of the declared features or feature groups in a feature group must be a pair-wise complement v	
eature Groups an p82		•	0 (L10) If both feature group types have zero features, then they are considered to complement each other;	
ature Groups an p82		0		
ature Groups an p82		0		
ature Groups an p82	2113	0	0 (L13) If an in or out direction is specified as part of a feature group declaration, then all features inside the	
s p83		-	0 (N1) A defining port identifier must adhere to the naming rules specified for all features (see Section 8).	
s p83			0 (N2) The defining identifier of a port refinement declaration must also appear in a feature declaration of a	
ts p83			0 (N3) The unique component type identifier of the data classifier reference must be the name of a data cor	
rts p83		-	0 (N4) The prototype identifier of a prototype identifier of a prototype reference, if specified, must exist in the namespace of the con	
ts p83		-	0 (L1) Ports can be declared in subprogram, thread, thread group, process, system, processor, virtual proc	
rts p83		•	0 (12) Data and event data ports may be incompletely defined by not specifying the data component classif	
rts p83			0 (L3) Data, event, and event data ports may be refined by adding a property association. The data compor	
rts p83	314	0	0 (L4) The port category of a port refinement must be the same as the category of the port being refined, or	
orts p83	315	0	0 (L5) The port direction of a port refinement must be the same as the direction of the feature being refined	
ibprogram and S p84			0 (N1) The defining identifier of a provides or requires subprogram or subprogram group access declaration	
bprogram and S p84		-	0 (N2) The defining identifier of a provides or requires subprogram or subprogram group refinement must e	
bprogram and S p84			0 (N3) The component type identifier or component implementation name of a subprogram or subprogram or subprogram in	
ubprogram and S p84			0 (N4) The prototype identifier of a subprogram group access classifier reference, if present	
bprogram and S p84		-	0 (L1) If a subprogram access refers to a component classifier or a component prototype, then the category	
bprogram and S p84			0 (L2) If a subprogram group access refers to a component classifier or a component prototype, then the ca	
ibprogram and S p84	413	0	0 (L3) An abstract feature can be refined into a subprogram access or a subprogram group access. In this of	
bprogram and S p84			0 (L4) A subprogram or subprogram group access declaration that does not specify a component classifier	
ubprogram and S p84		-	0 (L5) A subprogram or subprogram group access declaration may be refined by adding a property associa	
oprogram and S p84	416	0	0 (L6) A provides subprogram access cannot be refined to a requires subprogram access and a requires su	
bprogram and S p84	4c1	0	0 (C1) A provides subprogram access feature indicates that a subprogram is made available to be reference	
bprogram Paran p85	5n1	0	( )	
oprogram Paran p85	5n2	0	0 (N2) The defining parameter identifier of a parameter refinement declaration must also appear in a feature	
oprogram Paran p85	5n3	0	0 (N3) The data classifier reference must refer to a data component type or a data component implemental	
program Paran p85	5n4	0	0 (N4) The prototype identifier, if present, must exist in the namespace of the subprogram classifier that cor	
oprogram Paran p85	511	0	0 (L1) Parameters can be declared for subprogram component types.	
ibprogram Paran p85			0 (L2) A parameter declaration that does not specify a data classifier reference is incomplete. Such a refere	
ibprogram Paran p85		0	( )	
bprogram Paran p85	514	0	0 (L4) The parameter direction of a parameter refinement must be the same as the direction of the feature t	
ta Component A p86	6n1	0		
ita Component A p86			0 (N2) The defining identifier of a provides or requires data access refinement must exist as a defining iden	
ta Component A p86		•	0 (N3) The component type identifier or component implementation name of a data access classifier referei	
ta Component A p86		-	0 (N4) The prototype identifier, if present, must exist in the namespace of the classifier that contains the dal	
ta Component A p86		-	0 (L1) If a data access refers to a component classifier or a component prototype, then the category of the or	
ta Component A p86			0 (L2) A data access declaration may be refined by refining the data classifier, by adding a property association	
ta Component A p86			0 (L3) A provides data access cannot be refined to a requires data access and a requires data access cann	
ta Component A p86			0 (L4) An abstract feature can be refined into a data access. In this case, the abstract feature must not have	
ta Component A p86		-	0 (C1) A data access declaration that does not specify a data classifier reference is incomplete. Such a refe	
ta Component A p86			0 (C2) if the source code of a component does access shared data, then the component type declaration m	
ta Component A p86	6c3	0	0 (C3) A data access refinement may refine an abstract feature declaration. If the abstract feature declaration	
Component Ac p87		0		
s Component Ac p87			0 (N2) The defining identifier of a provides or requires bus refinement must exist as a defining identifier of a	
Component Ac p87			0 (N3) The component type identifier or component implementation name of a bus access classifier referen	
Component Ac p87		-	0 (N4) The prototype identifier, if present, must exist in the namespace of the classifier that contains the but	
Component Ac p87			0 (L1) If a bus access refers to a component classifier or a component prototype, then the category of the c	
s Component Ac p87			0 (L2) A bus access declaration may be refined by refining the bus classifier, by adding a property associated	
s Component Ac p87	713	0	0 (L3) A provides bus access cannot be refined to a requires bus access and a requires bus access cannot	
is Component Ac p87	714	0	0 (L4) An abstract feature can be refined into a bus access. In this case, the abstract feature must not have	
is Component Ac p87	7c1	0	0 (C1) A bus access declaration that does not specify a bus classifier reference is incomplete. Such a refere	
s Component Ac p87	7c2	0	0 (C2) If a bus access feature is a refinement of an abstract feature, then the direction of the abstract feature	
is Component Ac p87	7n1	0	0 (N1) The defining identifier of a defined connection declaration must be unique in the local namespace of	

Bus Component Ac p87n2	0 0	0 (N2) The connection identifier in a connection refinement declaration must refer to a named connection d
Bus Component Ac p87I1	0 0	0 (L1) A connection refinement must contain at least one of the following: a connection source and destinat
Bus Component Ac p87l2	0 0	0 (L2) If a semantic connection may be active in a particular mode, then the ultimate source and ultimate of
Bus Component Ac p87I3	0 0	0 (L3) If a semantic connection may be active in a particular mode transition, then the ultimate source comp
Feature Connection p91n1	0 0	0 (N1) A source or destination reference in a feature connection or feature connection refinement declaration
Feature Connection p91n2	0 0	0 (N2) The subcomponent reference may refer to a subcomponent or a subcomponent array.
Feature Connection p9111	0 0	0 (L1) If the feature connection declaration represents a connection between features of sibling component
Feature Connection p9112	0 0	(E1) If the leading defined to the leading de
Feature Connection p9113	0 0	(EZ) If the realistic definition of the control of
Feature Connection p91l4	0 0	(ES) If the realistic definition of the process of the second of the sec
		(E-7) If the realistic confined on the confined of the confined on the confine
Feature Connection p9115	0 0	0 (L5) The individual connections of a semantic connection must be bidirectional or have the same direction
Port Connections p92n1	0 0	0 (N1) The connection identifier in a port connection refinement declaration must refer to a named port or fe
Port Connections p92n2	0 0	0 (N2) A source or destination reference in a port connection or port connection refinement declaration must
Port Connections p92n3	0 0	0 (N3) The subcomponent reference may also consist of a reference to a subcomponent array.
Port Connections p92n4	0 0	0 (N4) The event_or_event_data identifier of event source specifications (self.event_or_event_data_identifi
Port Connections p92l1	0 0	(L1) In the case of a directional port connection the connection end representing the source of the flow m
Port Connections p92l2	0 0	0 (L2) In the case of a bidirectional port connection either connection end can be the source. If the bidirection
Port Connections p92l3	0 0	0 (L3) If the source connection end is a data access feature it must have read access rights; if the destination
Port Connections p92l4	0 0	0 (L4) The feature identifier of a subcomponent reference may refer to a feature array, if the subcomponent
Port Connections p92l5	0 0	(L5) The following are acceptable sources and destinations of port connections. The left column shows or
Port Connections p92l6	0 0	(L6) If the port connection declaration represents a connection between ports of sibling components, then
Port Connections p92l7	0 0	0 (L7) If the port connection declaration represents a connection between ports up the containment hierarch
Port Connections p92l8	0 0	0 (L8) If the port connection declaration represents a connection between ports down the containment hiera
Port Connections p92l9	0 0	0 (L9) The individual connections of a semantic port connection must be bidirectional or have the same dire
Port Connections p92l10	0 0	0 (L10) Self.≺identifier> must only be referenced as the source of a connection.
Port Connections p92l11	0 0	0 (L11) A data port cannot be the destination of more than one semantic port connection unless each sema
Port Connections p92l12	0 0	0 (L12) A semantic connection cannot contain connection declarations with both immediate and delayed Tin
Port Connections p92I13	0 0	0 (L13) For connections between data ports, event data ports and data access, the data classifier of the sou
Port Connections p92I14	0 0	0 (L14) The following rules are supported: ΒЂŷ ΒЂŷ вЂŷ αЂŷ αδρ Classifier_Match: The source data type and of
Port Connections p92l15	0 0	0 (L15) If more than one port connection declaration in a semantic port connection has a property association
Port Connections p92l16	0 0	0 (L16) A processor port specification must only be used in event connections within threads and subprogra
Port Connections p92c1	0 0	0 (C1) There cannot be cycles of immediate connections between threads, devices, and processors.
Port Connections p92c2	0 0	(C2) The processor port identifier of a processor port specification (processor_processor_port_identifier) m
Port Connections p92c3	0 0	0 (C3) The Supports Classifier Subset Matches property may be associated with a bus or virtual bus. This
Port Connections p92c4	0 0	0 (C4) The Supports_Onespine_Converginons properly may be associated with a bus or virtual bus. This specifie
r ort commediane pezer		(O4) The appending type—contrensions properly may be associated with a bus of virtual bus. This specific
Parameter Connec p93n1	0 0	(N1) The connection identifier in a parameter connection refinement declaration must refer to a named or
Parameter Connec p93n2	0 0	(tt) The controlled that parameter controlled the parameter controlled to the controlled that the parameter controlled to the controlled that the controlled to the controlled
Parameter Connec p93l1	0 0	(NZ) / Found (addition) found of a parameter commence of a parameter
		(E) The source of a parameter connection made to an incoming data of order data port of the containing
Parameter Connec p93l2		\
Parameter Connec p93l3	0 0	0 (L3) A parameter cannot be the destination feature reference of more than one parameter connection dec
Parameter Connec p93l4	0 0	0 (L4) The data classifier of the source and destination must match. The matching rules as specified by the
1		
Access Connection p94n1	0 0	0 (N1) The connection identifier in an access connection refinement declaration must refer to a named acce
Access Connection p94n2	0 0	0 (N2) An access reference in an access connection declaration must reference an access feature of a sub
Access Connection p94I1	0 0	0 (L1) The category of the source and the destination of a access connection declaration must be the same
Access Connection p94l2	0 0	0 (L2) In the case of a bidirectional semantic access connection either connection end can be the source.
Access Connection p94l3	0 0	0 (L3) In the case of a directional data or bus access connection end representing the comp
Access Connection p94l4	0 0	0 (L4) In a partial AADL model the ultimate source or destination may be a provides access feature of a cor
Access Connection p94I5	0 0	0 (L5) If the access connection declaration represents an access connection between access features of si
Access Connection p94l6	0 0	(L6) If the access connection declaration represents a feature mapping up the containment hierarchy, the
Access Connection p94I7	0 0	(LT) If the access connection declaration represents a feature mapping down the containment hierarchy,
Access Connection p94l8	0 0	0 (L8) A requires access cannot be the source or destination feature reference of more than one access co
Access Connection p94l9	0 0	(L9) For access connections the classifier of the provider access must match to the classifier of the requir
Access Connection p94I10	0 0	0 (L10) If more than one access feature in a semantic access connection has an Access_Right property ass
Access Connection p94I11	0 0	0 (L11) The category of the access connection source and destination must be identical. If the component of
·		
		0 (N1) The connection identifier in a feature group connection refinement declaration must refer to a feature
Feature Group Cor p95n1	0 0	

Feature Group Cor p95l1	0	0	(L1) If the feature group connection declaration represents a component connection between sibling com
Feature Group Cor p95l2	0	0	(L2) The Classifier_Matching_Rule property specifies the rule to be applied to match the feature group cla
Feature Group Cor p95l3	0	0	(L3) The following rules are supported for feature group connection declarations that represent a connect 0
Feature Group Cor p95l4	0	0	(L4) The following rules are supported for feature group connection declarations that represent a connect 0
Feature Group Cor p95l5	0	0	(L5) If the feature group connection declaration represents a connection between feature group of sibling 0
Feature Group Cor p95l6	0	0	(L6) If the feature group connection declaration represents a connection between feature groups up the c 0
Feature Group Cor p95I7	0	0	(L7) If the feature group connection declaration represents a connection between feature groups down the
Feature Group Cor p95l8	0	0	(L8) A feature group connection must be bidirectional or be consistent with the direction of the source and