Verilog Design: Race-Car Fastest Lap Tracking

There are 3 racing cars, numbered #1, #2, and #3 competing at a "fastest lap" event. Instead of racing each other, each car takes turn running on the course. Each lap time is measured and fed into a digital "fastest lap tracking" circuit. This digital circuit shows the winner's car number and the best time achieved.

This circuit has 2 inputs, *n* = car number (from 1-3), and *t* = time to complete the course as unsigned 8-bit integer. It has 2 outputs, *n_best* = car number which currently has the best time, and *t_best* = the best time that is achieved.

n and *n_best* are 2-bit quantities, and *t* and *t_best* are 8-bit unsigned integer. *n_best* and *t_best* should be reset to 2'b00 and 8'd255, respectively. On the input side, if *n* = 0 appears, *t* is ignored, since there are only cars numbered 1 through 3.

In motor racing, if equal times appear, the one who set the time first is considered the winner. Here is an example of this digital circuit in action, right after reset:

clk#	1	2	3	4	5	6	7	8	9	10	11	12
n	0	1	2	3	0	2	2	1	3	1	2	0
t	x	128	127	129	x	126	129	124	124	125	126	x
n_best	0	1	2	2	2	2	2	1	1	1	1	1
t_best	255	128	127	127	127	126	126	124	124	124	124	124

In clk#9, you can see that, even if car #3 matches car #1's time, car #1 is still considered the winner since car #1 has set the best time first.

Design this "fastest lap tracking" circuit. Use the following code header and finish up the design:

```
module flt (clk, reset, n, t, n_best, t_best);
  input clk, reset;
  input [1:0] n;
  input [7:0] t;
  output [1:0] n_best;
  output [7:0] t_best;
endmodule
```