1. Design a Verilog module with 3 inputs: a, b, c, and one output, m. The output m is the majority of its 3 inputs. Copy the following code header to a `majority.v` and finish up the design:

```
module majority (a, b, c, m);
  input a, b, c;
  output m;

  // add verilog code here
endmodule
```