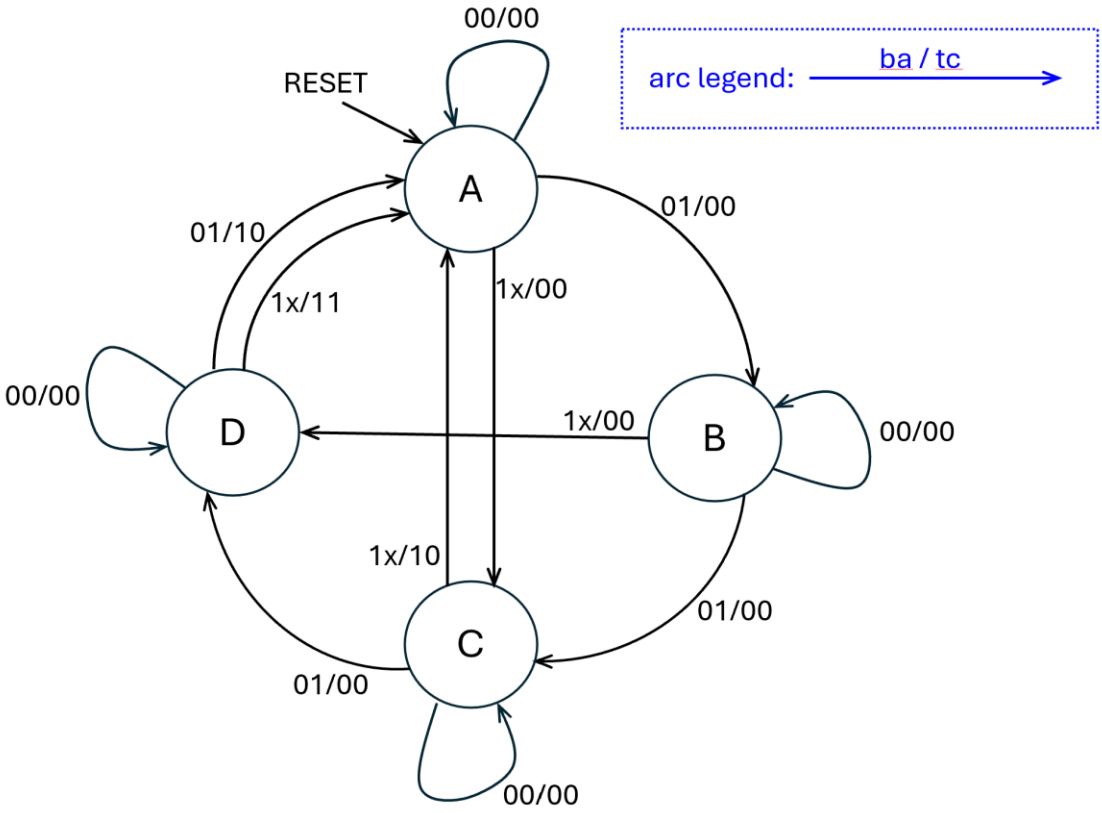
Implement Verilog from a state transition diagram:

Consider the following state transition diagram, consisting of 2 inputs, a and b, and 2 Mealy outputs, t and c.



Implement this FSM in Verilog using the following code header. Finish up the design:

```
module vend (clk, reset, a, b, t, c);
  input clk, reset, a, b;
  output t, c;

endmodule
```