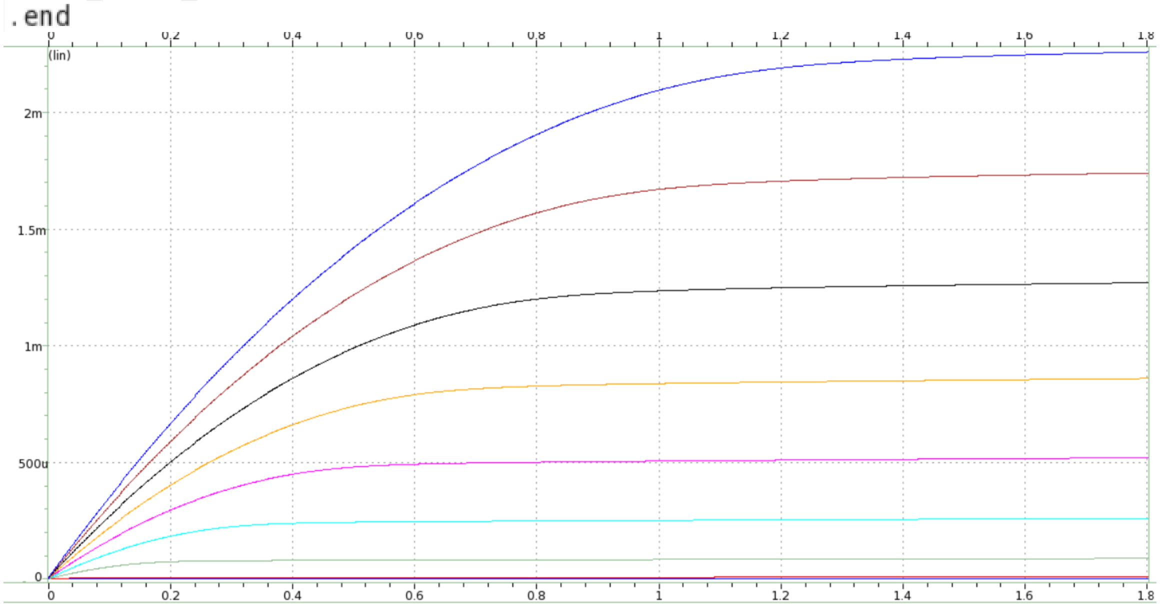
Hspice HW1

(1) Compare both I-V curves and make comments on their differences.

W=18um, L=1.8um

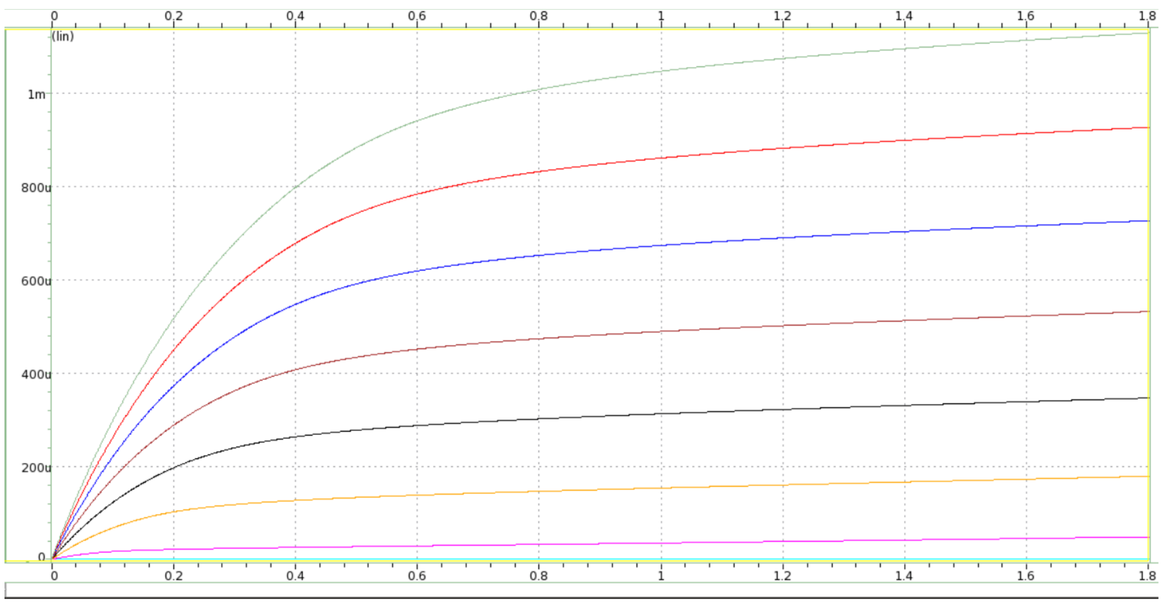
```
Hw1_1_long channel
.option post
*ciruit
mm vd vg vs gnd n_18_mm  l=1.8u  w=18u AS="0.48u*18u" AD="0.48u*18u" PS="0.96u
+18u" PD="0.96u+18u"

*source
vdd vd 0 dd
vgg vg 0 gg
vss vs 0 0
*sim
.dc dd 0 1.8 1m sweep gg 0 1.8 0.2

.lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/
mm180_reg18_v124.lib" tt
.end
```



X-axis: VDS, Y-axis: Ids, VGS varies from 0 to 1.8V, step=0.2V

W=1.8um, L=0.18um

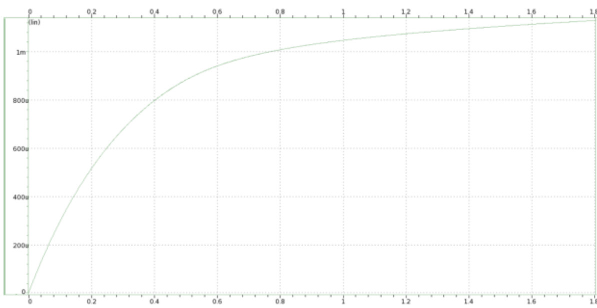
```
Hw1_1_short channel
.option post
*ciruit
mm vd vg vs gnd n_18_mm  l=0.18u  w=1.8u AS="0.48u*1.8u" AD="0.48u*1.8u"
PS="0.96u+1.8u" PD="0.96u+1.8u"

*source
vdd vd 0 dd
vgg vg 0 gg
vss vs 0 0
*sim
.dc dd 0 1.8 1m sweep gg 0 1.8 0.2

.lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/
mm180_reg18_v124.lib" tt
.end
```

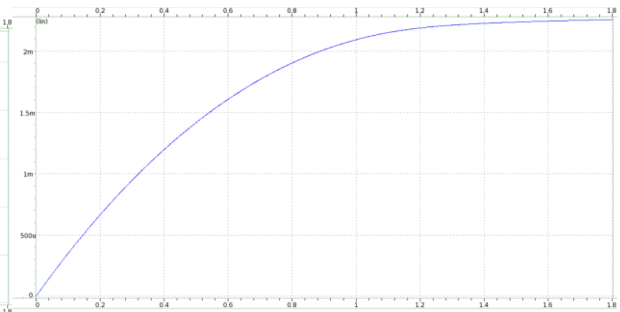


X-axis: VDS, Y-axis: Ids, VGS varies from 0 to 1.8V, step=0.2V

Lab1 summary:

We can see that ID will increase as VDS increase at first. However, When VDS>VGS-VTh, the transistor enters the saturation region. This means that in the ideal condition ID won’t increase as VDS increase. The small change of ID after entering the saturation region is due to channel length modulation.





In the above pictures, we can see that when VGS is the same, short channel’s ID,sat is smaller than the long channel’s ID,sat. Take these two pictures as example. Both pictures are when VGS=1.8V. The short channel’s ID,sat is about 1mA, and the long channel’s ID,sat is about 2mA.This is because the velocity saturation. I will clearly illustrate it in the Lab3.

(2) Compare the simulated current and the calculated current at different conditions.

(a) VGS=1.8V, VDS=1.8V, W/L=18um/1.8um

ID,calculated

=0.5*314.1/10000*(3.4515*10^-11)/(4.2*10^-9)*(18u/1.8u)*(1.8-0.3075)^2=2.875mA

ID,simulation

=2.259mA

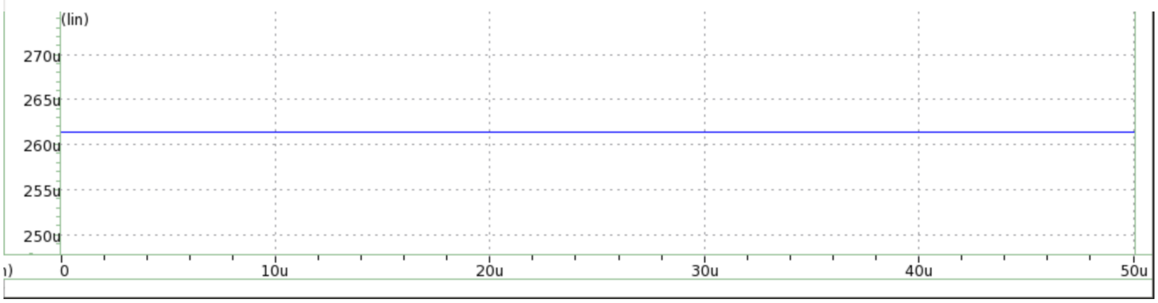
It is found that the ID,calculated and ID,simulation is almost the same. And a slight difference between them is because Hspice consider a lot of effect which we didn't consider in the formula ID=0.5UnCox(W/L)(VGS-VTh)^2.

```
Hw1_2_VGS=1.8V VDS=1.8V W/L=18u/1.8u
.option post
*ciruit
mm vd vg vs gnd n_18_mm  l=1.8u  w=18u AS="0.48u*18u" AD="0.48u*18u" PS="0.96u
+18u" PD="0.96u+18u"

*source
vdd vd 0 1.8
vgg vg 0 1.8
vss vs 0 0
*sim
.tran 1n 10m

.lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/
mm180_reg18_v124.lib" tt
.end
```

(b) VGS=0.8V, VDS=1.8V, W/L=18um/1.8um
ID,calculated=0.5*314.1/10000*(3.4515*10^-11)/(4.2*10^-9)*(18u/1.8u)*(0.8-0.3075)^2=0.313mA
ID,simulation=0.261.5mA

The difference between the calculation result and the simulation result is larger than the difference in part(a).However, this difference is still acceptable. Because the n_18_mm consider more than 40 parameter, and the calculated result only consider few parameter. Also, from High VGS to LOW VGS, The ID will be lower. It is because Iout (ID)= gm*VGS(Vin) in the small signal model.

```
Hw1_2_VGS=0.8V VDS=1.8V W/L=18u/1.8u
.option post
mm1 vd vg vs gnd n_18_mm l=1.8u w=18u AS="0.48u*18u" AD="0.48u*18u" PS="0.96u
+18u" PD="0.96u+18u"
*source
vd vd 0 1.8
vg vg 0 0.8
vsb vs 0 0
.tran 10n 50u
.lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/
mm180_reg18_v124.lib" tt
.end
```



(c) VGS=1.8V, VDS=1.8V, W/L=1.8um/0.18um
ID,calculated
=Vsat*W*Cox*(VGS-VTH)=5.2*10^4*1.8u*(3.4515*10^-11)/(4.2*10^-9)*(1.8-0.3075)=1.148mA
ID,simulation
=1.135mA

Using the formula ID=0.5UnCoxW/L*(VGS-VTH)^2 may get the same result as in part a. However, it is found that there's a big gap between the ID,simulation and the ID,calculation. Thus, it has to change different formula for this short channel effect. The formula ID=Vsat*W*Cox(VGS-VTH) is used. The short channel devices have to consider the velocity saturation, which will restrict our ID.

```
Hw1_2_VGS=1.8V VDS=1.8V W/L=1.8u/0.18u
.option post
mm1 vd vg vs gnd n_18_mm l=0.18u w=1.8u AS="0.48u*1.8u" AD="0.48u*1.8u"
PS="0.96u+1.8u" PD="0.96u+1.8u"
*source
vd vd 0 1.8
vg vg 0 1.8
vsc vs 0 0
.tran 10n 50u
.lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/
mm180_reg18_v124.lib" tt
.end
```

(d) VGS=0.8V, VDS=1.8V, W/L=1.8um/0.18um

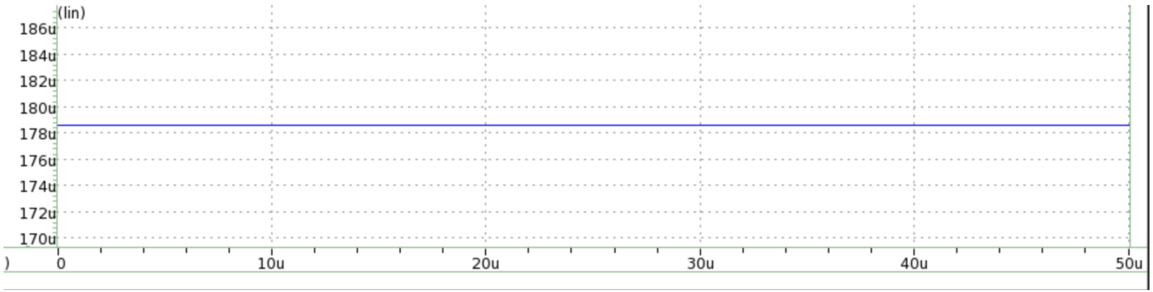
ID,calculated

=Vsat*W*Cox*(VGS-VTH)=5.2*10^4*1.8u*(3.4515*10^-11)/(4.2*10^-9)*(0.8-0.3075)=0.378mA

ID,simulation=0.178mA

This is similar as part c. When operating the short channel devices, the formula ID=0.5UnCox W/L(VGS-VTH)^2 is not longer suitable. Instead, it is more precious to use the formula ID=Vsat*W*Cox(VGS-VTH), which is due to the velocity saturation. And like the result changing from High VGS to LOW VGS, The ID will be lower. It is because Iout (ID)= gm*VGS(Vin) in the small signal model.

```
Hw1_2_VGS=0.8V VDS=1.8V W/L=1.8u/0.18u
.option post
mm1 vd vg vs gnd n_18_mm w=1.8u l=0.18u AS="0.48u*1.8u" AD="0.48u*1.8u"
PS="0.96u+1.8u" PD="0.96u+1.8u"
*source
vd vd 0 1.8
vg vg 0 0.8
vsd vs 0 0
.tran 10n 50u
.lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/
mm180_reg18_v124.lib" tt
.end
```



Lab2 format:

	W=18um, L=1.8um	W=1.8um, L=0.18um
VGS=1.8V, VDS=1.8V	ID,calculated =2.875mA ID,simulation =2.259mA	ID,calculated =1.148mA ID,simulation =1.135mA
VGS=0.8V, VDS=1.8V	ID,calculated =0.313mA ID,simulation =0.261.5mA	ID,calculated =0.378mA ID,simulation =0.178mA

The calculate and the illustrate is at each part above.

(3) Describe the observed channel-length modulation effect and velocity saturation effect from the I-V curves.(Blue curve W=1.8u L=0.18u, Red curve W=18u L=0.18u**)**

1.Hspice code:

Red curve long channel:

```
Hw1_3
.option post

*circuit
mm vd vg vs gnd n_18_mm  l=1.8u  w=18u AS="0.48u*18u" AD="0.48u*18u" PS="0.96u+18u"
PD="0.96u+18u"

*source
vdd vd gnd dd
vgg vg gnd 1.8
vss vs gnd 0

.dc dd 0 1.8 1m

.lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/mm180_reg18_v124.lib"
tt
.end
```

Blue curve short channel:

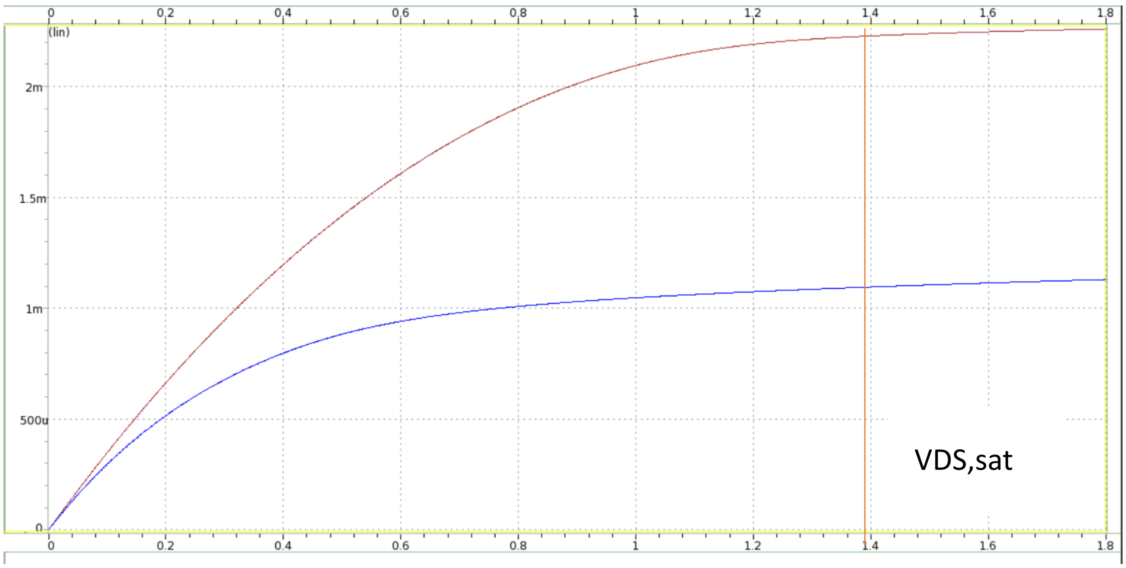
```
Hw1_33
.option post

*circuit
mm vd vg vs gnd n_18_mm  l=0.18u  w=1.8u AS="0.48u*1.8u" AD="0.48u*1.8u" PS="0.96u+1.8u"
PD="0.96u+1.8u"

*source
vdd vd gnd dd
vgg vg gnd 1.8
vss vs gnd 0

.dc dd 0 1.8 1m

.lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/mm180_reg18_v124.lib"
tt
.end
```

2.3. Simulation result and illustrate:

(4) channel-length modulation effect (Blue curve W=1.8u L=0.18u, Red curve W=18u L=0.18u**)**

Even when VDS>=VDS,sat, which means the transistor enters the saturation region, IDS still varies as VDS increase. This is due to the channel length modulation. When VDS getting bigger and bigger, the Leff will became shorter and shorter. Thus, the speed of the carriers going through the channel will be faster, that is, ID will still increase.

We observe that the effect of channel length modulation is more significant on the short channel device. This is because lambda is proportional to 1/L.



velocity saturation effect (Blue curve W=1.8u L=0.18u, Red curve W=18u L=0.18u**)**

The velocity saturation effect happens on the short channel device. It goes in the saturation region when VDS didn't reach VDS,sat. That is, Short channel devices increasing VDS may reach the velocity saturation before the transistor pinch off. Therefore, ID may approximate a constant at an early time. This result can be used to illustrate Lab1. and Lab 2. above. In Lab2. Part (c) and part(d), it shows us how this effect influence the ID so much.