

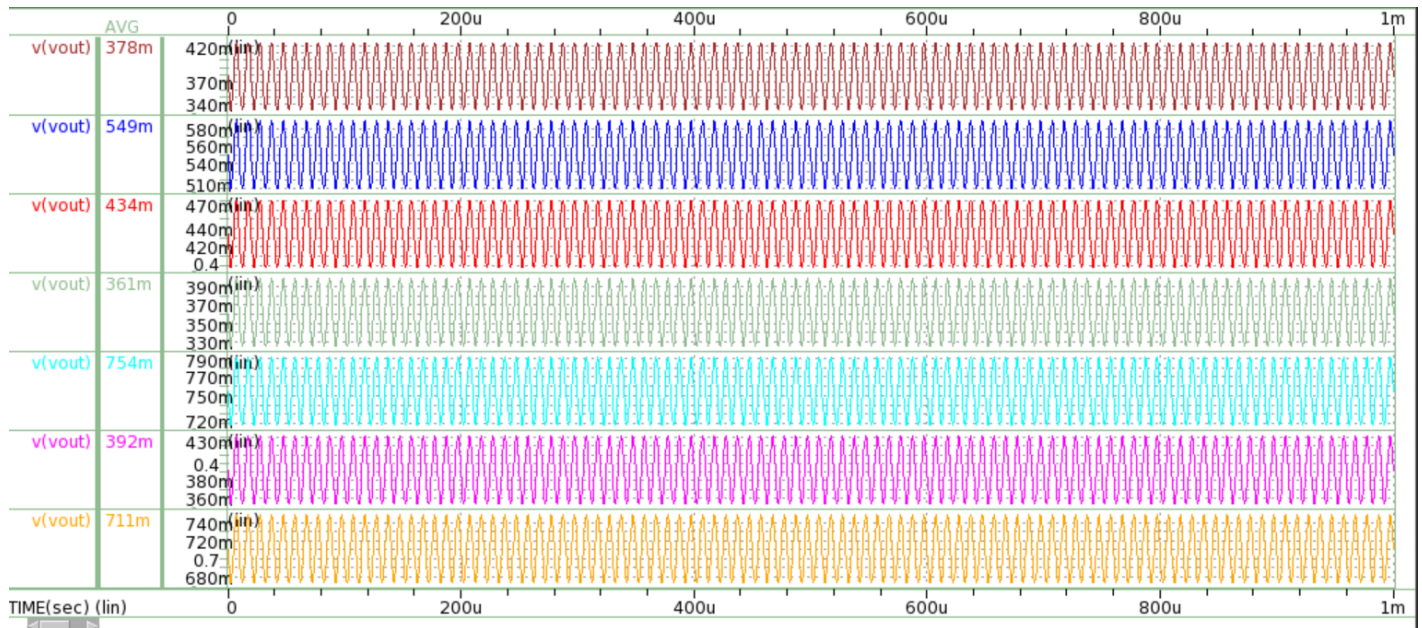
HSPICE Homework #2

Hw2.1

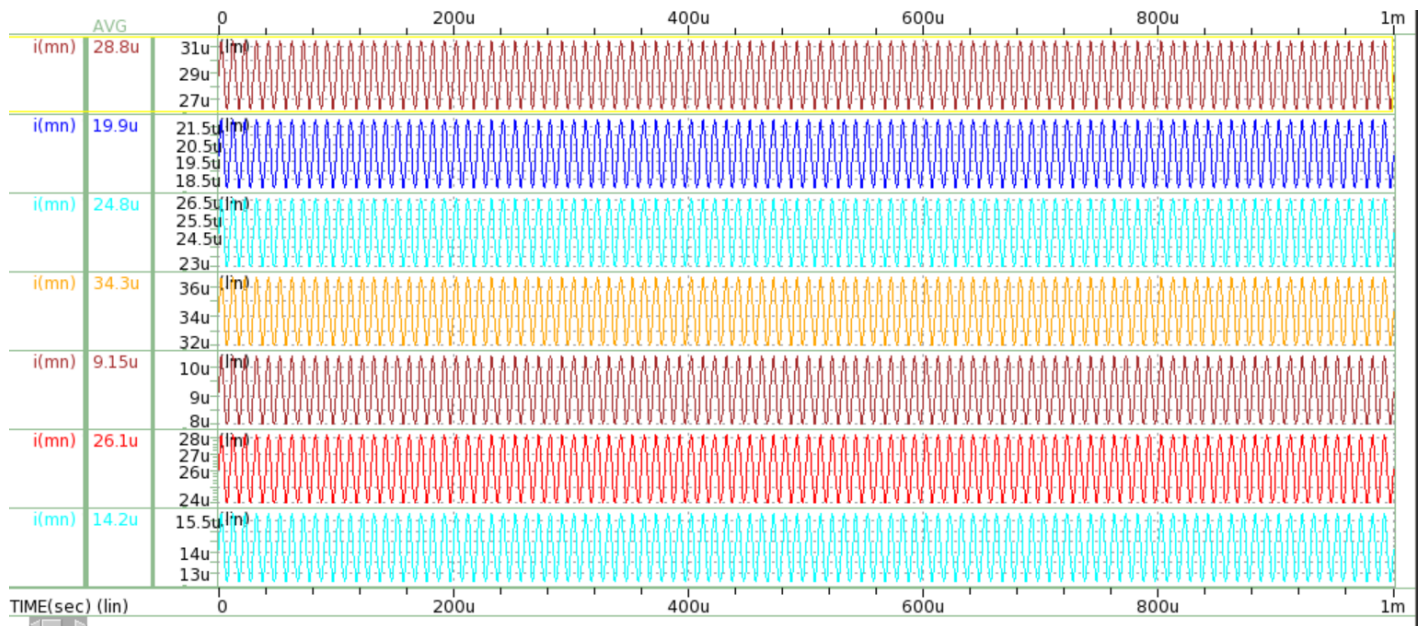
```
1  Hw2_1
2  .option post
3  .temp 25
4  *source
5  Vdd vdd gnd 1.8
6  vss vss gnd 0
7  vin vin gnd sin(0.6 0.01 100k)
8  *ckt
9  mn vout vin gnd gnd n_18_mm w=1.2u l=0.18u
10 mp vout vout vdd vdd p_18_mm w=1.5u l=1u
11
12 *sim
13 .print LV1(mn)
14 .tran 10n 1m
15 .tf V(vout) vin
16 .print cin=cap(vin) cout= cap(vout)
17
18 .lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/mm180_reg18_v124.lib" tt
19
20 .alter
21 mn vout vin gnd gnd n_18_mm w=3.6u l=0.54u
22
23 .alter
24 mn vout vin gnd gnd n_18_mm w=1.2u l=0.18u
25 .temp 75
26
27 .alter
28 .temp 25
29 .lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/mm180_reg18_v124.lib" ff
30
31 .alter
32 .lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/mm180_reg18_v124.lib" ss
33
34 .alter
35 .lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/mm180_reg18_v124.lib" fnsp
36
37 .alter
38 .lib "/RAID2/COURSE/AICIntro/AICIntro071/U18_model/U18_Spice_model/mm180_reg18_v124.lib" snfp
39
40 .end
41
```

The pictures below are all in the order as the chart.

Vout waveform:



Ids waveform:

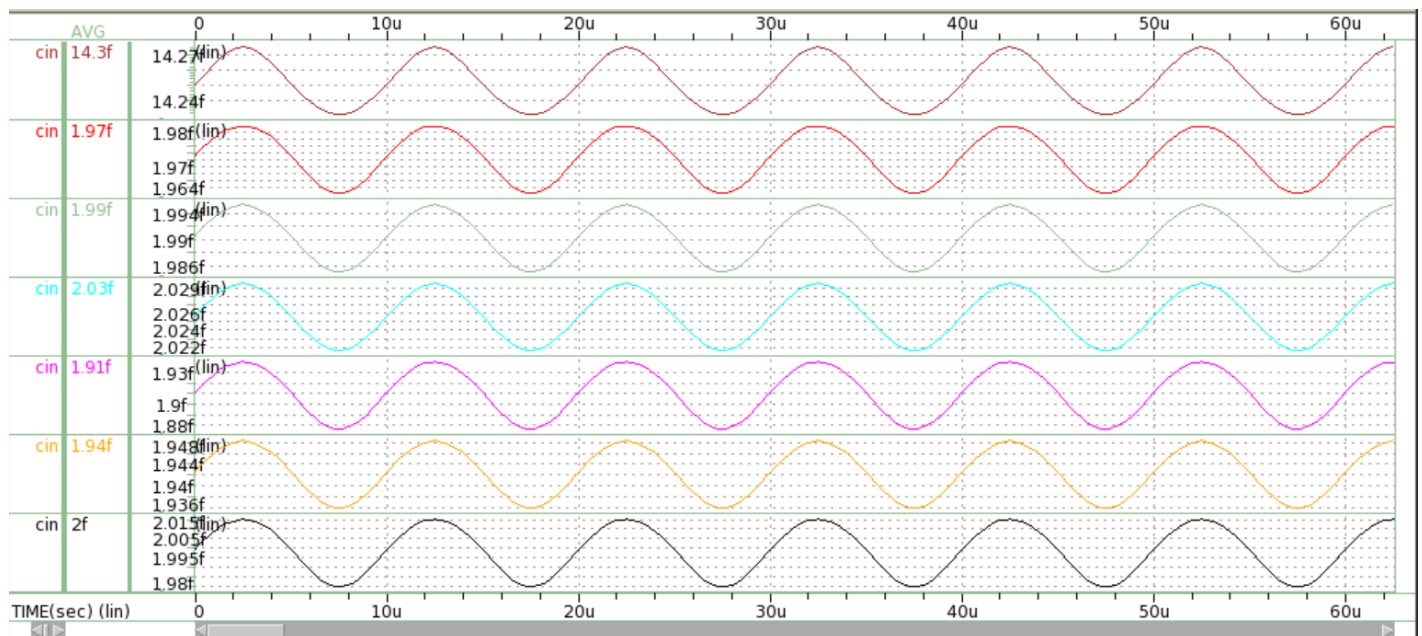


Small signal:

v(vout)/vin	=	-4.6039
input resistance at vin	=	1.000e+20
output resistance at v(vout)	=	15.8225k
v(vout)/vin	=	-4.0196
input resistance at vin	=	1.000e+20
output resistance at v(vout)	=	16.9394k
v(vout)/vin	=	-3.6654
input resistance at vin	=	1.000e+20
output resistance at v(vout)	=	15.4508k

$v(vout)/v_{in}$		=	-3.7296
input resistance at	v_{in}	=	1.000e+20
output resistance at $v(vout)$		=	11.4275k
$v(vout)/v_{in}$		=	-3.6566
input resistance at	v_{in}	=	1.000e+20
output resistance at $v(vout)$		=	26.7409k
$v(vout)/v_{in}$		=	-3.9386
input resistance at	v_{in}	=	1.000e+20
output resistance at $v(vout)$		=	14.1657k
$v(vout)/v_{in}$		=	-3.8254
input resistance at	v_{in}	=	1.000e+20
output resistance at $v(vout)$		=	20.2288k

Cin:



Cout:

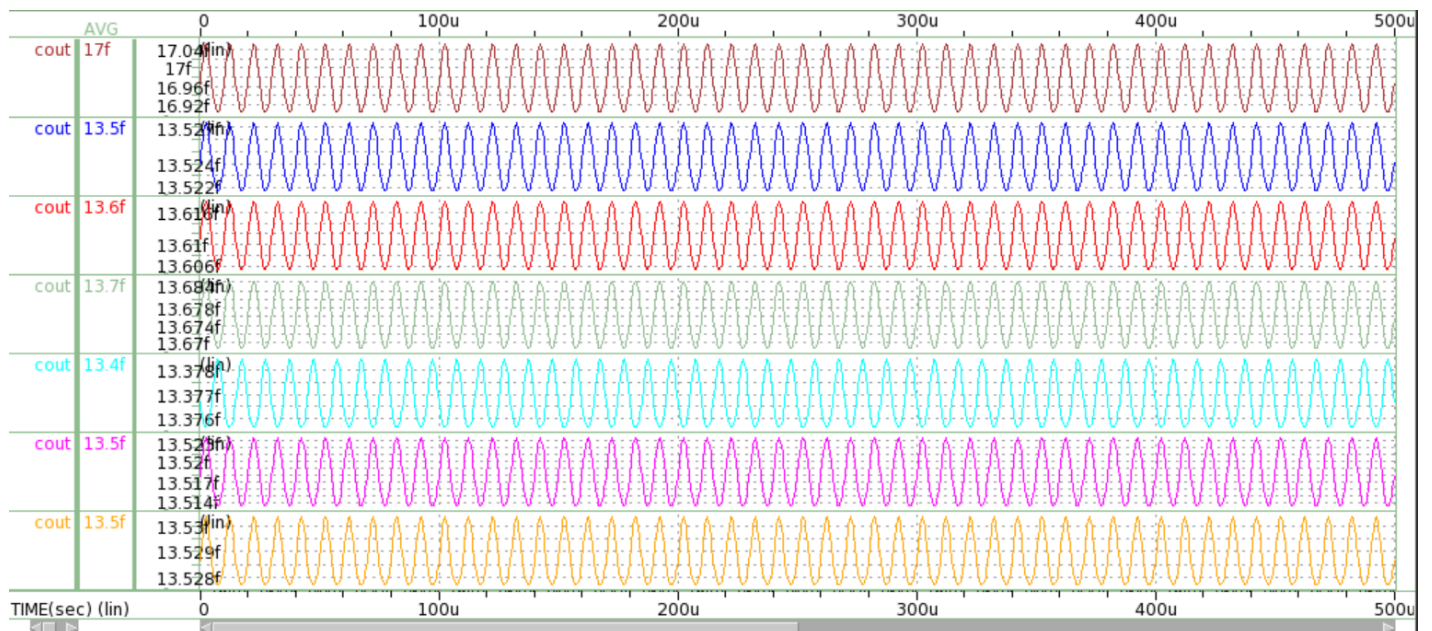


Table: NMOS common-source amplifier

Corner	Temp (°C)	Circuit	Vout (V)	Ids (mA)	DC gain (V/V)	Rout (Ω)	Cin (F)	Cout (F)
TT	25	Fig. 2	378m	0.0288	-4.604	15.823k	14.3f	17f
TT	25	Fig. 1	549m	0.0199	-4.019	16.939k	1.97f	13.5f
TT	75	Fig. 1	434m	0.0248	-3.665	15.451k	1.99f	13.6f
FF	25	Fig. 1	361m	0.0343	-3.73	11.428k	2.03f	13.7f
SS	25	Fig. 1	754m	0.00915	-3.657	26.741k	1.91f	13.4f
FnSp	25	Fig. 1	392m	0.0261	-3.939	14.166k	1.94f	13.5f
SnFp	25	Fig. 1	711m	0.0142	-3.825	20.229k	2f	13.5f

Hw2.2

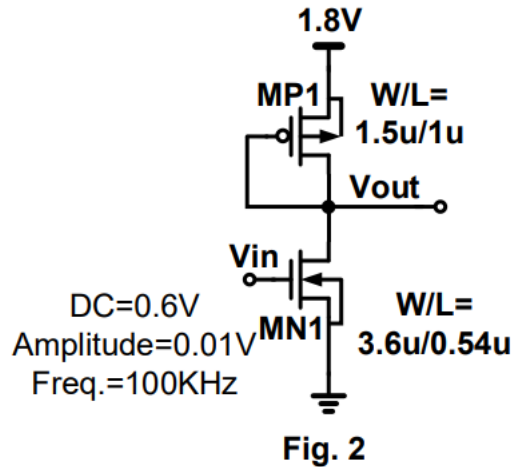
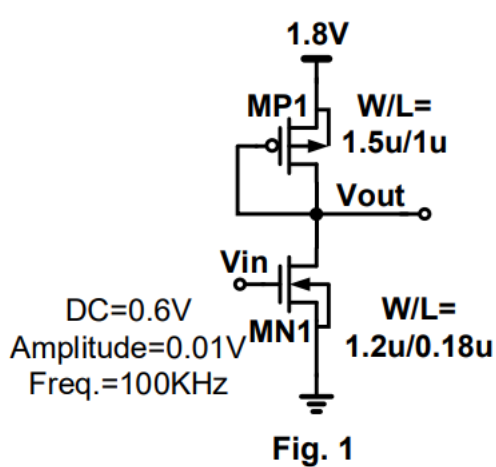


Figure 1. $W/L = 1.2\mu/0.18\mu = 6.6667$

**** **small**-signal transfer characteristics

```

v(vout)/vin          = -4.0196
input resistance at  vin = 1.000e+20
output resistance at v(vout) = 16.9394k

```

Figure 2. $W/L = 3.6\mu/0.54\mu = 6.6667$

**** **small**-signal transfer characteristics

```

v(vout)/vin          = -4.6039
input resistance at  vin = 1.000e+20
output resistance at v(vout) = 15.8225k

```

Rout analysis:

The picture above shows the output resistance of Figure1 is larger than Figure2. Some reasons determine this result. First, the Rout of both circuits is equal to $\frac{1}{g_{mp}} // r_{op} // r_{on}$.

And we know g_{mp} is proportional to I_D . Due to the velocity saturation on short channel devices, I_D will prematurely saturate, which causes I_D much smaller than expected. Thus, the smaller g_{mp} and I_D are, the larger the Rout will be.

Also, the r_{on} is equal to $\frac{1}{\lambda I_D}$. Thus, As I_D decreases, r_{on} will also get larger. What's more, λ is proportional to $\frac{1}{L}$, which will cause a **larger Rout when the Length is small**.

Gain analysis:

The two figures show the gain of figure2 is larger than the figure1. Recall that we just mention the velocity saturation above, which will let I_D be smaller on the short-channel devices. Once I_D gets smaller, g_{mn} will also get smaller. This will **result in a smaller gain**.

Hw2.3

Figure1 temp25 (ID=19.9uA)

```
v(vout)/vin          = -4.0196
input resistance at   vin      = 1.000e+20
output resistance at v(vout)   = 16.9394k

gm      47.0712u    237.4156u
gds     677.9233n    11.2949u
```

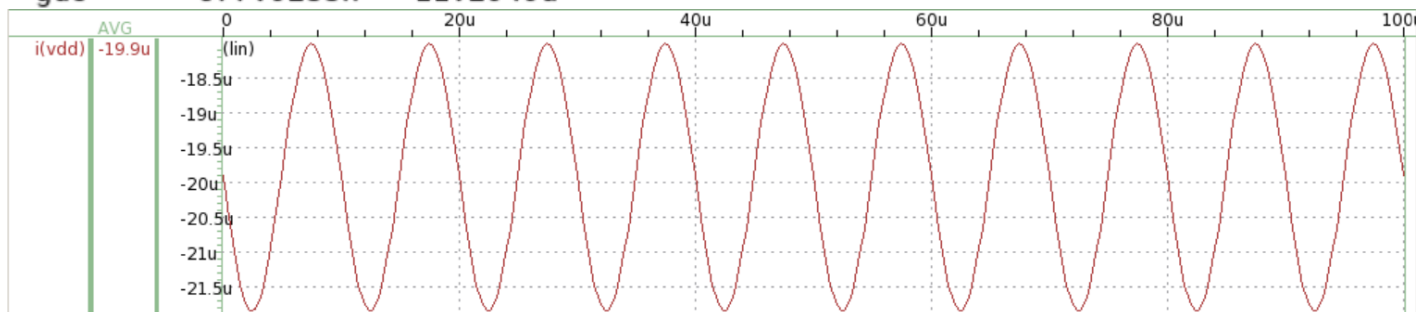
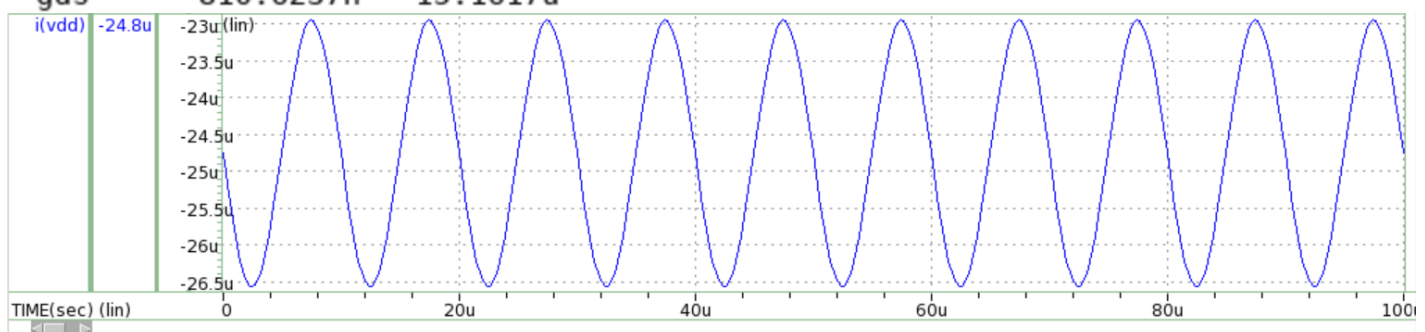
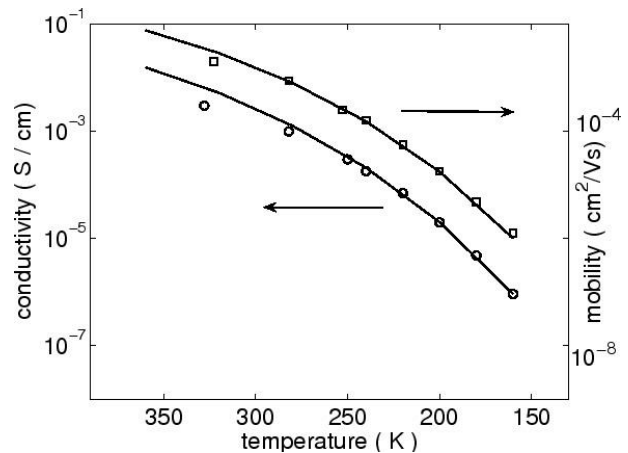
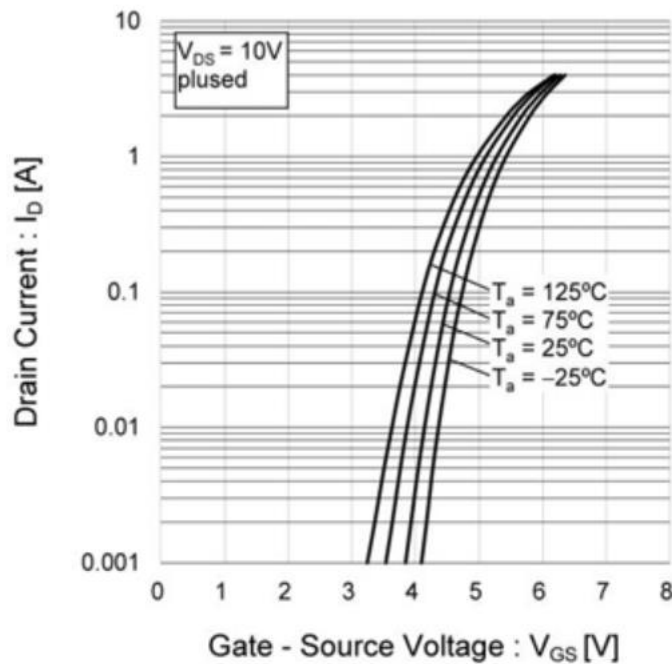


Figure1 temp 75 (ID=24.8uA)

```
v(vout)/vin          = -3.6654
input resistance at   vin      = 1.000e+20
output resistance at v(vout)   = 15.4508k

gm      48.7617u    237.3561u
gds     810.6237n    15.1617u
```





Rout analysis:

The left picture shows that if V_{GS} is a constant, I_D will increase as temperature increases. The reason is that $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$, and the right picture shows that as temperature increases, μ_n will increase too. Thus, we can know that if temperature increases, I_D will increase.

We know that $r_o = 1/g_{ds}$. The result above shows that g_{ds} increase when the temperature increases from 25 degrees to 75 degrees, which implies r_o decrease.

It is known that $R_{out} = \frac{1}{g_{mp}} // r_{op} // r_{on}$, and r_{on} and r_{op} are equal to $\frac{1}{\lambda I_D}$. Thus, as I_D increase, **R_{out} will get smaller**. This is totally the same as the result in hspice.

Gain analysis:

It is proved that a higher temperature results in a lower R_{out} in this circuit. And it is known that the gain formula is $A_v = -g_{mn} * R_{out}$. From the result above, it shows that g_m didn't change obviously due to the cancelation of V_{th} and μ_n . Therefore, if R_{out} gets smaller, **A_v gain will also get smaller**. This deduction exactly accords with the Hspice result.