FSA0M
UMC 0.18 µm Mixed-Mode and RFCMOS Process

MEMAKER (200901.2.1)

Release Note
Rev.: 200901.2.1v1.0
Issue Date: December 2009

DATABASE REVISION HISTORY

Version	Release Date	Revision Note
200802.2.1	August 2008	• Terminated the model generation process by clicking the “Cancel” button • Changed the GUI style of the memory type selection from the radio button to the combo box • Fixed the syntax errors of the single-port SRAM VHDL models when the byte number is larger than 1 • Enhanced the power conditions of all SRAM clock pins (CK)
200901.1.1	April 2009	• Upgraded to version 200901.1.1 • Removed the gate count information from the data sheets
200901.2.1	December 2009	• Changed the minimum pulse width, minimum period, and the internal power of the clock pin from a single value to values of using a mapping table in the Synopsys Liberty model • Assigned the DO signal to unknown (x) when the specific address is out of range in the Verilog model • Changed the power consumption data from a single value to values of using a mapping table in the data sheet

Printed in Taiwan 2009

Faraday Technology Corporation
No. 5, Li-Hsin Road III, Hsinchu Science Park, Hsinchu City, Taiwan 300, R.O.C.

Faraday's home page can be found at:
http://www.faraday-tech.com

TABLE OF CONTENTS

1 Description

This release note contains the descriptions of new features of the Faraday FSA0M memory generator, Memaker. This release note also contains the supported model descriptions for both the front-end and back-end designs.

2 Quick Reference Specification

Process technology	UMC 0.18 µm Mixed-Mode and RFCMOS process	
Version	200901.2.1	
UMC process specifications	Spec. name	Version
	FSA0M_A_SJ (Synchronous dual-port RAM)	
	G-02-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC-EDR	2.0.P1
	G-03-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC-TLR	2.10.P1
	G-03L-GENERATION18-TLR/LATCH_UP	2.0.P1
	G-03DS-GENERATION15_ABOVE-METAL-TLR/DUMMY_SLOT	1.3.P1
	G-03D-GENERATION15_ABOVE-DIFFUSION-TLR/DUMMY	1.2.P1
	G-03D-GENERATION15_ABOVE-POLY1-TLR/DUMMY	1.4.P1
	G-03BO-GENERATION18-OPC_BLOCK-TLR/BOUNDARY	2.0.P1
	G-04-MIXED_MODE/RFCMOS18-1P6M-MMC-INTERCAP	1.2.P1
	G-05-MIXED_MODE/RFCMOS18-1.8V/3.3V-TWIN_WELL/MMC-SPICE-8C	1.5.P3
	G-06-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC-MASKTOOL-8C	2.6.P1
	G-06LMT-GENERATION18-LAYER_MAPPING_TABLE	2.10.P1
	G-DF-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC/CALIBRE-DRC	2.9.P2
	G-DF-MIXED_MODE/RFCMOS18-1P6M-MMC/TOP_METAL8.6K/XRC-LPE	1.2.P3
	G-DF-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC/CALIBRE-LVS	2.0.P2
	G-1C-LOGIC18-UMC/DPSRAM10.2GENERICII-CELL	S.2.P1
	FSA0M_A_SU (Synchronous single-port RAM)	
	G-02-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC-EDR	2.0.P1
	G-03-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC-TLR	2.10.P1
	G-03L-GENERATION18-TLR/LATCH_UP	2.0.P1
	G-03DS-GENERATION15_ABOVE-METAL-TLR/DUMMY_SLOT	1.3.P1
	G-03D-GENERATION15_ABOVE-DIFFUSION-TLR/DUMMY	1.2.P1
	G-03D-GENERATION15_ABOVE-POLY1-TLR/DUMMY	1.4.P1
	G-03BO-GENERATION18-OPC_BLOCK-TLR/BOUNDARY	2.0.P1
	G-04-MIXED_MODE/RFCMOS18-1P6M-MMC-INTERCAP	1.2.P1
	G-05-MIXED_MODE/RFCMOS18-1.8V/3.3V-TWIN_WELL/MMC-SPICE-8C	1.5.P3
	G-06-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC-MASKTOOL-8C	2.6.P1
	G-06LMT-GENERATION18-LAYER_MAPPING_TABLE	2.10.P1
	G-DF-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC/CALIBRE-DRC	2.9.P2
	G-DF-MIXED_MODE/RFCMOS18-1P6M-MMC/TOP_METAL8.6K/XRC-LPE	1.2.P3
	G-DF-MIXED_MODE/RFCMOS18-1.8V/3.3V-1P6M-MMC/CALIBRE-LVS	2.0.P2
	G-1C-LOGIC18-UMC/6TSRAM4.0-CELL	G.2.P2

Design kit models supported	• Verilog simulation model • VHDL simulation model • Synopsys simulation model • Mentor FastScan model • Mentor MBIST model • TetraMAX ATPG model • Memory Definition Table (MDT) model
Tape-out kit models supported	• LEF P & R model • Layout GDSII • LVS netlist
Supported platforms	• Solaris: SunOS 5.8 or later • Linux 2.4.21 or later • Linux x86_64 (AMD64) with 64-bit core 2.4.21 or later
Memory types	• Synchronous dual-port RAM (FSA0M_A_SJ) • Synchronous single-port RAM (FSA0M_A_SU)
Documents and files	• Memaker data sheet • Memaker user guide • Memaker overview • Memaker environment source file • Memaker release note

3 Supported Memory Types

The Faraday FSA0M memaker consists of the following memory types:

- Synchronous dual-port RAM (FSA0M_A_SJ)
- Synchronous single-port RAM (FSA0M_A_SU)

The memory types are used in the chip logic design. These memories are verified with the UMC 0.18 µm Mixed-Mode and RFCMOS process design rules.

Please refer to the following table for the release status of each type:

Memory Type	Design Kit	Tape-out Kit
FSA0M_A_SJ	Yes	Yes
FSA0M_A_SU	Yes	Yes

Note: Please refer to Chapter 9 for detailed information about the package types.

4 Memory Design Kit Models

The Faraday FSA0M Memaker supports the synthesis and simulation models for project designs at the front-end stage as well as the P & R models for project designs at the back-end stage.

- Synopsys synthesis model

  This synthesis model is used for timing analysis with PrimeTime, power analysis with DesignPower, and conducting the internal scan synthesis with the DFT compiler.
- Verilog and VHDL simulation models

  These simulation models are used for the Verilog timing simulations.
- FastScan and MBIST models

  These models are used for the ATPG and MBIST simulations.
- TetraMAX ATPG model

  This model is used to define the RAM or ROM behavior of the ATPG usage.
- MDT (Memory Definition Table) model

  This model is used in Novas Verdi to compute the content of the memory block during debugging.
- P & R model

  This model is used for P & R with the Cadence Silicon Ensemble tool.

5 Document Names

5.1 Application Documents

The Faraday FSA0M Memaker provides a complete set of supporting documents, including:

- Faraday FSA0M Memaker Release Note
  The release note contains the descriptions of the latest enhancements and improvements of the Faraday FSA0M Memaker. It also contains the latest model features as well as all known problems and the corresponding solutions for both the front-end and back-end model designs.
- Faraday Memaker User Guide
  The user guide describes how to set up the execution environment and save the license file. It will outline all the steps required for installing the Faraday Memaker and operating the program.
- Faraday FSA0M Memaker Overview
  The overview describes the features and timing diagrams of each memory type within the Faraday FSA0M Memaker.

Each document can be found in Memaker with the "Help" pull-down menu or can be found in the following path:

"<install_path>/ftclib/EXE/memaker.package/doc"

5.2 Environment Source File

The environment source file can be found in the following path:

"<install_path>/ftclib/memaker.env"

File name: "memaker.env"

File version: 1.0

This environment source file defines the FTC environment. After installation, please proceed to edit the install paths by sourcing the environment source file.

Example:

The install path = "/home"

Please replace "setenv FTC your_install_path/ftclib" with "setenv FTC /home/ftclib."

6 Known Bugs and Workarounds

200802.2.1

- New features
  - Terminated the model generation process by clicking the “Cancel” button
  - Changed the GUI style of the memory type selection from the radio button to the combo box
  - Enhanced the power conditions of all SRAM clock pins (CK)
- Bug fixed

  Fixed the syntax errors of the single-port SRAM VHDL models when the byte number is larger than 1.
- Backward incompatibility

Please update the byte-write single-port SRAM VHDL models and all SRAM Liberty models.

200901.1.1

- New features
  - Upgraded to version 200901.1.1
  - Removed the gate count information from the data sheets
- Bug fixed

  N/A
- Backward incompatibility

  N/A

200901.2.1

- New features
  - Changed the minimum pulse width, minimum period, and the internal power of the clock pin from a single value to values of using a mapping table in the Synopsys Liberty model
  - Assigned the DO signal to unknown (x) when the specified address is out of range in the Verilog model
  - Changed the power consumption data from a single value to values of using a mapping table in the data sheet
- Bug fixed

  N/A
- Backward incompatibility

  Please update your Verilog and Synopsys Liberty models

7 Summary of UMC DRC/LVS Deck

UMC DRC Command Files

For FSA0M_A_SJ (Synchronous dual-port RAM):

Spec. Name	Version
G-DF-MIXED_MODE_RFCMOS18-1.8V-3.3V-1P3M_4M_5M_6M-MMC-Calibre-drc	2.10-P1
umc_ant_0.18um_Metal5_calibre	1.0-P3
G-DF-GENERATION18-ESD-Calibre-drc	2.0-P2
G-DF-GENERATION18-OPC_BLOCK-BOUNDARY-CALIBRE-DRC	2.0-P1

Please waive the following DRC errors:

The die corner rule must verify the whole chip with the seal ring; the IP level check is not necessary.

- 6Ab.M1, 6Ab.M2, 6Ab.M3, 6Ab.M4, 6Ab.M5, and 6Ab.M6

The mask house will add a dummy metal layer; do not need to check these rules.

- 4.21F, 4.23F, 4.21G, and 4.23E

For FSA0M_A_SU (Synchronous single-port RAM):

Spec. Name	Version
G-DF-MIXED_MODE_RFCMOS18-1.8V-3.3V-1P3M_4M_5M_6M-MMC-Calibre-drc	2.10-P1
umc_ant_0.18um_Metal5_calibre	1.0-P3
G-DF-GENERATION18-ESD-Calibre-drc	2.0-P2
G-DF-GENERATION18-OPC_BLOCK-BOUNDARY-CALIBRE-DRC	2.0-P1

Please waive the following DRC errors:

This rule only applies to the chip check.

- NOTICE_IODI

This rule only applies to the chip check.

- 4.20F, 4.22F, 4.22G, 4.31E, and 4.31F

The die corner rule must verify the whole chip with the seal ring; do not need to check the IP level.

- 6Bb.ME1, 6Bb.ME2, 6Bb.ME3, and 6Bb.ME4

There is no SEALRMARK in the GDS file. It is only the recommended rule

- 5.NOTICE1

UMC LVS Command File

Spec. Name	Version
G-DF-MIXED_MODE_RFCMOS18-1_8V_3_3V-1P6M-MMC_CALIBRE-LVS	2_0-P3

Calibre LVS result: Passed

8 EDA Tool View

Synthesis Tool	Version[1]
Synopsys Library Compiler	200809-sp3
Simulation Tool	**Version[1]**
Cadence Verilog_XL	6.2
Mentor ModelSim (VHDL)	5.8e
Mentor MBISTArchitect	8.2006_4.10
Synopsys TetraMAX	2004.06
P & R Tool	**Version[1]**
SoC Encounter (LEF)	7.1.s219
Verification Tool	**Version[1]**
Mentor Calibre	2009.3_15
Novas Verdi	200804v2

[1] Each tool only applies to the very version cited in this table.

9 Package Information

Package Name	Deliverable Name	Description
Design kit	Synthesis model	Synopsys Liberty model
	Simulation models	Verilog model
		Verilog-HDL model
	ATPG model	Mentor FastScan model
	MBIST model	Mentor Architect MBIST model
	TetraMAX model	Synopsys TetraMAX model
	MDT model	Novas Verdi MDT behavior model
	P & R physical model	Cadence LEF P & R model
Tape-out kit	Netlist	LVS netlist
	Physical layout	GDSII

10 Contact Information

- Help Desk on e-Service

  Faraday offers an-around-the clock web help desk. This service provides a solid communication flow for your requests to our qualified IP service teams in either HQ or the USA. The help desk tracks and logs all communications so that your opinions can be readily reviewed. Users can enter the requests by accessing the faraday website at http://freelibrary.faraday-tech.com.

- USA and Europe Contact Information

  E-mail: IPsales@faraday-usa.com

- Asia Contact Information

  E-mail: IPsales@faraday-tech.com

11 Ordering Information

To download the database, please visit the Faraday website at:

http://freelibrary.faraday-tech.com

Procedures:

- To obtain the Faraday design kit data:
  1. Sign the Non-Disclosure Agreement (NDA) online.
  2. Receive a user account and password from Faraday within two working days.
  3. Download the design kit database.
  4. Download the license file to initiate Memaker.

- To obtain the Faraday tape-out kit data:
  1. Contact our IP sales representatives.
  2. Sign an agreement.
  3. Receive the license update from Faraday within two working days.
  4. Download the license file to generate the related back-end data.

DOCUMENT REVISION HISTORY

FSA0M Memaker Release Note

Date	Rev.	From	To
Dec. 2009	200901.2.1v1.0	-	Original