Abstract Interpretation for Code Analysis and Verification

(Week 9)

Yulei Sui

School of Computer Science and Engineering

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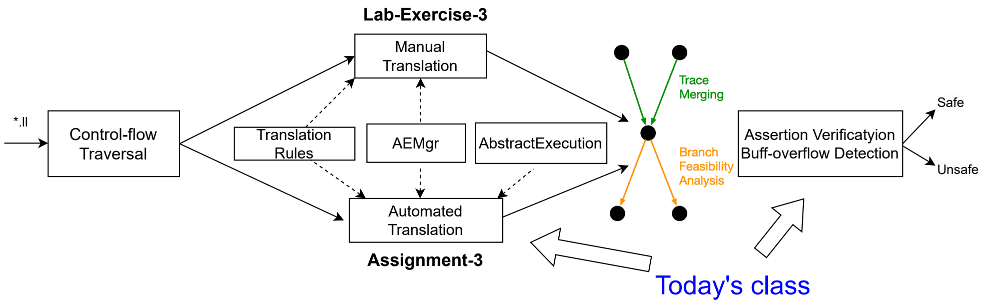
Today's class



Topological Order

Analysis Order of Nodes on Control-Flow Graph

? How to analyze a program **free of loop**?

✓ Analyze each node **once** adhering to the **topological order** on the acyclic control-flow graph of the program.

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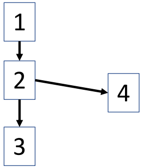
A **topological order** of a graph $G(V, E)$ is a linear ordering of its nodes such that for every directed edge $a \rightarrow b$, node a always precedes node b in the ordering.

- Must be a **direct acyclic graph** (DAG) and has at least one topo ordering.
- The ordering respects the **direction of edges**.

Example of topological order:



acyclic graph G

1 2 3 4 ✓

1 2 4 3 ✓

1 3 2 4 ✗

Valid/invalid topological order

How About Analyzing Loops?

- **Topological Order** can only be used for directed acyclic graphs (DAGs).
- **Weak Topological Order (WTO)** is a relaxation of the more stringent topological order for graphs with loops.
  - **Cycles Permitted**: allows for cycles within the graph.
  - **Hierarchical Decomposition**: A graph is decomposed into a hierarchical structure where each node or a strongly connected component (SCC) can contain subnodes.
  - **Weak Topological Order or Partial Order**: In a WTO, nodes and SCCs are arranged in a partial order (not enumerating possible infinite loop paths). This order respects the dependencies in a way that allows for iterative analysis.
  - We will practice loop handling using WTO in `Assignment-3`. Function recursions will not be handled in this Assignment.

Weak Topological Order

Analysis Order of Nodes on Control-Flow Graph

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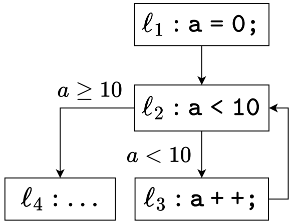
✓ We can analyze a program containing loops adhering to the **weak topological order** (WTO) on its control flow graph.

What is the weak topological order?



Control Flow Graph

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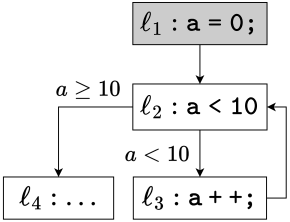
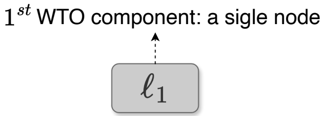


Control Flow Graph



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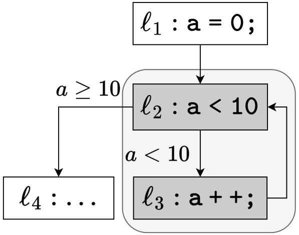

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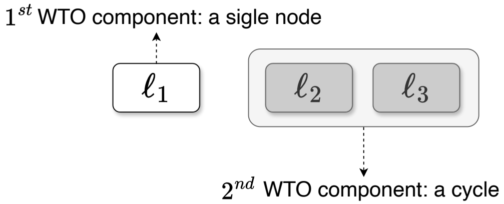

1^{st} WTO component: a sigle node
ℓ_1
ℓ_2
ℓ_3
2^{nd} WTO component: a cycle

Weak Topological Order

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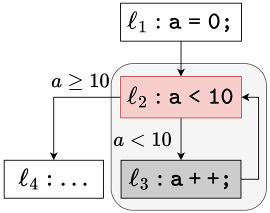
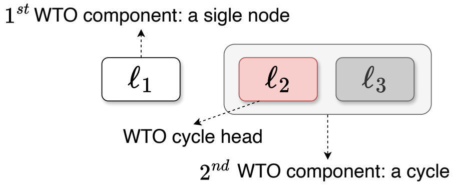


Control Flow Graph



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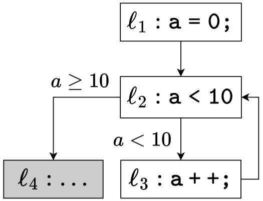

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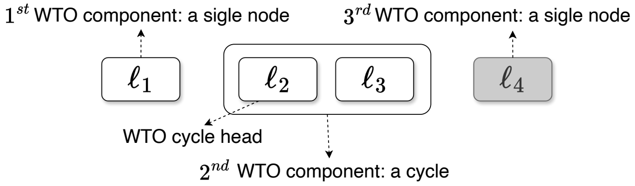

1^{st} WTO component: a sigle node
3^{rd} WTO component: a sigle node
ℓ_1
ℓ_2
ℓ_3
ℓ_4
WTO cycle head
2^{nd} WTO component: a cycle

Weak Topological Order

Analysis Order of Nodes on Control-Flow Graph

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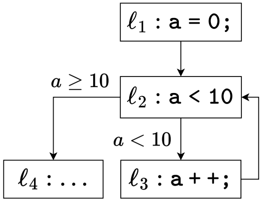
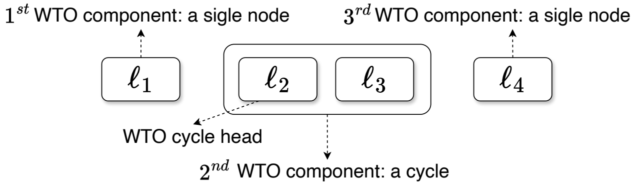


Control Flow Graph

What is the weak topological order?



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ℓ_1
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WTO cycle head
2nd WTO component: a cycle

Analyze each node following the WTO

Analyze ℓ_1 ⇨ Repeat: analyze ℓ_2 and ℓ_3 ⇨ Analyze ℓ_4

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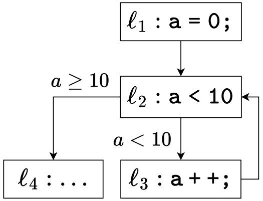

Control Flow Graph

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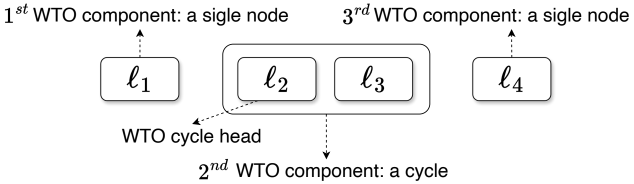

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Perform widening when analyzing the cycle heads (i.e., ℓ_2)

WTO, Widening and Narrowing

Why Weak Topological Order?

- Handling cyclic dependencies
- Efficient fixed-point computation

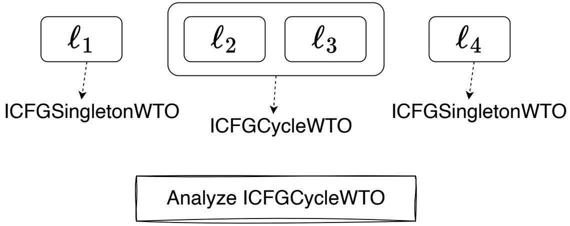
Why Widening?

- Over-approximation
- Prevent non-termination

Why Narrowing?

- Refine precision after widening converges
- The specific conditions or constraints used for narrowing:
    - Loop exit conditions (this course)
    - Type constraints (8-bit integer ranging from [-128, 127])
    - Bounds from arithmetic operations If `x = y + z`, and $y \in [1, 5]$ and $z \in [2, 3]$, then $x \in [3, 8]$. If widening gives [1, 10], narrowing can refine this to [3, 8].
    - User-specification (assertions and guard conditions)

Widening and Narrowing



Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        if $cur\_iter \geq Options :: WidenDelay()$ then
            $prev\_head\_state := postAbsTrace[cycle\_head]$;
            handleICFGNode(cycle→head());
            $cur\_head\_state := postAbsTrace[cycle\_head]$;
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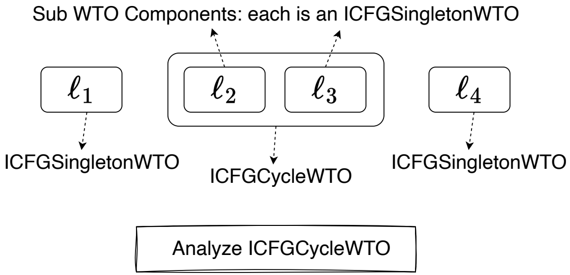
Widening and Narrowing



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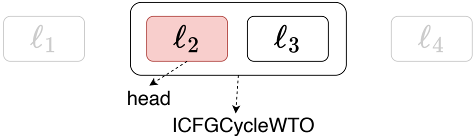
Weak Topological Order



Get ICFGCycleWTO head ℓ_2

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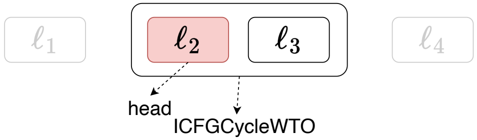
Weak Topological Order



Handle ICFGCycleWTO head ℓ_2

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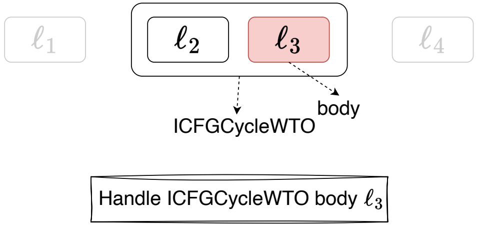
Widening and Narrowing



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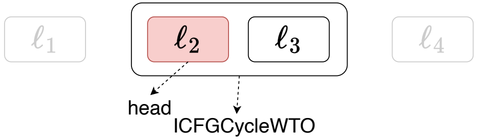
Note: getIWTOcomponents returns Cycle WTO body, i.e., ℓ_3

Widening and Narrowing



When $cur\_iter \geq Options :: WidenDelay()$
perform widening on ℓ_2

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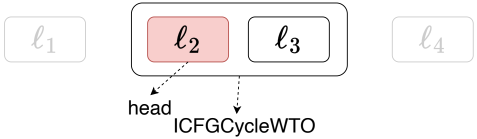
Widening and Narrowing



Widening reaches a fixpoint

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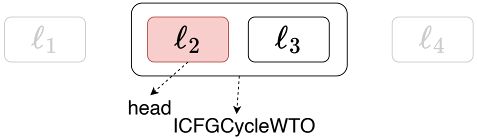
Widening and Narrowing



Perform narrowing on ℓ_2

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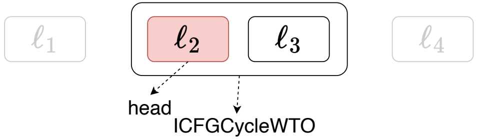
Widening and Narrowing



Narrowing reaches a fixpoint, Finish!

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Abstract Interpretation on SVFIR

Week 9

Yulei Sui

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Abstract Interpretation on Pointer-Free SVFIR

Interval Domain

- For simplicity, let's first consider abstract execution on a pointer-free language.
- This means there are no operations for memory allocation (like $\texttt{p} = \texttt{alloc}_{\texttt{o}}$) or for indirect memory accesses (such as `p = *q` or `*p = q`).
- Here are the pointer-free SVFSTMTs and their C-like forms:

SVFSTMT	**C-Like form**
CONSSTMT	$\ell : \texttt{p} = \texttt{c}$
COPYSTMT	$\ell : \texttt{p} = \texttt{q}$
BINARYSTMT	$\ell : \texttt{r} = \texttt{p} \otimes \texttt{q}$
PHISTMT	$\ell : \texttt{r} = \texttt{phi}(\texttt{p}_1, \texttt{p}_2, \ldots, \texttt{p}_n)$
SEQUENCE	$\ell_1 ; \ell_2$
BRANCHSTMT	ℓ_1 : if$(x < c)$ then ℓ_2 else ℓ_3

Abstract Interpretation on Pointer-Free SVFIR

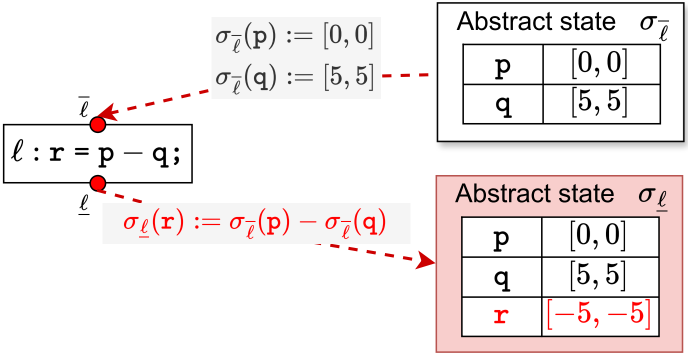
Interval Domain

Let’s use the *Interval* abstract domain to update σ based on the following rules for different SVFSTMT:

SVFSTMT	**C-Like form**	**Abstract Execution Rule**
CONSSTMT	$\ell : \mathtt{p} = \mathtt{c}$	$\sigma_{\underline{\ell}}(\mathtt{p}) := [\mathtt{c}, \mathtt{c}]$
COPYSTMT	$\ell : \mathtt{p} = \mathtt{q}$	$\sigma_{\underline{\ell}}(\mathtt{p}) := \sigma_{\overline{\ell}}(\mathtt{q})$
BINARYSTMT	$\ell : \mathtt{r} = \mathtt{p} \otimes \mathtt{q}$	$\sigma_{\underline{\ell}}(r) := \sigma_{\overline{\ell}}(p) \hat{\otimes} \sigma_{\overline{\ell}}(q)$
PHISTMT	$\ell : \mathtt{r} = \mathtt{phi}(\mathtt{p}_1, \mathtt{p}_2, \ldots, \mathtt{p}_n)$	$\sigma_{\underline{\ell}}(r) := \bigsqcup_{i=1}^{n} \sigma_{\overline{\ell}}(p_i)$
SEQUENCE	$\ell_1 ; \ell_2$	$\forall v \in \mathbb{V}, \sigma_{\overline{\ell_2}}(v) \sqsupseteq \sigma_{\underline{\ell_1}}(v)$
BRANCHSTMT	ℓ_1 : if$(x < c)$ then ℓ_2 else ℓ_3	$\sigma_{\overline{\ell_2}}(x) := \sigma_{\underline{\ell_1}}(x) \sqcap [-\infty, c-1],\ \text{if } \sigma_{\underline{\ell_1}}(x) \sqcap [-\infty, c-1] \neq \bot$ $\sigma_{\overline{\ell_3}}(x) := \sigma_{\underline{\ell_1}}(x) \sqcap [c, +\infty],\ \text{if } \sigma_{\underline{\ell_1}}(x) \sqcap [c, +\infty] \neq \bot$

Abstract Interpretation on BINARYSTMT

SVFSTMT	C-Like form	Abstract Execution Rule
BINARYSTMT	$\ell : \mathtt{r} = \mathtt{p} \otimes \mathtt{q}$	$\sigma_{\underline{\ell}}(r) := \sigma_{\overline{\ell}}(p) \hat{\otimes} \sigma_{\overline{\ell}}(q)$



$\sigma_{\overline{\ell}}(\mathtt{p}) := [0, 0]$
$\sigma_{\overline{\ell}}(\mathtt{q}) := [5, 5]$
$\overline{\ell}$
$\ell : \mathtt{r} = \mathtt{p} - \mathtt{q};$
$\underline{\ell}$
$\sigma_{\underline{\ell}}(\mathtt{r}) := \sigma_{\overline{\ell}}(\mathtt{p}) - \sigma_{\overline{\ell}}(\mathtt{q})$
Abstract state $\sigma_{\overline{\ell}}$
Abstract state $\sigma_{\underline{\ell}}$

Abstract state $\sigma_{\overline{\ell}}$

p	$[0, 0]$
q	$[5, 5]$

Abstract state $\sigma_{\underline{\ell}}$

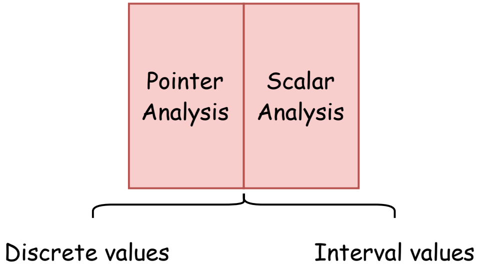
p	$[0, 0]$
q	$[5, 5]$
r	$[-5, -5]$

Abstract Interpretation in the Presence of Pointers

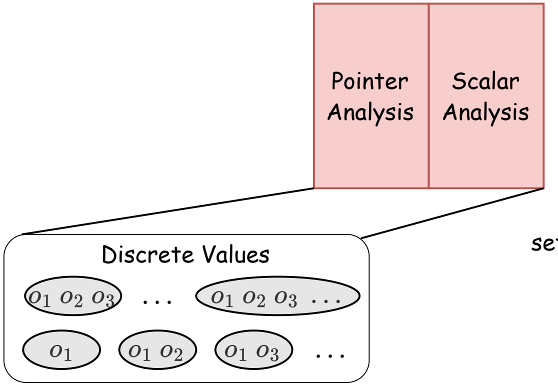
- SVFIR in the presence of pointers contain pointer-related statements including ADDRSTMT, GEPSTMT, LOADSTMT and STORESTMT.
- Abstract interpretation needs to be performed on **a combined domain of intervals and addresses**.

SVFSTMT	**C-Like form**
CONSSTMT	$\ell : \mathtt{p} = \mathtt{c}$
COPYSTMT	$\ell : \mathtt{p} = \mathtt{q}$
BINARYSTMT	$\ell : \mathtt{r} = \mathtt{p} \otimes \mathtt{q}$
PHISTMT	$\ell : \mathtt{r} = \mathtt{phi}(\mathtt{p}_1, \mathtt{p}_2, \ldots, \mathtt{p}_n)$
SEQUENCE	$\ell_1 ; \ell_2$
BRANCHSTMT	ℓ_1 : if($x < c$) then ℓ_2 else ℓ_3
ADDRSTMT	$\ell : \mathtt{p} = \mathtt{alloc}$
GEPSTMT	$\ell : \mathtt{p} = \&(\mathtt{q} \rightarrow \mathtt{i})$ or $\mathtt{p} = \&\mathtt{q}[\mathtt{i}]$
LOADSTMT	$\ell : \mathtt{p} = *\mathtt{q}$
STORESTMT	$\ell : *\mathtt{p} = \mathtt{q}$

Combined Analysis



Combined Analysis Using Discrete Values



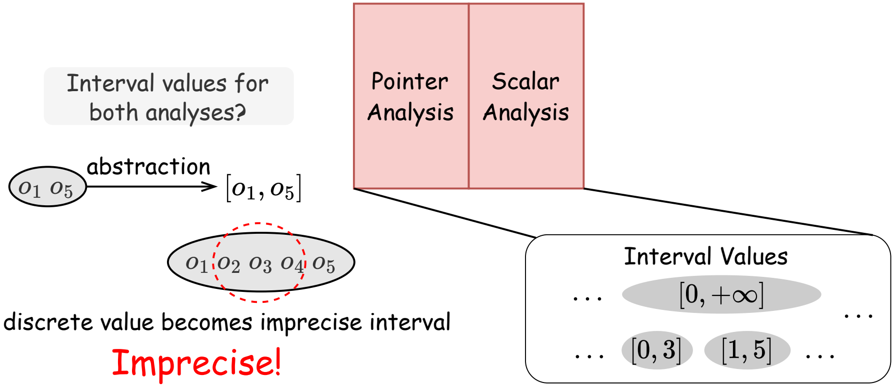
Discrete values for both analyses?

{1, 2, 3, ..., infinite numbers}

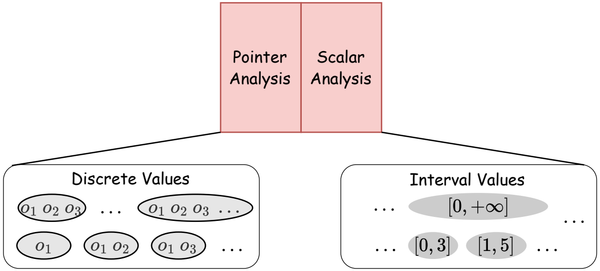
set of all possible values with inputs

Unscalable!

Combined Analysis Using Interval Values



Abstract Interpretation Over a Combined Domain

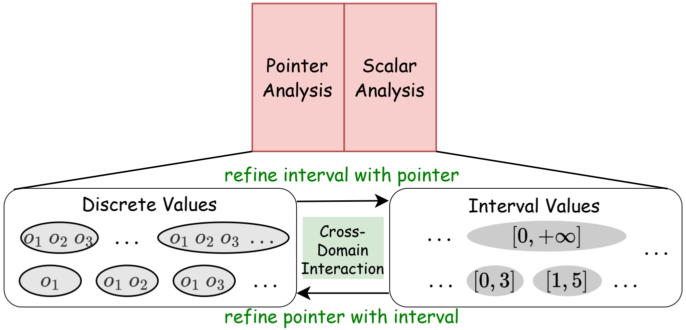


```
p = malloc(m*sizeof(int)); // p points to an array of size m
q = malloc(n*sizeof(int)); // q points to an array of size n
```

```
m = r[i];
```

- The discrete values for points-to set of `p`, `q` depend on interval values of `m` and `n`.
- The interval value of `m` depends on the pointer aliasing between `p`, `q` and `&r[i]`.
- Cyclic dependency between two domains requiring a bi-directional refinement. (variables highlighted in blue and red denote the discrete values and interval values dependent),

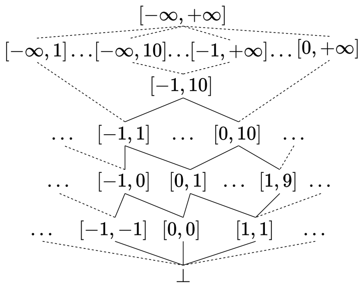
Abstract Interpretation Over a Combined Domain



We require **a combination of interval and memory address domains** to precisely and efficiently perform abstract execution on SVFIR in the presence of pointers.

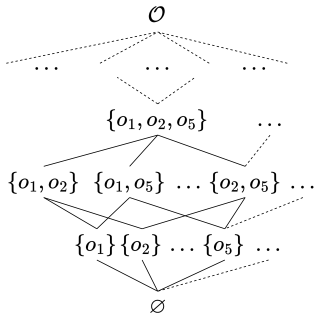
Abstract Interpretation over Interval and MemAddress Domains

A Combined Domain of Intervals and Discrete Memory Addresses



$[-\infty, +\infty]$
$[-\infty, 1] \ldots [-\infty, 10] \ldots [-1, +\infty] \ldots [0, +\infty]$
$[-1, 10]$
$\ldots$ $[-1, 1]$ $\ldots$ $[0, 10]$ $\ldots$
$\ldots$ $[-1, 0]$ $[0, 1]$ $\ldots$ $[1, 9]$ $\ldots$
$\ldots$ $[-1, -1]$ $[0, 0]$ $[1, 1]$ $\ldots$
$\perp$

Interval domain for scalar variables



$\mathcal{O}$
$\ldots$ $\ldots$ $\ldots$
$\{o_1, o_2, o_5\}$ $\ldots$
$\{o_1, o_2\}$ $\{o_1, o_5\}$ $\ldots$ $\{o_2, o_5\}$ $\ldots$
$\{o_1\}$ $\{o_2\}$ $\ldots$ $\{o_5\}$ $\ldots$
$\varnothing$

MemAddress domain for discrete memory address values

SVF Program Variables (SVFVar)

Program Variables	Domain	Meanings
`SVFVar`	$\mathbb{V} = \mathbb{P} \cup \mathbb{O}$	Program Variables
`ValVar`	$\mathbb{P}$	Top-level variables (scalars and pointers)
`ObjVar`	$\mathbb{O} = \mathbb{S} \cup \mathbb{G} \cup \mathbb{H} \cup \mathbb{C}$	Memory Objects (constant data, stack, heap, global) (function objects are considered as global objects)
`FIObjVar`	$o \in (\mathbb{S} \cup \mathbb{G} \cup \mathbb{H})$	A single (base) memory object
`GepObjVar`	$o_i \in (\mathbb{S} \cup \mathbb{G} \cup \mathbb{H}) \times \mathbb{P}$	*i*-th subfield/element of an (aggregate) object
`ConstantData`	$\mathbb{C}$	Constant data (e.g., numbers and strings)
Program Statement	$\ell \in \mathbb{L}$	Statements labels

Abstract Trace for The Combined Domain

- For top-level variables $\mathbb{P}$, we use $\sigma \in \mathbb{L} \times \mathbb{P} \to \mathit{Interval} \times \mathit{MemAddress}$ to track the memory addresses or interval values of these variables.
- For memory objects $\mathbb{O}$, we use $\delta \in \mathbb{L} \times \mathbb{O} \to \mathit{Interval} \times \mathit{MemAddress}$ to track their abstract values

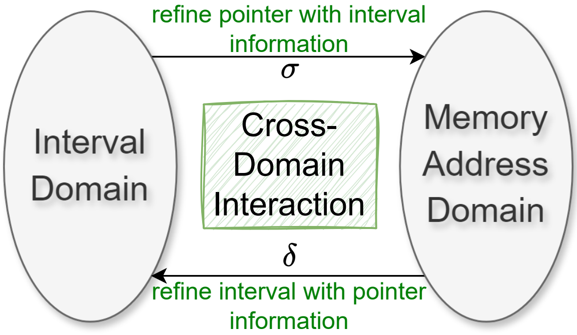
	Notation	**Domain**	**Data Structure Implementation**
Abstract trace	σ	$\mathbb{L} \times \mathbb{P} \to \mathit{Interval} \times \mathit{MemAddress}$	*preAbsTrace*, *postAbsTrace*
	δ	$\mathbb{L} \times \mathbb{O} \to \mathit{Interval} \times \mathit{MemAddress}$	
Abstract state	σ_L	$\mathbb{P} \to \mathit{Interval} \times \mathit{MemAddress}$	*AbstractState.varToAbsVal*
	δ_L	$\mathbb{O} \to \mathit{Interval} \times \mathit{MemAddress}$	*AbstractState.addrToAbsVal*
Abstract value	$\sigma_L(p)$	$\mathit{Interval} \times \mathit{MemAddress}$	*AbstractValue*
	$\delta_L(o)$		

- *Interval* is used for tracking the interval value of **scalar variables** $\mathbb{P}$.
- *MemAddress* is used for tracking the memory addresses of **memory address variables** $\mathbb{O}$.

Implementation of Abstract Trace and State in Assignment-3

- For a program point L, the abstract state is an instance of class *AEState*, consisting of:
  - Top-level variable, *varToAbsVal* : $\sigma_L \in \mathbb{P} \rightarrow \mathit{Interval} \times \mathit{MemAddress}$
  - Memory object, *addrToAbsVal* : $\delta_L \in \mathit{MemAddress} \rightarrow \mathit{Interval} \times \mathit{MemAddress}$
- The abstract trace has two maps, *preAbsTrace* and *postAbsTrace*, which maintains abstract states before and after each `ICFGNode` respectively.
  - For an `ICFGNode` ℓ, *preAbsTrace*(ℓ) retrieves the abstract state $\langle \sigma_{\overline{\ell}}, \delta_{\overline{\ell}} \rangle$, and *postAbsTrace*$(\ell)$ represents $\langle \sigma_{\underline{\ell}}, \delta_{\underline{\ell}} \rangle$.
  - For each abstract state $\langle \sigma_{\overline{\ell}}, \delta_{\overline{\ell}} \rangle$ we use `as[varId]` to operate $\sigma_{\underline{\ell}}$ and use `storeValue` and `loadValue` to operate $\delta_{\underline{\ell}}$.
  - Each variable's `AbstractValue` (e.g., `as[VarId]`) is initialized as $\perp$ in an `AbstractState` before assigned a new value.
  - Each `AbstractValue` (e.g., `as[VarId]`) is a 2-element tuple consisting of an interval `as[VarId].getInterval()` and an address set `as[Varid].getAddrs()`.
  - Print out `SVFVars` and their `AbstractValues` in an `AbstractState` by invoking `as.printAbstractState()`

Abstract Trace for The Combined Domain


refine pointer with interval information
σ
Interval Domain
Cross-Domain Interaction
Memory Address Domain
δ
refine interval with pointer information

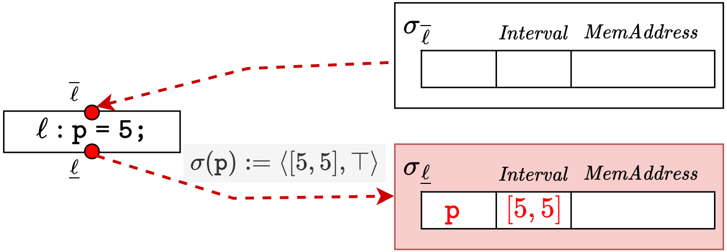
Abstract Execution Rules on SVFIR in the Presence of Pointers

Now let's use the *Interval* $\times$ *MemAddress* abstract domain to update σ and δ based on the following rules for different SVFSTMT:

SVFSTMT	**C-Like form**	**Abstract Execution Rule**
CONSSTMT	$\ell : \mathtt{p} = \mathtt{c}$	$\sigma_{\underline{\ell}}(\mathtt{p}) := \langle[\mathtt{c}, \mathtt{c}], \bot\rangle$
COPYSTMT	$\ell : \mathtt{p} = \mathtt{q}$	$\sigma_{\underline{\ell}}(\mathtt{p}) := \sigma_{\overline{\ell}}(\mathtt{q})$
BINARYSTMT	$\ell : \mathtt{r} = \mathtt{p} \otimes \mathtt{q}$	$\sigma_{\underline{\ell}}(r) := \sigma_{\overline{\ell}}(p) \hat{\otimes} \sigma_{\overline{\ell}}(q)$
PHISTMT	$\ell : \mathtt{r} = \mathtt{phi}(\mathtt{p_1}, \mathtt{p_2}, \ldots, \mathtt{p_n})$	$\sigma_{\underline{\ell}}(r) := \bigsqcup_{i=1}^{n} \sigma_{\overline{\ell}}(p_i)$
BRANCHSTMT	ℓ_1 : if$(x < c)$ then ℓ_2 else ℓ_3	$\sigma_{\overline{\ell_2}}(x) := \sigma_{\underline{\ell_1}}(x) \sqcap [-\infty, c-1],\ \text{if } \sigma_{\underline{\ell_1}}(x) \sqcap [-\infty, c-1] \neq \bot$ $\sigma_{\overline{\ell_3}}(x) := \sigma_{\underline{\ell_1}}(x) \sqcap [c, +\infty],\ \text{if } \sigma_{\underline{\ell_1}}(x) \sqcap [c, +\infty] \neq \bot$
SEQUENCE	$\ell_1; \ell_2$	$\delta_{\overline{\ell_2}} \sqsupseteq \delta_{\underline{\ell_1}}, \sigma_{\overline{\ell_2}} \sqsupseteq \sigma_{\underline{\ell_1}}$
ADDRSTMT	$\ell : \mathtt{p} = \mathtt{alloc}_{\mathtt{o_i}}$	$\sigma_{\underline{\ell}}(\mathtt{p}) := \langle\top, \{o_i\}\rangle$
GEPSTMT	$\ell : \mathtt{p} = \&(\mathtt{q} \rightarrow \mathtt{i})$ or $\mathtt{p} = \&\mathtt{q}[\mathtt{i}]$	$\sigma_{\underline{\ell}}(\mathtt{p}) := \bigsqcup_{\mathtt{o} \in \gamma(\sigma_{\overline{\ell}}(\mathtt{q}))} \bigsqcup_{j \in \gamma(\sigma_{\overline{\ell}}(\mathtt{i}))} \langle\top, \{\mathtt{o.fld}_j\}\rangle$
LOADSTMT	$\ell : \mathtt{p} = *\mathtt{q}$	$\sigma_{\underline{\ell}}(\mathtt{p}) := \bigsqcup_{o \in \{o \mid o \in \sigma_{\overline{\ell}}(q)\}} \delta_{\overline{\ell}}(o)$
STORESTMT	$\ell : *\mathtt{p} = \mathtt{q}$	$\delta_{\underline{\ell}} := (\{o \mapsto \sigma_{\overline{\ell}}(\mathtt{q}) \mid o \in \gamma(\sigma_{\overline{\ell}}(\mathtt{p}))\} \sqcup \delta_{\underline{\ell}})$

Abstract Execution on CONSSTMT

SVFSTMT	C-Like form	Abstract Execution Rule
CONSSTMT	$\ell : p = c$	$\sigma_{\underline{\ell}}(p) := \langle [c, c], \bot \rangle$



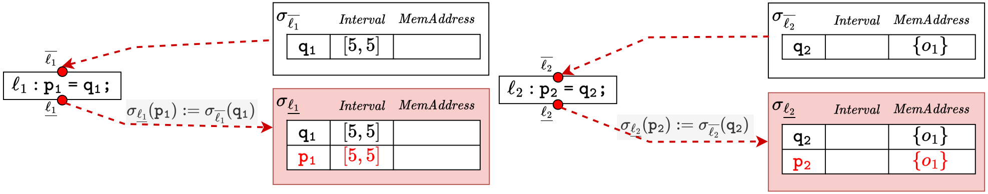
$\overline{\ell}$
ℓ : p = 5;
$\underline{\ell}$
$\sigma(p) := \langle [5, 5], \top \rangle$
$\sigma_{\overline{\ell}}$
Interval
MemAddress
$\sigma_{\underline{\ell}}$
Interval
MemAddress
p
[5, 5]

Algorithm 13: Abstract Execution Rule for CONSSTMT

```
Function updateStateOnAddr(addr):
    node = addr→getICFGNode();
    as = getAbsStateFromTrace(node);
    initObjVar(as, SVFUtil :: cast⟨ObjVar⟩(addr→getRHSVar()));
    as[addr→getLHSVarID()] = as[addr→getRHSVarID()];
```

Abstract Execution on CopyStmt

SVFStmt	C-Like form	Abstract Execution Rule
CopyStmt	$\ell : p = q$	$\sigma_{\underline{\ell}}(p) := \sigma_{\overline{\ell}}(q)$

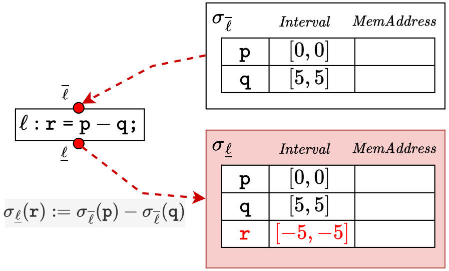

$\overline{\ell_1}$
ℓ_1 : p₁ = q₁ ;
$\underline{\ell_1}$
$\sigma_{\underline{\ell_1}}(p_1) := \sigma_{\overline{\ell_1}}(q_1)$
$\sigma_{\overline{\ell_1}}$ Interval MemAddress
q₁ [5, 5]
$\sigma_{\underline{\ell_1}}$ Interval MemAddress
q₁ [5, 5]
p₁ [5, 5]
$\overline{\ell_2}$
ℓ_2 : p₂ = q₂ ;
$\underline{\ell_2}$
$\sigma_{\underline{\ell_2}}(p_2) := \sigma_{\overline{\ell_2}}(q_2)$
$\sigma_{\overline{\ell_2}}$ Interval MemAddress
q₂ {o₁}
$\sigma_{\underline{\ell_2}}$ Interval MemAddress
q₂ {o₁}
p₂ {o₁}

Algorithm 14: Abstract Execution Rule for CopyStmt

```
Function updateStateOnCopy(copy):
    node = copy→getICFGNode();
    as = getAbsStateFromTrace(node);
    lhs = copy→getLHSVarID();
    rhs = copy→getRHSVarID();
    as[lhs] = as[rhs];
```

Abstract Execution on BinaryStmt

SVFStmt	C-Like form	Abstract Execution Rule
BinaryStmt	$\ell : \texttt{r} = \texttt{p} \otimes \texttt{q}$	$\sigma_{\ell}(r) := \sigma_{\overline{\ell}}(p) \hat{\otimes} \sigma_{\overline{\ell}}(q)$



$\overline{\ell}$
ℓ : r = p − q;
$\underline{\ell}$
$\sigma_{\underline{\ell}}(\texttt{r}) := \sigma_{\overline{\ell}}(\texttt{p}) - \sigma_{\overline{\ell}}(\texttt{q})$

$\sigma_{\overline{\ell}}$	*Interval*	*MemAddress*
p	$[0,0]$	
q	$[5,5]$	

$\sigma_{\underline{\ell}}$	*Interval*	*MemAddress*
p	$[0,0]$	
q	$[5,5]$	
r	$[-5,-5]$	

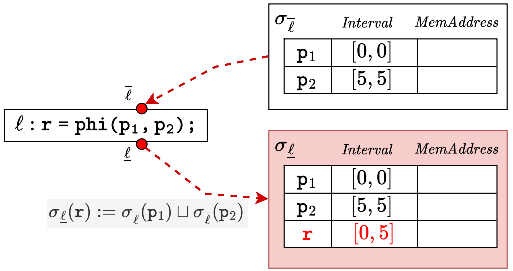
Algorithm 15: Abstract Execution Rule for BinaryStmt

```
Function updateStateOnBinary(binary):
    node = binary→getICFGNode();
    as = getAbsStateFromTrace(node);
    op0 = binary→getOpVarID(0);
    op1 = binary→getOpVarID(1);
    res = binary→getResID();
    as[res] = as[op0] $\hat{\otimes}$ as[op1]
```

Operands `op0` and `op1` are assumed to be properly initialized (no uninitialized variables or randomization).

Abstract Execution on PHISTMT

SVFSTMT	C-Like form	Abstract Execution Rule
PHISTMT	$\ell : \mathtt{r} = \mathtt{phi}(\mathtt{p_1}, \mathtt{p_2}, \ldots, \mathtt{p_n})$	$\sigma_{\underline{\ell}}(r) := \bigsqcup_{i=1}^{n} \sigma_{\overline{\ell}}(p_i)$



$\overline{\ell}$
ℓ : r = phi(p₁, p₂);
$\underline{\ell}$
$\sigma_{\underline{\ell}}(\mathtt{r}) := \sigma_{\overline{\ell}}(\mathtt{p_1}) \sqcup \sigma_{\overline{\ell}}(\mathtt{p_2})$

$\sigma_{\overline{\ell}}$	*Interval*	*MemAddress*
$\mathtt{p_1}$	$[0, 0]$	
$\mathtt{p_2}$	$[5, 5]$	

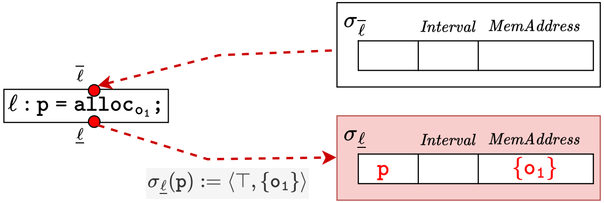
$\sigma_{\underline{\ell}}$	*Interval*	*MemAddress*
$\mathtt{p_1}$	$[0, 0]$	
$\mathtt{p_2}$	$[5, 5]$	
$\mathtt{r}$	$[0, 5]$	

Algorithm 16: Abstract Execution Rule for PHISTMT

```
Function updateStateOnPhi(phi):
    node = phi → getICFGNode();
    as = getAbsStateFromTrace(node);
    res = phi → getResID();
    rhs = AbstractValue();
    for i = 0; i < phi → getOpVarNum(); i + + do
        curId = phi → getOpVarID(i);
        rhs.join_with(as[curId])
    as[res] = rhs
```

Abstract Execution on ADDRSTMT

SVFSTMT	C-Like form	Abstract Execution Rule
ADDRSTMT	$\ell : \texttt{p} = \texttt{alloc}_{\texttt{o}_i}$	$\sigma_{\underline{\ell}}(\texttt{p}) := \langle \top, \{o_i\} \rangle$



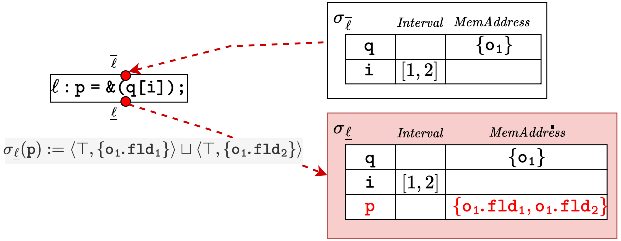
$\overline{\ell}$
ℓ : p = alloc$_{o_1}$;
$\underline{\ell}$
$\sigma_{\overline{\ell}}$ Interval MemAddress
$\sigma_{\underline{\ell}}$ Interval MemAddress
p
{o$_1$}
$\sigma_{\underline{\ell}}(\texttt{p}) := \langle \top, \{\texttt{o}_1\} \rangle$

Algorithm 17: Abstract Execution Rule for ADDRSTMT

```
Function updateStateOnAddr(addr):
    node = addr → getICFGNode();
    as = getAbsStateFromTrace(node);
    initObjVar(as, SVFUtil :: cast⟨ObjVar⟩(addr → getRHSVar()));
    as[addr → getLHSVarID()] = as[addr → getRHSVarID()];
```

Abstract Execution on GEPSTMT

SVFSTMT	C-Like form	Abstract Execution Rule
GEPSTMT	$\ell : \texttt{p} = \&(\texttt{q} \to \texttt{i})$ or $\texttt{p} = \&\texttt{q}[\texttt{i}]$	$\sigma_{\underline{\ell}}(\texttt{p}) := \bigsqcup_{o \in \gamma(\sigma_{\overline{\ell}}(\texttt{q}))} \bigsqcup_{j \in \gamma(\sigma_{\overline{\ell}}(\texttt{i}))} \langle \top, \{\texttt{o.fld}_j\} \rangle$


$\overline{\ell}$
ℓ : p = &(q[i]);
$\underline{\ell}$
$\sigma_{\underline{\ell}}(\texttt{p}) := \langle \top, \{\texttt{o}_1.\texttt{fld}_1\} \rangle \sqcup \langle \top, \{\texttt{o}_1.\texttt{fld}_2\} \rangle$

$\sigma_{\overline{\ell}}$

	Interval	*MemAddress*
q		$\{\texttt{o}_1\}$
i	$[1, 2]$	

$\sigma_{\underline{\ell}}$

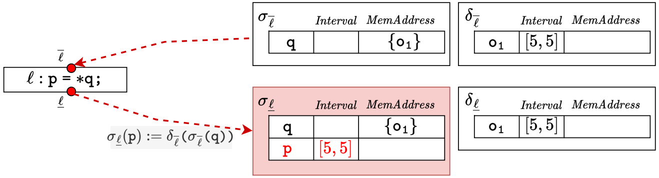
	Interval	*MemAddress*
q		$\{\texttt{o}_1\}$
i	$[1, 2]$	
p		$\{\texttt{o}_1.\texttt{fld}_1, \texttt{o}_1.\texttt{fld}_2\}$

Algorithm 18: Abstract Execution Rule for GEPSTMT

```
Function updateStateOnGep(gep):
    node = gep→getICFGNode();
    as = getAbsStateFromTrace(node);
    rhs = gep→getRHSVarID();
    lhs = gep→getLHSVarID();
    as[lhs] = as.getGepObjAddrs(rhs, as.getElementIndex(gep));;
```

Abstract Execution on LOADSTMT

SVFSTMT	C-Like form	Abstract Execution Rule
LOADSTMT	$\ell : \mathtt{p} = *\mathtt{q}$	$\sigma_{\underline{\ell}}(\mathtt{p}) := \bigsqcup_{o\in\{o \mid o\in\sigma_{\overline{\ell}}(q)\}} \delta_{\overline{\ell}}(o)$



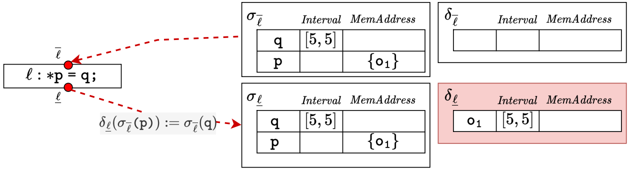
$\overline{\ell}$
ℓ : p = *q;
$\underline{\ell}$
$\sigma_{\underline{\ell}}(\mathtt{p}) := \delta_{\overline{\ell}}(\sigma_{\overline{\ell}}(\mathtt{q}))$
$\sigma_{\overline{\ell}}$ Interval MemAddress
q {o₁}
$\delta_{\overline{\ell}}$ Interval MemAddress
o₁ [5, 5]
$\sigma_{\underline{\ell}}$ Interval MemAddress
q {o₁}
p [5, 5]
$\delta_{\underline{\ell}}$ Interval MemAddress
o₁ [5, 5]

Algorithm 19: Abstract Execution Rule for LOADSTMT

```
Function updateStateOnLoad(load):
    node = load→getICFGNode();
    as = getAbsStateFromTrace(node);
    rhs = load→getRHSVarID();
    lhs = load→getLHSVarID();
    as[lhs] = as.loadValue(rhs)
```

Abstract Execution on STORESTMT

SVFSTMT	C-Like form	Abstract Execution Rule
STORESTMT	$\ell : *\mathtt{p} = \mathtt{q}$	$\delta_{\underline{\ell}} := (\{o \mapsto \sigma_{\overline{\ell}}(\mathtt{q}) \mid o \in \gamma(\sigma_{\overline{\ell}}(\mathtt{p}))\} \sqcup \delta_{\underline{\ell}})$



$\overline{\ell}$
ℓ : *p = q;
$\underline{\ell}$
$\delta_{\underline{\ell}}(\sigma_{\overline{\ell}}(\mathtt{p})) := \sigma_{\overline{\ell}}(\mathtt{q})$
$\sigma_{\overline{\ell}}$ Interval MemAddress
q [5, 5]
p {o₁}
$\delta_{\overline{\ell}}$ Interval MemAddress
$\sigma_{\underline{\ell}}$ Interval MemAddress
q [5, 5]
p {o₁}
$\delta_{\underline{\ell}}$ Interval MemAddress
o₁ [5, 5]

Algorithm 20: Abstract Execution Rule for STORESTMT

```
Function updateStateOnStore(store):
    node = store→getICFGNode();
    as = getAbsStateFromTrace(node);
    rhs = store→getRHSVarID();
    lhs = store→getLHSVarID();
    as.storeValue(lhs, as[rhs])
```

Overall Algorithm of Abstract Interpretation in Assignment-3

Algorithm 1: Analyse from main function

```
Function analyse() // driver function to start the analysis:
    initWTO();
    handleGlobalNode();
    if getSVFFunction (main) then
        wto := funcToWTO[main];
        handleWTOComponents(wto → getWTOComponents());
```

Algorithm 2: Handle WTO components

```
Function handleWTOComponents (wtoComps):
    for wtoNode ∈ wtoComps do
        if node = SVFUtil :: dyn_cast⟨ICFGSingletonWTO⟩(wtoNode) then
            handleSingletonWTO(node)
        else if cycle = SVFUtil :: dyn_cast⟨ICFGCycleWTO⟩(wtoNode) then
            handleCycleWTO(cycle)
        else
            assert(false&&"unknownWTOtype!")
```

Algorithm 3: Handle Singleton WTO

```
Function handleSingletonWTO(singletonWTO):
    node := singletonWTO → node();
    feasible := mergeStatesFromPredecessors(node, preAbsTrace[node]);
    if feasible then
        postAbsTrace[node] := preAbsTrace[node];
    else
        return;
    foreach stmt ∈ node → getSVFStmts() do
        updateAbsState(stmt);
        bufOverflowDetection(stmt);
    if callnode = SVFUtil :: dyn_cast⟨CallICFGNode⟩(node) then
        funName := callnode → getCallSite() → getCallee() → getName()
        if funName == "OVERFLOW"&&funName == "svf_assert" then
            // Handle svf_assert and OVERFLOW stub function for
            correctness validation;
            handleStubFunctions(callnode);
        else
            // Does not analyze recursive functions in this course;
            handleCallSite(callnode);
```

Overall Algorithm of Abstract Interpretation in Assignment-3

Algorithm 4: Handle Cycle WTO

```
Function handleCycleWTO (cycle):
    feasible := mergeStatesFromPredecessors(cycle_head, preAbsTrace[cycle_head]);
    increasing := true;
    if !feasible then
        return;
    else
        cur_iter := 0;
        while true do
            if cur_iter >= Options.WidenDelay() then
                prev_head_as := postAbsTrace[cycle_head];
                handleSingletonWTO(cycle.head());
                cur_head_as := postAbsTrace[cycle_head];
                if increasing then
                    postAbsTrace[cycle_head] := prev_head_as.widening(cur_head_as);
                    if postAbsTrace[cycle_head] == prev_head_as then
                        increasing := false;
                        Continue;
                else
                    postAbsTrace[cycle_head] := prev_head_as.narrowing(cur_head_as);
                    if postAbsTrace[cycle_head] == prev_head_as then
                        Break;
            else
                handleSingletonWTO(cycle.head());
            cur_iter++;
```

An Example: Abstract Trace σ for Top-level Variables

```
extern void assert(int);

int main(){
    int a = 0;
    while(a < 10) {
        a++;
    }
    assert(a == 10);
    return 0;
}
```

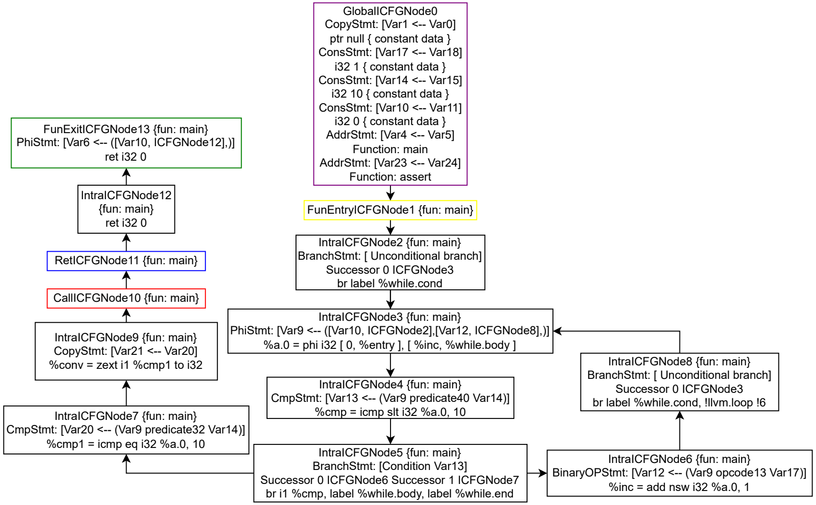
Source Code

Compile to LLVM IR

```
define dso_local i32 @main() {
entry:
  br label %while.cond
while.cond:
  %a.0 = phi i32 [ 0, %entry ], [ %inc, %while.body ]
  %cmp = icmp slt i32 %a.0, 10
  br i1 %cmp, label %while.body, label %while.end
while.body:
  %inc = add nsw i32 %a.0, 1
  br label %while.cond,
while.end:
  %cmp1 = icmp eq i32 %a.0, 10
  %conv = zext i1 %cmp1 to i32
  call void @assert(i32 noundef %conv)
  ret i32 0
}
```

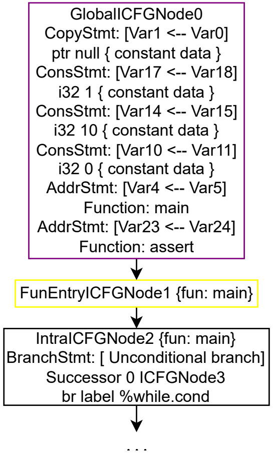
LLVM IR

An Example: Abstract Trace σ for Top-level Variables


GlobalICFGNode0
CopyStmt: [Var1 <-- Var0]
ptr null { constant data }
ConsStmt: [Var17 <-- Var18]
i32 1 { constant data }
ConsStmt: [Var14 <-- Var15]
i32 10 { constant data }
ConsStmt: [Var10 <-- Var11]
i32 0 { constant data }
AddrStmt: [Var4 <-- Var5]
Function: main
AddrStmt: [Var23 <-- Var24]
Function: assert
FunEntryICFGNode1 {fun: main}
IntraICFGNode2 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond
IntraICFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [0, %entry], [%inc, %while.body]
IntraICFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10
IntraICFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end
IntraICFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1
IntraICFGNode8 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
IntraICFGNode7 {fun: main}
CmpStmt: [Var20 <-- (Var9 predicate32 Var14)]
%cmp1 = icmp eq i32 %a.0, 10
IntraICFGNode9 {fun: main}
CopyStmt: [Var21 <-- Var20]
%conv = zext i1 %cmp1 to i32
CallICFGNode10 {fun: main}
RetICFGNode11 {fun: main}
IntraICFGNode12
{fun: main}
ret i32 0
FunExitICFGNode13 {fun: main}
PhiStmt: [Var6 <-- ([Var10, ICFGNode12],)]
ret i32 0

ICFG

An Example: Abstract Trace σ for Top-level Variables



GlobalICFGNode0
CopyStmt: [Var1 <-- Var0]
ptr null { constant data }
ConsStmt: [Var17 <-- Var18]
i32 1 { constant data }
ConsStmt: [Var14 <-- Var15]
i32 10 { constant data }
ConsStmt: [Var10 <-- Var11]
i32 0 { constant data }
AddrStmt: [Var4 <-- Var5]
Function: main
AddrStmt: [Var23 <-- Var24]
Function: assert
FunEntryICFGNode1 {fun: main}
IntraICFGNode2 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond
...

ICFG

Algorithm 5: Abstract execution guided by WTO

```
Function handleStatement($\ell$):
    $tmpAS := preAbsTrace[\ell]$;
    if $\ell$ is ConsStmt or AddrStmt then
        updateStateOnAddr($\ell$);
    else if $\ell$ is CopyStmt then
        updateStateOnCopy($\ell$);
    ...;
```

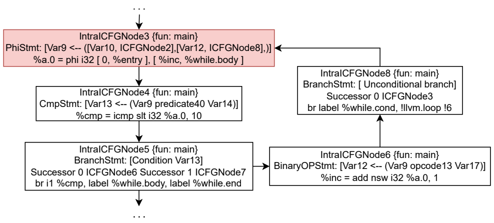
$postAbsTrace[\ell_0].varToAbsVal$:

SVFVar	AbstractValue$\langle Interval, MemAddress \rangle$
$Var0$	$\langle \bot, \{0x7f00\} \rangle$
$Var1$	$\langle \bot, \{0x7f00\} \rangle$
$Var18$	$\langle [1,1], \bot \rangle$
$Var17$	$\langle [1,1], \bot \rangle$
$Var14$	$\langle [10,10], \bot \rangle$
$Var15$	$\langle [10,10], \bot \rangle$
$Var10$	$\langle [0,0], \bot \rangle$
$Var11$	$\langle [0,0], \bot \rangle$
	...

Print out the table via `as.printAbstractState()`. The `AbstractValue` can **either be an interval or addresses**, but not both!

An Example: Abstract Trace σ for Top-level Variables

Widen Delay Phase (cur_iter is 0)


...
IntraICFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [0, %entry], [%inc, %while.body]
IntraICFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10
IntraICFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end
IntraICFGNode8 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
IntraICFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1
...

ICFG

$postAbsTrace[\ell_3].varToAbsVal$:

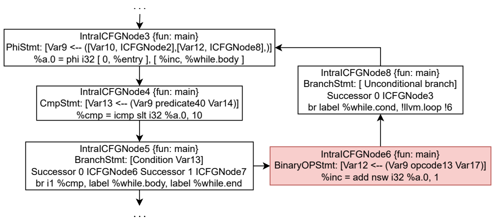
SVFVar	AbstractValue$\langle$*Interval*, *MemAddress*$\rangle$
...	
Var10	$\langle[0,0],\perp\rangle$
Var9	$\langle[0,0],\perp\rangle$
...	

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        // cur_iter ≡ 0, Options :: WidenDelay() ≡ 2
        if $cur\_iter \geq Options :: WidenDelay()$ then
            $prev\_head\_state := postAbsTrace[cycle\_head]$;
            handleSingletonWTO(cycle→head());
            $cur\_head\_state := postAbsTrace[cycle\_head]$;
            if increasing then
                $postAbsTrace[cycle\_head] := prev\_head\_state.widen(cur\_head\_state)$ ;
                if $postAbsTrace[cycle\_head] == prev\_head\_state$ then
                    increasing := false;
                    continue;
            else
                $postAbsTrace[cycle\_head] := prev\_head\_state.narrow(cur\_head\_state)$ ;
                if $postAbsTrace[cycle\_head] == prev\_head\_state$ then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents());
        cur_iter++;
```

An Example: Abstract Trace σ for Top-level Variables

Widen Delay Phase (cur_iter is 0)


...
IntraICFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [0, %entry], [%inc, %while.body]
IntraICFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10
IntraICFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end
IntraICFGNode8 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
IntraICFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1
...

ICFG

$postAbsTrace[\ell_6].varToAbsVal$:

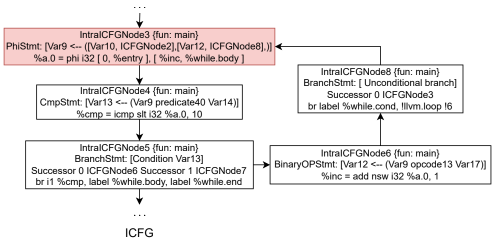
SVFVar	AbstractValue$\langle Interval, MemAddress\rangle$
...	
$Var10$	$\langle [0,0], \bot\rangle$
$Var9$	$\langle [0,0], \bot\rangle$
$Var12$	$\langle [1,1], \bot\rangle$
...	

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        // cur_iter ≡ 0,  Options :: WidenDelay() ≡ 2;
        if cur_iter ≥ Options :: WidenDelay() then
            prev_head_state := postAbsTrace[cycle_head];
            handleSingletonWTO(cycle→head());
            cur_head_state := postAbsTrace[cycle_head];
            if increasing then
                postAbsTrace[cycle_head] := prev_head_state.widen(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    increasing := false;
                    continue;
            else
                postAbsTrace[cycle_head] := prev_head_state.narrow(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents());
        cur_iter++;
```

An Example: Abstract Trace σ for Top-level Variables

Widen Delay Phase (cur_iter is 1)


...
IntraCFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [0, %entry], [%inc, %while.body]
IntraCFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10
IntraCFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end
IntraCFGNode8 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
IntraCFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1
...
ICFG

$postAbsTrace[\ell_3].varToAbsVal$:

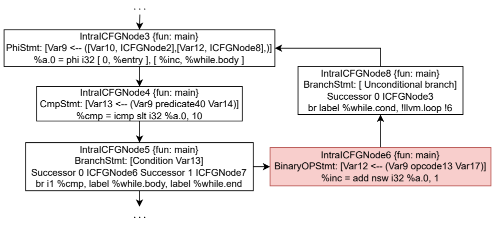
SVFVar	AbstractValue$\langle$*Interval*, *MemAddress*$\rangle$
...	...
Var9	$\langle[0,1],\perp\rangle$
Var12	$\langle[1,1],\perp\rangle$
...	...

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        // cur_iter ≡ 1, Options :: WidenDelay() ≡ 2;
        if cur_iter ≥ Options :: WidenDelay() then
            prev_head_state := postAbsTrace[cycle_head];
            handleSingletonWTO(cycle→head());
            cur_head_state := postAbsTrace[cycle_head];
            if increasing then
                postAbsTrace[cycle_head] := prev_head_state.widen(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    increasing := false;
                    continue;
            else
                postAbsTrace[cycle_head] := prev_head_state.narrow(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents());
        cur_iter++ ;
```

An Example: Abstract Trace σ for Top-level Variables

Widen Delay Phase (cur_iter is 1)



```
IntraCFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [ 0, %entry ], [ %inc, %while.body ]

IntraCFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10

IntraCFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end

IntraCFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1

IntraCFGNode8 {fun: main}
BranchStmt: [ Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
```

ICFG

$postAbsTrace[\ell_6].varToAbsVal$:

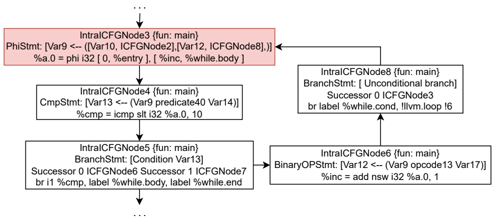
SVFVar	AbstractValue⟨*Interval*, *MemAddress*⟩
	. . .
Var9	$\langle [0,1], \bot \rangle$
Var12	$\langle [1,2], \bot \rangle$
	. . .

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        // cur_iter ≡ 1,  Options :: WidenDelay() ≡ 2;
        if cur_iter ≥ Options :: WidenDelay() then
            prev_head_state := postAbsTrace[cycle_head];
            handleSingletonWTO(cycle→head());
            cur_head_state := postAbsTrace[cycle_head];
            if increasing then
                postAbsTrace[cycle_head] := prev_head_state.widen(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    increasing := false;
                    continue;
            else
                postAbsTrace[cycle_head] := prev_head_state.narrow(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents());
        cur_iter++ ;
```

An Example: Abstract Trace σ for Top-level Variables

Widen Phase (cur_iter is 2)


...
IntraICFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [0, %entry], [%inc, %while.body]
IntraICFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10
IntraICFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end
IntraICFGNode8 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
IntraICFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1
...

ICFG

$postAbsTrace[\ell_3].varToAbsVal$:

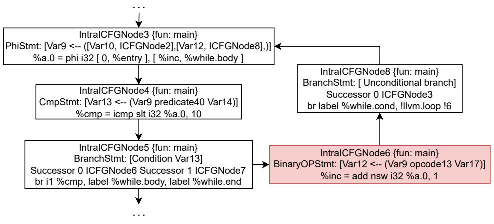
SVFVar	$\langle Interval, MemAddress\rangle$
...	
Var9	$\langle[0,+\infty],\perp\rangle$
Var12	$\langle[1,+\infty],\perp\rangle$
...	

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        // cur_iter ≡ 2,  Options :: WidenDelay() ≡ 2
        if cur_iter ≥ Options :: WidenDelay() then
            prev_head_state := postAbsTrace[cycle_head];
            handleSingletonWTO(cycle→head());
            cur_head_state := postAbsTrace[cycle_head];
            if increasing then
                postAbsTrace[cycle_head] := prev_head_state.widen(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    increasing := false;
                    continue;
            else
                postAbsTrace[cycle_head] := prev_head_state.narrow(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents());
        cur_iter++ ;
```

An Example: Abstract Trace σ for Top-level Variables

Widen Phase (cur_iter is 2)


...
IntraICFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [0, %entry], [%inc, %while.body]
IntraICFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10
IntraICFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end
IntraICFGNode8 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
IntraICFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1
...

ICFG

$postAbsTrace[\ell_6].varToAbsVal$:

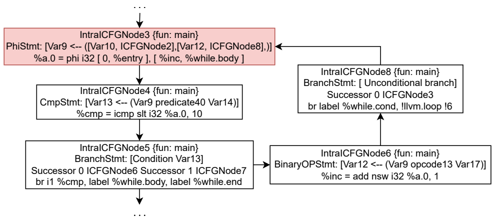
SVFVar	AbstractValue⟨*Interval*, *MemAddress*⟩
...	
Var9	$\langle [0,9], \perp \rangle$
Var12	$\langle [1,10], \perp \rangle$
...	

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        // cur_iter ≡ 2,  Options :: WidenDelay() ≡ 2
        if cur_iter ≥ Options :: WidenDelay() then
            prev_head_state := postAbsTrace[cycle_head];
            handleSingletonWTO(cycle→head());
            cur_head_state := postAbsTrace[cycle_head];
            if increasing then
                postAbsTrace[cycle_head] := prev_head_state.widen(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    increasing := false;
                    continue;
            else
                postAbsTrace[cycle_head] := prev_head_state.narrow(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents())
        cur_iter++ ;
```

An Example: Abstract Trace σ for Top-level Variables

Widen Phase Fixed Point


...
IntraICFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [0, %entry], [%inc, %while.body]
IntraICFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10
IntraICFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end
IntraICFGNode8 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
IntraICFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1
...

ICFG

$postAbsTrace[\ell_3].varToAbsVal$:

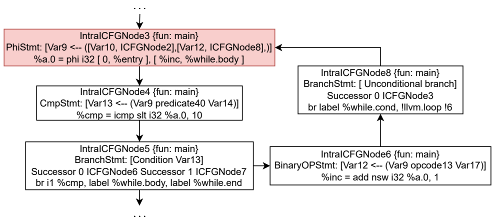
SVFVar	$\langle Interval, MemAddress \rangle$
...	
Var9	$\langle [0, +\infty], \bot \rangle$
Var12	$\langle [1, +\infty], \bot \rangle$
...	

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0;
    while true do
        // cur_iter ≡ 3, Options :: WidenDelay() ≡ 2
        if cur_iter ≥ Options :: WidenDelay() then
            prev_head_state := postAbsTrace[cycle_head];
            handleSingletonWTO(cycle→head());
            cur_head_state := postAbsTrace[cycle_head];
            if increasing then
                postAbsTrace[cycle_head] := prev_head_state.widen(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    increasing := false;
                    continue;
            else
                postAbsTrace[cycle_head] := prev_head_state.narrow(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents());
        cur_iter++ ;
```

An Example: Abstract Trace σ for Top-level Variables

Narrow Phase


...
IntraICFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [0, %entry], [%inc, %while.body]
IntraICFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10
IntraICFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end
IntraICFGNode8 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
IntraICFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1
...

ICFG

$postAbsTrace[\ell_3].varToAbsVal$:

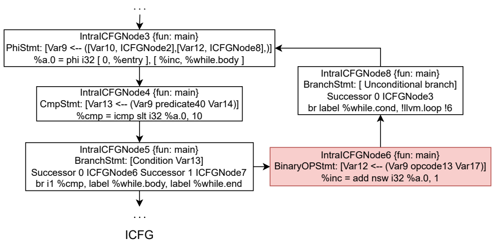
SVFVar	$\langle Interval, MemAddress \rangle$
	...
Var9	$\langle [0, 10], \perp \rangle$
Var12	$\langle [1, 10], \perp \rangle$
	...

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        // cur_iter ≡ 3,  Options :: WidenDelay() ≡ 2
        if cur_iter ≥ Options :: WidenDelay() then
            prev_head_state := postAbsTrace[cycle_head];
            handleSingletonWTO(cycle→head()) // increasing ≡ false;
            cur_head_state := postAbsTrace[cycle_head];
            if increasing then
                postAbsTrace[cycle_head] := prev_head_state.widen(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    increasing := false;
                    continue;
            else
                postAbsTrace[cycle_head] := prev_head_state.narrow(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents());
        cur_iter++ ;
```

An Example: Abstract Trace σ for Top-level Variables

Narrow Phase



...
IntraICFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [0, %entry], [%inc, %while.body]
IntraICFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10
IntraICFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end
IntraICFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1
IntraICFGNode8 {fun: main}
BranchStmt: [Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
...
ICFG

$postAbsTrace[\ell_6].varToAbsVal$:

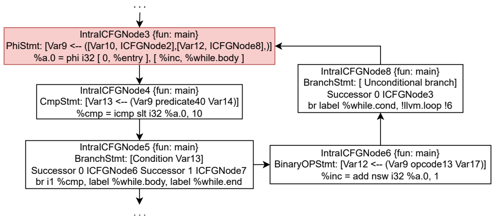
SVFVar	$\langle Interval, MemAddress \rangle$
...	
Var9	$\langle [0, 9], \perp \rangle$
Var12	$\langle [1, 10], \perp \rangle$
...	

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        // cur_iter ≡ 3,  Options :: WidenDelay() ≡ 2
        if cur_iter ≥ Options :: WidenDelay() then
            prev_head_state := postAbsTrace[cycle_head];
            handleSingletonWTO(cycle→head());
            cur_head_state := postAbsTrace[cycle_head];
            if increasing then
                postAbsTrace[cycle_head] := prev_head_state.widen(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    increasing := false;
                    continue;
            else
                postAbsTrace[cycle_head] := prev_head_state.narrow(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents()) ;
        cur_iter++;
```

An Example: Abstract Trace σ for Top-level Variables

Narrow Phase Fixed Point



```
...
IntraICFGNode3 {fun: main}
PhiStmt: [Var9 <-- ([Var10, ICFGNode2],[Var12, ICFGNode8],)]
%a.0 = phi i32 [ 0, %entry ], [ %inc, %while.body ]

IntraICFGNode4 {fun: main}
CmpStmt: [Var13 <-- (Var9 predicate40 Var14)]
%cmp = icmp slt i32 %a.0, 10

IntraICFGNode5 {fun: main}
BranchStmt: [Condition Var13]
Successor 0 ICFGNode6 Successor 1 ICFGNode7
br i1 %cmp, label %while.body, label %while.end

IntraICFGNode6 {fun: main}
BinaryOPStmt: [Var12 <-- (Var9 opcode13 Var17)]
%inc = add nsw i32 %a.0, 1

IntraICFGNode8 {fun: main}
BranchStmt: [ Unconditional branch]
Successor 0 ICFGNode3
br label %while.cond, !llvm.loop !6
...
```

ICFG

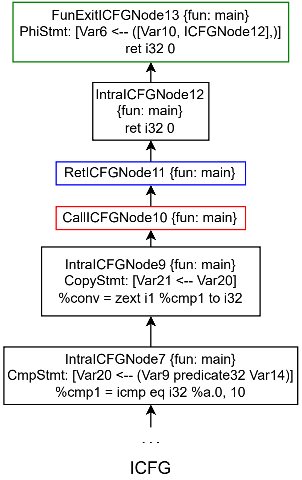
$postAbsTrace[\ell_3].varToAbsVal$:

SVFVar	$\langle Interval, MemAddress\rangle$
...	
Var9	$\langle[0,10],\bot\rangle$
Var12	$\langle[1,10],\bot\rangle$
...	

Algorithm 12: Handle Cycle WTO

```
Function handleCycleWTO(cycle):
    cycle_head := cycle→head()→node() ;
    increasing := true ;
    cur_iter := 0 ;
    while true do
        // cur_iter ≡ 4,  Options :: WidenDelay() ≡ 2
        if cur_iter ≥ Options :: WidenDelay() then
            prev_head_state := postAbsTrace[cycle_head];
            handleSingletonWTO(cycle→head()) // increasing ≡ false;
            cur_head_state := postAbsTrace[cycle_head];
            if increasing then
                postAbsTrace[cycle_head] := prev_head_state.widen(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    increasing := false;
                    continue;
            else
                postAbsTrace[cycle_head] := prev_head_state.narrow(cur_head_state) ;
                if postAbsTrace[cycle_head] == prev_head_state then
                    break ;
        else
            handleSingletonWTO(cycle→head());
        handleWTOComponents(cycle→getWTOComponents());
        cur_iter++ ;
```

An Example: Abstract Trace σ for Top-level Variables


FunExitICFGNode13 {fun: main}
PhiStmt: [Var6 <-- ([Var10, ICFGNode12],)]
ret i32 0
IntraICFGNode12
{fun: main}
ret i32 0
RetICFGNode11 {fun: main}
CallICFGNode10 {fun: main}
IntraICFGNode9 {fun: main}
CopyStmt: [Var21 <-- Var20]
%conv = zext i1 %cmp1 to i32
IntraICFGNode7 {fun: main}
CmpStmt: [Var20 <-- (Var9 predicate32 Var14)]
%cmp1 = icmp eq i32 %a.0, 10
. . .
ICFG

Algorithm 13: Abstract execution guided by WTO

```
Function handleStatement($\ell$):
    $tmpAS := preAbsTrace[\ell]$;
    if $\ell$ is BinaryStmt then
        updateStateOnBinary($\ell$);
    ...;
```

$postAbsTrace[\ell_7].varToAbsVal$:

SVFVar	$\langle Interval, MemAddress \rangle$
...	
$Var9$	$\langle [10, 10], \perp \rangle$
$Var20$	$\langle [1, 1], \perp \rangle$
...	