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Faculty of Engineering, Architecture and Science

Department of Electrical and Computer Engineering

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| Instructor | Dr. Mike Kassam |

# ASSIGNMENT No. 8

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| Assignment Title | Linear Voltage-Controlled Function Generator (Milestone 5) |

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| Submission Date | November 5, 2021 |
| Due Date | November 5, 2021 |



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## 1. Abstract

In automatic control and measurement, electronic music synthesis and data encoding, it is essential to program the generation of frequency utilizing an external control signal $V_C$. The circuit consisting of these properties is called a VCFG (Linear Voltage-Controlled Function Generator), where the output frequency is dependant on the control signal by the $f_o = k \times V_C$ relationship ("K" uses the proportionality constant, expressed in Hz/Volt). Using a combination of non-linear circuits such as integrators and Hysteresis comparators, combined with an appropriate voltage-controlled interface, the VCFG is created and tested in comparison with its design analysis to perform design verification and validation for each individual milestone leading to the final overall design. However, for this design project, the design is limited to the generation of only symmetrical square-wave and triangular waveforms with a Total Harmonic Distortion percentage of less than 1% for the triangular waveforms.

## 2. Objectives

The purpose of this design project is to fully design a Voltage-Controlled Function Generator with the specifications from the project manual through five separate milestone sub-projects. Each milestone aims to improve and optimize the design on a step-by-step basis. The first specification of the design project is the assigned output frequency of $f_o = 3100\ Hz$, which determines two frequency ranges of approximately 100 Hz to 3100 Hz (range #1) and 20 Hz to 620 Hz (range #2). The second part of specifications includes a user-selectable triangular or square-wave output waveform with 0 to 4 volts peak amplitude (amplitude control is implemented through using a potentiometer). One last specification is the use of +/- 10 Volts D.C power supplies for the completed design.

## 3. Introduction

The goal of this design project is to develop a product that accurately meets all specifications from the project manual and is consistent with its design analysis with little or no error. The product, known as the linear Voltage-Controlled Function Generator, has the ability to operate in two separate output frequency ranges (20 Hz to 620 Hz, and 100 Hz to 3100 Hz) when its control voltage is varied from 0.1 to 5 Volts D.C. The project is split into five milestones, where each milestone verifies an individual component of the final design. Every milestone consists of a design analysis section, which is then verified using the experimental data from the simulation of the corresponding circuit schematics.

The first milestone starts off by verifying the output frequency equation ($f_o = \frac{L^+}{2 \times R \times C \times (V_{TH} - V_{TL})}$) and designing a fixed-frequency waveform generator, consisting of an inverting integrator and a noninverting bistable comparator. The appropriate choice of OP-AMPs for this milestone is made using the simulation results with respect to slew rate constraints on the circuit. The second milestone is continuing the design of milestone 1 with the addition of a DC-to-(+/-) DC converter that will be placed in cascading manner before the inverting integrator. A limiter circuit is used to provide a consistent output waveform for the circuit with the usage of Zener diodes, and the two circuit components are tested separately.

The third milestone brings forward the combined testing of the converter and waveform generator circuits together to verify the functionality of the circuit for all values of the control voltage (0.1 volts to 5 volts D.C). The fourth milestone implements the frequency range and amplitude control ranges for the overall circuit using the implementation of additional switches and OP-AMPs, along with potentiometers to control the amplitude of the output voltage to stay at around 4 volts for all control voltage values.

## 4. Theory

The **Function generator** is one of the most essential electronic circuit components in use for the project. It creates different kinds of waveforms such as square, triangular and sinusoidal waves over a variety of different frequencies for varying voltages. It is constructed by using a **DC-to-(+/-) DC Converter**, **Integrator**, **Bistable Comparator**, and **Gain Control circuit**.

The **DC-to-(+/-) DC Converter** is an electronic device that converts a D.C voltage to a square wave signal. It's used to control the amplitude of the input wave that is fed to the integrator.

**Figure 4.1** contains the design structure of the DC converter from the project manual.

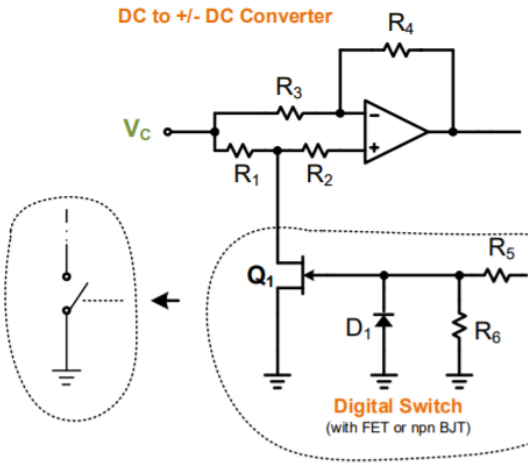



**Figure 4.1: DC-to-(+/-) DC Converter circuit structure.**

When the base voltage of the transistor $Q_1$ is less than $V_{BE} = 0.7$volts, the transistor operates in cut-off mode. It would work like an open switch ($I_B = I_C = I_E = 0$A), meaning that the switch is off. The saturation voltage is found through the following derivation:

$V_B < (V_{BE} = 0.7\ V)$ => $V^+ = V^- = V_C$, and $I = -I_f = 0$A. Therefore, $V_C = L^+$.

If the circuit happens to be operating in saturation mode, the transistor looks like a short circuit. It would work as a closed switch with current flow from collector to emitter. The derivation of appropriate quantities is shown below:

$V_B > (V_{BE} = 0.7\,V)$=> $V^+ = 0\,V$, $V^- = V_C$, $I = V_C/R = -V_O/R$, and so, $V_O = -V_C$ and $V_C = L^-$.

The DC converter has an electronic switch that is used to be able to control the operation of the circuit and provide a precise square wave output. It contains two resistors, a diode and a transistor. The diode works as normal when in forwarding bias ($V_D = 0.7$Volts), whereas in reverse bias, $I_Z = 0$A. The diode regulates the voltage across the transistor to minimize the current flowing through it and protect it from any damaging issues. When the switch is closed, the collector-emitter current is $I_C = (V_C - V_E)/R$ and since $V_E = 0$Volts as the emitter is connected to ground, $I_C = V_C/R$ is the expression for the current.

**Figure 4.2** displays the output square wave of the DC converter. It will toggle between $L^+$ and $L^-$ values that have been derived above. The period and output frequency expressions are derived below:

$T = 2\,RC\,(V_{TH} - V_{TL})\,/\,V_C$, and $f_o = 1/T$.

Therefore, $f_o = V_C\,/\,2\,RC\,(V_{TH} - V_{TL})$.

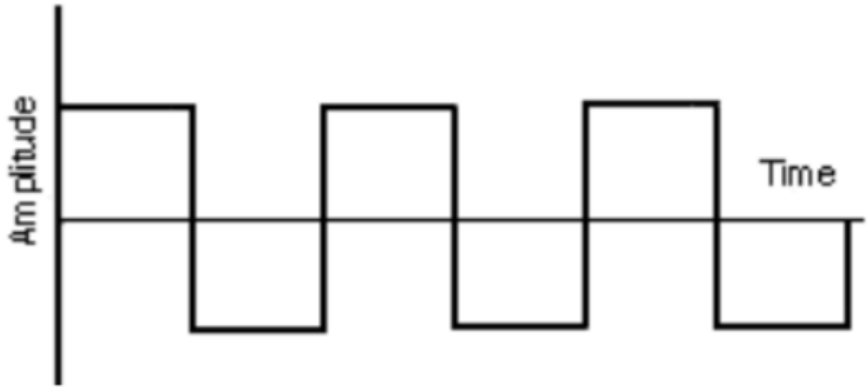



**Figure 4.2: Square wave output of the DC-to-(+/-) DC converter.**

The **Integrator** consists of an input resistor and a capacitor in its feedback path. The input voltage is time-dependent, and changes by time. **Figure 4.3** contains the circuit structure of the integrator component.

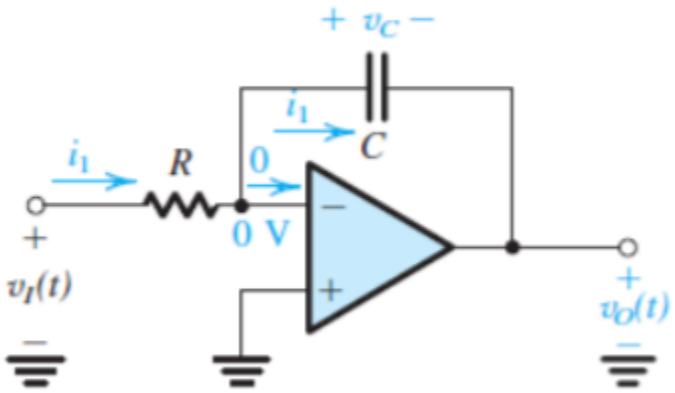



**Figure 4.3: Inverting integrator circuit structure.**

The derivation for the integrator's output voltage is demonstrated below:

$I(t) = V_I(t) / R$, $I(t) = -I_f(t)$ (currents through R and C are in different direction but with same magnitude.

$I_f(t) = dq/dt \Rightarrow Q = -\int_a^b I(t)\,dt$ and $V_C(t) = -\frac{1}{C}\int_a^b I(t)\,dt + V_C(t = 0^+)$.

Since $V_C(t = 0^+) = 0$Volts, $V_O(t) = \frac{-1}{RC}\int_a^b V_I(t)\,dt + V_C(t = 0^+)$.

**Figure 4.4** contains the output waveform of the integrator, which toggles between the high and low threshold voltage values.

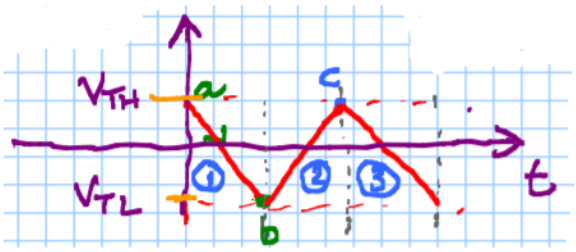



**Figure 4.4: Triangular wave output of the inverting integrator.**

The **Bistable Comparator** is an essential component in avoiding noise and unintended negative effects around the threshold voltage levels using the concept of "Hysteresis". Hysteresis, or "memory lag", allows for the output signal to "trip" at a slower rate relative to the input signal to prevent unwanted noise and distortion. **Figures 4.5-4.6** demonstrate the circuit structures of an inverting and noninverting bistable comparator.

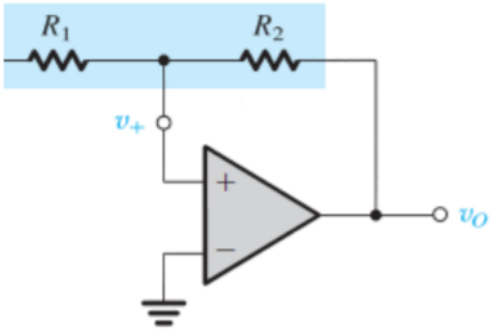



**Figure 4.5: Noninverting bistable comparator circuit structure.**

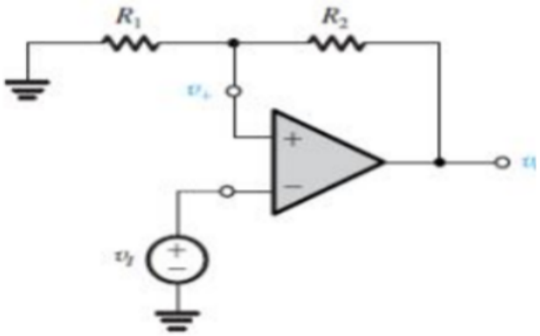



**Figure 4.6: Inverting bistable comparator circuit structure.**

Due to the voltage divider network that can be observed from the inverting bistable's feedback network, the output voltage and $V^+$relationship is defined as $V^+ = \frac{R_1}{R_1+R_2}V_O$.

With respect to the input and feedback resistors and the saturation voltages, it is necessary to understand the meaning of **high and low threshold** voltages.

When observing the combination of the integrator and the bistable comparator (noninverting), we have $V_{TH} = -\frac{R_1}{R_2}L^-$ and $V_{TL} = -\frac{R_1}{R_2}L^+$. However, with an inverting bistable comparator (used extensively to keep the overall feedback loop of the final design as negative, we have the same equations applying for high and low threshold voltage values. The major

difference is in the square wave output waveform, as when the polarity of the bistable is reversed, the output waveform is reflected through the x-axis.

**Amplitude control** is another key concept in this project that is used to meet one of the key requirements from the project manual. It is used to control the amplitude of the square and triangular output waveforms over two unique frequency ranges. This feature was implemented by using a gain control circuit, where a potentiometer is placed at the OP-AMP's feedback path to regulate the amplitude of the output waveform that is available. **Figure 4.7** demonstrates the block diagram representation of the amplitude control feature.

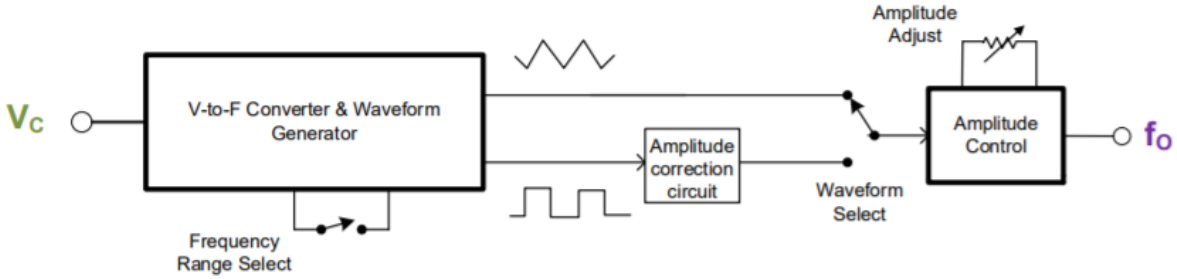



**Figure 4.7: Block diagram representation of the amplitude control feature when added to the voltage-controlled waveform generator.**

## 5. Design Analysis

The design of the voltage-controlled function generator consists of a DC-to-(+/-) DC converter, an inverting integrator, an inverting bistable multivibrator, and gain control circuits (contain potentiometer for gain control). There are certain requirements that must be met in order for the design to be successful and valid as per the project manual. First, the final circuit design must be able to operate at two frequency ranges: 100 Hz to 3100 Hz, and 20 Hz to 620 Hz. Next, amplitude control features must be added to have output voltage waveforms of 4 volts peak. Another major requirement is to use the control voltage $V_C$ and vary it from 0.1 to 5 volts D.C at the user's convenience to be able to test the frequency ranges #1 and #2. One final design requirement is to use +/- 10 volts D.C power supplies for design analysis, testing and verification stages of the project.

**Milestone 1** asks to design a fixed-frequency waveform generator using an inverting integrator and a noninverting bistable comparator. The output voltage is set at +/- 4 volts, whereas the high and low threshold voltages are calculated to be approximately 5.71 volts to stay below 6 volts. Using the equation $f_o = L^+ / 2\,RC\,(V_{TH} - V_{TL})$, along with a chosen capacitor value of 0.1 micro-farads, resistors $R = 1.2\text{k}\Omega$, $R_1 = 13.44\text{k}\Omega$, and $R_2 = 20\text{k}\Omega$ were calculated. By using these calculations to verify the output frequency, it is determined that the design analysis for this milestone is accurate with respect to the specifications. **Figure 5.1** demonstrates the overall circuit design for milestone 1.

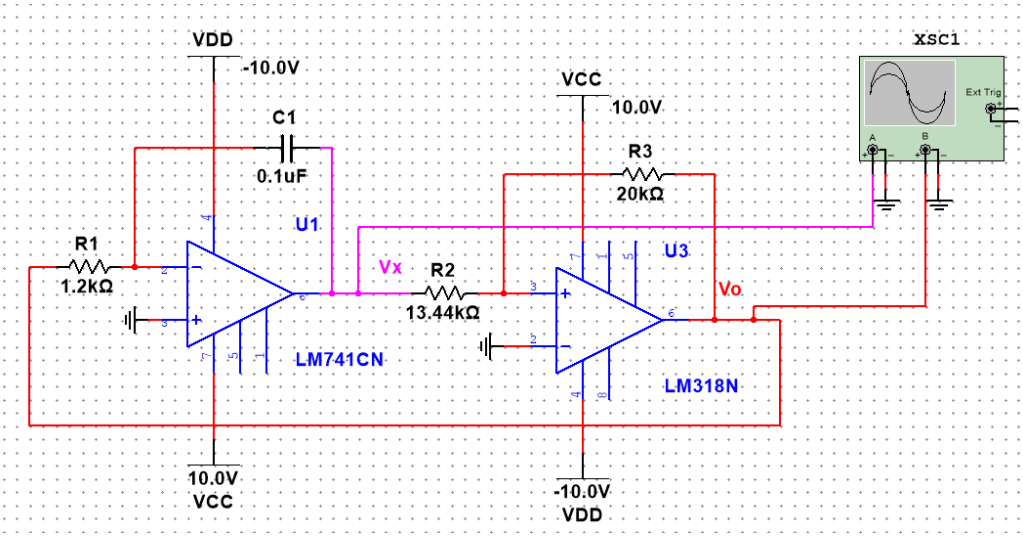



**Figure 5.1: Multisim schematic of the fixed-frequency waveform generator of milestone 1.**

**Milestone 2** requires a minor re-design of the fixed-frequency waveform generator, along with a separate design of a DC-to-(+/-) DC converter. Resistor values $R = 847.41\ \Omega$, $R_1 = 19.033$ kΩ, and $R_2 = 20\text{k}\Omega$ were calculated as per the given parameters from milestone 1. Next, the Zener diodes' voltages are calculated to be 5.3 volts with the assumption of 0.7 volts voltage drop for the regular diodes and the $L^+ = V_Z + V_D$ equation. Since it is assumed that $L^+ = |L^-|$, the equation $I_Z = (8.5\,V - 6\,V) / R_Z$ is used to calculate the resistor value at the bistable's output. The 1N4734 Zener diodes are chosen with a maximum Zener current of 20 mA and the LM318N OP-AMP has a maximum current of 22 A as per the datasheet. A 15 Amperes Zener current is chosen to calculate $R_Z = 166.67\Omega$ for milestone 2's design.

As for the DC converter, two cases of $V_o = 6$ V (output is at -5 volts for converter) and $V_o = -6$ V (output is at 5 volts for converter) are observed. From these two cases, resistor

values $R_1 = R_2 = R_4 = 100\text{k}\Omega$ and $R_3 = 100\Omega$ are picked with the conditions $R_1 = R_3$and $R_1 >> R_2$from the design analysis. **Figures 5.2-5.3** display the circuit schematics of the DC converter and the re-designed waveform generator.

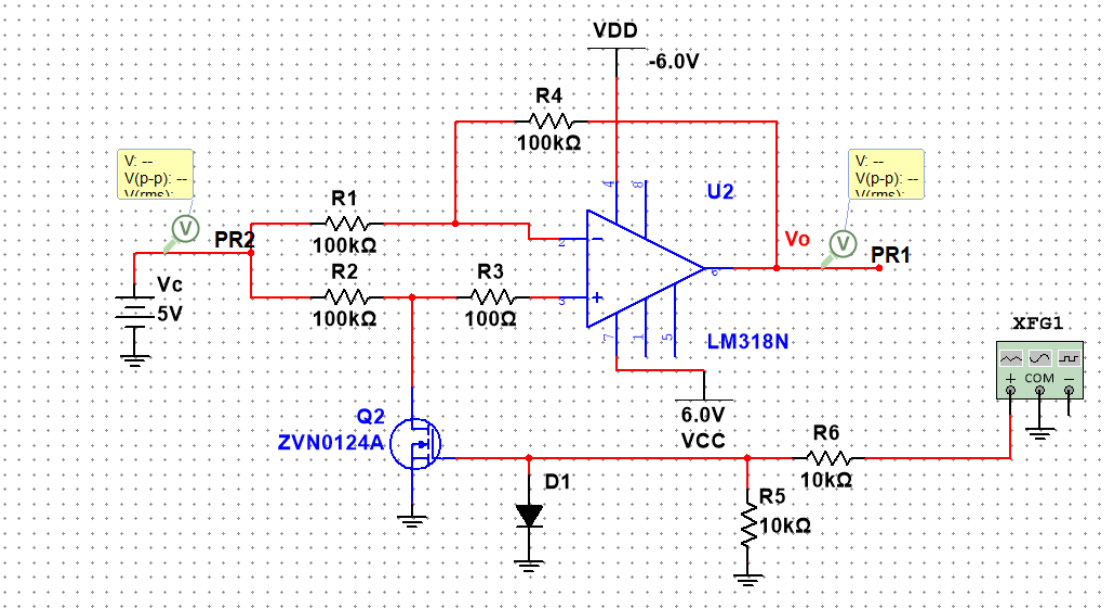



**Figure 5.2: Multisim schematic of the DC-to-(+/-) DC of milestone 2.**

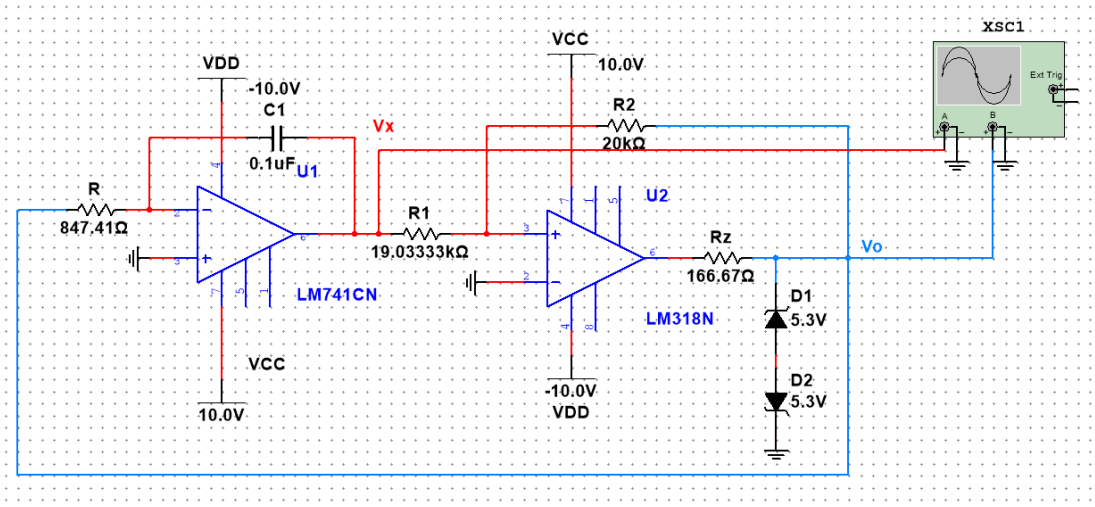



**Figure 5.3: Multisim schematic of the fixed-frequency waveform generator of milestone 2.**

**Milestone 3** combines puts together the DC converter and the waveform generator of milestone 2 to be tested together. From the new output frequency equation, the resistor value for integrator's input is calculated to be R = 706.18 Ω and based on $V_{TH} = 5.71$volts, $R_7 = 393,793.1\Omega$ and $R_8 = 20\text{k}\Omega$ are calculated as well. For the converter and the bistable's limiting circuit, the same parameters and values from milestone 2 are carried over to milestone 3's design. **Figure 5.4** depicts the circuit schematic of milestone 3 with all appropriate values for the components used.

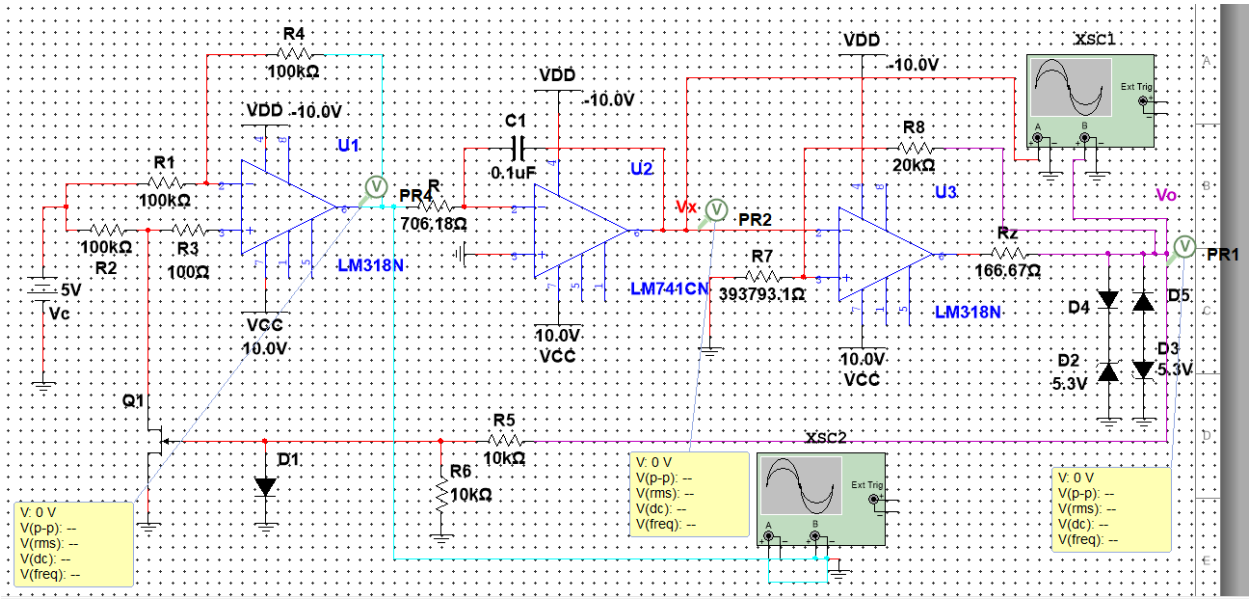



**Figure 5.4: Multisim schematic of linear voltage-controlled function generator (milestone 3).**

**Milestone 4** puts on the finishing touches to the work completed in milestone 3 to finalize the design of the linear voltage-controlled function generator. Features such as amplitude control and two different output frequency ranges are added as part of the major requirements of the design project. Using the output frequency equation, $R_{x1} = 706.18\Omega$ (for frequency range #1) and $R_{x2} = 3530.87$(for frequency range #2) Ω are calculated in the design analysis. A switch is used to alternate between these two input resistors. Next, the characteristic equation $V_C = L^+ \frac{R_7}{R_7+R_8}$is used to calculate $R_7 = 140845.07\Omega$ for the bistable's input resistor. The gain control circuits are implemented using an inverting OP-AMP with a potentiometer at its feedback path. The potentiometer is responsible for keeping the output voltage at around 4 volts peak. **Figures 5.5-5.6** contain the circuit schematics for frequency ranges #1 and #2.

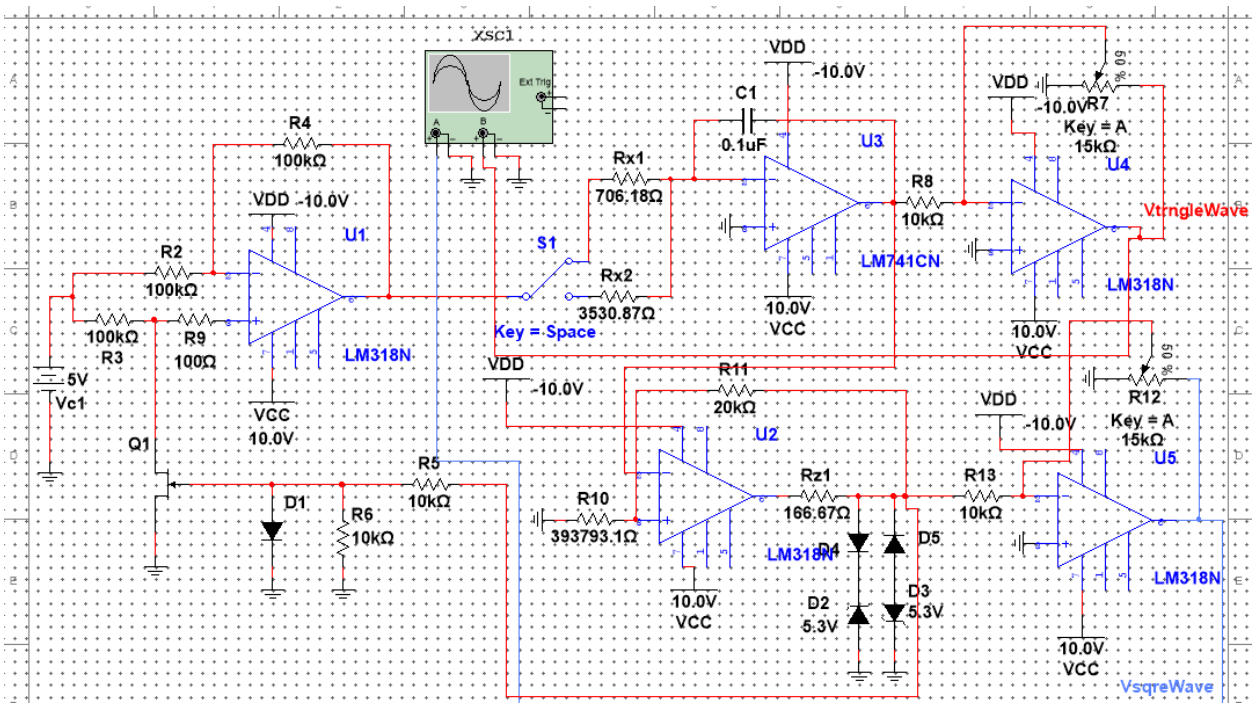



**Figure 5.5: Linear voltage-controlled waveform generator (frequency range #1).**

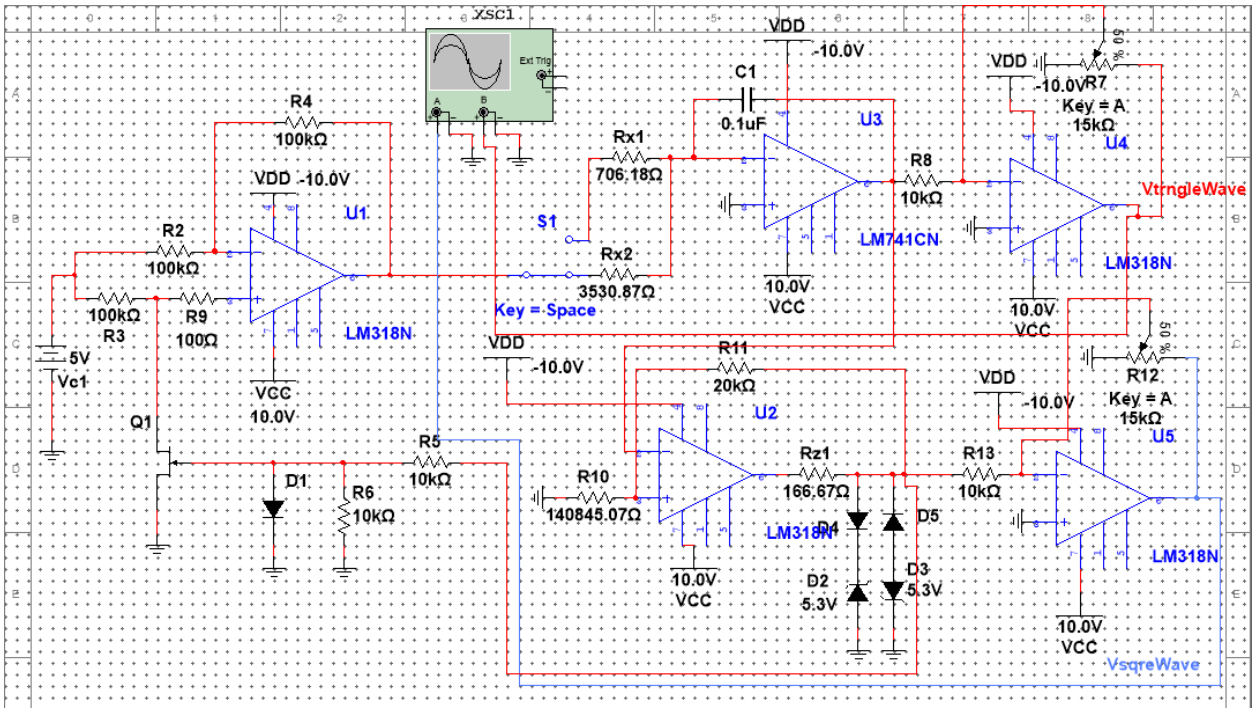



**Figure 5.6: Linear voltage-controlled waveform generator (frequency range #2).**

## 6. Experimental Procedure

The **fixed-frequency waveform generator** is constructed using an inverting integrator and a non-inverting bistable comparator, along with appropriate resistor and capacitor values from milestone 1. A triangular waveform is observed from the integrator's output and a square waveform is observed from the bistable's output. The Multisim schematic for this component is demonstrated in **Figure 6.1**.

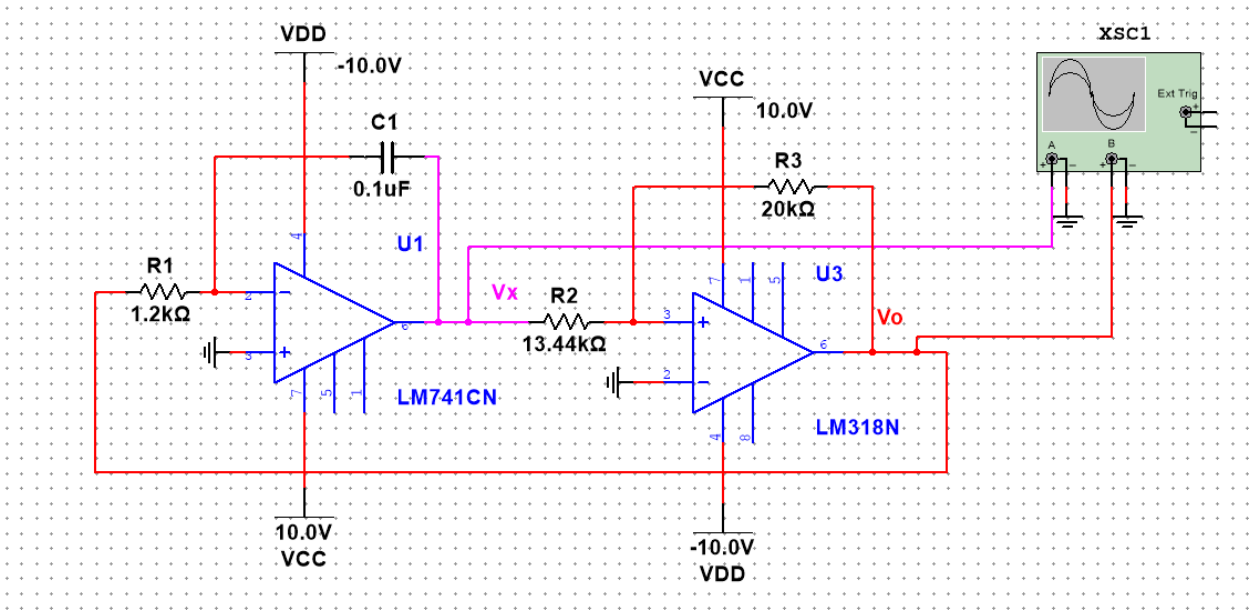



**Figure 6.1: Multisim schematic of the fixed-frequency waveform generator.**

The **DC-to-(+/-) DC converter** is used to provide a +/- DC signal of the control voltage as input for the inverting integrator. It is also responsible for ensuring that the overall feedback of the loop stays negative and has a consistent output. The output of this component is a square waveform with amplitude $V_C$, and its Multisim schematic is presented in **Figure 6.2**.

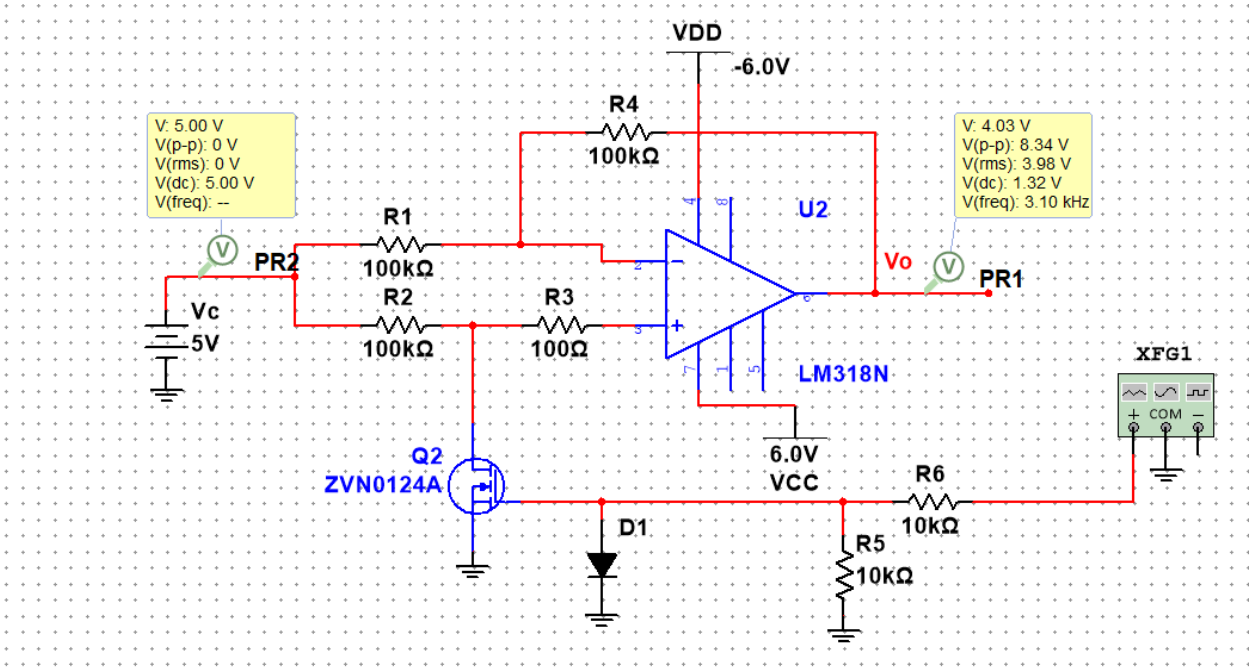



**Figure 6.2: Multisim schematic of the DC-to-(+/-) DC converter.**

With the proper implementation of the two components mentioned above, the **linear voltage-controlled function generator** can be built by putting together the DC converter and the waveform generator in cascading manner. One change to the circuit is the change of the bistable's polarity to inverting mode, as a way of keeping the overall feedback loop of the circuit negative. A BJT (Bipolar Junction Transistor) is also used in saturation mode to allow the comparator to oscillate between its upper and lower saturation voltage levels ($L^+$and $L^-$).

**Figure 6.3** demonstrates the Multisim schematic of the linear voltage-controlled function generator.

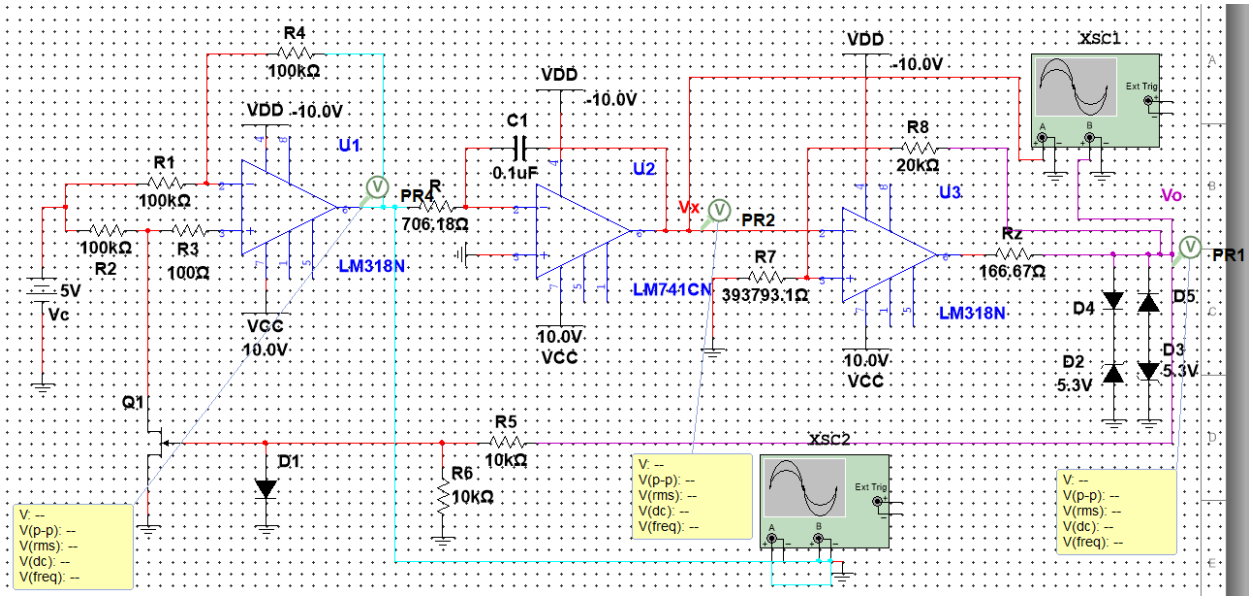



**Figure 6.3: Multisim schematic of the linear voltage-controlled Function Generator.**

In order to accommodate for the **frequency and range control features** at the user's end, the voltage-controlled function generator is re-designed using a switch and gain control circuits to add these features for the final design. The switch allows to alternate between different input resistors for the integrator's input, where the circuit can operate in frequency range #1 (100 Hz to 3100 Hz) or frequency range #2 (20 Hz to 620 Hz). As for the gain control circuit, a potentiometer is included in its feedback loop to control the amplitude of the output voltage for the square and triangular waveforms.

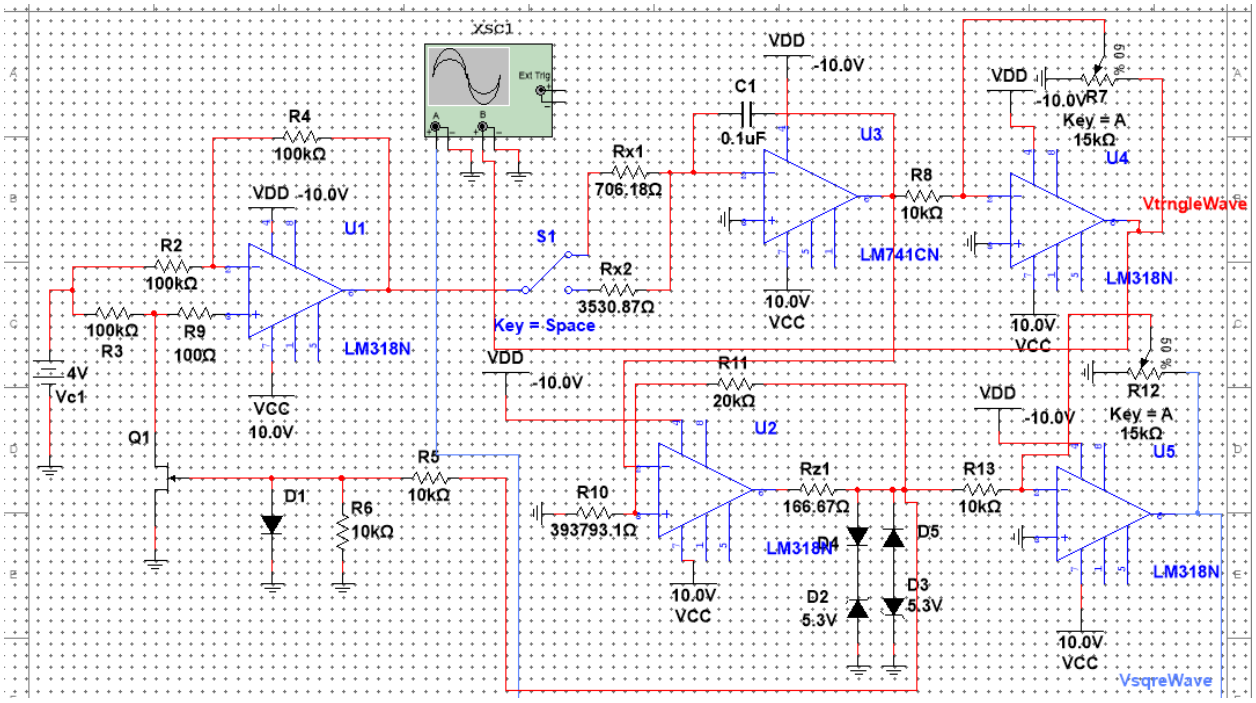



**Figure 6.4: Multisim schematic of the linear voltage-controlled Function Generator (Range #1).**

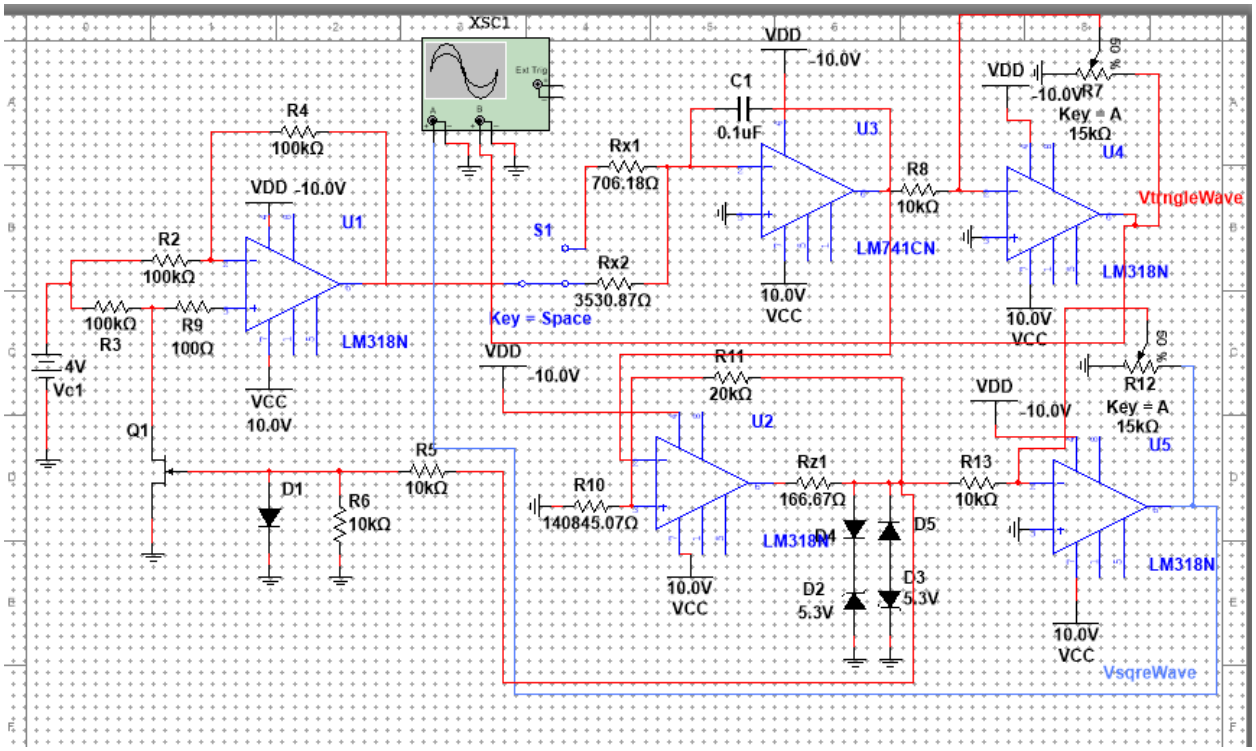



**Figure 6.5: Multisim schematic of the linear voltage-controlled Function Generator (Range #2).**

All circuits are tested for verification using the Multisim simulation environment. For each testing stage, appropriate waveforms and data are extracted for further analysis to compare experimental results with the respective design analysis.

## 7. Results and Observations

In **milestone 1**, the fixed-frequency waveform generator was tested with an LM741CN and an LM318 OP-AMP connected in cascading manner. The output frequency was measured to be approximately 3104.65 Hz, very close to the desired frequency of 3100 Hz. The output waveforms for this milestone are presented in **Figure 7.1**.

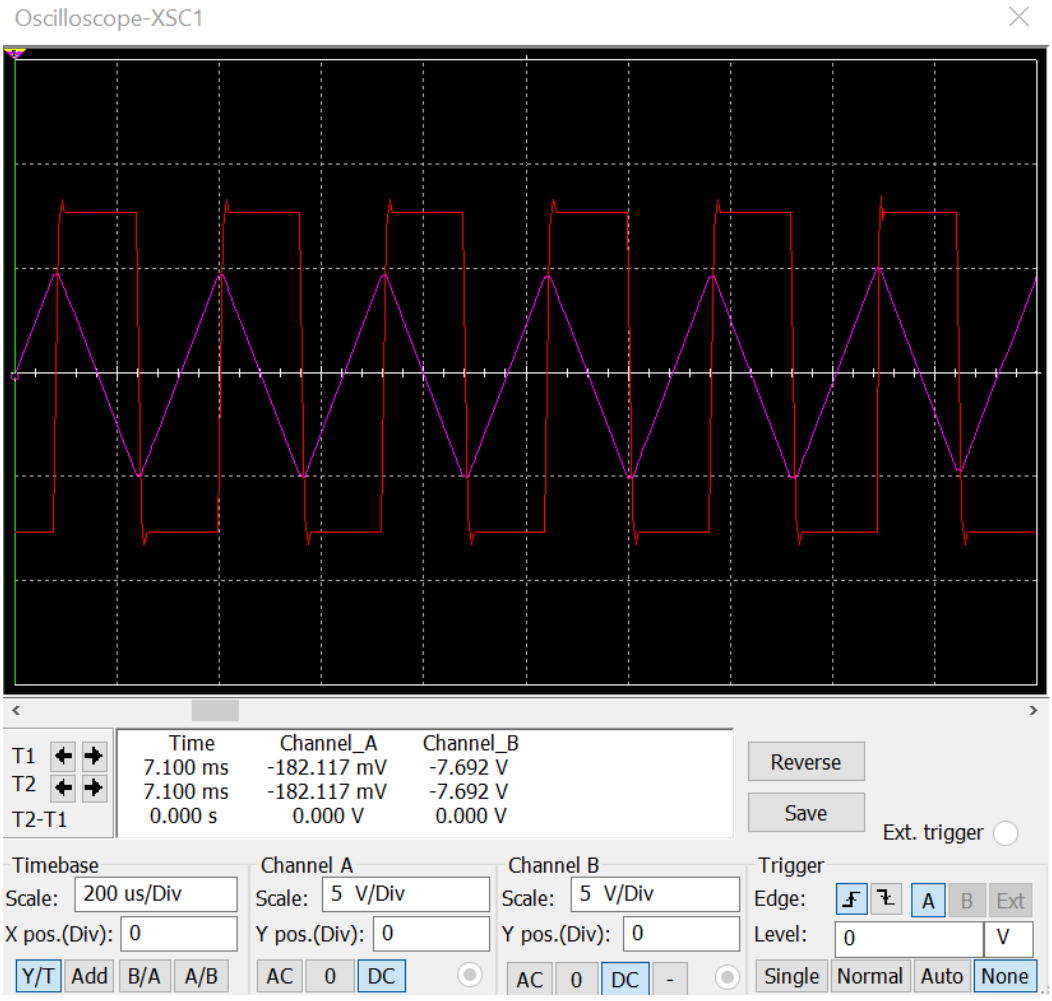



**Figure 7.1: Square and triangular waveforms of the fixed-frequency waveform generator.**

In **milestone 2**, the fixed-frequency waveform generator was re-designed with an additional limiting circuit to provide more of a consistent output voltage waveform from the bistable's output. The frequency measurement is now 3141.18 Hz, slightly higher than the measurement in milestone 1 but in an acceptable range. In addition, a DC-to-(+/-) DC converter was also built and tested as a separate component. This component will be combined with the waveform generator for milestone 3 to provide an input control voltage that will vary the circuit's output frequency. **Figures 7.2-7.3** contain the output waveforms for the re-designed waveform generator and the simulation results of the DC converter.

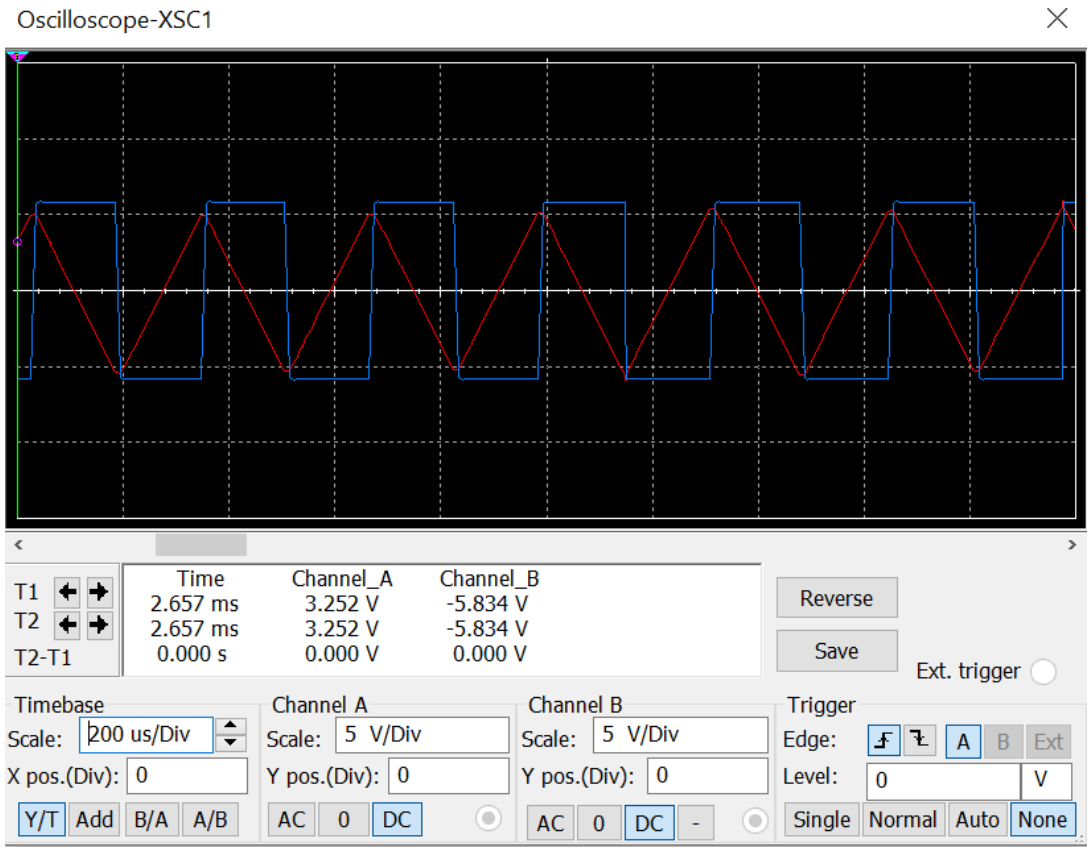



**Figure 7.2: Output waveforms of the re-designed fixed-frequency waveform generator.**

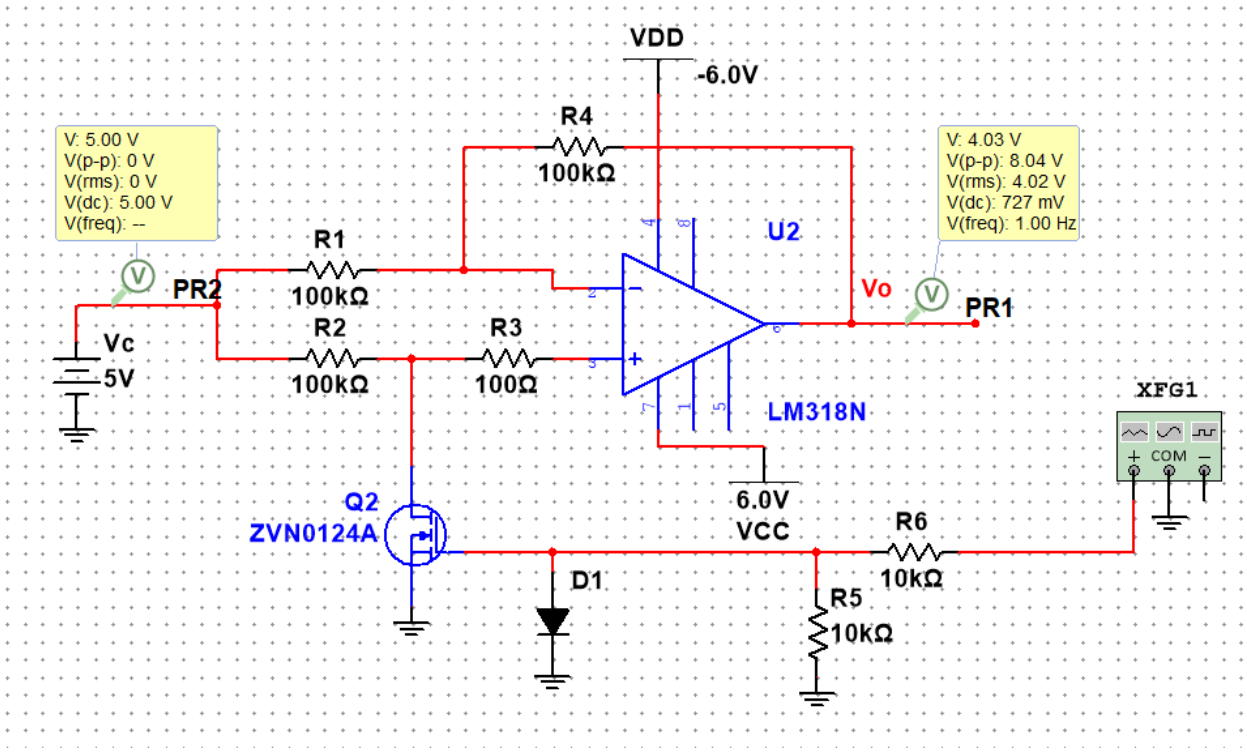



**Figure 7.3: Simulation result of the DC-to-(+/-) DC converter (5 Volts D.C control voltage).**

In **milestone 3**, the DC converter and the re-designed waveform generator are combined together for testing. One change that has been made is to use an inverting bistable comparator, to keep the overall feedback loop of the circuit negative. The output frequency measurement continues to be very accurate and close to the desired 3100 Hz, whereas the outputs of integrator and bistable are not available for 3 volts D.C control voltage due to a bizarre error with the circuit. **Figures 7.4-7.5** demonstrate the output waveforms for the overall circuit and the DC converter. In addition, **Table 7.1** is used to compare the outputs of the integrator and the bistable for control voltage values of 0.1 to 5 volts D.C.

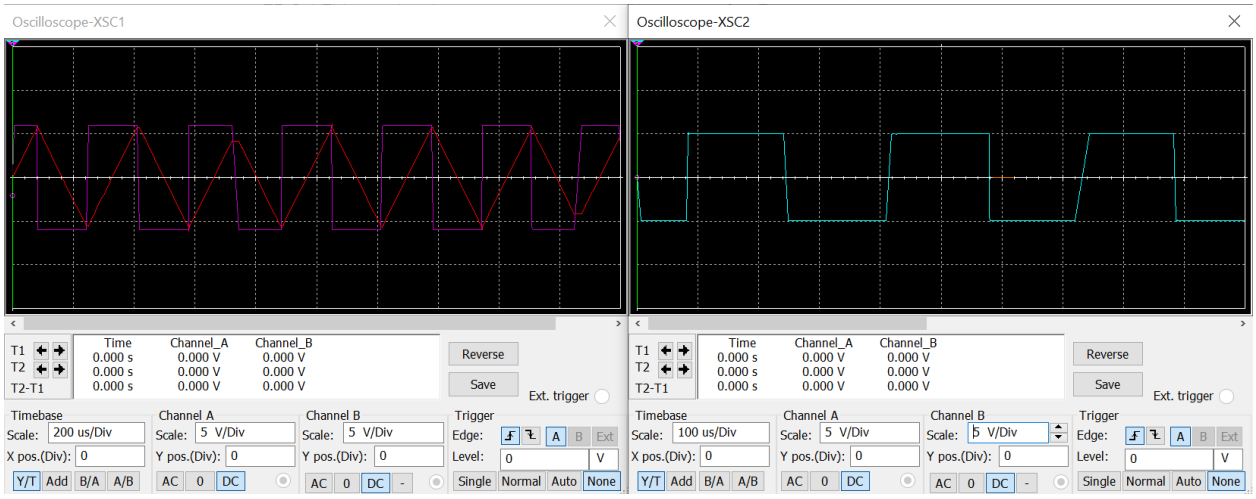



**Figure 7.4: Output waveforms of the re-designed fixed-frequency waveform generator in milestone 3.**

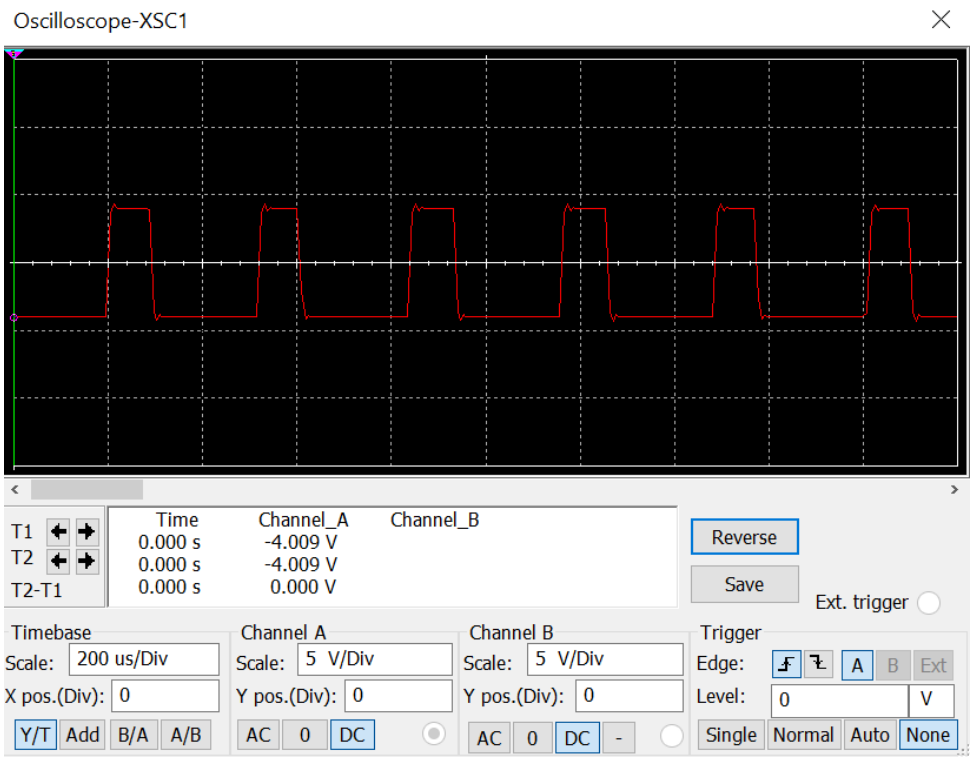



**Figure 7.5: Output waveform of the DC-to-(+/-) DC converter.**

**Table 7.1: Outputs of the integrator and bistable for control voltage values of 0.1 volts to 5 volts.**

| Control Voltage [Volts] | Expected Frequency [Hz] | Actual Frequency [Hz] | DC-DC Output Peak Voltage [Volts] | Expected Integrator Output Peak Voltage [Volts] | Actual Integrator Output Peak Voltage [Volts] | Bistable Output Peak Voltage [Volts] |
|---|---|---|---|---|---|---|
| **0.1** | 62 | 50.9 | 5.996 | 5.71 | 5.75 | 7.6 |
| **1** | 620 | 604 | 5.996 | 5.71 | 5.9 | 7.7 |
| **2** | 1240 | N/A | N/A | 5.71 | N/A | N/A |
| **3** | 1860 | 1872 | 5.996 | 5.71 | 5.95 | 7.75 |
| **4** | 2480 | 2410 | 5.996 | 5.71 | 5.4 | 7.85 |
| **5** | 3100 | 3060 | 5.996 | 5.71 | 5.6 | 7.85 |

In **milestone 4**, the frequency range and amplitude control features are added to the final design from milestone 3. The square and triangular output waveforms from the integrator and bistable are amplitude-modulated using the gain control circuits that contain potentiometers. The amplitude of the output voltage was controlled to be at around 4.33 volts, which is very close to the desired 4 volts requirement. As for the frequency range, the output frequencies for each frequency range are fairly consistent with the desired values from the project manual, with the only exception being the frequency of range #1 at 4 volts D.C failing to display in Multisim. It is another bizarre error that was, unfortunately, damaging to the gathering process of results for this milestone. **Figure 7.6-7.7** demonstrates the output waveforms (square and triangular) for the linear voltage-controlled function generator, and **table 7.2** contains the expected and actual output frequencies for frequency ranges #1 and #2.

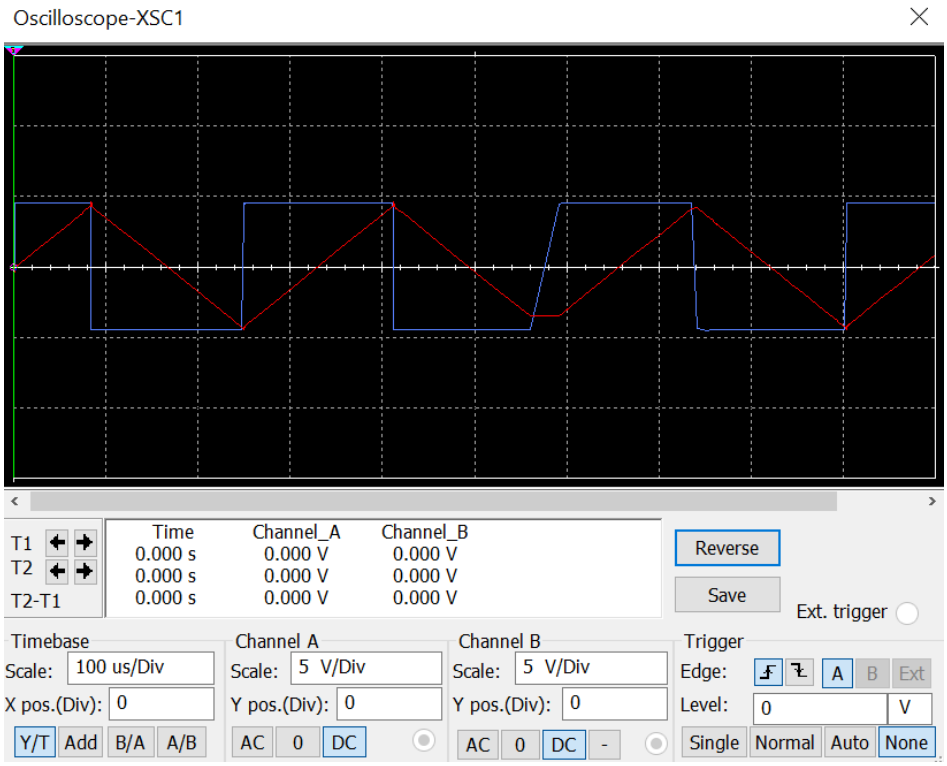



**Figure 7.5: Output waveforms of the linear voltage-controlled function generator (frequency range #1).**

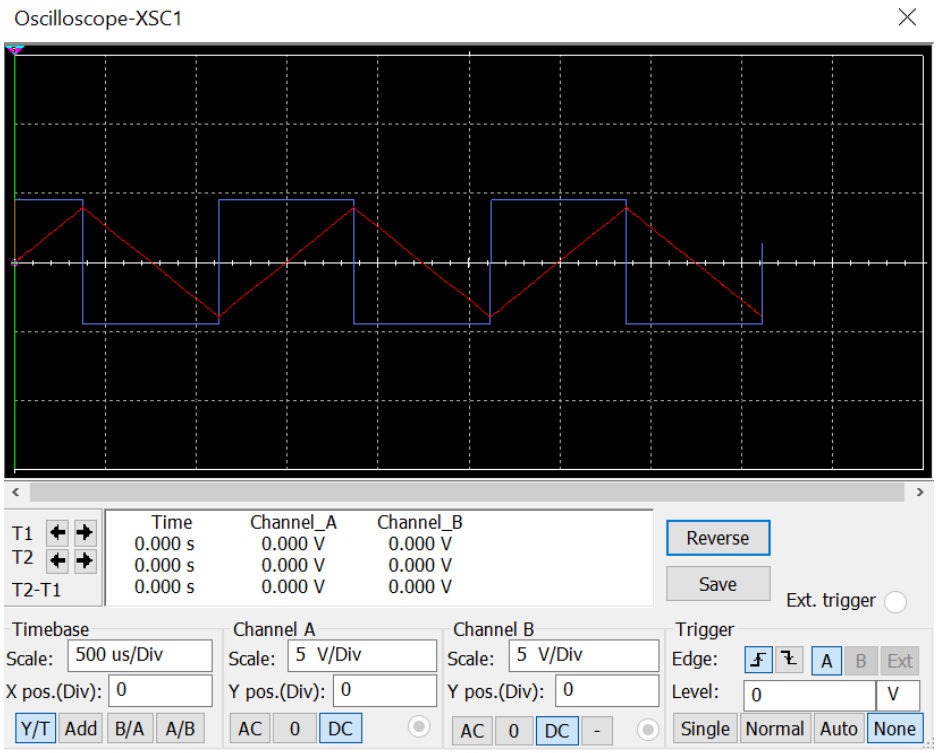



**Figure 7.6: Output waveforms of the linear voltage-controlled function generator (frequency range #2).**

**Table 7.2: Expected and actual frequency for control voltage values of 0.1 volts to 5 volts (range #1 and range #2 under examination).**

| Control Voltage [V] | Expected Frequency (fx range) [Hz] | Actual Frequency (fx range) [Hz] | Expected Frequency (fx/5 range) [Hz] | Expected Frequency (fx/5 range) [Hz] |
|---|---|---|---|---|
| **0.1** | 62 | 46.97 | 12.4 | 10.35 |
| **1** | 620 | 550.66 | 124 | 132.17 |
| **2** | 1240 | 1224.77 | 248 | 267.88 |
| **3** | 1860 | 1832.95 | 372 | 402.58 |
| **4** | 2480 | N/A | 496 | 539.37 |
| **5** | 3100 | 3045.60 | 620 | 672.95 |

## 8. Conclusions and Recommendations

This design project is considered to be a successful project where the voltage-controlled function generator's design analysis is well-aligned with the Multisim simulation results. Through the use of 5 OP-AMPs, a Bipolar Junction Transistor, Zener diodes, resistors, and capacitors, the output frequency of 3100 Hz was achieved as one of the fundamental requirements of this project. This parameter was essential in calculating the quantities of resistors and capacitors, thus leading to the completion of the design analysis and using Multisim simulations to verify each design milestone. The square and triangular output waveforms (with an amplitude of around 4.33 volts) are clearly visible in the simulation results, which meets another of the important requirements. Another major requirement is to accommodate for user-selectable frequency ranges, which has been completed using a switch to alternate between frequency ranges #1 and #2 at the user's convenience.

The first milestone was a great opportunity to gain an understanding of the design and operation of a fixed-frequency waveform generator. As per the expectations from the design analysis, the integrator's triangular waveform output varies between $V_{TH}$and $V_{TL}$values, whereas the bistable's square wave output varies between $L^{+}$and $L^{-}$.

The second milestone introduces a voltage-controlled waveform generator to be able to control the output frequency of the circuit by varying its control voltage, $V_{C}$. A DC-to-(+/-) DC converter was also used to convert the DC control voltage to a square wave signal that is fed to the integrator. This milestone's major accomplishment was the stabilization of the output voltage waveforms and the varying of the output frequency with the control voltage.

The third milestone integrates the waveform generator and the DC converter together to allow for the frequency modulation feature to be active for the whole circuit. It also reiterates the importance of the Zener diodes used to provide a stable and consistent output waveform for the circuit. As this milestone finalizes the design for frequency range #1 without amplitude control, another milestone is required to add the final features of the circuit for the final design.

The fourth milestone adds the finishing touches to the voltage-controlled function generator: frequency range and amplitude control. Through the use of a switch at the integrator's input, the user can alternate between frequency range #1 (100 Hz to 3100 Hz) and frequency range #2 (20 Hz to 620 Hz). A gain control circuit is used at the integrator and the bistable's outputs to control the amplitude of the output waveforms at around 4 volts. There are certain imperfections of the nature of the circuit that make the simulation results deviate slightly from the design analysis, but the amount of error is not a significant issue. However, the major issue is the failure to obtain an output frequency for range #1 at one of the control voltage values, which bizarrely occurred in milestone 3 as well, despite the circuit being wired properly.

As part of the design process, it is necessary to always look for ways to resolve further issues that may arise in the future. One recommendation is to implement the final design on real-life lab hardware (which contains breadboard with circuit components) to be able to re-test and obtain the missing results for finalizing the data collected from the simulations. It is also important to accommodate for design limitations at earlier stages of the 5 milestones, as a way of preventing future re-calculations and adjustments that can be time-consuming. With all things considered, this project has been a success and an overall great experience.

## 9. References and Bibliography

[1] A. Sedra and K. Smith, Microelectronic Circuits. New York, NY: Oxford University Press, 2016.

[2] Major Project - MP (virtual). Kassam M S, 2021.

[3] “Datasheets”, ELE504, 2021. [Online]. Available:

https://courses.ryerson.ca/d2l/le/content/528142/viewContent/3806349/View

## 10. Appendix

For this project, the LM741CN and LM318N OP-AMPs’ data sheets were provided and used extensively in the design analysis section to appropriately design circuits for each milestone with adherence to specifications and conditions of the circuits and their components. In addition, the 1N4734 Zener diodes’ data sheet was also used in the design analysis of the limiting circuit component for the bistable’s output. The data sheets are attached to this report for further reference.

# LM741 Operational Amplifier

**Check for Samples: LM741**

## FEATURES

- **Overload Protection on the Input and Output**
- **No Latch-Up When the Common Mode Range is Exceeded**

## DESCRIPTION

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance ensured over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

## Connection Diagrams

LM741H is available per JM38510/10101

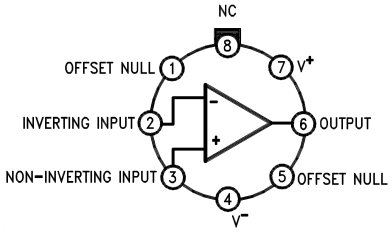



**Figure 1. TO-99 Package**
**See Package Number LMC0008C**

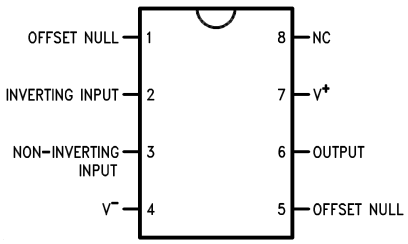



**Figure 2. CDIP or PDIP Package**
**See Package Number NAB0008A, P0008E**

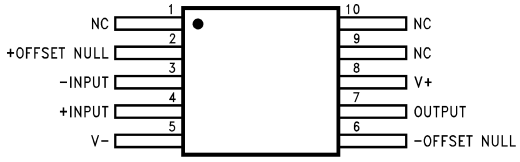



**Figure 3. CLGA Package**
**See Package Number NAD0010A**

## Typical Application

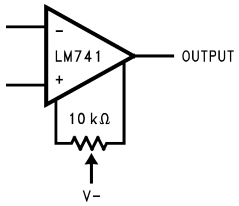



**Figure 4. Offset Nulling Circuit**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)(3)

| | LM741A | LM741 | LM741C |
|---|---|---|---|
| Supply Voltage | ±22V | ±22V | ±18V |
| Power Dissipation (4) | 500 mW | 500 mW | 500 mW |
| Differential Input Voltage | ±30V | ±30V | ±30V |
| Input Voltage (5) | ±15V | ±15V | ±15V |
| Output Short Circuit Duration | Continuous | Continuous | Continuous |
| Operating Temperature Range | −55°C to +125°C | −55°C to +125°C | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Junction Temperature | 150°C | 150°C | 100°C |
| Soldering Information | | | |
| P0008E-Package (10 seconds) | 260°C | 260°C | 260°C |
| NAB0008A- or LMC0008C-Package (10 seconds) | 300°C | 300°C | 300°C |
| M-Package | | | |
| Vapor Phase (60 seconds) | 215°C | 215°C | 215°C |
| Infrared (15 seconds) | 215°C | 215°C | 215°C |
| ESD Tolerance (6) | 400V | 400V | 400V |

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) For military specifications see RETS741X for LM741 and RETS741AX for LM741A.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) For operation at elevated temperatures, these devices must be derated based on thermal resistance, and $T_j$ max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.
(5) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
(6) Human body model, 1.5 kΩ in series with 100 pF.

## Electrical Characteristics(1)

| Parameter | Test Conditions | LM741A | | | LM741 | | | LM741C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A$ = 25°C<br>$R_S \le 10$ kΩ<br>$R_S \le 50$Ω | | 0.8 | 3.0 | | 1.0 | 5.0 | | 2.0 | 6.0 | mV |
| | $T_{AMIN} \le T_A \le T_{AMAX}$<br>$R_S \le 50$Ω<br>$R_S \le 10$ kΩ | | | 4.0 | | | 6.0 | | | 7.5 | mV |
| Average Input Offset Voltage Drift | | | | 15 | | | | | | | µV/°C |

(1) Unless otherwise specified, these specifications apply for $V_S$ = ±15V, −55°C ≤ $T_A$ ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ $T_A$ ≤ +70°C.

## Electrical Characteristics[1] (continued)

| Parameter | Test Conditions | LM741A | | | LM741 | | | LM741C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage Adjustment Range | $T_A$ = 25°C, $V_S$ = ±20V | ±10 | | | | ±15 | | | ±15 | | mV |
| Input Offset Current | $T_A$ = 25°C | | 3.0 | 30 | | 20 | 200 | | 20 | 200 | nA |
| | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | 70 | | 85 | 500 | | | 300 | |
| Average Input Offset Current Drift | | | | 0.5 | | | | | | | nA/°C |
| Input Bias Current | $T_A$ = 25°C | | 30 | 80 | | 80 | 500 | | 80 | 500 | nA |
| | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | 0.210 | | | 1.5 | | | 0.8 | µA |
| Input Resistance | $T_A$ = 25°C, $V_S$ = ±20V | 1.0 | 6.0 | | 0.3 | 2.0 | | 0.3 | 2.0 | | MΩ |
| | $T_{AMIN} \le T_A \le T_{AMAX}$, $V_S$ = ±20V | 0.5 | | | | | | | | | |
| Input Voltage Range | $T_A$ = 25°C | | | | | | | ±12 | ±13 | | V |
| | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | | ±12 | ±13 | | | | | |
| Large Signal Voltage Gain | $T_A$ = 25°C, $R_L \ge 2$ kΩ | | | | | | | | | | V/mV |
| | $V_S$ = ±20V, $V_O$ = ±15V | 50 | | | | | | | | | |
| | $V_S$ = ±15V, $V_O$ = ±10V | | | | 50 | 200 | | 20 | 200 | | |
| | $T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2$ kΩ, | | | | | | | | | | V/mV |
| | $V_S$ = ±20V, $V_O$ = ±15V | 32 | | | | | | | | | |
| | $V_S$ = ±15V, $V_O$ = ±10V | | | | 25 | | | 15 | | | |
| | $V_S$ = ±5V, $V_O$ = ±2V | 10 | | | | | | | | | |
| Output Voltage Swing | $V_S$ = ±20V | | | | | | | | | | V |
| | $R_L \ge 10$ kΩ | ±16 | | | | | | | | | |
| | $R_L \ge 2$ kΩ | ±15 | | | | | | | | | |
| | $V_S$ = ±15V | | | | | | | | | | V |
| | $R_L \ge 10$ kΩ | | | | ±12 | ±14 | | ±12 | ±14 | | |
| | $R_L \ge 2$ kΩ | | | | ±10 | ±13 | | ±10 | ±13 | | |
| Output Short Circuit Current | $T_A$ = 25°C | 10 | 25 | 35 | | 25 | | | 25 | | mA |
| | $T_{AMIN} \le T_A \le T_{AMAX}$ | 10 | | 40 | | | | | | | |
| Common-Mode Rejection Ratio | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | | | | | | | | dB |
| | $R_S \le 10$ kΩ, $V_{CM}$ = ±12V | | | | 70 | 90 | | 70 | 90 | | |
| | $R_S \le 50$Ω, $V_{CM}$ = ±12V | 80 | 95 | | | | | | | | |
| Supply Voltage Rejection Ratio | $T_{AMIN} \le T_A \le T_{AMAX}$, | | | | | | | | | | dB |
| | $V_S$ = ±20V to $V_S$ = ±5V | | | | | | | | | | |
| | $R_S \le 50$Ω | 86 | 96 | | | | | | | | |
| | $R_S \le 10$ kΩ | | | | 77 | 96 | | 77 | 96 | | |
| Transient Response | $T_A$ = 25°C, Unity Gain | | | | | | | | | | |
| Rise Time | | | 0.25 | 0.8 | | 0.3 | | | 0.3 | | µs |
| Overshoot | | | 6.0 | 20 | | 5 | | | 5 | | % |
| Bandwidth [2] | $T_A$ = 25°C | 0.437 | 1.5 | | | | | | | | MHz |
| Slew Rate | $T_A$ = 25°C, Unity Gain | 0.3 | 0.7 | | | 0.5 | | | 0.5 | | V/µs |
| Supply Current | $T_A$ = 25°C | | | | | 1.7 | 2.8 | | 1.7 | 2.8 | mA |
| Power Consumption | $T_A$ = 25°C | | | | | | | | | | mW |
| | $V_S$ = ±20V | | 80 | 150 | | | | | | | |
| | $V_S$ = ±15V | | | | | 50 | 85 | | 50 | 85 | |

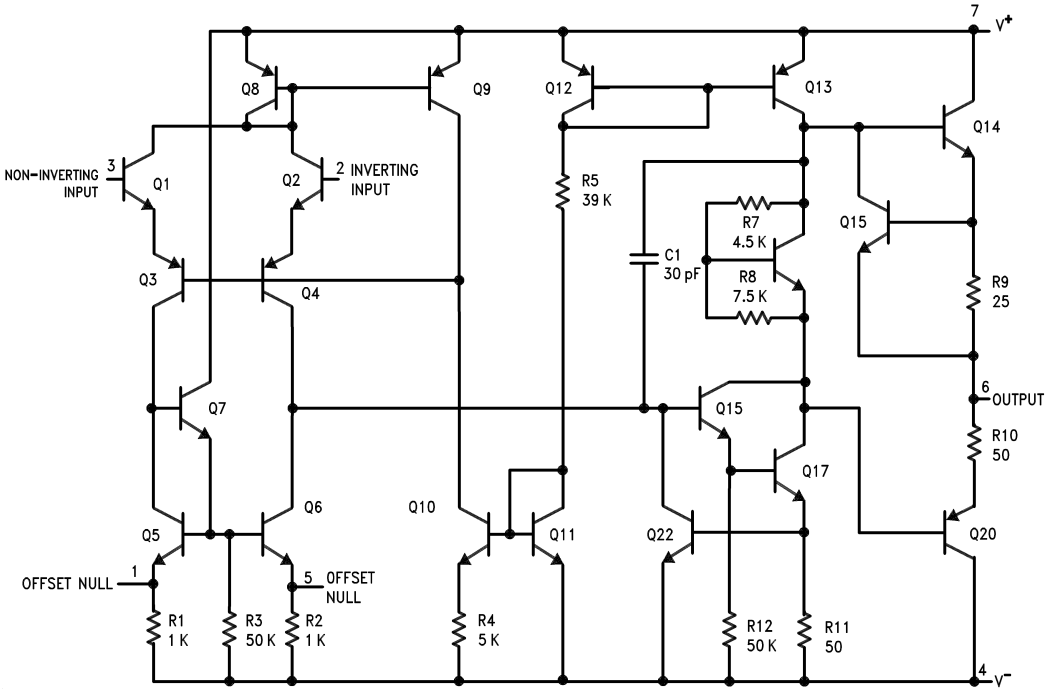
(2) Calculated value from: BW (MHz) = 0.35/Rise Time (µs).

## Electrical Characteristics[1] (continued)

| Parameter | Test Conditions | LM741A | | | LM741 | | | LM741C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| LM741A | $V_S$ = ±20V | | | | | | | | | | |
| | $T_A = T_{AMIN}$ | | | 165 | | | | | | | mW |
| | $T_A = T_{AMAX}$ | | | 135 | | | | | | | |
| LM741 | $V_S$ = ±15V | | | | | | | | | | |
| | $T_A = T_{AMIN}$ | | | | | 60 | 100 | | | | mW |
| | $T_A = T_{AMAX}$ | | | | | 45 | 75 | | | | |

| Thermal Resistance | CDIP (NAB0008A) | PDIP (P0008E) | TO-99 (LMC0008C) | SO-8 (M) |
|---|---|---|---|---|
| $\theta_{jA}$ (Junction to Ambient) | 100°C/W | 100°C/W | 170°C/W | 195°C/W |
| $\theta_{jC}$ (Junction to Case) | N/A | N/A | 25°C/W | N/A |

## SCHEMATIC DIAGRAM



## REVISION HISTORY

| Changes from Revision B (March 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 4 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM741CH | ACTIVE | TO-99 | LMC | 8 | 500 | TBD | Call TI | Call TI | 0 to 70 | LM741CH | Samples |
| LM741CH/NOPB | ACTIVE | TO-99 | LMC | 8 | 500 | Green (RoHS & no Sb/Br) | POST-PLATE | Level-1-NA-UNLIM | 0 to 70 | LM741CH | Samples |
| LM741CN | LIFEBUY | PDIP | P | 8 | 40 | TBD | Call TI | Call TI | 0 to 70 | LM 741CN | |
| LM741CN/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | 0 to 70 | LM 741CN | Samples |
| LM741H | ACTIVE | TO-99 | LMC | 8 | 500 | TBD | Call TI | Call TI | -55 to 125 | LM741H | Samples |
| LM741H/NOPB | ACTIVE | TO-99 | LMC | 8 | 500 | Green (RoHS & no Sb/Br) | POST-PLATE | Level-1-NA-UNLIM | -55 to 125 | ( LM741H ~ LM741H) | Samples |
| LM741J | ACTIVE | CDIP | NAB | 8 | 40 | TBD | Call TI | Call TI | -55 to 125 | LM741J | Samples |
| U5B7741312 | ACTIVE | TO-99 | LMC | 8 | 500 | TBD | Call TI | Call TI | -55 to 125 | LM741H | Samples |
| U5B7741393 | ACTIVE | TO-99 | LMC | 8 | 500 | TBD | Call TI | Call TI | 0 to 70 | LM741CH | Samples |
| U9T7741393 | LIFEBUY | PDIP | P | 8 | 40 | TBD | Call TI | Call TI | 0 to 70 | LM 741CN | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

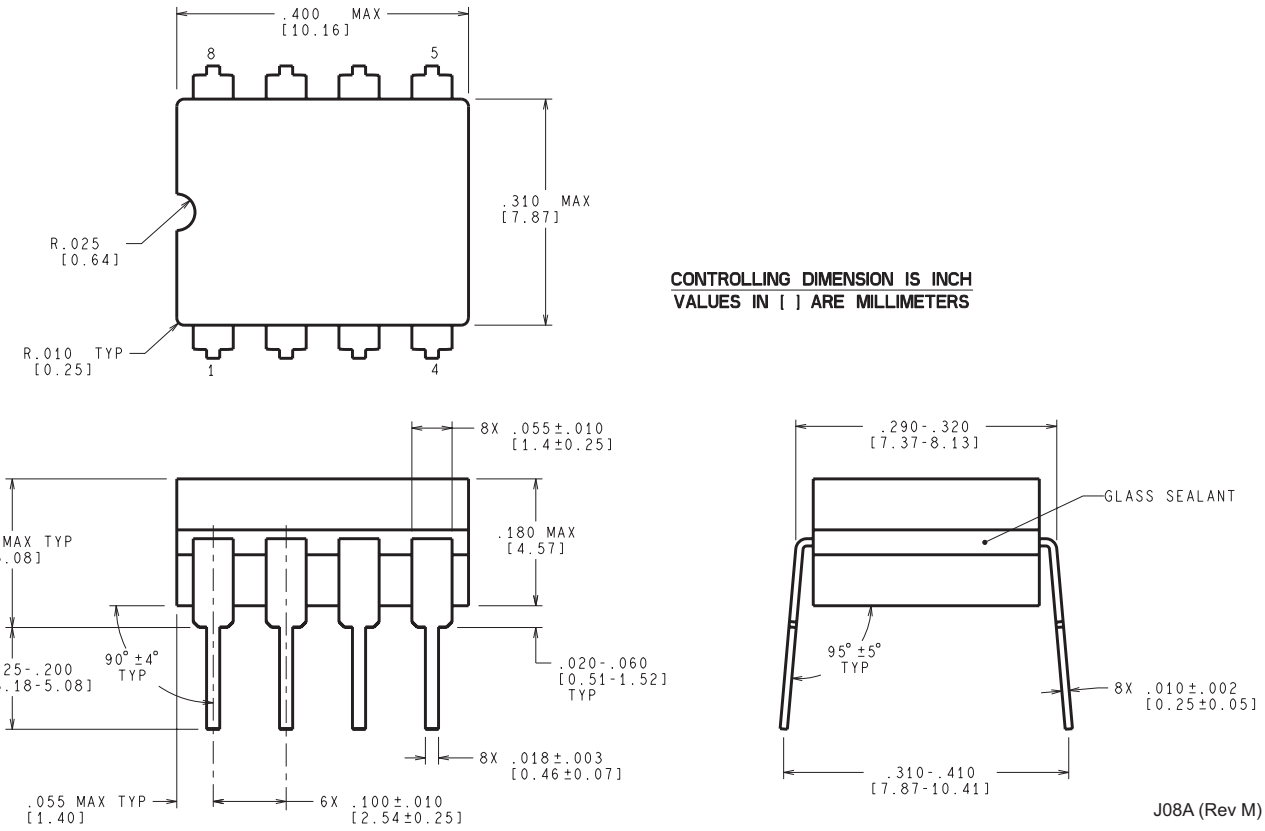
**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

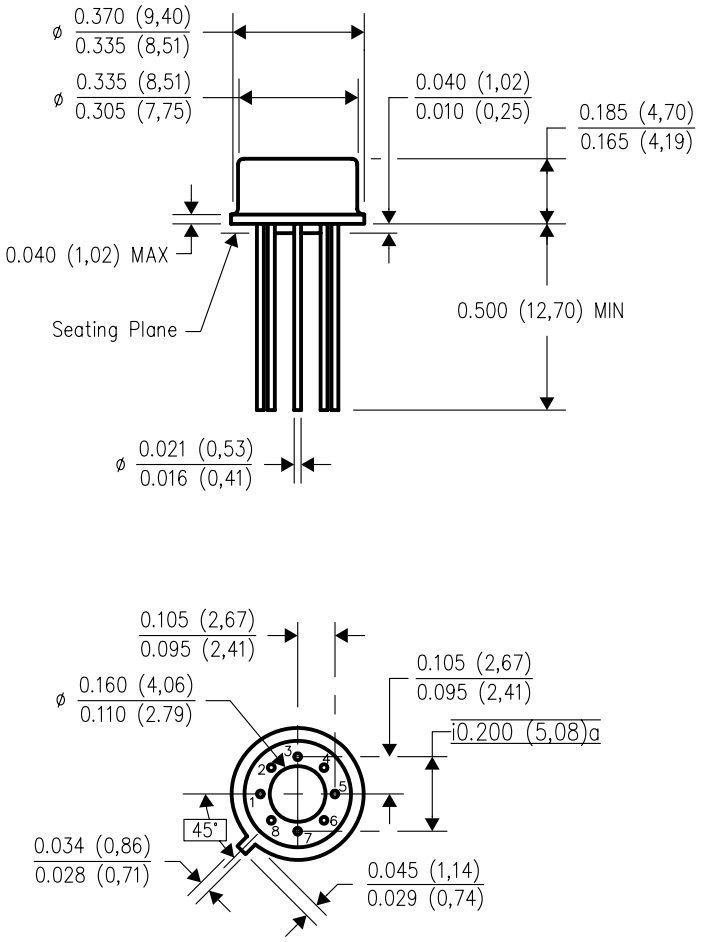
**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

# NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

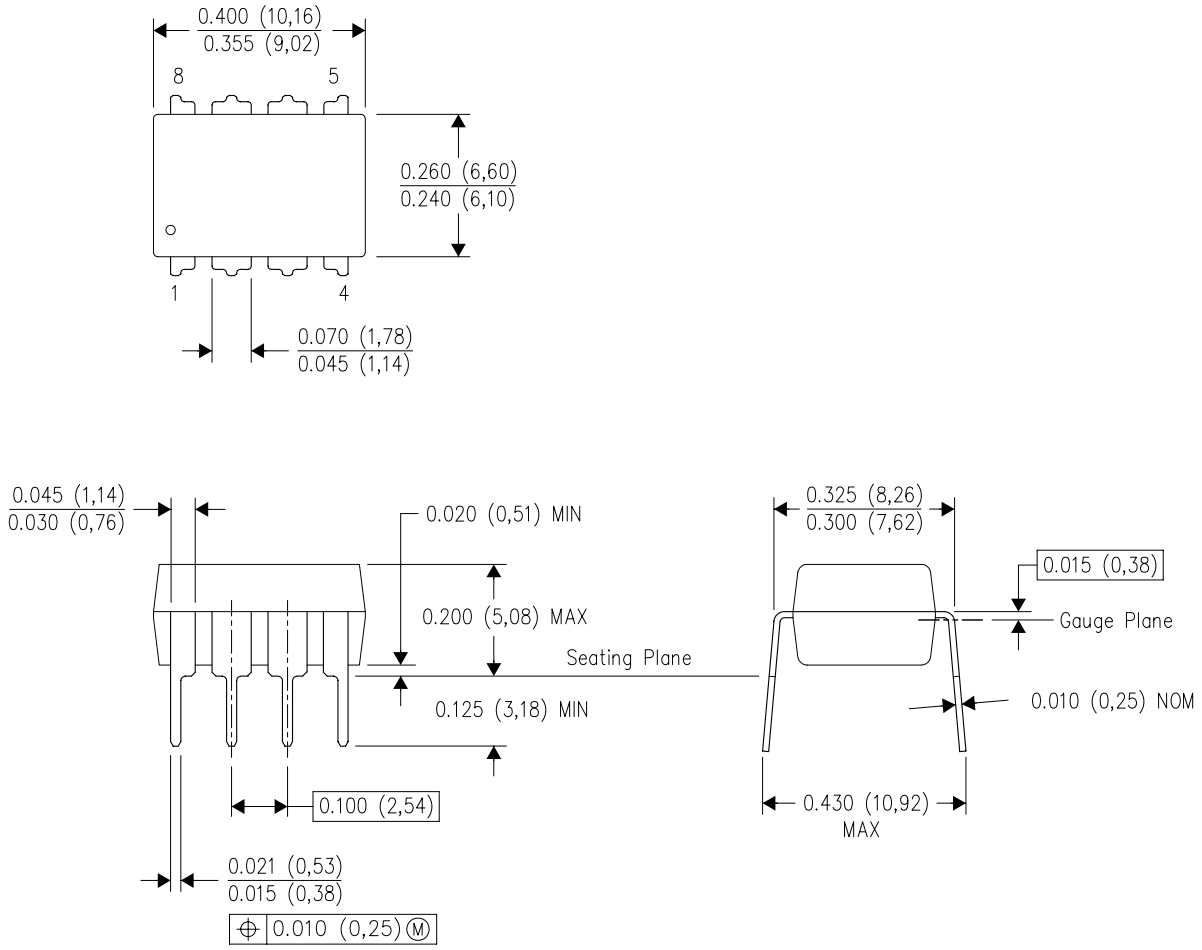
## LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE




4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

# LM118-N/lm218-N/LM318-N Operational Amplifiers

**Check for Samples: LM118-N, LM218-N, LM318-N**

## FEATURES

- **15 MHz Small Signal Bandwidth**
- **Ensured 50V/µs Slew Rate**
- **Maximum Bias Current of 250 nA**
- **Operates from Supplies of ±5V to ±20V**
- **Internal Frequency Compensation**
- **Input and Output Overload Protected**
- **Pin Compatible with General Purpose Op Amps**

## DESCRIPTION

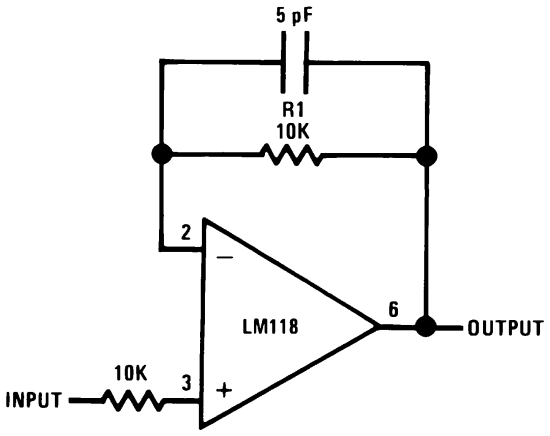
The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/µs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 µs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM218-N is identical to the LM118 except that the LM218-N has its performance specified over a −25°C to +85°C temperature range. The LM318-N is specified from 0°C to +70°C.

### Fast Voltage Follower




Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1) (2)

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation (3) | 500 mW |
| Differential Input Current (4) | ±10 mA |
| Input Voltage (5) | ±15V |
| Output Short-Circuit Duration | Continuous |
| Operating Temperature Range | |
| lm118-n | −55°C to +125°C |
| LM218-N | −25°C to +85°C |
| LM318-N | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | |
| TO-99 Package | 300°C |
| PDIP Package | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| SOIC Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |
| ESD Tolerance (6) | 2000V |

(1) Refer to RETS118X for LM118H and LM118J military specifications.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum junction temperature of the lm118-n is 150°C, the LM218-N is 110°C, and the LM318-N is 110°C. For operating at elevated temperatures, devices in the LMC package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
(4) The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
(5) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
(6) Human body model, 1.5 kΩ in series with 100 pF.

## Electrical Characteristics (1)

| Parameter | Conditions | LM118-N/LM218-N | | | LM318-N | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A$ = 25°C | | 2 | 4 | | 4 | 10 | mV |
| Input Offset Current | $T_A$ = 25°C | | 6 | 50 | | 30 | 200 | nA |
| Input Bias Current | $T_A$ = 25°C | | 120 | 250 | | 150 | 500 | nA |
| Input Resistance | $T_A$ = 25°C | 1 | 3 | | 0.5 | 3 | | MΩ |
| Supply Current | $T_A$ = 25°C | | 5 | 8 | | 5 | 10 | mA |
| Large Signal Voltage Gain | $T_A$ = 25°C, $V_S$ = ±15V<br>$V_{OUT}$ = ±10V, $R_L$ ≥ 2 kΩ | 50 | 200 | | 25 | 200 | | V/mV |
| Slew Rate | $T_A$ = 25°C, $V_S$ = ±15V, $A_V$ = 1 (2) | 50 | 70 | | 50 | 70 | | V/µs |
| Small Signal Bandwidth | $T_A$ = 25°C, $V_S$ = ±15V | | 15 | | | 15 | | MHz |
| Input Offset Voltage | | | | 6 | | | 15 | mV |
| Input Offset Current | | | | 100 | | | 300 | nA |

(1) These specifications apply for ±5V ≤ $V_S$ ≤ ±20V and −55°C ≤ $T_A$ ≤ +125°C (lm118-n), −25°C ≤ $T_A$ ≤ +85°C (LM218-N), and 0°C ≤ $T_A$ ≤ +70°C (LM318-N). Also, power supplies must be bypassed with 0.1 µF disc capacitors.
(2) Slew rate is tested with $V_S$ = ±15V. The lm118-n is in a unity-gain non-inverting configuration. $V_{IN}$ is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and specified to exceed 50V/µs.

## Electrical Characteristics [1] (continued)

| Parameter | Conditions | LM118-N/LM218-N | | | LM318-N | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | | | | 500 | | | 750 | nA |
| Supply Current | $T_A$ = 125°C | | 4.5 | 7 | | | | mA |
| Large Signal Voltage Gain | $V_S$ = ±15V, $V_{OUT}$ = ±10V<br>$R_L$ ≥ 2 kΩ | 25 | | | 20 | | | V/mV |
| Output Voltage Swing | $V_S$ = ±15V, $R_L$ = 2 kΩ | ±12 | ±13 | | ±12 | ±13 | | V |
| Input Voltage Range | $V_S$ = ±15V | ±11.5 | | | ±11.5 | | | V |
| Common-Mode Rejection Ratio | | 80 | 100 | | 70 | 100 | | dB |
| Supply Voltage Rejection Ratio | | 70 | 80 | | 65 | 80 | | dB |

## TYPICAL PERFORMANCE CHARACTERISTICS

LM118-N, LM218-N

**Input Current**

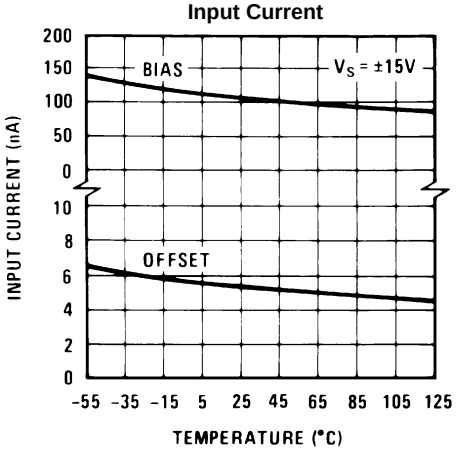



**Figure 1.**

**Voltage Gain**

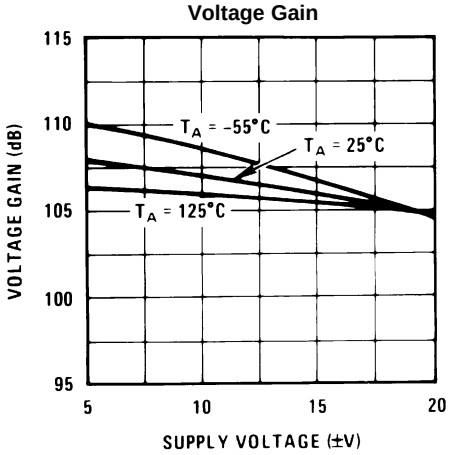



**Figure 2.**

**Power Supply Rejection**

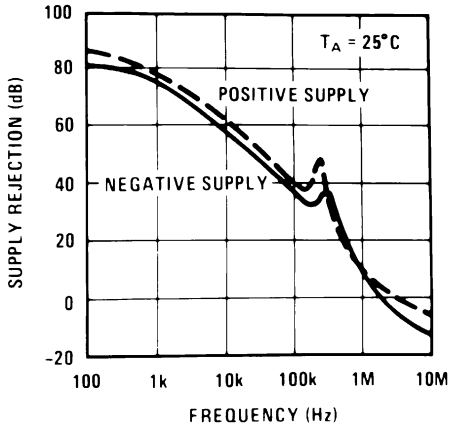



**Figure 3.**

**Input Noise Voltage**

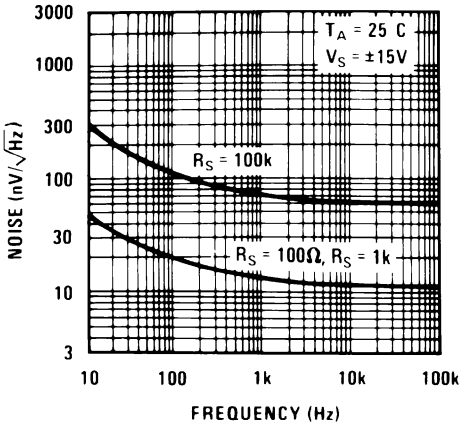



**Figure 4.**

**Common Mode Rejection**

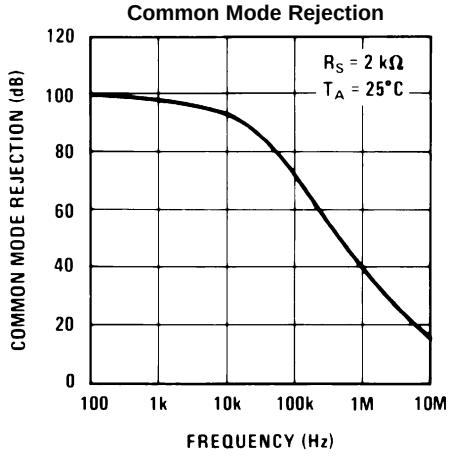



**Figure 5.**

**Supply Current**

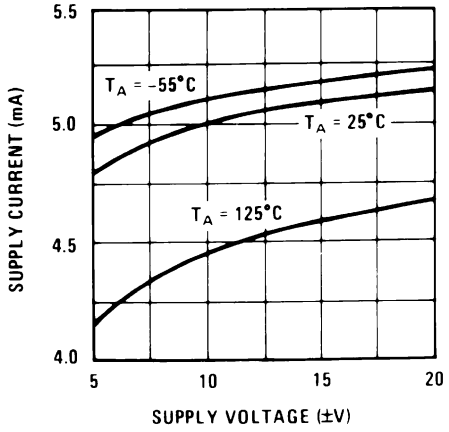



**Figure 6.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

**Closed Loop Output Impedance**

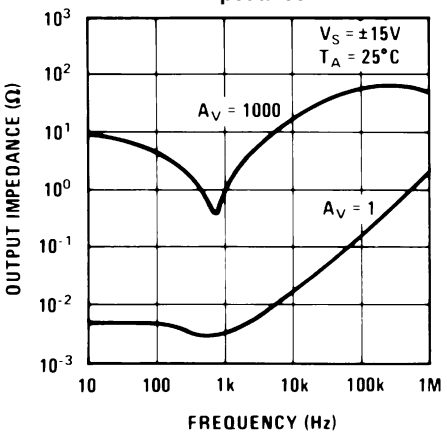



**Figure 7.**

**Current Limiting**

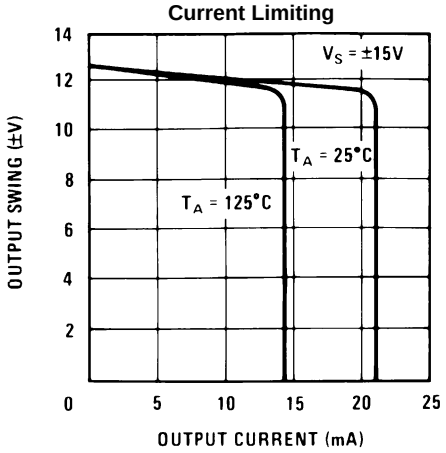



**Figure 8.**

**Input Current**

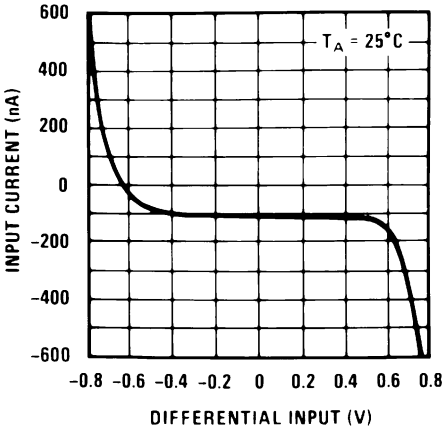



**Figure 9.**

**Unity Gain Bandwidth**

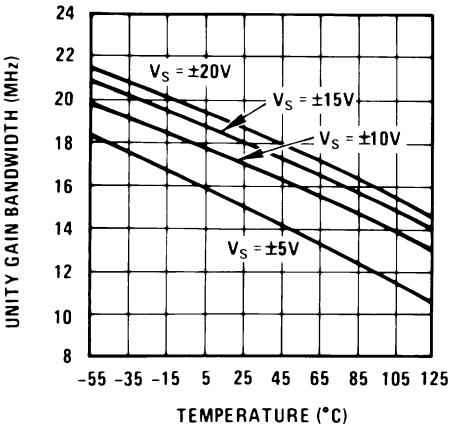



**Figure 10.**

**Voltage Follower Slew Rate**

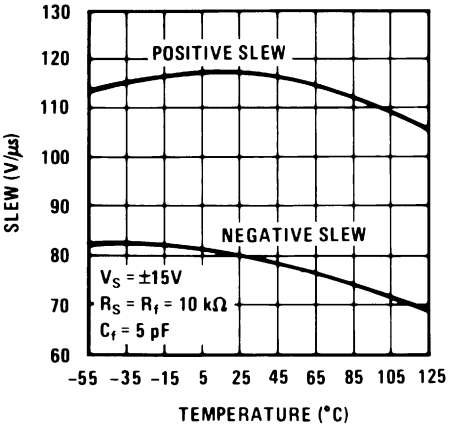



**Figure 11.**

**Inverter Settling Time**

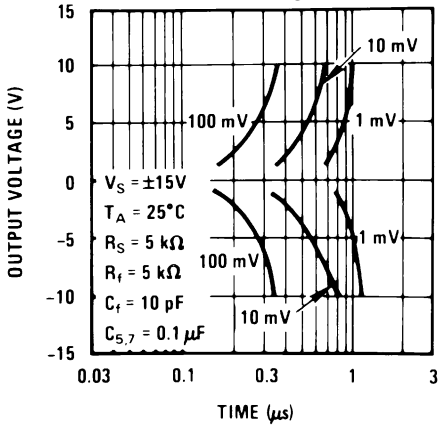



**Figure 12.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

**Large Signal Frequency Response**

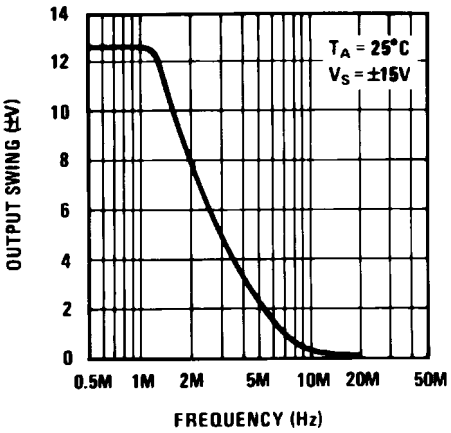



Figure 13.

**Open Loop Frequency Response**

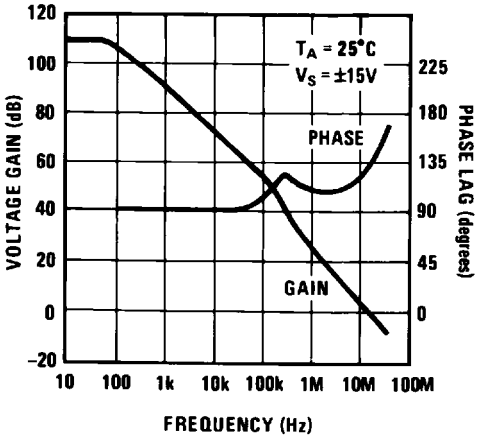



Figure 14.

**Voltage Follower Pulse Response**

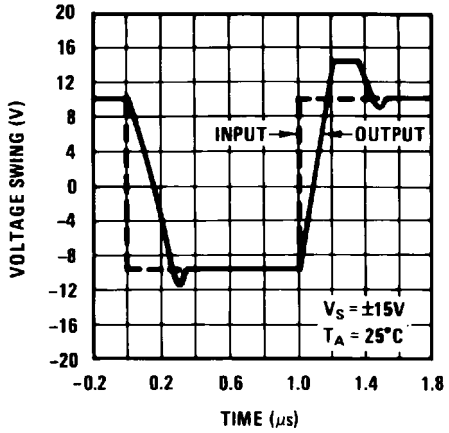



Figure 15.

**Large Signal Frequency Response**

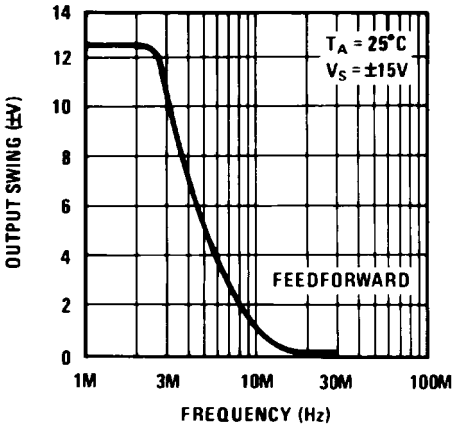



Figure 16.

**Open Loop Frequency Response**

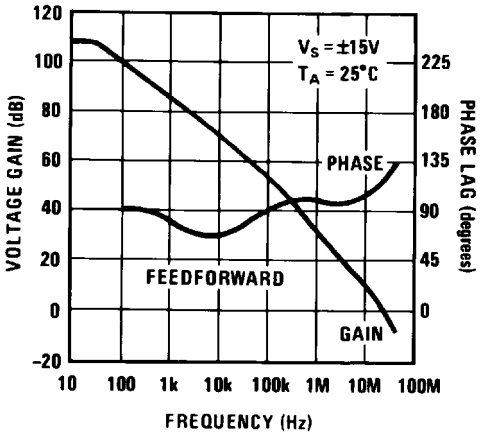



Figure 17.

**Inverter Pulse Response**

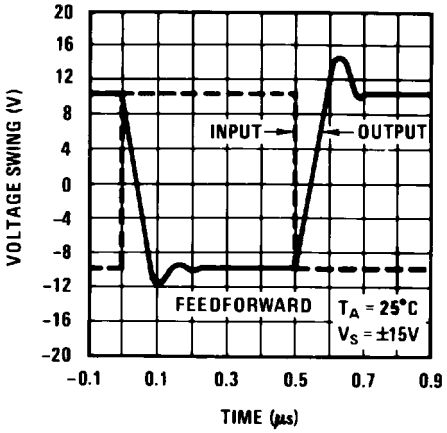



Figure 18.

## Typical Performance Characteristics

LM318-N

Input Current

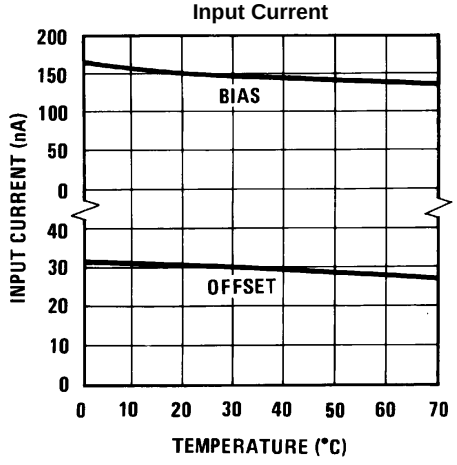



Figure 19.

Voltage Gain

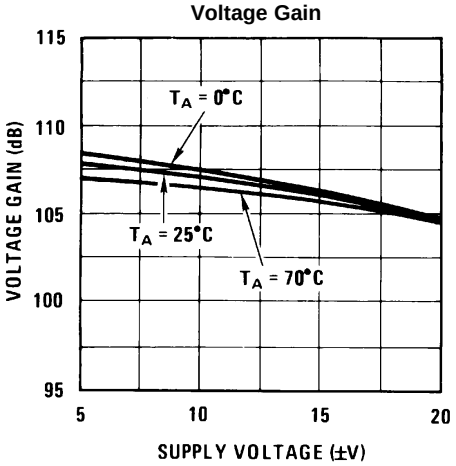



Figure 20.

Power Supply Rejection

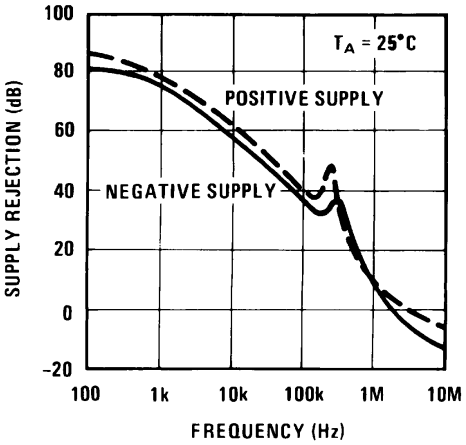



Figure 21.

Input Noise Voltage

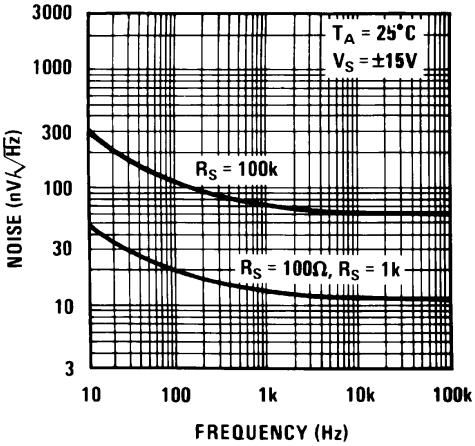



Figure 22.

Common Mode Rejection

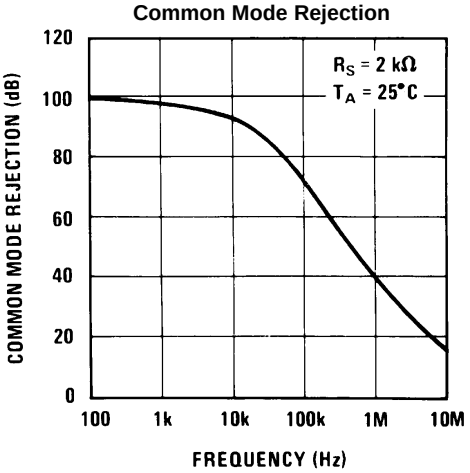



Figure 23.

Supply Current

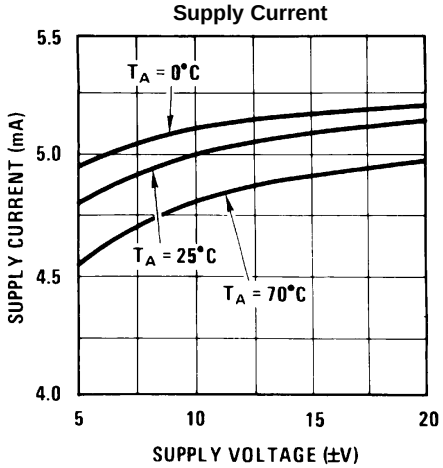



Figure 24.

## Typical Performance Characteristics (continued)

LM318-N

**Closed Loop Output Impedance**

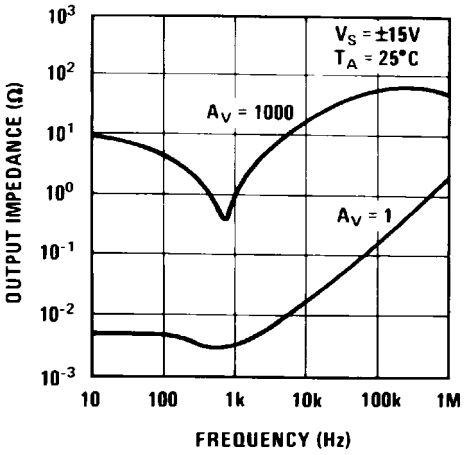



Figure 25.

**Current Limiting**

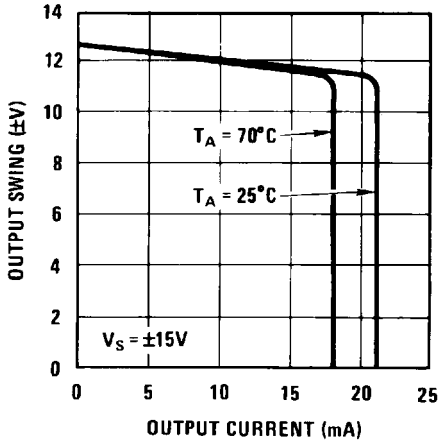



Figure 26.

**Input Current**

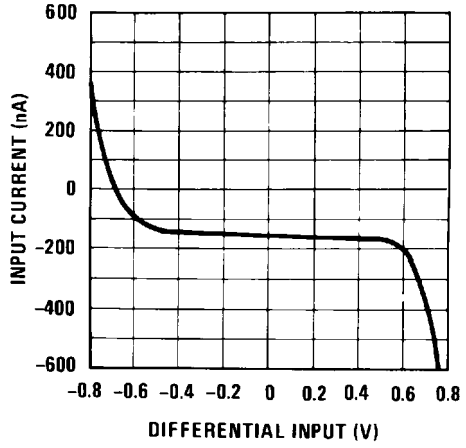



Figure 27.

**Unity Gain Bandwidth**

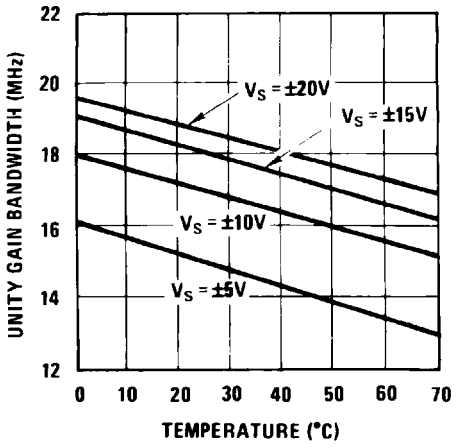



Figure 28.

**Voltage Follower Slew Rate**

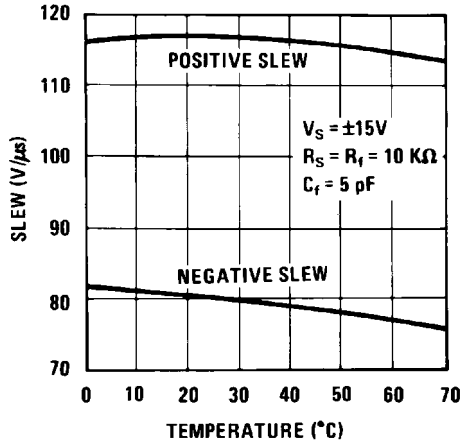



Figure 29.

**Inverter Settling Time**

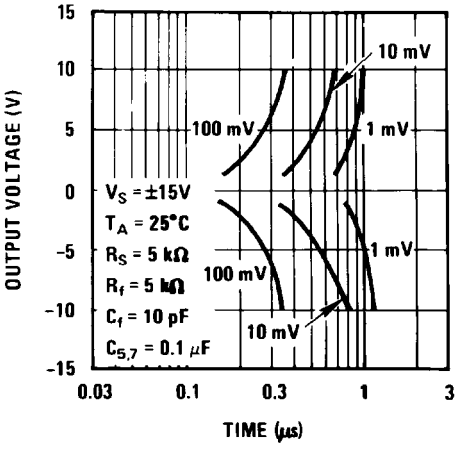



Figure 30.

## Typical Performance Characteristics (continued)

LM318-N

**Large Signal Frequency Response**

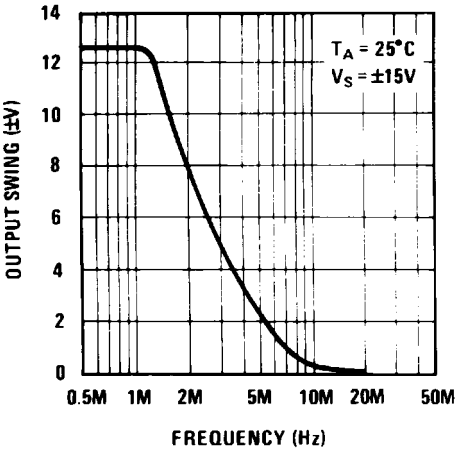



**Figure 31.**

**Open Loop Frequency Response**

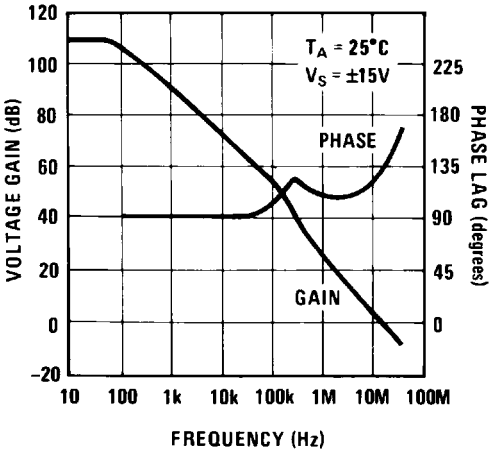



**Figure 32.**

**Voltage Follower Pulse Response**

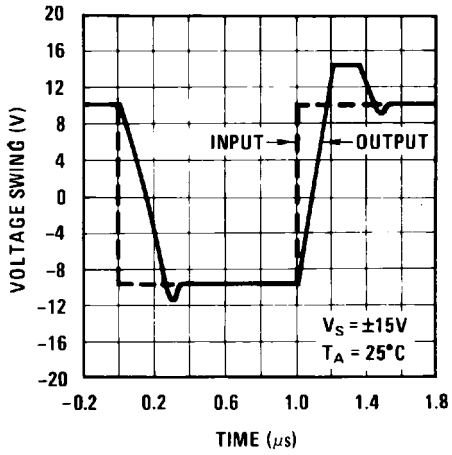



**Figure 33.**

**Large Signal Frequency Response**

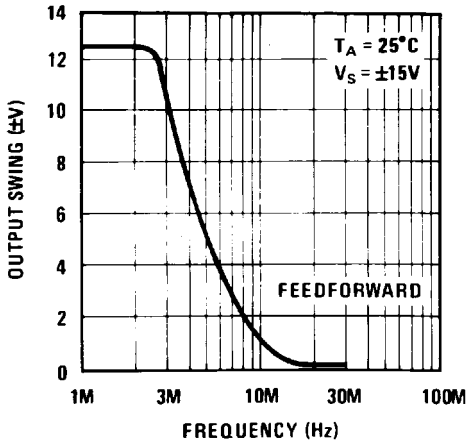



**Figure 34.**

**Open Loop Frequency Response**

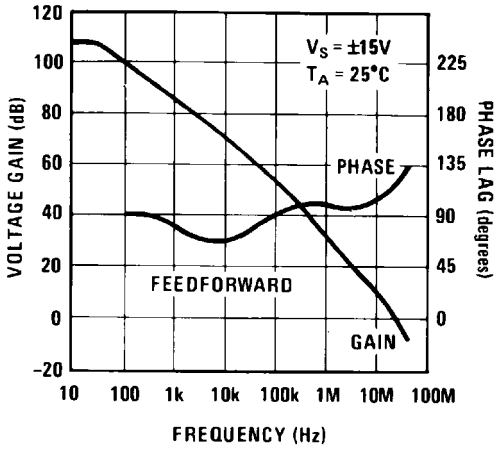



**Figure 35.**

**Inverter Pulse Response**

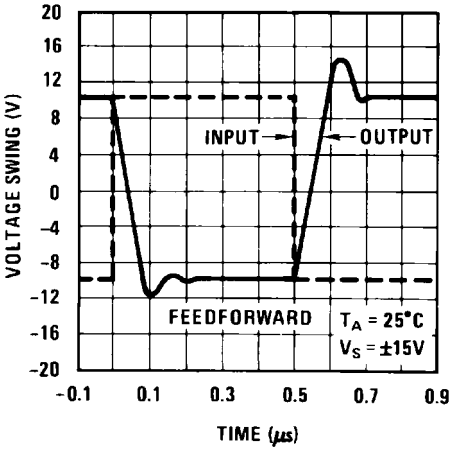
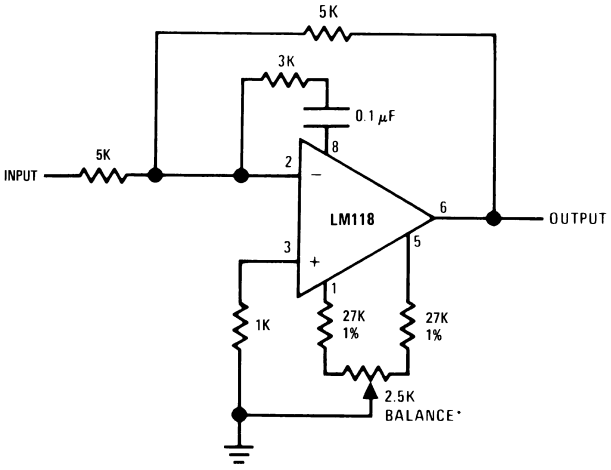



**Figure 36.**

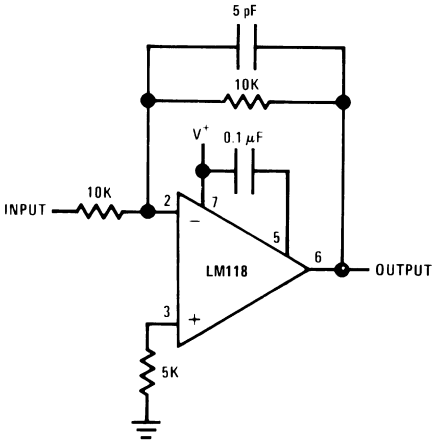
## AUXILIARY CIRCUITS




*Balance circuit necessary for increased slew.

Slew rate typically 150V/µs.

**Figure 37. Feedforward Compensation for Greater Inverting Slew Rate**




Slew and settling time to 0.1% for a 10V step change is 800 ns.

**Figure 38. Compensation for Minimum Settling Time**

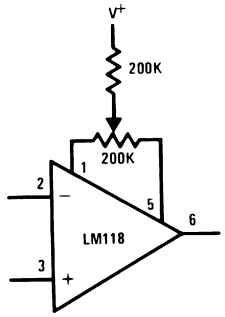



**Figure 39. Offset Balancing**

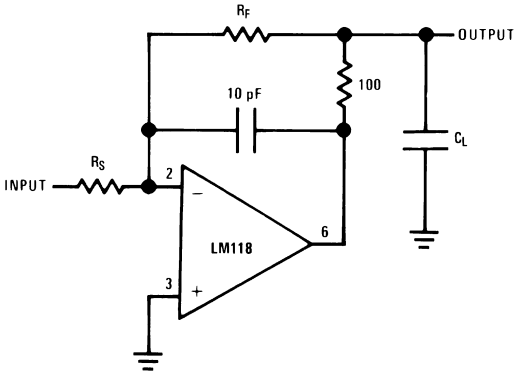



**Figure 40. Isolating Large Capacitive Loads**

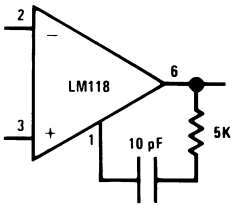
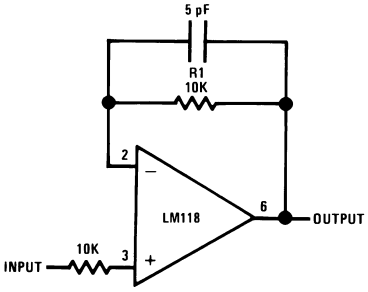


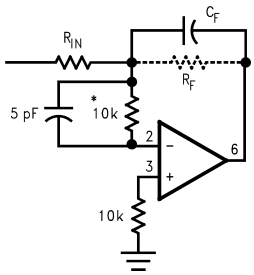

**Figure 41. Overcompensation**

## TYPICAL APPLICATIONS




Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

**Figure 42. Fast Voltage Follower**




$C_F$ = Large
($C_F$ ≥ 50 pF)
*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

**Figure 43.**

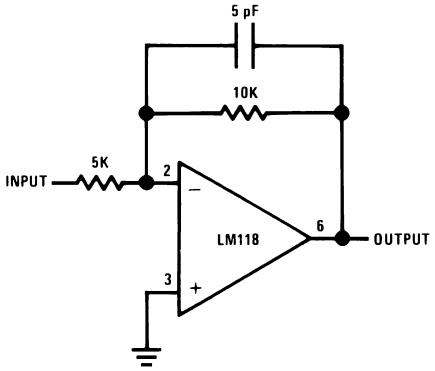



**Figure 44. Fast Summing Amplifier**

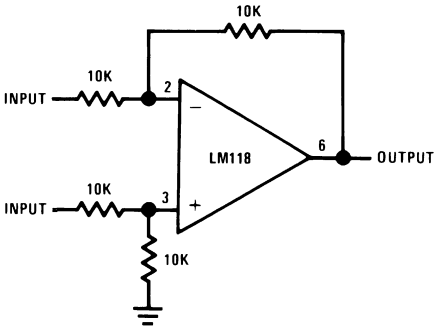



**Figure 45. Differential Amplifie**

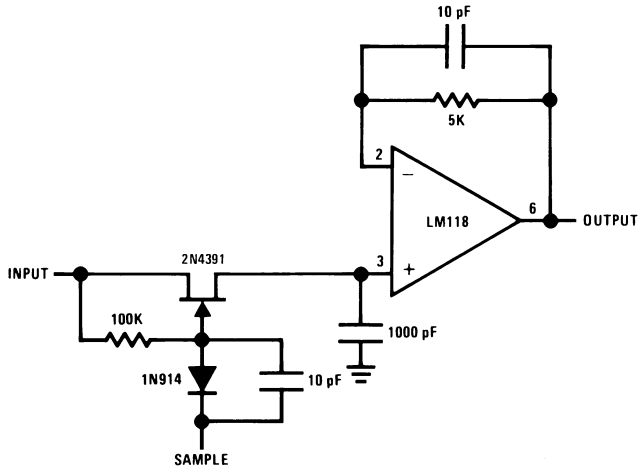
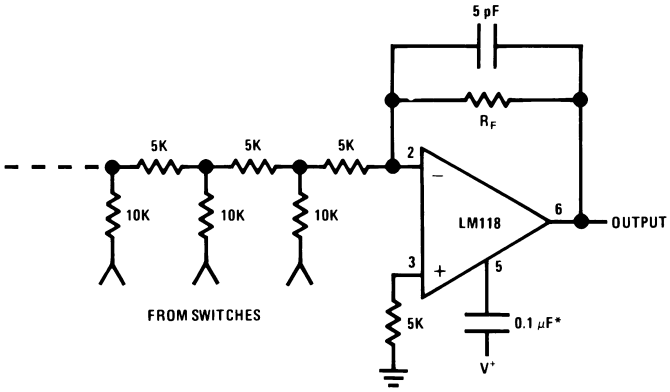
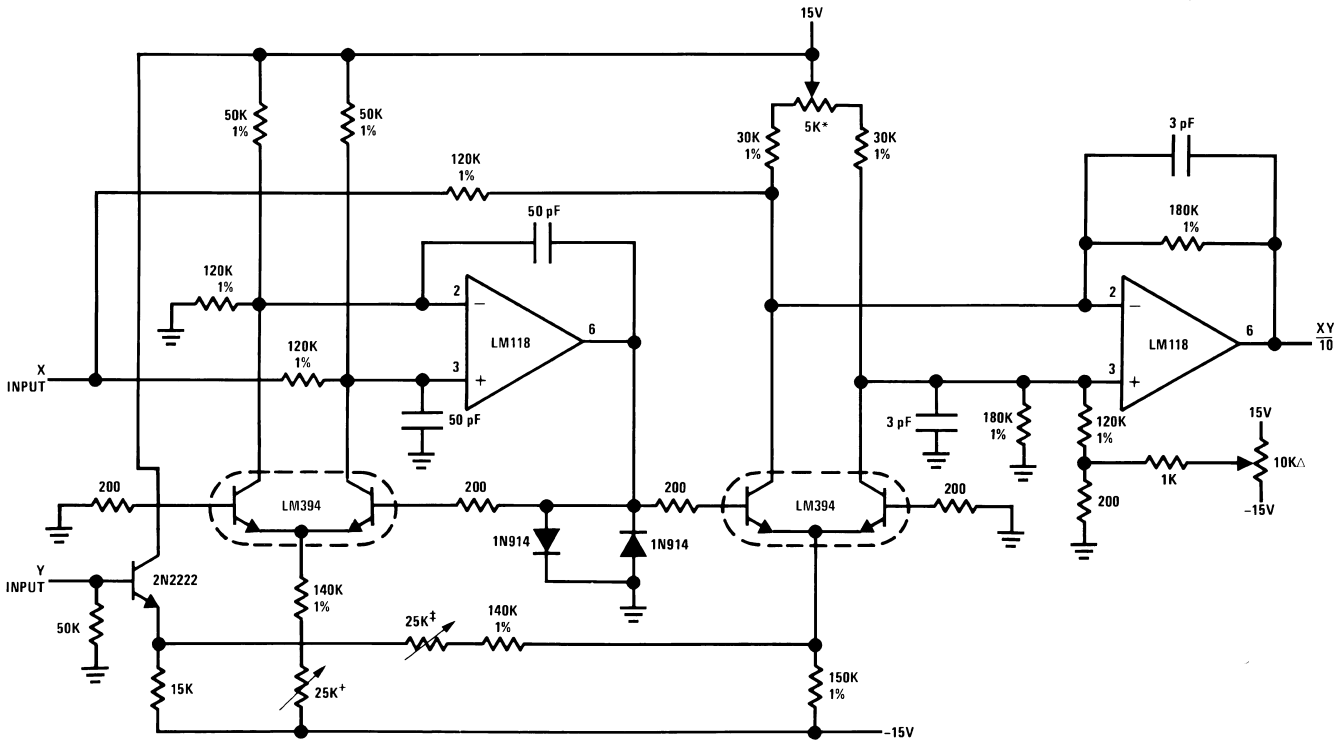



**Figure 46. Fast Sample and Hold**



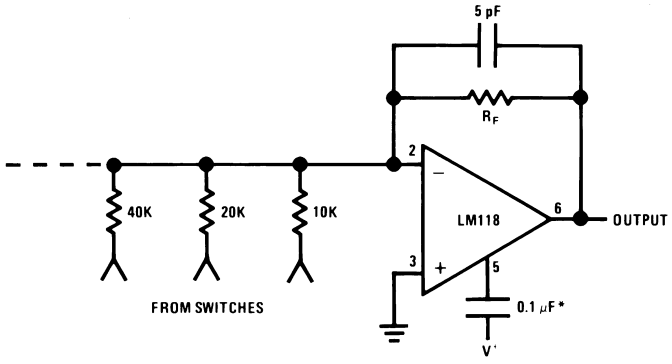

*Optional—Reduces settling time.

**Figure 47. D/A Converter Using Ladder Network**




ΔOutput zero.
*"Y" zero
+"X" zero
‡Full scale adjust.

**Figure 48. Four Quadrant Multiplier**




*Optional—Reduces settling time.

**Figure 49. D/A Converter Using Binary Weighted Network**

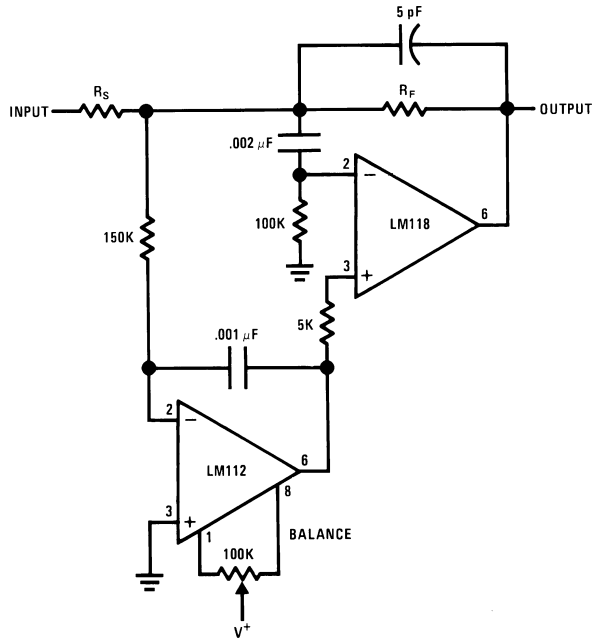
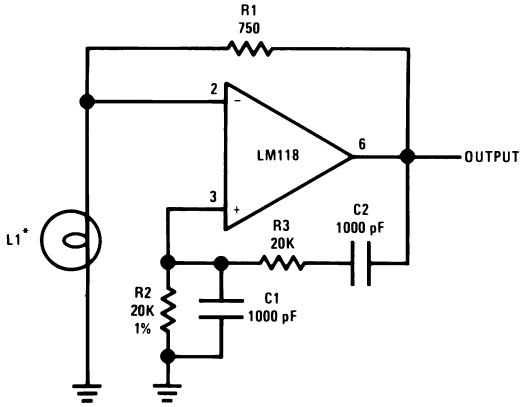



**Figure 50. Fast Summing Amplifier with Low Input Current**



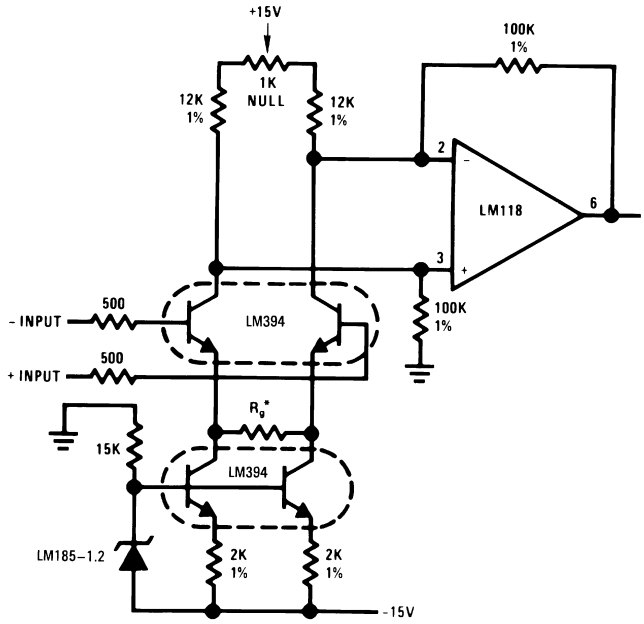

*L1—10V—14 mA bulb ELDEMA 1869

R1 = R2

C1 = C2

$$f = \frac{1}{2\pi R2\, C1}$$

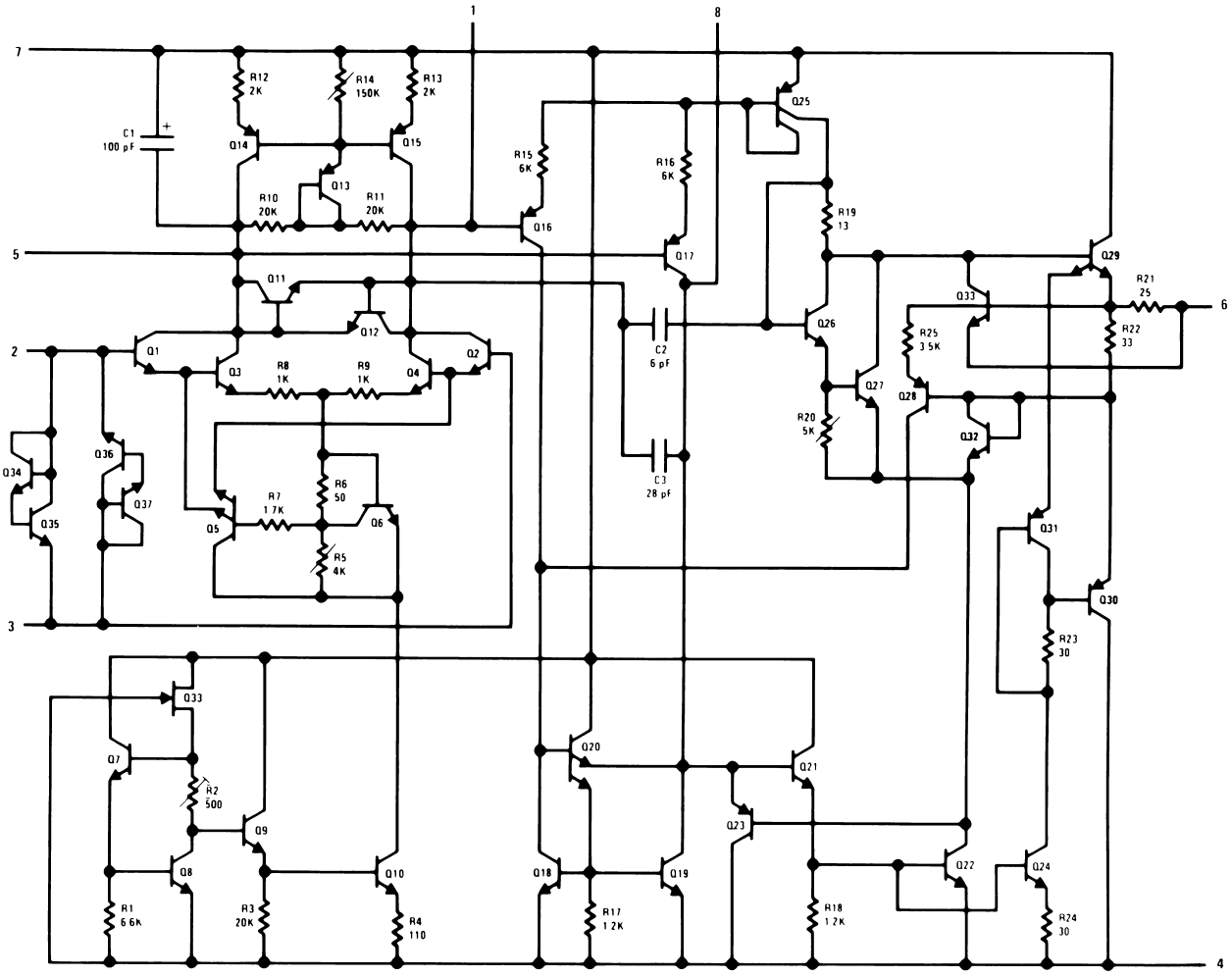
**Figure 51. Wein Bridge Sine Wave Oscillator**



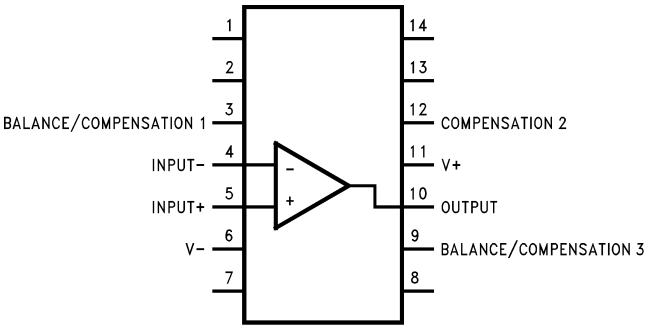

*Gain $\geq \frac{200K}{R_g}$ for $1.5K \leq R_g \leq 200K$

**Figure 52. Instrumentation Amplifier**

## Schematic Diagram

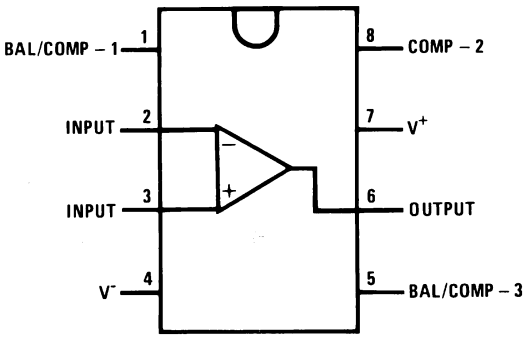


## Pin Diagram



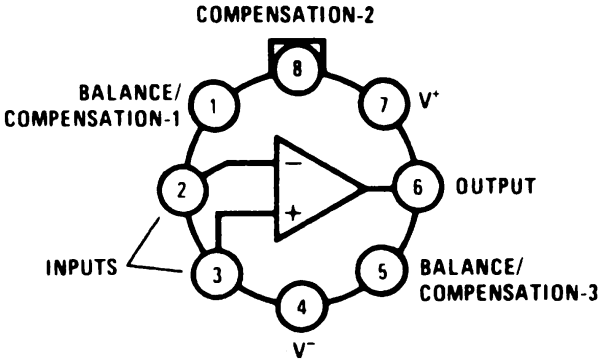

Available per JM38510/10107.

**Dual-In-Line Package**
**(Top View)**
**See Package Number J (R-GDIP-T14)**




Available per JM38510/10107.

**Dual-In-Line Package**
**(Top View)**
**See Package Number NAB008A, D (R-PDSO-G8), or P (R-PDIP-T8)**




Pin connections shown on schematic diagram and typical applications are for TO-99 package.

**TO-99 Package**
**(Top View)**
**See Package Number LMC (O-MBCY-W8)**

## REVISION HISTORY

| Changes from Revision B (March 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 16 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM118H | ACTIVE | TO-99 | LMC | 8 | 500 | TBD | Call TI | Call TI | -55 to 125 | LM118H | Samples |
| LM118H/NOPB | ACTIVE | TO-99 | LMC | 8 | 500 | Green (RoHS & no Sb/Br) | POST-PLATE | Level-1-NA-UNLIM | -55 to 125 | LM118H | Samples |
| LM318M | NRND | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | 0 to 70 | LM 318M | |
| LM318M/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | 0 to 70 | LM 318M | Samples |
| LM318MX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | 0 to 70 | LM 318M | Samples |
| LM318N | LIFEBUY | PDIP | P | 8 | 40 | TBD | Call TI | Call TI | 0 to 70 | LM 318N | |
| LM318N/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | 0 to 70 | LM 318N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

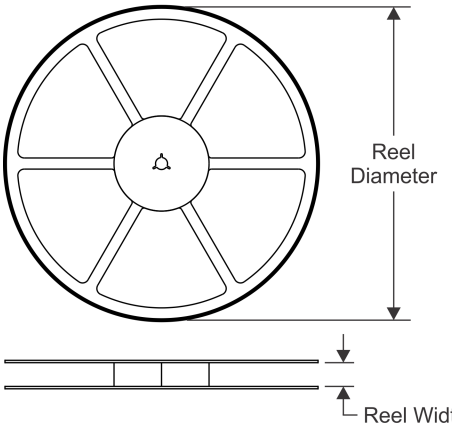
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

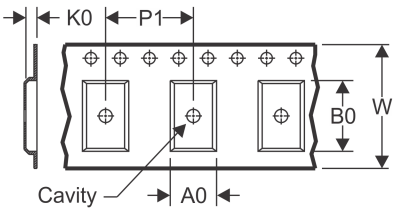
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

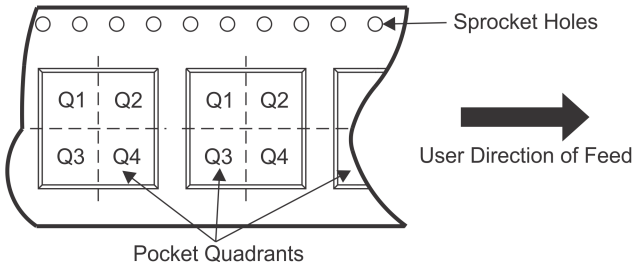



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

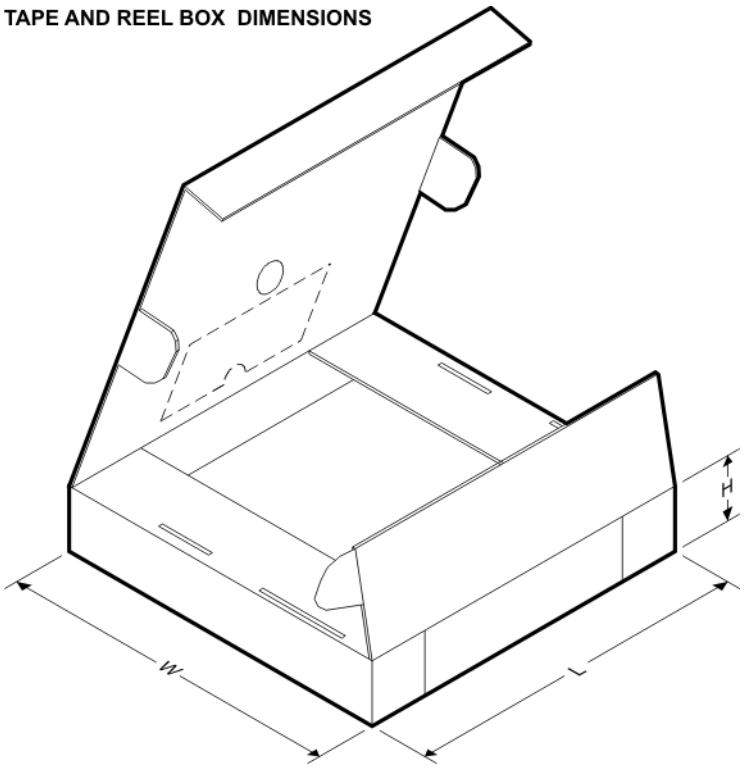
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM318MX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

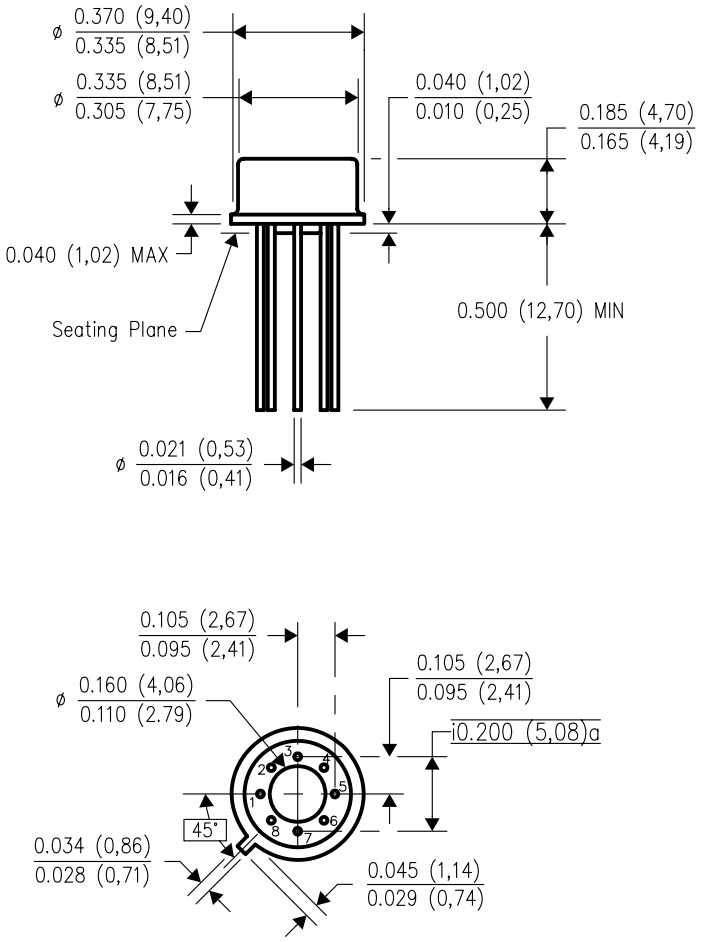
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM318MX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

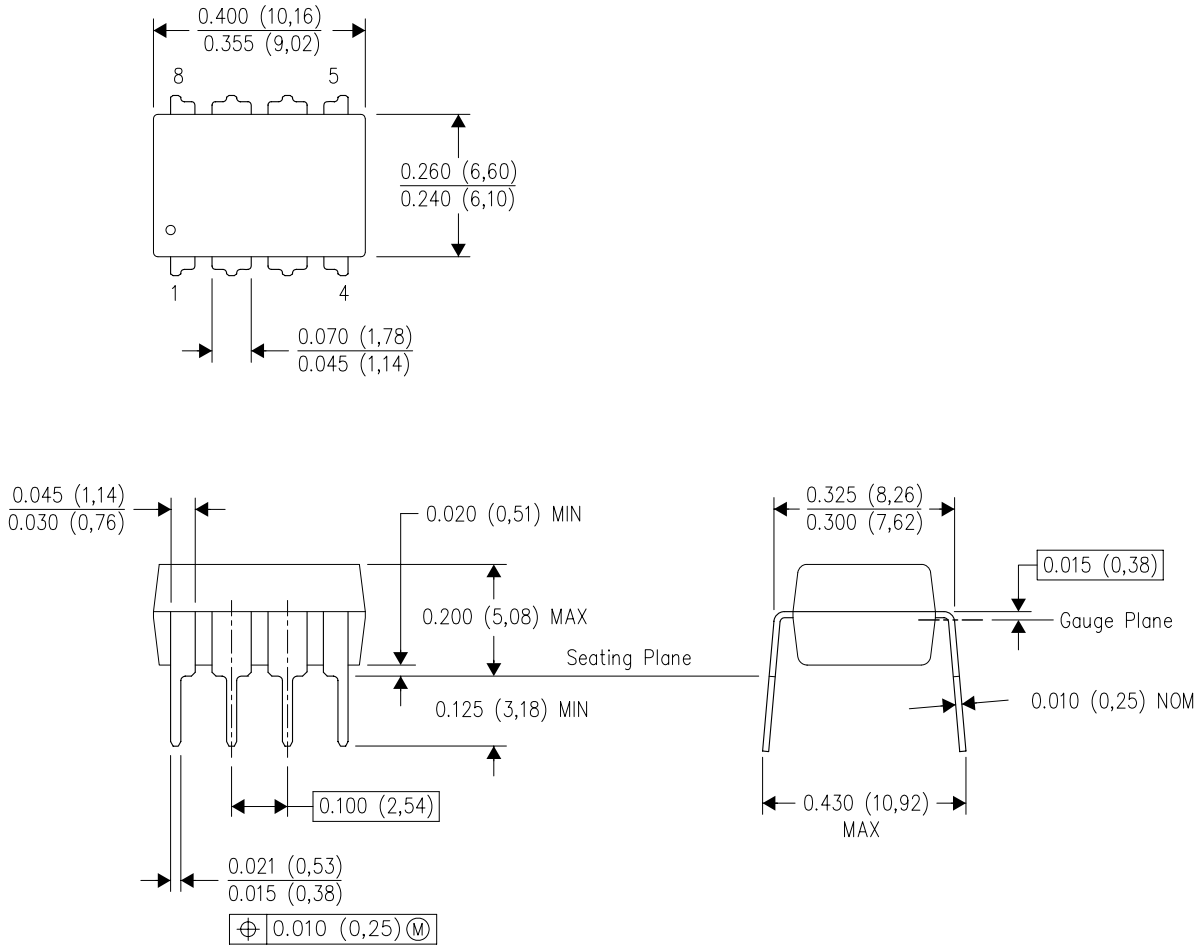
## LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE




4202483/B 09/07

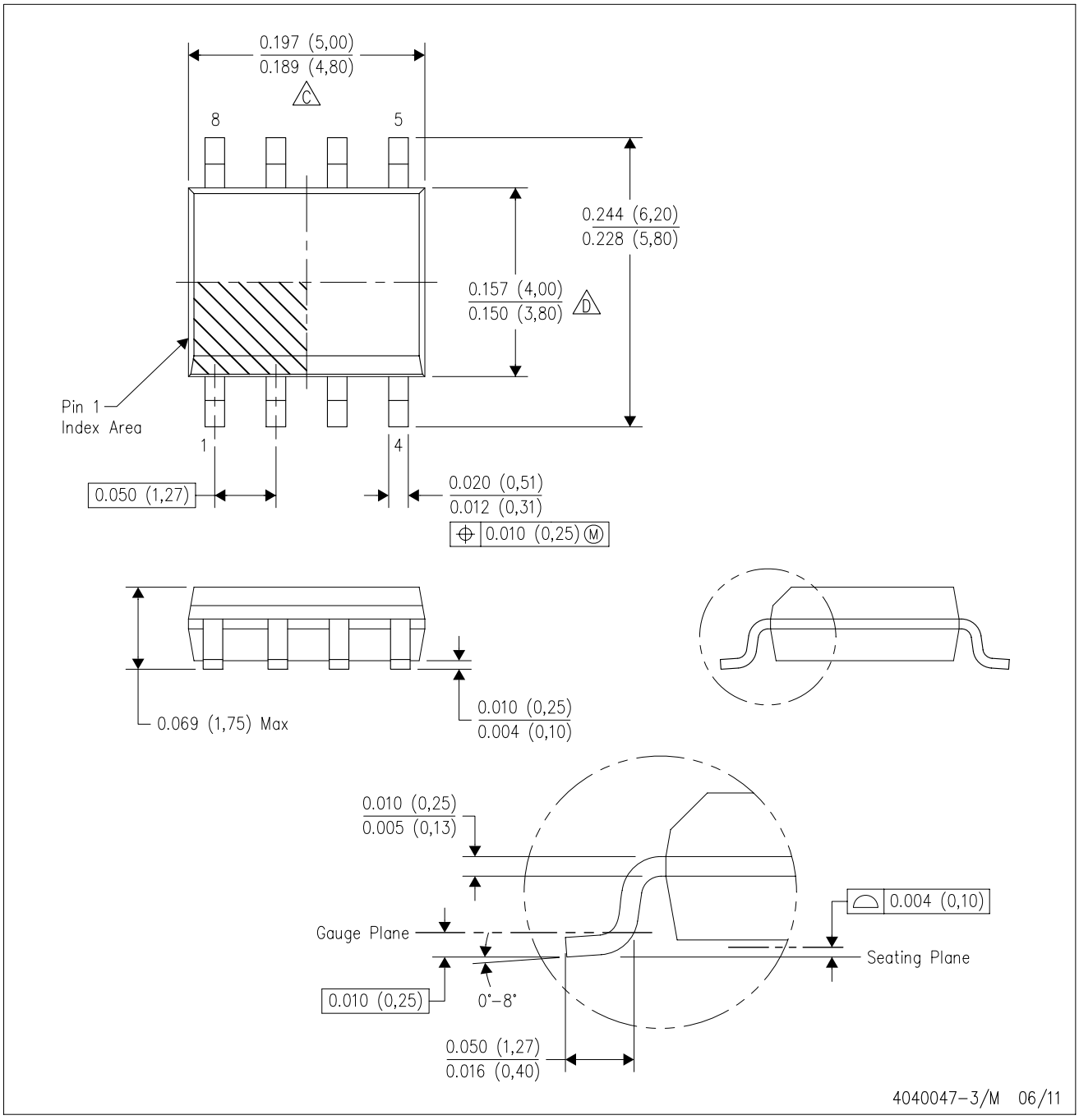
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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# Zener Diode

## Features:

- High reliability.
- Very sharp reverse characteristic.
- Low reverse current level.
- $V_Z$-tolerance ±5%.

## Application:

Voltage stabilization.

## Absolute Maximum Ratings $T_j$ = 25°C

| Parameter | Test Conditions | Symbol | Value | Unit |
|---|---|---|---|---|
| Power dissipation | $T_{amb} \leq 50°C$ | $P_v$ | 1 | W |
| Z-current | - | $I_z$ | $P_v / V_z$ | mA |
| Junction temperature | - | $T_j$ | 200 | °C |
| Storage temperature range | - | $T_{stg}$ | -65 to +175 | |

## Maximum Thermal Resistance $T_j$ = 25°C

| Parameter | Test Conditions | Symbol | Value | Unit |
|---|---|---|---|---|
| Junction ambient | I = 9.5 mm (3/8") $T_L$ = constant | $R_{thJA}$ | 100 | K/W |

Stresses exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.

## Electrical Characteristics $T_j$ = 25°C

| Parameter | Test Conditions | Symbol | Maximum | Unit |
|---|---|---|---|---|
| Forward voltage | $I_F$ = 200 mA | $V_F$ | 1.2 | V |

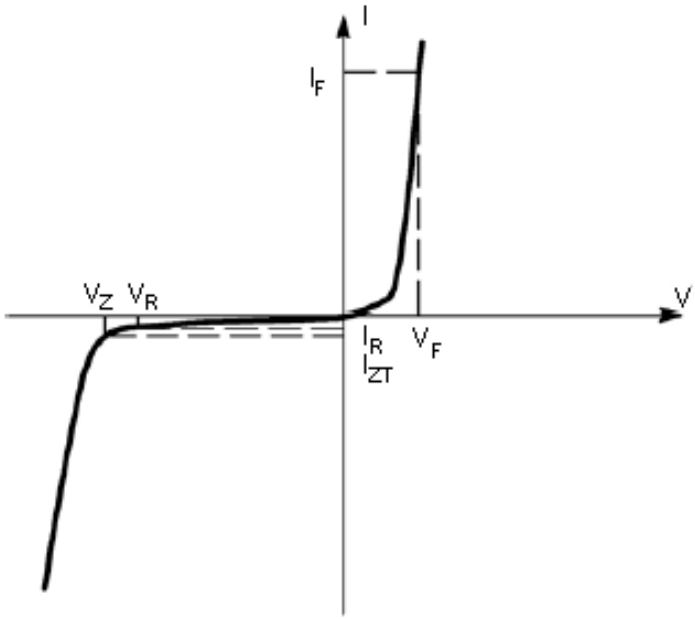
## Specification Table

| $V_{Znom}$ [1] | $I_{ZT}$ for $r_{ziT}$ | | $r_{ziK}$ at $I_{ZK}$ | | $I_R$ at $V_R$ | | Part Number |
|---|---|---|---|---|---|---|---|
| V | mA | Ω | Ω | mA | µA | V | |
| 3.3 | 76 | < 10 | < 400 | 1 | < 100 | 1 | 1N4728A |
| 3.6 | 69 | < 10 | < 400 | 1 | < 100 | 1 | 1N4729A |
| 3.9 | 64 | < 9 | < 400 | 1 | < 50 | 1 | 1N4730A |
| 4.7 | 53 | < 8 | < 500 | 1 | < 10 | 1 | 1N4732A |
| 5.1 | 49 | < 7 | < 550 | 1 | < 10 | 1 | 1N4733A |
| 5.6 | 45 | < 5 | < 600 | 1 | < 10 | 2 | 1N4734A |
| 6.2 | 41 | < 2 | < 700 | 1 | < 10 | 3 | 1N4735A |
| 6.8 | 37 | < 3.5 | < 700 | 1 | < 10 | 4 | 1N4736A |
| 7.5 | 34 | < 4 | < 700 | 0.5 | < 10 | 5 | 1N4737A |
| 8.2 | 31 | < 4.5 | < 700 | 0.5 | < 10 | 6 | 1N4738A |
| 9.1 | 28 | < 5 | < 700 | 0.5 | < 10 | 7 | 1N4739A |
| 10 | 25 | < 7 | < 700 | 0.25 | < 10 | 7.6 | 1N4740A |
| 11 | 23 | < 8 | < 700 | 0.25 | < 5 | 8.4 | 1N4741A |
| 12 | 21 | < 9 | < 700 | 0.25 | < 5 | 9.1 | 1N4742A |
| 13 | 19 | < 10 | < 700 | 0.25 | < 5 | 9.9 | 1N4743A |
| 15 | 17 | < 14 | < 700 | 0.25 | < 5 | 11.4 | 1N4744A |
| 16 | 15.5 | < 16 | < 700 | 0.25 | < 5 | 12.2 | 1N4745A |
| 18 | 14 | < 20 | < 750 | 0.25 | < 5 | 13.7 | 1N4746A |
| 20 | 12.5 | < 22 | < 750 | 0.25 | < 5 | 15.2 | 1N4747A |
| 22 | 11.5 | < 23 | < 750 | 0.25 | < 5 | 16.7 | 1N4748A |
| 24 | 10.5 | < 25 | < 750 | 0.25 | < 5 | 18.2 | 1N4749A |
| 27 | 9.5 | < 35 | < 750 | 0.25 | < 5 | 20.6 | 1N4750A |
| 30 | 8.5 | < 40 | < 1000 | 0.25 | < 5 | 22.8 | 1N4751A |
| 33 | 7.5 | < 45 | < 1000 | 0.25 | < 5 | 25.1 | 1N4752A |
| 36 | 7 | < 50 | < 1000 | 0.25 | < 5 | 27.4 | 1N4753A |
| 39 | 6.5 | < 60 | < 1000 | 0.25 | < 5 | 29.7 | 1N4754A |
| 43 | 6 | < 70 | < 1500 | 0.25 | < 5 | 32.7 | 1N4755A |
| 47 | 5.5 | < 80 | < 1500 | 0.25 | < 5 | 35.8 | 1N4756A |
| 51 | 5 | < 95 | < 1500 | 0.25 | < 5 | 38.8 | 1N4757A |
| 56 | 4.5 | < 110 | < 2000 | 0.25 | < 5 | 42.6 | 1N4758A |
| 62 | 4 | < 125 | < 2000 | 0.25 | < 5 | 47.1 | 1N4759A |
| 68 | 3.7 | < 150 | < 2000 | 0.25 | < 5 | 51.7 | 1N4760A |
| 75 | 3.3 | < 175 | < 2000 | 0.25 | < 5 | 56 | 1N4761A |

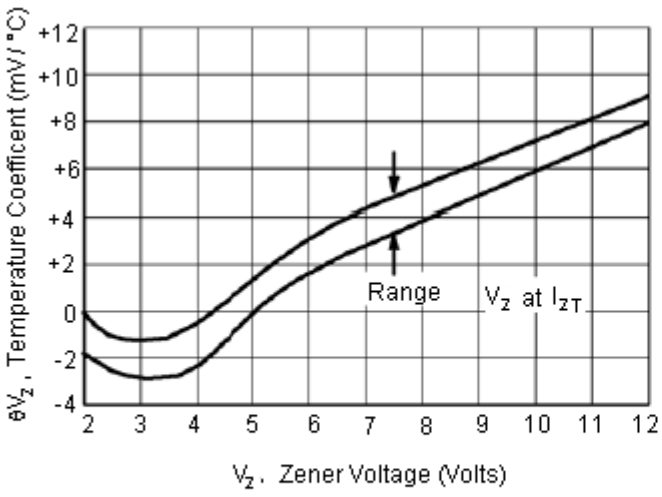
[1] Based on DC-measurement at thermal equilibrium while maintaining the lead temperature ($T_L$) at 30°C, 9.5 mm (3/8”) from the diode body.

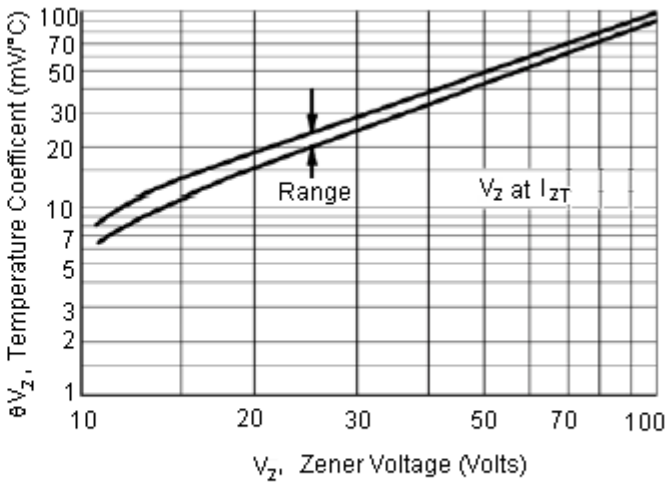
## Characteristics ($T_j$ = 25°C unless otherwise specified)

| Symbol | Parameter |
|---|---|
| $V_Z$ | Reverse zener voltage at $I_{ZT}$ |
| $I_{ZT}$ | Reverse current |
| $Z_{ZT}$ | Maximum zener impedance at $I_{ZT}$ |
| $I_{ZK}$ | Reverse current |
| $Z_{ZK}$ | Maximum zener impedance at $I_{ZK}$ |
| $I_R$ | Reverse leakage current at $V_R$ |
| $V_R$ | Breakdown voltage |
| $I_F$ | Forward current |
| $V_F$ | Forward voltage at $I_F$ |




**Zener Voltage Regulator**

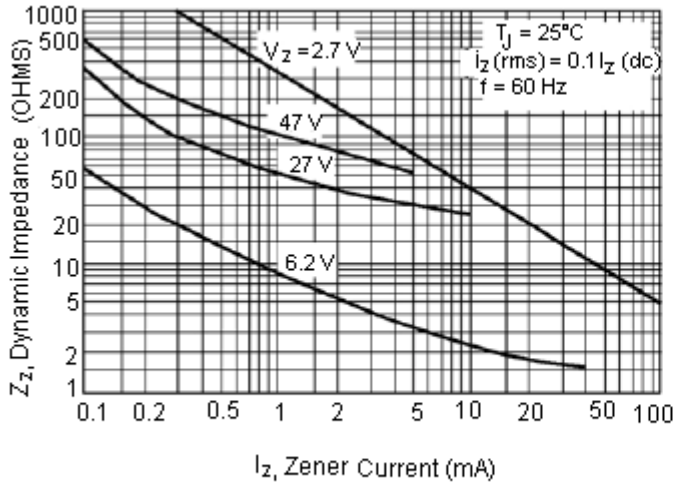


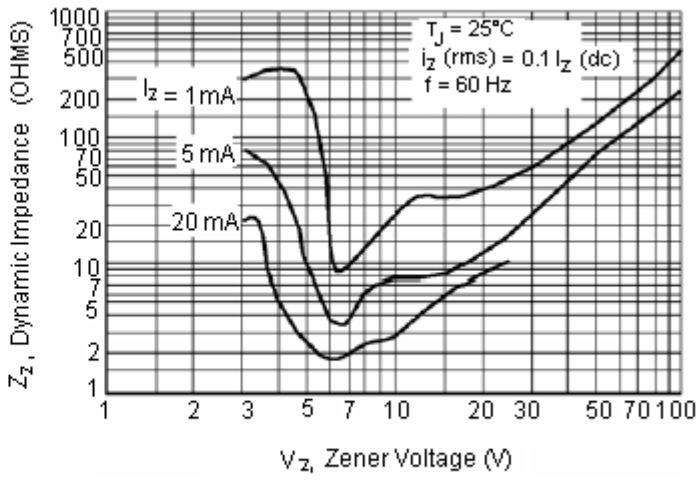

**Temperature Coefficients**

**(-55°C to +150°C temperature range; 90% of the units are in the ranges indicated)**

## Characteristics ($T_j$ = 25°C unless otherwise specified)

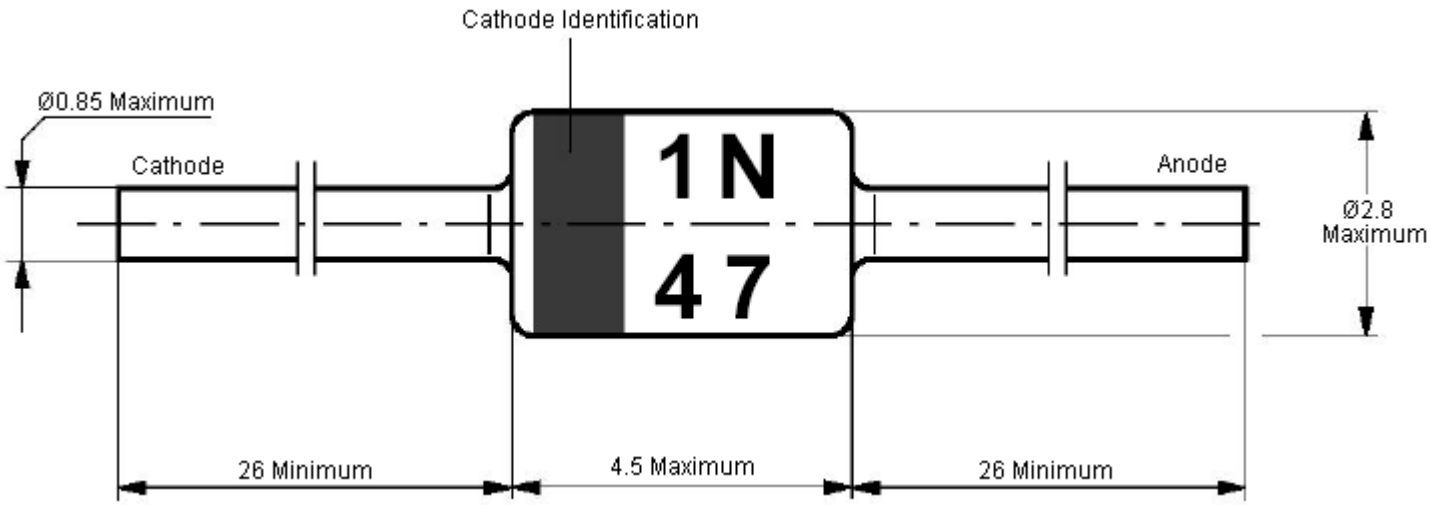



**Effect of Zener Current on Zener Impedance**




**Effect of Zener Voltage on Zener Impedance**

## Dimensions




Standard Glass case
JEDEC DO-41

Dimensions: Millimetres