

Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.15 secs

--> Parameter xsthdmdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.16 secs

--> Reading design: decryption_behav.prj

TABLE OF CONTENTS

- 1) Synthesis Options Summary
- 2) HDL Parsing
- 3) HDL Elaboration
- 4) HDL Synthesis
 - 4.1) HDL Synthesis Report
- 5) Advanced HDL Synthesis
 - 5.1) Advanced HDL Synthesis Report
- 6) Low Level Synthesis
- 7) Partition Report
- 8) Design Summary
 - 8.1) Primitive and Black Box Usage
 - 8.2) Device utilization summary
 - 8.3) Partition Resource Summary
 - 8.4) Timing Report
 - 8.4.1) Clock Information
 - 8.4.2) Asynchronous Control Signals Information
 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

```
=====
*                               Synthesis Options Summary                               *
```

```
----- Source Parameters
```

```
Input File Name           : "decryption_behav.prj"
Ignore Synthesis Constraint File : NO
```

```
----- Target Parameters
```

```
Output File Name          : "decryption_behav"
Output Format               : NGC
Target Device              : xc7vx330t-3-ffg1157
```

```
----- Source Options
```

```
Top Module Name           : decryption_behav
Automatic FSM Extraction   : YES
FSM Encoding Algorithm     : Auto
Safe Implementation       : No
FSM Style                  : LUT
RAM Extraction             : Yes
RAM Style                  : Auto
ROM Extraction             : Yes
Shift Register Extraction  : YES
ROM Style                  : Auto
```

Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer (BUFG) : 32
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Parsing *

=====

Parsing VHDL file "E:\uni\term
5\FPGA\project\RSA_virtex_decryption\decryption\decryption_behav.vhd" into library work
Parsing entity <decryption_behav>.
Parsing architecture <Behavioral> of entity <decryption_behav>.

=====

* HDL Elaboration *

=====

Elaborating entity <decryption_behav> (architecture <Behavioral>) from library <work>.

=====

* HDL Synthesis *

=====

Synthesizing Unit <decryption_behav>.

Related source file is "E:\uni\term

5\FPGA\project\RSA_virtex_decryption\decryption\decryption_behav.vhd".

WARNING:Xst:647 - Input <encryptdata<31:31>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 32-bit register for signal <cnt>.

Found 64-bit register for signal <dout>.

Found 256-bit register for signal <power_result>.

Found 32-bit adder for signal <cnt[31]_GND_7_o_add_3_OUT> created at line 39.

Found 16x16-bit multiplier for signal <n0024> created at line 35.

Found 31x31-bit multiplier for signal <n0025> created at line 38.

Found 33-bit comparator greater for signal <GND_7_o_cnt[31]_LessThan_2_o> created at line 37

Found 33-bit comparator equal for signal <GND_7_o_cnt[31]_equal_5_o> created at line 40

Summary:

inferred 2 Multiplier(s).

inferred 1 Adder/Subtractor(s).

inferred 352 D-type flip-flop(s).

inferred 2 Comparator(s).

Unit <decryption_behav> synthesized.

Synthesizing Unit <rem_31u_31u>.

Related source file is "".

Found 62-bit adder for signal <n3236> created at line 0.

Found 62-bit adder for signal <GND_10_o_b[30]_add_1_OUT> created at line 0.

Found 61-bit adder for signal <n3240> created at line 0.

Found 61-bit adder for signal <GND_10_o_b[30]_add_3_OUT> created at line 0.

Found 60-bit adder for signal <n3244> created at line 0.

Found 60-bit adder for signal <GND_10_o_b[30]_add_5_OUT> created at line 0.

Found 59-bit adder for signal <n3248> created at line 0.

Found 59-bit adder for signal <GND_10_o_b[30]_add_7_OUT> created at line 0.

Found 58-bit adder for signal <n3252> created at line 0.

Found 58-bit adder for signal <GND_10_o_b[30]_add_9_OUT> created at line 0.

Found 57-bit adder for signal <n3256> created at line 0.

Found 57-bit adder for signal <GND_10_o_b[30]_add_11_OUT> created at line 0.

Found 56-bit adder for signal <n3260> created at line 0.

Found 56-bit adder for signal <GND_10_o_b[30]_add_13_OUT> created at line 0.

Found 55-bit adder for signal <n3264> created at line 0.

Found 55-bit adder for signal <GND_10_o_b[30]_add_15_OUT> created at line 0.

Found 54-bit adder for signal <n3268> created at line 0.

Found 54-bit adder for signal <GND_10_o_b[30]_add_17_OUT> created at line 0.

Found 53-bit adder for signal <n3272> created at line 0.

Found 53-bit adder for signal <GND_10_o_b[30]_add_19_OUT> created at line 0.

Found 52-bit adder for signal <n3276> created at line 0.

Found 52-bit adder for signal <GND_10_o_b[30]_add_21_OUT> created at line 0.

Found 51-bit adder for signal <n3280> created at line 0.

Found 51-bit adder for signal <GND_10_o_b[30]_add_23_OUT> created at line 0.

Found 50-bit adder for signal <n3284> created at line 0.

Found 50-bit adder for signal <GND_10_o_b[30]_add_25_OUT> created at line 0.

Found 49-bit adder for signal <n3288> created at line 0.

Found 49-bit adder for signal <GND_10_o_b[30]_add_27_OUT> created at line 0.

Found 48-bit adder for signal <n3292> created at line 0.

Found 48-bit adder for signal <GND_10_o_b[30]_add_29_OUT> created at line 0.

Found 47-bit adder for signal <n3296> created at line 0.

Found 47-bit adder for signal <GND_10_o_b[30]_add_31_OUT> created at line 0.

Found 46-bit adder for signal <n3300> created at line 0.

Found 46-bit adder for signal <GND_10_o_b[30]_add_33_OUT> created at line 0.

Found 45-bit adder for signal <n3304> created at line 0.

Found 45-bit adder for signal <GND_10_o_b[30]_add_35_OUT> created at line 0.

Found 44-bit adder for signal <n3308> created at line 0.


```
        inferred 32 Comparator(s).
        inferred 932 Multiplexer(s).
Unit <rem_31u_31u> synthesized.
```

=====

HDL Synthesis Report

Macro Statistics

# Multipliers	: 2
16x16-bit multiplier	: 1
31x31-bit multiplier	: 1
# Adders/Subtractors	: 65
31-bit adder	: 2
32-bit adder	: 3
33-bit adder	: 2
34-bit adder	: 2
35-bit adder	: 2
36-bit adder	: 2
37-bit adder	: 2
38-bit adder	: 2
39-bit adder	: 2
40-bit adder	: 2
41-bit adder	: 2
42-bit adder	: 2
43-bit adder	: 2
44-bit adder	: 2
45-bit adder	: 2
46-bit adder	: 2
47-bit adder	: 2
48-bit adder	: 2
49-bit adder	: 2
50-bit adder	: 2
51-bit adder	: 2
52-bit adder	: 2
53-bit adder	: 2
54-bit adder	: 2
55-bit adder	: 2
56-bit adder	: 2
57-bit adder	: 2
58-bit adder	: 2
59-bit adder	: 2
60-bit adder	: 2
61-bit adder	: 2
62-bit adder	: 2
# Registers	: 3
256-bit register	: 1
32-bit register	: 1
64-bit register	: 1
# Comparators	: 34
31-bit comparator lessequal	: 1
32-bit comparator lessequal	: 1
33-bit comparator equal	: 1
33-bit comparator greater	: 1
33-bit comparator lessequal	: 1
34-bit comparator lessequal	: 1
35-bit comparator lessequal	: 1
36-bit comparator lessequal	: 1
37-bit comparator lessequal	: 1
38-bit comparator lessequal	: 1
39-bit comparator lessequal	: 1
40-bit comparator lessequal	: 1

41-bit comparator lessequal	: 1
42-bit comparator lessequal	: 1
43-bit comparator lessequal	: 1
44-bit comparator lessequal	: 1
45-bit comparator lessequal	: 1
46-bit comparator lessequal	: 1
47-bit comparator lessequal	: 1
48-bit comparator lessequal	: 1
49-bit comparator lessequal	: 1
50-bit comparator lessequal	: 1
51-bit comparator lessequal	: 1
52-bit comparator lessequal	: 1
53-bit comparator lessequal	: 1
54-bit comparator lessequal	: 1
55-bit comparator lessequal	: 1
56-bit comparator lessequal	: 1
57-bit comparator lessequal	: 1
58-bit comparator lessequal	: 1
59-bit comparator lessequal	: 1
60-bit comparator lessequal	: 1
61-bit comparator lessequal	: 1
62-bit comparator lessequal	: 1
# Multiplexers	: 932
1-bit 2-to-1 multiplexer	: 930
31-bit 2-to-1 multiplexer	: 2

```
=====
*
Advanced HDL Synthesis
*
=====
```

WARNING:Xst:1710 - FF/Latch <dout_63> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dout_62> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dout_61> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dout_60> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dout_59> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dout_58> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dout_57> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dout_56> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dout_55> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dout_54> (without init value) has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

[illegible]

has a constant value of 0 in block <decryption_behav>. This FF/Latch will be trimmed during the optimization process.

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

<decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_241> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_242> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_243> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_244> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_245> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_246> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_247> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_248> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_249> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_250> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_251> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_252> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_253> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_254> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_255> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2404 - FFs/Latches <dout<63:31>> (without init value) have a constant value of 0 in block <decryption_behav>.

Synthesizing (advanced) Unit <decryption_behav>.

The following registers are absorbed into counter <cnt>: 1 register on signal <cnt>.

Unit <decryption_behav> synthesized (advanced).

[WARNING](#):Xst:2677 - Node <power_result_31> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_32> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_33> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_34> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_35> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_36> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_37> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_38> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_39> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_40> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_41> of sequential type is unconnected in block <decryption_behav>.
[WARNING](#):Xst:2677 - Node <power_result_42> of sequential type is unconnected in block <decryption_behav>.

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

=====

Advanced HDL Synthesis Report

Macro Statistics

# Multipliers	: 2
16x16-bit multiplier	: 1
31x31-bit multiplier	: 1
# Adders/Subtractors	: 32
31-bit adder carry in	: 32
# Counters	: 1
32-bit up counter	: 1
# Registers	: 62
Flip-Flops	: 62
# Comparators	: 34
31-bit comparator lessequal	: 1
32-bit comparator lessequal	: 1
33-bit comparator equal	: 1
33-bit comparator greater	: 1
33-bit comparator lessequal	: 1
34-bit comparator lessequal	: 1
35-bit comparator lessequal	: 1
36-bit comparator lessequal	: 1
37-bit comparator lessequal	: 1
38-bit comparator lessequal	: 1
39-bit comparator lessequal	: 1
40-bit comparator lessequal	: 1
41-bit comparator lessequal	: 1
42-bit comparator lessequal	: 1
43-bit comparator lessequal	: 1
44-bit comparator lessequal	: 1
45-bit comparator lessequal	: 1
46-bit comparator lessequal	: 1
47-bit comparator lessequal	: 1
48-bit comparator lessequal	: 1
49-bit comparator lessequal	: 1
50-bit comparator lessequal	: 1
51-bit comparator lessequal	: 1
52-bit comparator lessequal	: 1
53-bit comparator lessequal	: 1
54-bit comparator lessequal	: 1
55-bit comparator lessequal	: 1
56-bit comparator lessequal	: 1
57-bit comparator lessequal	: 1
58-bit comparator lessequal	: 1
59-bit comparator lessequal	: 1
60-bit comparator lessequal	: 1
61-bit comparator lessequal	: 1
62-bit comparator lessequal	: 1
# Multiplexers	: 932
1-bit 2-to-1 multiplexer	: 930
31-bit 2-to-1 multiplexer	: 2

=====

* Low Level Synthesis *

=====

[WARNING](#):Xst:2677 - Node <Mmult_n00253> of sequential type is unconnected in block <decryption_behav>.

Optimizing unit <decryption_behav> ...

Optimizing unit <rem_31u_31u> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block decryption_behav, actual ratio is 0.

Final Macro Processing ...

=====

Final Register Report

Macro Statistics

# Registers	: 94
Flip-Flops	: 94

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

* Design Summary *

=====

Top Level Output File Name : decryption_behav.ngc

Primitive and Black Box Usage:

# BELS	: 3048
# GND	: 1
# INV	: 7
# LUT1	: 31
# LUT2	: 10
# LUT3	: 243
# LUT4	: 525
# LUT5	: 409
# LUT6	: 447
# MUXCY	: 861
# VCC	: 1
# XORCY	: 513
# FlipFlops/Latches	: 94
# FDE	: 31
# FDRE	: 62
# FDSE	: 1
# Clock Buffers	: 1
# BUFGP	: 1
# IO Buffers	: 160
# IBUF	: 96
# OBUF	: 64
# DSPs	: 4
# DSP48E1	: 4

Device utilization summary:

Selected Device : 7vx330tffg1157-3

Slice Logic Utilization:

Number of Slice Registers:	94	out of	408000	0%
Number of Slice LUTs:	1672	out of	204000	0%
Number used as Logic:	1672	out of	204000	0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used:	1703			
Number with an unused Flip Flop:	1609	out of	1703	94%
Number with an unused LUT:	31	out of	1703	1%
Number of fully used LUT-FF pairs:	63	out of	1703	3%
Number of unique control sets:	2			

IO Utilization:

Number of IOs:	162			
Number of bonded IOBs:	161	out of	600	26%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs:	1	out of	32	3%
Number of DSP48E1s:	4	out of	1120	0%

Partition Resource Summary:

No Partitions were found in this design.

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	95

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: 44.231ns (Maximum Frequency: 22.609MHz)
Minimum input arrival time before clock: 46.972ns
Maximum output required time after clock: 0.511ns

Maximum combinational path delay: No path found

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 44.231ns (frequency: 22.609MHz)

Total number of paths / destination ports:

1515425629946615100000000000000000000000000000000 / 267

Delay: 44.231ns (Levels of Logic = 424)

Source: power_result_30 (FF)

Destination: dout_30 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: power_result_30 to dout_30

Cell:in->out	fanout	Gate	Net	Logical Name (Net Name)
		Delay	Delay	
FDRE:C->Q	4	0.232	0.357	power_result_30 (power_result_30)
LUT5:I3->O	1	0.043	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_lut<0>				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_lut<0>)
MUXCY:S->O	1	0.230	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<0>				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<0>)
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<1>				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<1>)
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<2>				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<2>)
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<3>				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<3>)
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<4>				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<4>)
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<5>				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<5>)
MUXCY:CI->O	2	0.147	0.293	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<6>				(power_result[30]_p_in[15]_rem_5/BUS_0002_INV_67_o)
LUT3:I2->O	2	0.043	0.460	
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_279_o1231				(power_result[30]_p_in[15]_rem_5/a[30]_GND_10_o_MUX_249_o)
LUT5:I1->O	0	0.043	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_lutdi				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_lutdi)
MUXCY:DI->O	1	0.218	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<0>				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<0>)
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<1>				(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<1>)
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<2>				

```

(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<5>)
MUXCY:CI->O      6  0.147  0.312
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<6>
(power_result[30]_p_in[15]_rem_5/BUS_0003_INV_129_o)
LUT3:I2->O      5  0.043  0.475
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_399_o1211
(power_result[30]_p_in[15]_rem_5/a[29]_GND_10_o_MUX_370_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<5>)
MUXCY:CI->O      7  0.147  0.317
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<6>
(power_result[30]_p_in[15]_rem_5/BUS_0004_INV_190_o)
LUT3:I2->O      4  0.043  0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_517_o1201
(power_result[30]_p_in[15]_rem_5/a[28]_GND_10_o_MUX_489_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<4>)

```

```

MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<5>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<6>)
MUXCY:CI->O      8    0.147    0.321
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<7>
(power_result[30]_p_in[15]_rem_5/BUS_0005_INV_250_o)
LUT3:I2->O      3    0.043    0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_633_o1191
(power_result[30]_p_in[15]_rem_5/a[27]_GND_10_o_MUX_606_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<5>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<6>)
MUXCY:CI->O     14    0.147    0.349
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<7>
(power_result[30]_p_in[15]_rem_5/BUS_0006_INV_309_o)
LUT3:I2->O      4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_747_o1181
(power_result[30]_p_in[15]_rem_5/a[26]_GND_10_o_MUX_721_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000

```

```

power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<5>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<6>)
MUXCY:CI->O      24      0.147      0.391
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<7>
(power_result[30]_p_in[15]_rem_5/BUS_0007_INV_367_o)
LUT3:I2->O      3      0.043      0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_859_o1171
(power_result[30]_p_in[15]_rem_5/a[25]_GND_10_o_MUX_834_o)
LUT4:I0->O      0      0.043      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_lutdi)
MUXCY:DI->O      1      0.218      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<0>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<1>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<2>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<3>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<4>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<5>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<6>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<7>)
MUXCY:CI->O      22      0.147      0.384
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<8>
(power_result[30]_p_in[15]_rem_5/BUS_0008_INV_424_o)
LUT3:I2->O      4      0.043      0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_969_o1161
(power_result[30]_p_in[15]_rem_5/a[24]_GND_10_o_MUX_945_o)
LUT4:I0->O      0      0.043      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_lutdi)
MUXCY:DI->O      1      0.218      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<0>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<1>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<2>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<3>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<4>

```

```

(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<6>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<7>)
MUXCY:CI->O      32  0.147  0.396
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<8>
(power_result[30]_p_in[15]_rem_5/BUS_0009_INV_480_o)
LUT3:I2->O       3  0.043  0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1077_o1151
(power_result[30]_p_in[15]_rem_5/a[23]_GND_10_o_MUX_1054_o)
LUT4:I0->O       0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<6>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<7>)
MUXCY:CI->O      28  0.147  0.395
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<8>
(power_result[30]_p_in[15]_rem_5/BUS_0010_INV_535_o)
LUT3:I2->O       4  0.043  0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1183_o1141
(power_result[30]_p_in[15]_rem_5/a[22]_GND_10_o_MUX_1161_o)
LUT4:I0->O       0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<2>)

```

```

MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<3>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<4>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<5>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<6>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<7>)
MUXCY:CI->O          40    0.147    0.397
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<8>
(power_result[30]_p_in[15]_rem_5/BUS_0011_INV_589_o)
LUT3:I2->O           3    0.043    0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1287_o1131
(power_result[30]_p_in[15]_rem_5/a[21]_GND_10_o_MUX_1266_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_lutdi)
MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<0>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<1>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<2>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<3>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<4>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<5>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<6>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<7>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<8>)
MUXCY:CI->O          34    0.147    0.396
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<9>
(power_result[30]_p_in[15]_rem_5/BUS_0012_INV_642_o)
LUT3:I2->O           4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1389_o1121
(power_result[30]_p_in[15]_rem_5/a[20]_GND_10_o_MUX_1369_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_lutdi)
MUXCY:DI->O          1    0.218    0.000

```



```

power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<0>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<1>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<2>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<3>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<4>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<5>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<6>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<7>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<8>)
MUXCY:CI->O      48      0.147      0.399
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<9>
(power_result[30]_p_in[15]_rem_5/BUS_0013_INV_694_o)
LUT3:I2->O      3      0.043      0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1489_o1101
(power_result[30]_p_in[15]_rem_5/a[19]_GND_10_o_MUX_1470_o)
LUT4:I0->O      0      0.043      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_lutdi)
MUXCY:DI->O      1      0.218      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<0>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<1>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<2>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<3>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<4>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<5>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<6>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<7>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<8>

```

```
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<8>)
MUXCY:CI->O      40  0.147  0.397
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<9>
(power_result[30]_p_in[15]_rem_5/BUS_0014_INV_745_o)
LUT3:I2->O      4  0.043  0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1587_o191
(power_result[30]_p_in[15]_rem_5/a[18]_GND_10_o_MUX_1569_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<6>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<7>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<8>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<9>)
MUXCY:CI->O      56  0.147  0.400
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<10>
(power_result[30]_p_in[15]_rem_5/BUS_0015_INV_795_o)
LUT3:I2->O      3  0.043  0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1683_o181
(power_result[30]_p_in[15]_rem_5/a[17]_GND_10_o_MUX_1666_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<3>)
```

```

MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<4>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<5>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<6>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<7>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<8>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<9>)
MUXCY:CI->O          46    0.147    0.398
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<10>
(power_result[30]_p_in[15]_rem_5/BUS_0016_INV_844_o)
LUT3:I2->O           4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1777_o171
(power_result[30]_p_in[15]_rem_5/a[16]_GND_10_o_MUX_1761_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_lutdi)
MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<0>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<1>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<2>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<3>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<4>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<5>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<6>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<7>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<8>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<9>)
MUXCY:CI->O          64    0.147    0.401
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<10>
(power_result[30]_p_in[15]_rem_5/BUS_0017_INV_892_o)
LUT3:I2->O           3    0.043    0.466

```

```

power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1869_o161
(power_result[30]_p_in[15]_rem_5/a[15]_GND_10_o_MUX_1854_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<5>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<6>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<7>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<8>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<9>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<10>)
MUXCY:CI->O      52    0.147    0.399
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<11>
(power_result[30]_p_in[15]_rem_5/BUS_0018_INV_939_o)
LUT3:I2->O      4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1959_o151
(power_result[30]_p_in[15]_rem_5/a[14]_GND_10_o_MUX_1945_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<4>

```

```

(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<6>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<7>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<8>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<9>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<10>)
MUXCY:CI->O      72  0.147  0.402
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<11>
(power_result[30]_p_in[15]_rem_5/BUS_0019_INV_985_o)
LUT3:I2->O       3  0.043  0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2047_o141
(power_result[30]_p_in[15]_rem_5/a[13]_GND_10_o_MUX_2034_o)
LUT4:I0->O       0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<6>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<7>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<8>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<9>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<10>)

```

```

MUXCY:CI->O          58    0.147    0.400
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<11>
(power_result[30]_p_in[15]_rem_5/BUS_0020_INV_1030_o)
LUT3:I2->O           4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2133_o131
(power_result[30]_p_in[15]_rem_5/a[12]_GND_10_o_MUX_2121_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_lutdi)
MUXCY:DI->O           1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<0>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<1>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<2>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<3>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<4>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<5>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<6>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<7>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<8>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<9>)
MUXCY:CI->O           1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<10>)
MUXCY:CI->O          80    0.147    0.403
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<11>
(power_result[30]_p_in[15]_rem_5/BUS_0021_INV_1074_o)
LUT3:I2->O           3    0.043    0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2217_o122
(power_result[30]_p_in[15]_rem_5/a[11]_GND_10_o_MUX_2206_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_lutdi)
MUXCY:DI->O           1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<0>)
MUXCY:CI->O           1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<1>)
MUXCY:CI->O           1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<2>)
MUXCY:CI->O           1    0.012    0.000

```

```
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<3>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<4>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<5>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<6>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<7>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<8>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<9>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<10>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<11>)
MUXCY:CI->O      64    0.148    0.401
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<12>
(power_result[30]_p_in[15]_rem_5/BUS_0022_INV_1117_o)
LUT3:I2->O      4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2299_o111
(power_result[30]_p_in[15]_rem_5/a[10]_GND_10_o_MUX_2289_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<0>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<1>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<2>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<3>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<4>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<5>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<6>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<7>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<8>
```

```

(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<8>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<9>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<10>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<11>)
MUXCY:CI->O      88  0.148  0.405
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<12>
(power_result[30]_p_in[15]_rem_5/BUS_0023_INV_1159_o)
LUT3:I2->O      3  0.043  0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2379_o1301
(power_result[30]_p_in[15]_rem_5/a[9]_GND_10_o_MUX_2370_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<0>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<1>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<2>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<3>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<4>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<5>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<6>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<7>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<8>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<9>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<10>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<11>)
MUXCY:CI->O      70  0.148  0.402
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<12>
(power_result[30]_p_in[15]_rem_5/BUS_0024_INV_1200_o)
LUT3:I2->O      4  0.043  0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2457_o1291
(power_result[30]_p_in[15]_rem_5/a[8]_GND_10_o_MUX_2449_o)

```



```

LUT4:I0->O          0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_lutdi)
MUXCY:DI->O          1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<0>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<1>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<2>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<3>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<4>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<5>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<6>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<7>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<8>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<9>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<10>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<11>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<12>)
MUXCY:CI->O          96  0.148  0.406
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<13>
(power_result[30]_p_in[15]_rem_5/BUS_0025_INV_1240_o)
LUT3:I2->O          3  0.043  0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2533_o1281
(power_result[30]_p_in[15]_rem_5/a[7]_GND_10_o_MUX_2526_o)
LUT4:I0->O          0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_lutdi)
MUXCY:DI->O          1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<0>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<1>)
MUXCY:CI->O          1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<2>)
MUXCY:CI->O          1  0.012  0.000

```

```
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<3>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<4>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<5>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<6>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<7>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<8>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<9>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<10>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<11>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<12>)
MUXCY:CI->O      76    0.148    0.403
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<13>
(power_result[30]_p_in[15]_rem_5/BUS_0026_INV_1279_o)
LUT3:I2->O      4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2607_o1271
(power_result[30]_p_in[15]_rem_5/a[6]_GND_10_o_MUX_2601_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<0>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<1>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<2>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<3>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<4>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<5>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<6>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<7>
```

```
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<7>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<8>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<9>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<10>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<11>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<12>)
MUXCY:CI->O     104  0.147  0.407
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<13>
(power_result[30]_p_in[15]_rem_5/BUS_0027_INV_1317_o)
LUT3:I2->O       3  0.043  0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2679_o1261
(power_result[30]_p_in[15]_rem_5/a[5]_GND_10_o_MUX_2674_o)
LUT4:I0->O       0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<0>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<1>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<2>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<3>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<4>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<5>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<6>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<7>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<8>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<9>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<10>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<11>)
```

```

MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<12>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<13>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<13>)
MUXCY:CI->O          82    0.148    0.404
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<14>
(power_result[30]_p_in[15]_rem_5/BUS_0028_INV_1354_o)
LUT3:I2->O           4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2749_o1251
(power_result[30]_p_in[15]_rem_5/a[4]_GND_10_o_MUX_2745_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_lutdi)
MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<0>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<1>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<2>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<3>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<4>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<5>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<6>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<7>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<8>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<9>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<10>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<11>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<12>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<13>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<13>)
MUXCY:CI->O          112    0.148    0.408
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<14>
(power_result[30]_p_in[15]_rem_5/BUS_0029_INV_1390_o)
LUT3:I2->O           4    0.043    0.470

```

```

power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2817_o1241
(power_result[30]_p_in[15]_rem_5/a[3]_GND_10_o_MUX_2814_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<5>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<6>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<7>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<8>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<9>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<10>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<11>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<12>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<13>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<13>)
MUXCY:CI->O     116    0.148    0.409
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<14>
(power_result[30]_p_in[15]_rem_5/BUS_0030_INV_1425_o)
LUT3:I2->O      3    0.043    0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2850_o1221
(power_result[30]_p_in[15]_rem_5/a[2]_GND_10_o_MUX_2848_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<1>

```

[illegible]

[illegible]

```

(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<27>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<28>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<28>)
MUXCY:CI->O          0    0.012    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<29>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<29>)
XORCY:CI->O          1    0.251    0.343
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_xor<30>
(power_result[30]_p_in[15]_rem_5/a[30]_b[30]_add_63_OUT[30:0]<30>)
LUT5:I3->O           1    0.043    0.000 power_result[30]_p_in[15]_rem_5/Mmux_o241
(power_result[30]_p_in[15]_rem_5_OUT<30>)
FDE:D                -0.001          dout_30
-----
Total                  44.231ns (18.064ns logic, 26.167ns route)
                        (40.8% logic, 59.2% route)

```

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports:
57888959203740727000 / 235

```

Offset:                46.972ns (Levels of Logic = 426)
Source:                q_in<15> (PAD)
Destination:          dout_30 (FF)
Destination Clock:    clk rising

```

Data Path: q_in<15> to dout_30

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	1	0.000	0.279	q_in_15_IBUF (q_in_15_IBUF)
DSP48E1:A15->P1	99	2.392	0.659	Mmult_n0024 (n0024<1>)
LUT5:I0->O	1	0.043	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_lut<0>				
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_lut<0>)				
MUXCY:S->O	1	0.230	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<0>				
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<0>)				
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<1>				
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<1>)				
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<2>				
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<2>)				
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<3>				
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<3>)				
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<4>				
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<4>)				
MUXCY:CI->O	1	0.013	0.000	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<5>				
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<5>)				
MUXCY:CI->O	2	0.147	0.293	
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0002_INV_67_o_cy<6>				
(power_result[30]_p_in[15]_rem_5/BUS_0002_INV_67_o)				
LUT3:I2->O	2	0.043	0.460	
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_279_o1231				
(power_result[30]_p_in[15]_rem_5/a[30]_GND_10_o_MUX_249_o)				
LUT5:I1->O	0	0.043	0.000	


```

power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<5>)
MUXCY:CI->O      6    0.147    0.312
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0003_INV_129_o_cy<6>
(power_result[30]_p_in[15]_rem_5/BUS_0003_INV_129_o)
LUT3:I2->O      5    0.043    0.475
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_399_o1211
(power_result[30]_p_in[15]_rem_5/a[29]_GND_10_o_MUX_370_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<5>)
MUXCY:CI->O      7    0.147    0.317
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0004_INV_190_o_cy<6>
(power_result[30]_p_in[15]_rem_5/BUS_0004_INV_190_o)
LUT3:I2->O      4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_517_o1201
(power_result[30]_p_in[15]_rem_5/a[28]_GND_10_o_MUX_489_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<1>

```

```

(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<6>)
MUXCY:CI->O      8  0.147  0.321
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0005_INV_250_o_cy<7>
(power_result[30]_p_in[15]_rem_5/BUS_0005_INV_250_o)
LUT3:I2->O      3  0.043  0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_633_o1191
(power_result[30]_p_in[15]_rem_5/a[27]_GND_10_o_MUX_606_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<6>)
MUXCY:CI->O     14  0.147  0.349
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0006_INV_309_o_cy<7>
(power_result[30]_p_in[15]_rem_5/BUS_0006_INV_309_o)
LUT3:I2->O      4  0.043  0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_747_o1181
(power_result[30]_p_in[15]_rem_5/a[26]_GND_10_o_MUX_721_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<1>)

```

```

MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<2>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<3>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<4>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<5>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<6>)
MUXCY:CI->O          24    0.147    0.391
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0007_INV_367_o_cy<7>
(power_result[30]_p_in[15]_rem_5/BUS_0007_INV_367_o)
LUT3:I2->O           3    0.043    0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_859_o1171
(power_result[30]_p_in[15]_rem_5/a[25]_GND_10_o_MUX_834_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_lutdi)
MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<0>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<1>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<2>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<3>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<4>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<5>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<6>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<7>)
MUXCY:CI->O          22    0.147    0.384
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0008_INV_424_o_cy<8>
(power_result[30]_p_in[15]_rem_5/BUS_0008_INV_424_o)
LUT3:I2->O           4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_969_o1161
(power_result[30]_p_in[15]_rem_5/a[24]_GND_10_o_MUX_945_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_lutdi)
MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<0>)
MUXCY:CI->O          1    0.013    0.000

```

```

power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<1>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<2>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<3>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<4>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<5>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<6>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<7>)
MUXCY:CI->O      32      0.147      0.396
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0009_INV_480_o_cy<8>
(power_result[30]_p_in[15]_rem_5/BUS_0009_INV_480_o)
LUT3:I2->O      3      0.043      0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1077_o1151
(power_result[30]_p_in[15]_rem_5/a[23]_GND_10_o_MUX_1054_o)
LUT4:I0->O      0      0.043      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_lutdi)
MUXCY:DI->O      1      0.218      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<0>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<1>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<2>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<3>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<4>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<5>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<6>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<7>)
MUXCY:CI->O      28      0.147      0.395
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0010_INV_535_o_cy<8>
(power_result[30]_p_in[15]_rem_5/BUS_0010_INV_535_o)
LUT3:I2->O      4      0.043      0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1183_o1141
(power_result[30]_p_in[15]_rem_5/a[22]_GND_10_o_MUX_1161_o)
LUT4:I0->O      0      0.043      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_lutdi

```

```

(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<6>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<7>)
MUXCY:CI->O      40  0.147  0.397
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0011_INV_589_o_cy<8>
(power_result[30]_p_in[15]_rem_5/BUS_0011_INV_589_o)
LUT3:I2->O      3  0.043  0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1287_o1131
(power_result[30]_p_in[15]_rem_5/a[21]_GND_10_o_MUX_1266_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<6>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<7>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<8>)

```

```

MUXCY:CI->O          34    0.147    0.396
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0012_INV_642_o_cy<9>
(power_result[30]_p_in[15]_rem_5/BUS_0012_INV_642_o)
LUT3:I2->O           4     0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1389_o1121
(power_result[30]_p_in[15]_rem_5/a[20]_GND_10_o_MUX_1369_o)
LUT4:I0->O           0     0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_lutdi)
MUXCY:DI->O           1     0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<0>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<1>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<2>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<3>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<4>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<5>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<6>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<7>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<8>)
MUXCY:CI->O          48     0.147    0.399
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0013_INV_694_o_cy<9>
(power_result[30]_p_in[15]_rem_5/BUS_0013_INV_694_o)
LUT3:I2->O           3     0.043    0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1489_o1101
(power_result[30]_p_in[15]_rem_5/a[19]_GND_10_o_MUX_1470_o)
LUT4:I0->O           0     0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_lutdi)
MUXCY:DI->O           1     0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<0>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<1>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<2>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<3>)
MUXCY:CI->O           1     0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<4>)
MUXCY:CI->O           1     0.013    0.000

```

```

power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<5>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<6>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<7>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<8>)
MUXCY:CI->O      40     0.147     0.397
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0014_INV_745_o_cy<9>
(power_result[30]_p_in[15]_rem_5/BUS_0014_INV_745_o)
LUT3:I2->O      4      0.043     0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1587_o191
(power_result[30]_p_in[15]_rem_5/a[18]_GND_10_o_MUX_1569_o)
LUT4:I0->O      0      0.043     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_lutdi)
MUXCY:DI->O      1      0.218     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<0>)
MUXCY:CI->O      1      0.013     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<1>)
MUXCY:CI->O      1      0.013     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<2>)
MUXCY:CI->O      1      0.013     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<3>)
MUXCY:CI->O      1      0.013     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<4>)
MUXCY:CI->O      1      0.013     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<5>)
MUXCY:CI->O      1      0.013     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<6>)
MUXCY:CI->O      1      0.013     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<7>)
MUXCY:CI->O      1      0.013     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<8>)
MUXCY:CI->O      1      0.013     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<9>)
MUXCY:CI->O      56     0.147     0.400
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0015_INV_795_o_cy<10>
(power_result[30]_p_in[15]_rem_5/BUS_0015_INV_795_o)
LUT3:I2->O      3      0.043     0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1683_o181
(power_result[30]_p_in[15]_rem_5/a[17]_GND_10_o_MUX_1666_o)
LUT4:I0->O      0      0.043     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_lutdi)
MUXCY:DI->O      1      0.218     0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<0>

```

```

(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<5>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<6>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<7>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<8>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<9>)
MUXCY:CI->O      46    0.147    0.398
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0016_INV_844_o_cy<10>
(power_result[30]_p_in[15]_rem_5/BUS_0016_INV_844_o)
LUT3:I2->O      4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1777_o171
(power_result[30]_p_in[15]_rem_5/a[16]_GND_10_o_MUX_1761_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<5>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<6>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<7>)

```



```

MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<8>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<9>)
MUXCY:CI->O      64    0.147    0.401
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0017_INV_892_o_cy<10>
(power_result[30]_p_in[15]_rem_5/BUS_0017_INV_892_o)
LUT3:I2->O       3    0.043    0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1869_o161
(power_result[30]_p_in[15]_rem_5/a[15]_GND_10_o_MUX_1854_o)
LUT4:I0->O       0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<5>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<6>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<7>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<8>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<9>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<10>)
MUXCY:CI->O      52    0.147    0.399
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0018_INV_939_o_cy<11>
(power_result[30]_p_in[15]_rem_5/BUS_0018_INV_939_o)
LUT3:I2->O       4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_1959_o151
(power_result[30]_p_in[15]_rem_5/a[14]_GND_10_o_MUX_1945_o)
LUT4:I0->O       0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000

```

```

power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<1>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<2>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<3>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<4>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<5>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<6>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<7>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<8>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<9>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<10>)
MUXCY:CI->O      72      0.147      0.402
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0019_INV_985_o_cy<11>
(power_result[30]_p_in[15]_rem_5/BUS_0019_INV_985_o)
LUT3:I2->O      3      0.043      0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2047_o141
(power_result[30]_p_in[15]_rem_5/a[13]_GND_10_o_MUX_2034_o)
LUT4:I0->O      0      0.043      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_lutdi)
MUXCY:DI->O      1      0.218      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<0>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<1>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<2>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<3>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<4>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<5>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<6>)
MUXCY:CI->O      1      0.013      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<7>

```

```

(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<7>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<8>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<9>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<10>)
MUXCY:CI->O      58  0.147  0.400
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0020_INV_1030_o_cy<11>
(power_result[30]_p_in[15]_rem_5/BUS_0020_INV_1030_o)
LUT3:I2->O      4  0.043  0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2133_o131
(power_result[30]_p_in[15]_rem_5/a[12]_GND_10_o_MUX_2121_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<0>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<1>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<2>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<3>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<4>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<5>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<6>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<7>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<8>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<9>)
MUXCY:CI->O      1  0.013  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<10>)
MUXCY:CI->O      80  0.147  0.403
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0021_INV_1074_o_cy<11>
(power_result[30]_p_in[15]_rem_5/BUS_0021_INV_1074_o)
LUT3:I2->O      3  0.043  0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2217_o122
(power_result[30]_p_in[15]_rem_5/a[11]_GND_10_o_MUX_2206_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_lutdi)

```

```

MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<0>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<1>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<2>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<3>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<4>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<5>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<6>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<7>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<8>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<9>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<10>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<11>)
MUXCY:CI->O          64    0.148    0.401
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0022_INV_1117_o_cy<12>
(power_result[30]_p_in[15]_rem_5/BUS_0022_INV_1117_o)
LUT3:I2->O           4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2299_o111
(power_result[30]_p_in[15]_rem_5/a[10]_GND_10_o_MUX_2289_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_lutdi)
MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<0>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<1>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<2>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<3>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<4>)
MUXCY:CI->O          1    0.012    0.000

```

```
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<5>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<6>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<7>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<8>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<9>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<10>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<11>)
MUXCY:CI->O      88      0.148      0.405
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0023_INV_1159_o_cy<12>
(power_result[30]_p_in[15]_rem_5/BUS_0023_INV_1159_o)
LUT3:I2->O      3      0.043      0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2379_o1301
(power_result[30]_p_in[15]_rem_5/a[9]_GND_10_o_MUX_2370_o)
LUT4:I0->O      0      0.043      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_lutdi)
MUXCY:DI->O      1      0.218      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<0>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<1>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<2>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<3>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<4>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<5>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<6>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<7>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<8>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<9>)
MUXCY:CI->O      1      0.012      0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<10>
```

```

(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<10>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<11>)
MUXCY:CI->O      70    0.148    0.402
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0024_INV_1200_o_cy<12>
(power_result[30]_p_in[15]_rem_5/BUS_0024_INV_1200_o)
LUT3:I2->O      4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2457_o1291
(power_result[30]_p_in[15]_rem_5/a[8]_GND_10_o_MUX_2449_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<0>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<1>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<2>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<3>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<4>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<5>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<6>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<7>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<8>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<9>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<10>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<11>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<12>)
MUXCY:CI->O      96    0.148    0.406
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0025_INV_1240_o_cy<13>
(power_result[30]_p_in[15]_rem_5/BUS_0025_INV_1240_o)
LUT3:I2->O      3    0.043    0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2533_o1281
(power_result[30]_p_in[15]_rem_5/a[7]_GND_10_o_MUX_2526_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_lutdi)

```

```

MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<0>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<1>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<2>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<3>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<4>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<5>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<6>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<7>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<8>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<9>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<10>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<11>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<12>)
MUXCY:CI->O          76    0.148    0.403
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0026_INV_1279_o_cy<13>
(power_result[30]_p_in[15]_rem_5/BUS_0026_INV_1279_o)
LUT3:I2->O           4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2607_o1271
(power_result[30]_p_in[15]_rem_5/a[6]_GND_10_o_MUX_2601_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_lutdi)
MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<0>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<1>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<2>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<3>)
MUXCY:CI->O          1    0.012    0.000

```

```
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<4>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<5>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<6>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<7>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<8>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<9>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<10>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<11>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<12>)
MUXCY:CI->O          104    0.147    0.407
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0027_INV_1317_o_cy<13>
(power_result[30]_p_in[15]_rem_5/BUS_0027_INV_1317_o)
LUT3:I2->O           3    0.043    0.466
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2679_o1261
(power_result[30]_p_in[15]_rem_5/a[5]_GND_10_o_MUX_2674_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_lutdi)
MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<0>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<1>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<2>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<3>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<4>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<5>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<6>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<7>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<8>
```



```
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<8>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<9>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<10>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<11>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<12>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<13>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<13>)
MUXCY:CI->O      82  0.148  0.404
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0028_INV_1354_o_cy<14>
(power_result[30]_p_in[15]_rem_5/BUS_0028_INV_1354_o)
LUT3:I2->O      4  0.043  0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2749_o1251
(power_result[30]_p_in[15]_rem_5/a[4]_GND_10_o_MUX_2745_o)
LUT4:I0->O      0  0.043  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_lutdi)
MUXCY:DI->O      1  0.218  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<0>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<1>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<2>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<3>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<4>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<5>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<6>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<7>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<8>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<9>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<10>)
MUXCY:CI->O      1  0.012  0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<11>)
```

```

MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<12>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<13>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<13>)
MUXCY:CI->O        112    0.148    0.408
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0029_INV_1390_o_cy<14>
(power_result[30]_p_in[15]_rem_5/BUS_0029_INV_1390_o)
LUT3:I2->O           4    0.043    0.470
power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2817_o1241
(power_result[30]_p_in[15]_rem_5/a[3]_GND_10_o_MUX_2814_o)
LUT4:I0->O           0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_lutdi)
MUXCY:DI->O          1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<0>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<1>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<2>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<3>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<4>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<5>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<6>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<7>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<8>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<9>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<10>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<11>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<12>)
MUXCY:CI->O          1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<13>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<13>)
MUXCY:CI->O        116    0.148    0.409
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0030_INV_1425_o_cy<14>
(power_result[30]_p_in[15]_rem_5/BUS_0030_INV_1425_o)
LUT3:I2->O           3    0.043    0.466

```

```

power_result[30]_p_in[15]_rem_5/Mmux_a[0]_GND_10_o_MUX_2850_o1221
(power_result[30]_p_in[15]_rem_5/a[2]_GND_10_o_MUX_2848_o)
LUT4:I0->O      0    0.043    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_lutdi
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_lutdi)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<0>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<0>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<1>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<1>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<2>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<2>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<3>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<3>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<4>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<4>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<5>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<5>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<6>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<6>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<7>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<7>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<8>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<8>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<9>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<9>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<10>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<10>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<11>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<11>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<12>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<12>)
MUXCY:CI->O      1    0.013    0.000
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<13>
(power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<13>)
MUXCY:CI->O      90    0.148    0.405
power_result[30]_p_in[15]_rem_5/Mcompar_BUS_0031_INV_1459_o_cy<14>
(power_result[30]_p_in[15]_rem_5/BUS_0031_INV_1459_o)
LUT3:I2->O      2    0.043    0.283
power_result[30]_p_in[15]_rem_5/Mmux_n3358121 (power_result[30]_p_in[15]_rem_5/n3358<1>)
MUXCY:DI->O      1    0.218    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<1>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<1>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<2>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<2>)
MUXCY:CI->O      1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<3>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<3>)

```

[illegible]

```

power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<24>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<24>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<25>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<25>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<26>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<26>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<27>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<27>)
MUXCY:CI->O          1    0.012    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<28>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<28>)
MUXCY:CI->O          0    0.012    0.000
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<29>
(power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_cy<29>)
XORCY:CI->O          1    0.251    0.343
power_result[30]_p_in[15]_rem_5/Madd_a[30]_b[30]_add_63_OUT[30:0]_Madd_xor<30>
(power_result[30]_p_in[15]_rem_5/a[30]_b[30]_add_63_OUT[30:0]<30>)
LUT5:I3->O          1    0.043    0.000 power_result[30]_p_in[15]_rem_5/Mmux_o241
(power_result[30]_p_in[15]_rem_5_OUT<30>)
FDE:D                -0.001          dout_30
-----
Total                46.972ns (20.224ns logic, 26.748ns route)
                        (43.1% logic, 56.9% route)

```

```

=====
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
Total number of paths / destination ports: 31 / 31
-----

```

```

Offset:              0.511ns (Levels of Logic = 1)
Source:              dout_30 (FF)
Destination:        dout<30> (PAD)
Source Clock:        clk rising

```

Data Path: dout_30 to dout<30>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDE:C->Q	1	0.232	0.279	dout_30 (dout_30)
OBUF:I->O		0.000		dout_30_OBUF (dout<30>)
Total		0.511ns (0.232ns logic, 0.279ns route) (45.4% logic, 54.6% route)		

```

=====
Cross Clock Domains Report:
-----

```

Clock to Setup on destination clock clk

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
clk	44.231			

Total REAL time to Xst completion: 23.00 secs

Total CPU time to Xst completion: 22.77 secs

-->

Total memory usage is 4647544 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 486 (0 filtered)

Number of infos : 0 (0 filtered)