Electronics 2 Projec(part 2) Report

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Design and Analysis of a Power Amplifier

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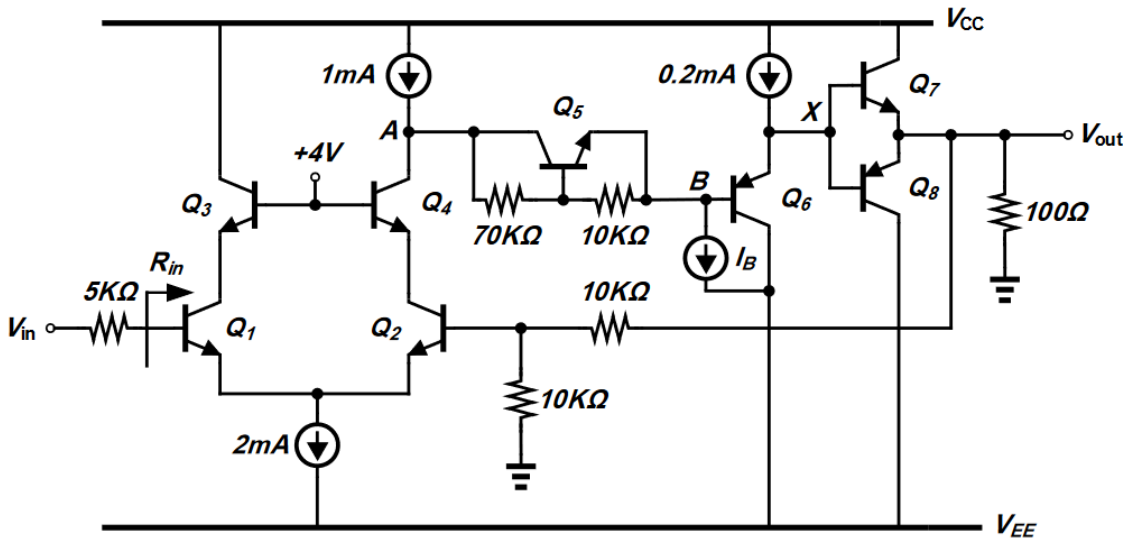

Figure 1: the given circuit for the project

3.1 Finding the input and output stages

it can be seen that the Q1, Q3 pair and Q2, Q4 pair are cascoded common emitter amplifiers that form the differential input stage.
also Q7 and Q8 form a push-pull output stage.

3.2 Explaining the operation of I_B and Q6

Q6 is a voltage buffer which is typically used for current gain(which we need because we want to design a power amplifier) and also for making the output resistance seen be previous stages larger.
Q5 is a V_{BE} multiplier and is used for changing the DC operating point to maximize swing. the V_{BE} multiplier only works when Q5 is on meaning the current passing from Q5 should always be positive, I_B current source ensures that the current passing through Q5 is large enough and never gets negative due to the base current of Q6.
the maximum current of the emitter of Q6 can be 0.2mA (when all of the current source current passes from Q6) thus the maximum of its base current is $\frac{0.2}{\beta}mA$.
and the current passing the Base Emitter resistor of Q5 is $\frac{0.7}{1k} = 0.7mA$. there also should be a reasonable operating point current given to Q5, thus we choose 1mA to be a reasonable amount of current for the current source and choose $I_B = 1mA$.

3.3 Finding the operation point of the Transistors

for finding the operating points we can see that when V_{in} is 0 then V_{out} is zero because:

$$V_{in} = 0, I_{B1} \backsimeq 0 \rightarrow V_{E1} = V_{E2} = -0.7 \rightarrow V_{B2} = 0 \rightarrow V_{out} = 0$$

thus we can calculate the floating node voltages(like the collector nodes of transistors) by knowing the output DC voltage.
here we list the operating point values(assuming $V_{BE} = 0.7V$):

Transistor	Ic	V_{CE}
Q1	1mA	4V
Q2	1mA	4V
Q3	1mA	1.6V
Q4	1mA	6.7V
Q5	I_B	5.6V
Q6	0.2mA	10V
Q7	0 A	10V
Q8	0 A	10V

3.4 Dead zone and its removal by feedback

in type B push-pull stages due to having no bias current on zero input the transistors will be in cutoff and will turn on when the input either reaches $V_{BE_{on}}$ or $-V_{BE_{on}}$.
this makes them efficient by dissipating no power at zero input and also dissipating low power on lower inputs. the disadvantage to these stages is that until the input turns on the transistor the output will be zero and their transfer characteristic won't be linear and they will have some distortion(see the figure below).

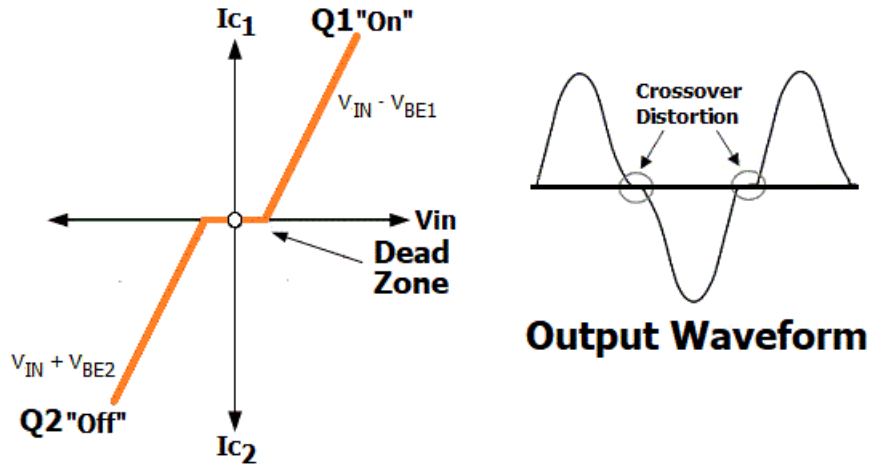

Figure 2: the B class amplifier characteristic and the output distortion

The problem of dead zone in push-pull amplifier can be solved (or somewhat minimized) by using a feedback loop consider the figure below which is a simple push-pull stage with a preAmp:

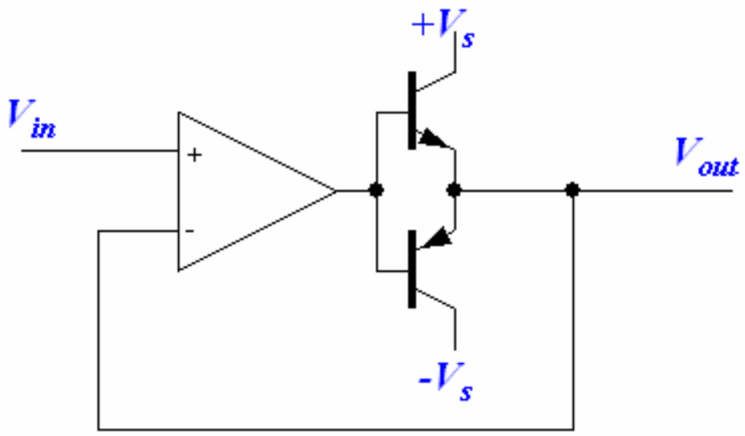

Figure 3: push-pull stage with preAmp

the open loop characteristic of the above circuit is that of a normal push-pull stage but with slop of A (A is the gain of the amplifier).
now the loop feedback has gain $f = 1$ and the type of feedback is voltage - voltage (or series - shunt). the closed loop gain will be $A_v = A\frac{1}{1+Af} = \frac{A}{1+A} \backsimeq 1$ which is the gain we desire from a push pull stage, but the dead zone limits will now be:

$$\frac{V_{BE_{on}}}{1+Af} = \frac{V_{BE_{on}}}{1+A} \backsimeq \frac{V_{BE_{on}}}{A}$$

considering that usually amplifiers have very high gain the distortion will be neglectable.
of course in real circuits we never put an op-amp before a push-pull stage because the push-pull stage is part of the op-amp! but putting the stage in a feedback loop within our amplifier (as done in the circuit of this project) will move the limits of the dead zone from $V_{BE_{on}}$ to $\frac{V_{BE_{on}}}{1+A_{OL}f}$ which again makes the dead zone size neglectable.

3.5 finding ICMR and Swing

the Input Common Mode Range (ICMR) is bounded by Q3 base voltage and the voltage needed to be on the current source thus the common mode minimum is $V_{EE} + V_{CS} + V_{BE_{on}} = -9.1V$ and the common mode maximum is $4 - V_{BE_{on3}} - V_{CB_{sat1}} = 2.8V$.
swing analysis will be done in the next part but the result will be a swing of about 0.7V which is very low compared to the range of our voltage sources.

3.6 Swing Analysis

there are two main things in this design that prevent us from getting a high swing. firstly node A swing is limited by the Q4 saturation voltage and node A should have a voltage of at least $4V + V_{CB_{sat}} = 4.4V$ which results in the output node swing minimum being limited at about $V_{out} = -0.7V$.
even if the above problem is solved the maximum swing would be limited by the $0.2mA$ current source. if we assume all of the current going into the base of Q7 the output current would be $I_{out} = 0.2\beta mA = 30mA$ assuming $\beta = 150$. now the output voltage will be $V_{out} = R_{out}I_{out} = 100 \times 30mA = 3V$ which is still low so we should either give the current source bigger current or make β larger by using Darlington pair or Sziklai pair instead of the output stages NPN and PNP single transistors.

3.7 the circuit schematic in LTspcie

the schematic is shown below:

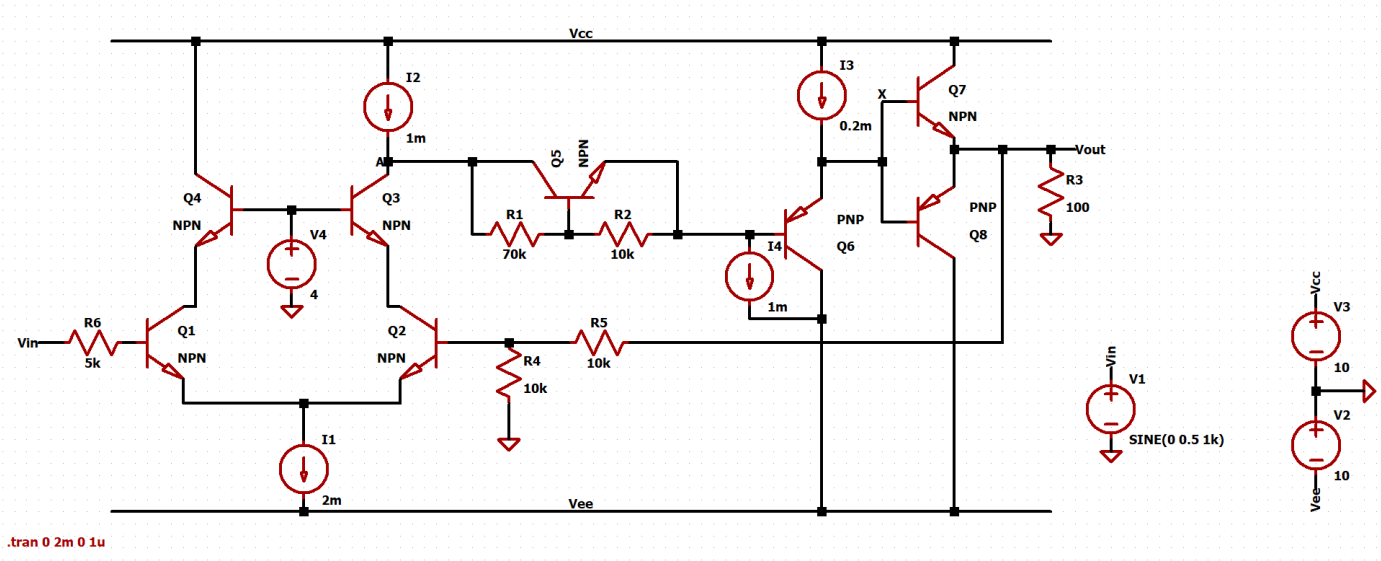

Figure 4: the circuit schematic in LTspice

3.8 Voltages of the output and X node

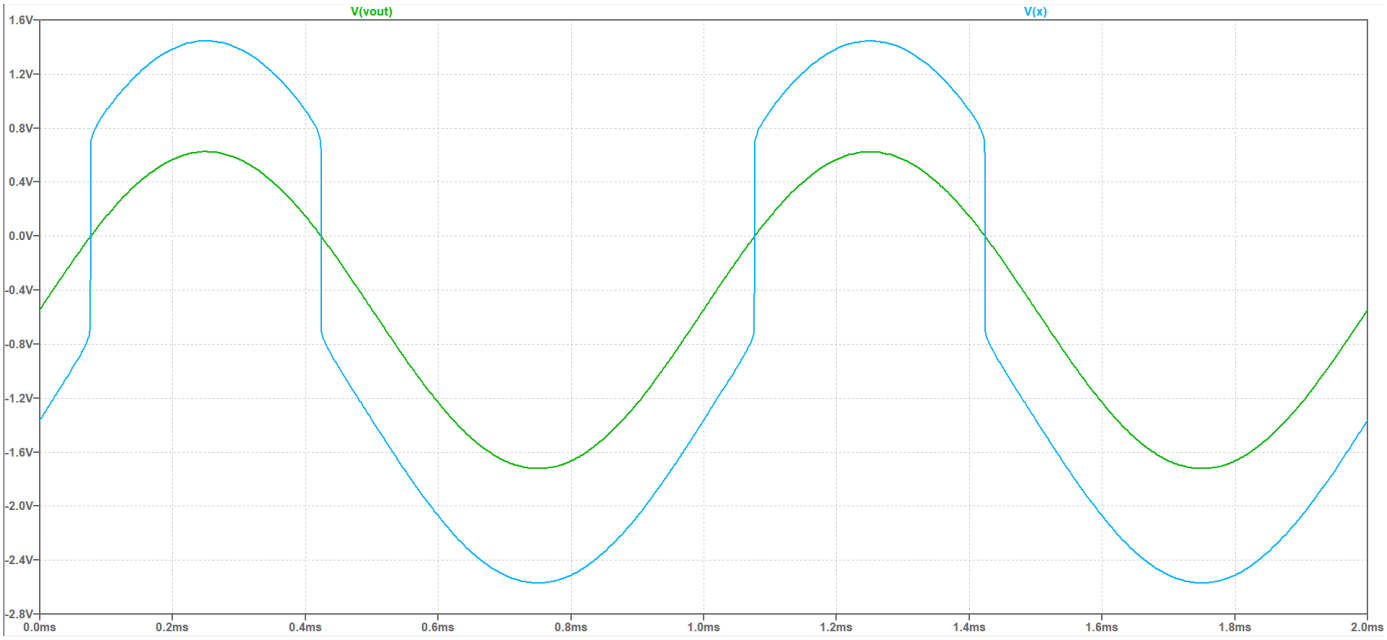

Figure 5: the plot of output and X node in LTspice

As it can be seen the dead zone that was present in the output is removed due to feedback (just as we expected from section 4 reasoning). it is interesting that the feedback automatically handles the dead zone problem and instead of creating a dead zone it creates sudden jumps in the voltage of node X to smooth the output signal.

3.9 Getting maximum achievable swing by changing operating points

Removing the swing limit of the 0.2m current source is relatively easy, we will just make the current larger. the real problem is the swing of node A which is limited by the 4V voltage source. the problem is we cannot just lower the value to any number because the base of Q3 and Q4 also limit the input voltage range and though by lowering this nodes voltage we get bigger output swing we lose our input swing which is quite troublesome.
We can see that the input higher voltage limit is $V_{source} - V_{BE_{on}} - V_{CB_{sat}}$ and the node A lower voltage limit is $V_{source} + V_{CB_{sat}}$ so the node should have a voltage to handle both input and output swing.
by experimenting and a little tweaking we found 2V to be a reasonable value.
below you can see the new tweaked circuit with the maximum swing it can give:

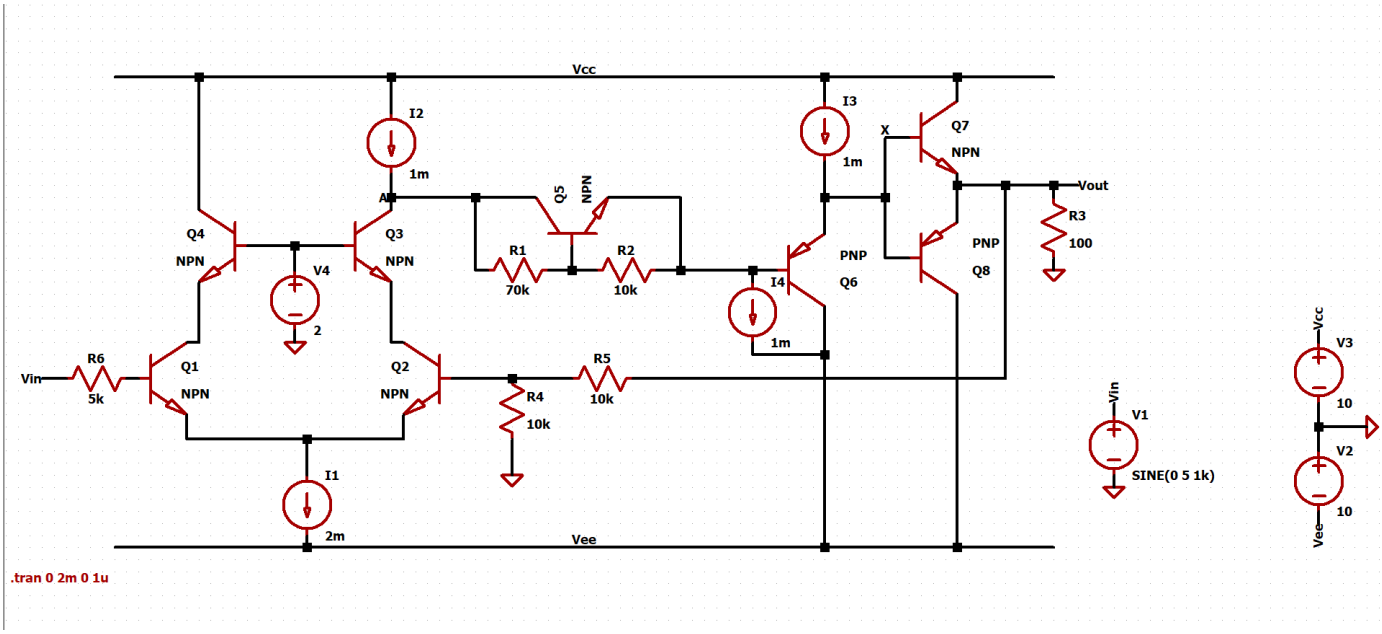

Figure 6: the circuit with changed bias points and maximum swing in LTSPICE

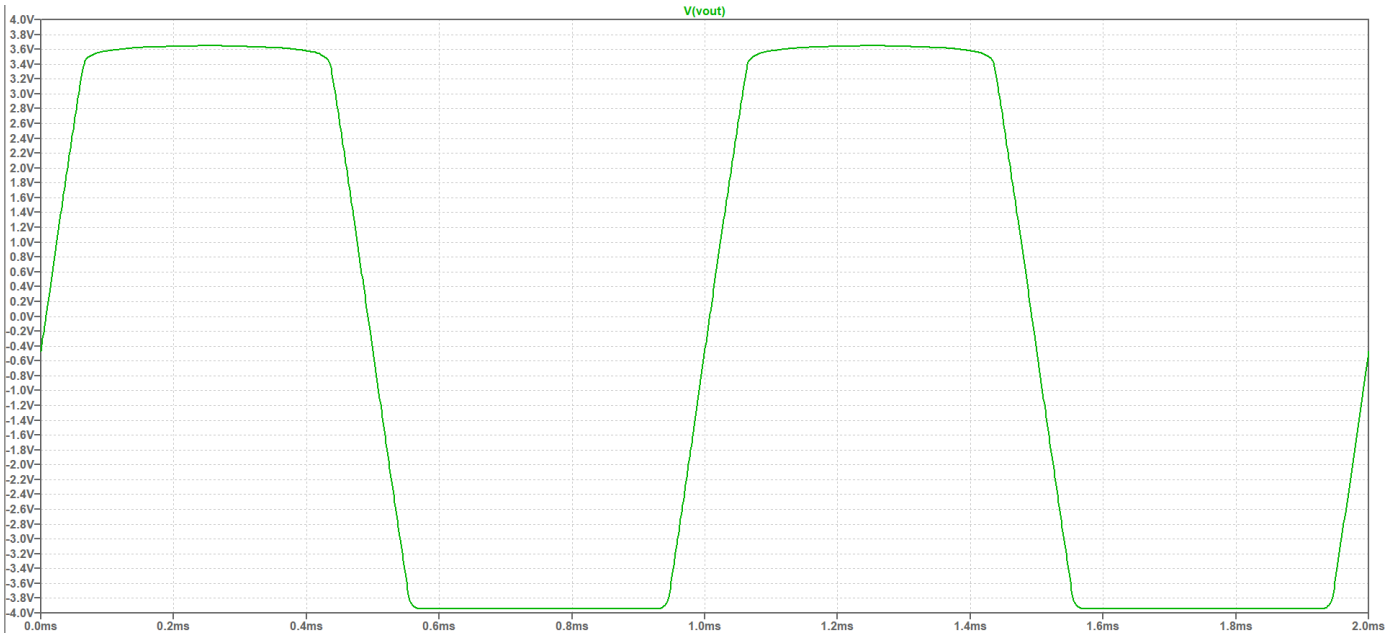

Figure 7: the output with changed bias points and maximum swing in LTSPICE

as it can be seen the circuit has a peak to peak swing of 7.6V or alternatively a swing of 3.8V which is still pretty low compared to the voltage sources but better than the given circuit.

3.10 Total Harmonic Distortion (THD)

THD or Total Harmonic Distortion is a measurement of how much a signal is distorted by computing the value of energy in the output harmonics other than the fundamental frequency(for example if the fundamental is 1kHz harmonics are 2kHz, 3kHz, 4kHz and ...) it is defined as:

$$\text{THD} = \frac{\text{rms value of output except fundamental}}{\text{rms of fundamental}}$$

in LTspice we can add the directive " .fourier Freq V(out) " to get the THD in out error log.

we did this with last part circuit and the result is as below:

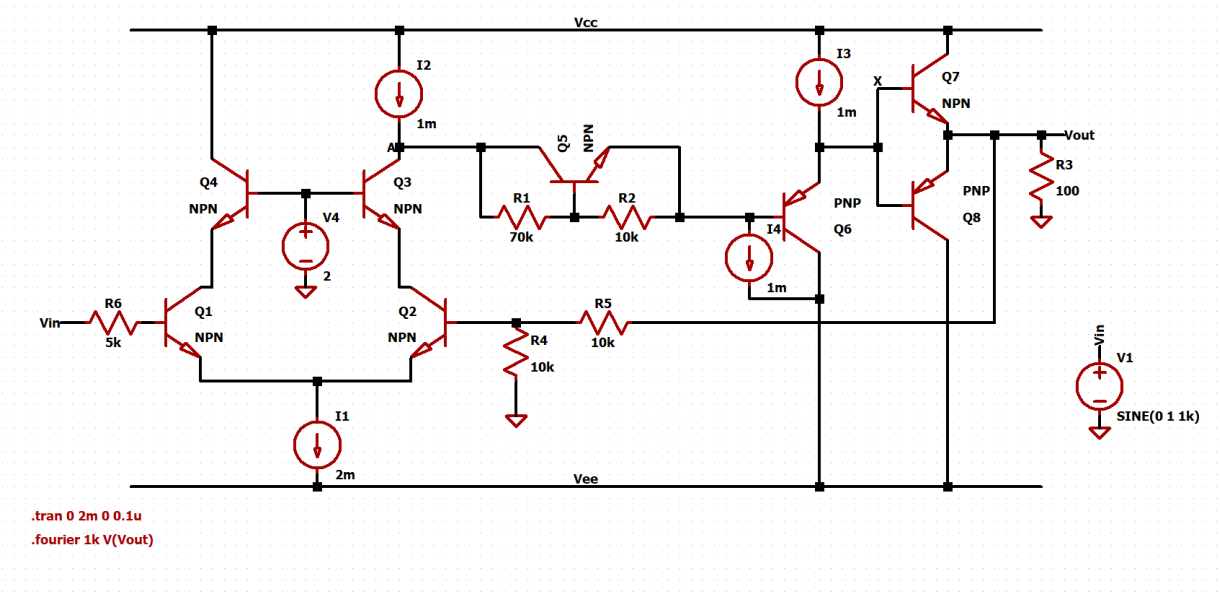

Figure 8: the circuit with THD directive in LTSPICE

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]
1	1.000e+03	1.990e+00	1.000e+00	-0.00°
2	2.000e+03	2.959e-04	1.487e-04	93.40°
3	3.000e+03	2.584e-04	1.299e-04	-15.26°
4	4.000e+03	1.583e-04	7.958e-05	43.96°
5	5.000e+03	1.970e-05	9.903e-06	-3.81°
6	6.000e+03	1.917e-04	9.636e-05	-5.09°
7	7.000e+03	4.807e-04	2.416e-04	86.33°
8	8.000e+03	4.511e-04	2.267e-04	179.37°
9	9.000e+03	3.198e-04	1.607e-04	-118.51°

Total Harmonic Distortion: 0.043626%(0.048564%)

Figure 9: THD of the circuit output in LTspice

as seen above THD = 0.0436%

4 Design

4.1 Folded Cascode Stage

below you can see normal Cascode stage:

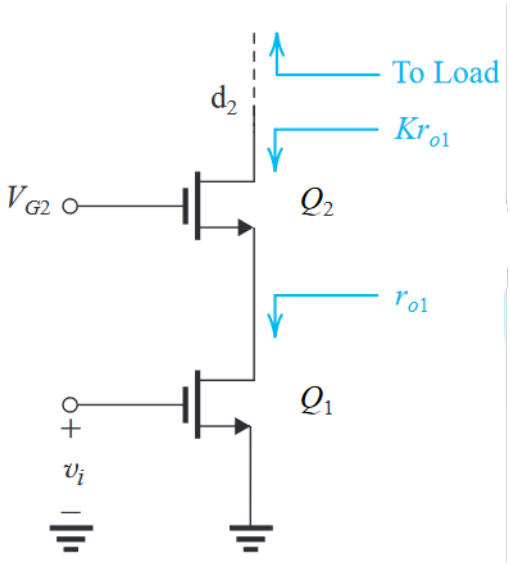

Figure 10: Cascode Stage

the problem of a normal Cascode stage is it gets a lot of headroom due to the existence of V_G (or V_B in bipolar). this problem is solved in the folded Cascode stage by making the second transistor PNP and placing it in another branch and connecting them along with a current source, this stage does exactly the same function in small signal but lets us swing better in large signal due to the freedom of choice for V_G.

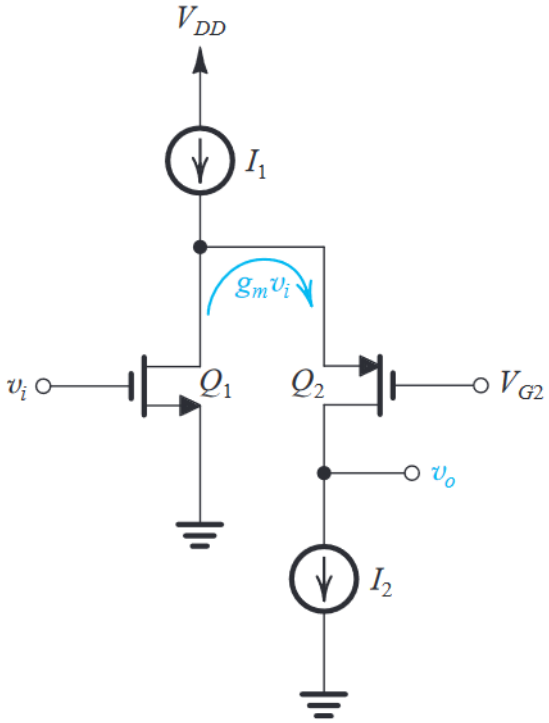

Figure 11: Cascode Stage

also it should be noted that the folded Cascode has the disadvantage of more power usage and the advantage that we can set I_2 small enough so g_{m2} can get very bigger.

4.2

there are no deliverables for this section.

4.3 Image of the Designed circuit

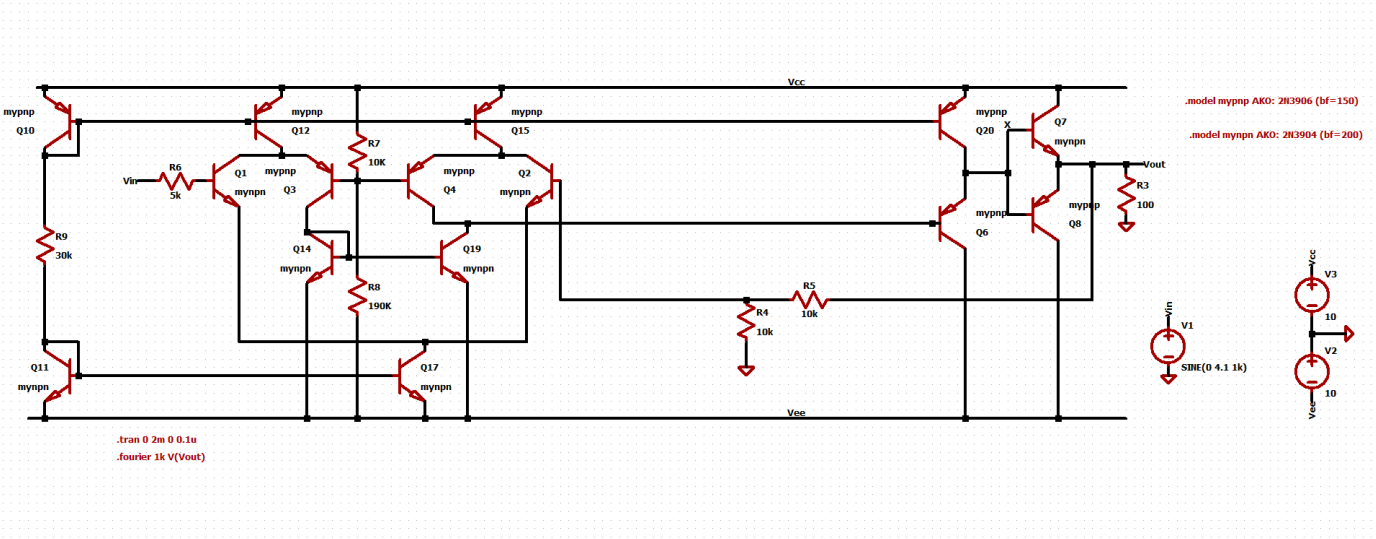

Figure 12: the Designed Circuit

4.4

I. Closed Loop Gain

As seen in the figure below the closed loop gain is 2:

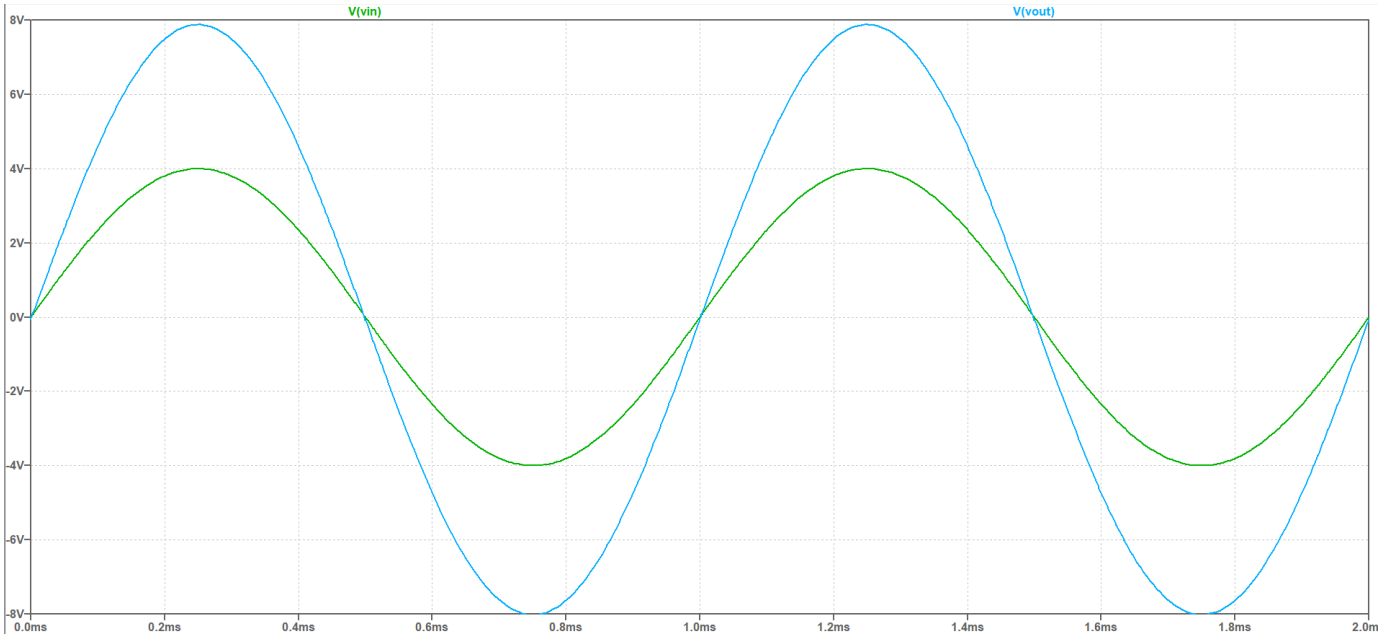

Figure 13: the input and output of the circuit near maximum swing

II. Swing

As seen below the swing is about 8.4V or 16.8V peak to peak:

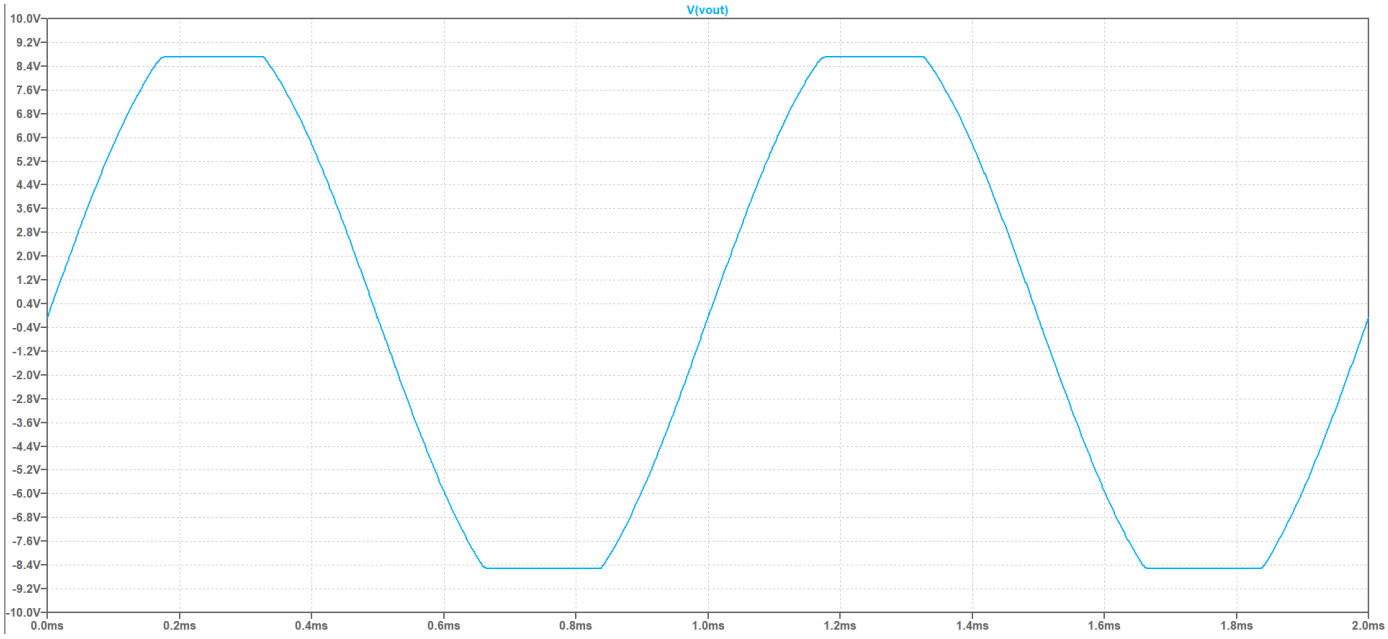

Figure 14: the circuit output in its maximum swing bounds

III. Power

As seen below the power given by sources about 49mW:

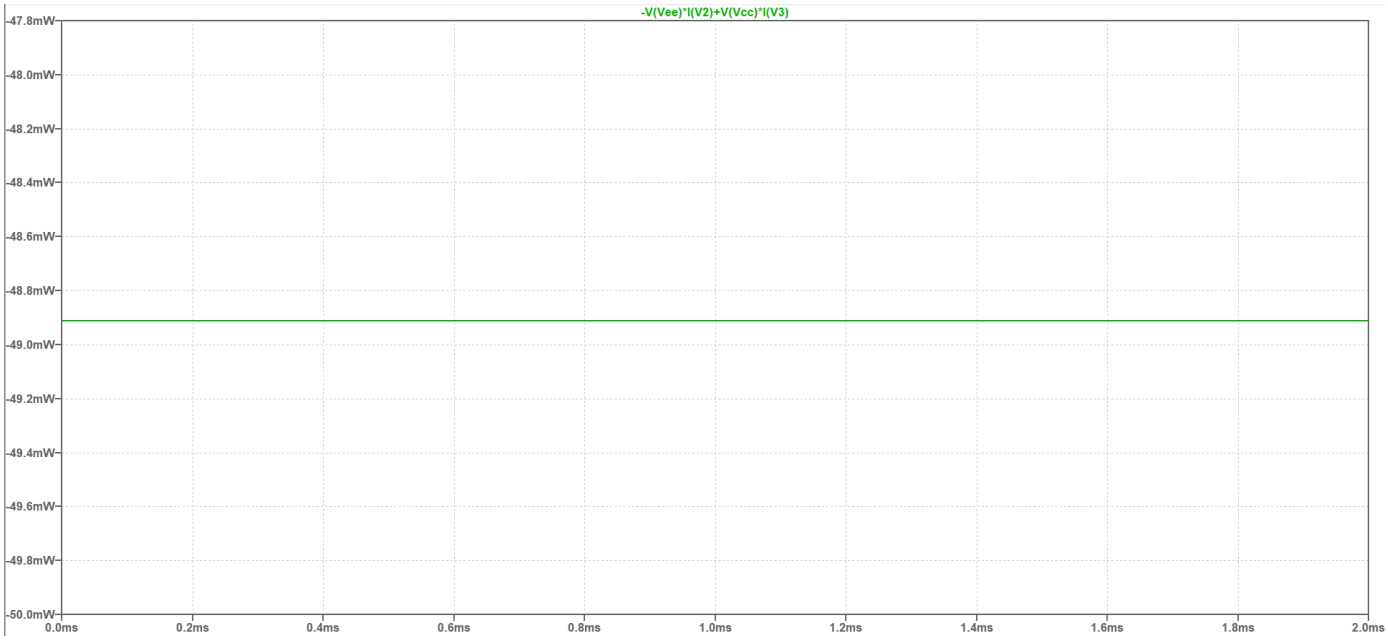

Figure 15: the circuit power in 0 input

IV. THD

As seen below the THD is about 0.026%:

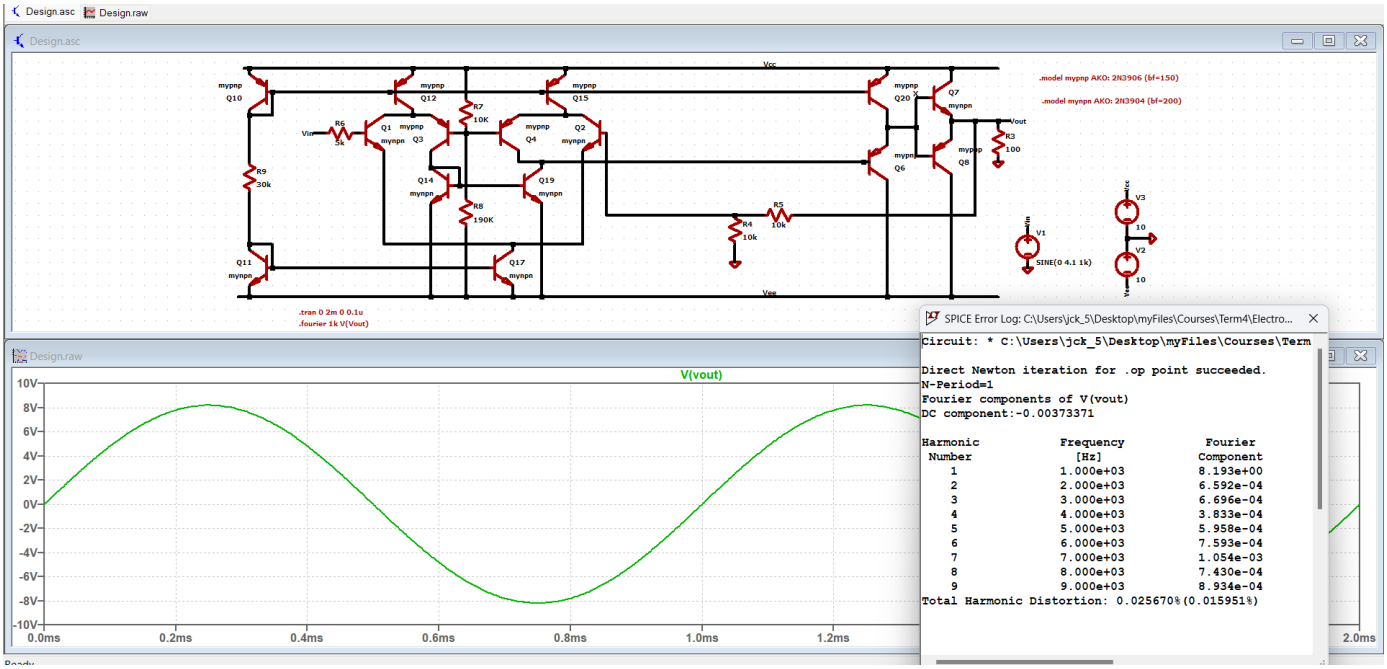

Figure 16: the THD of the circuit power in 16.4V peak to peak

V. changing feedback resistors

As seen below the THD increases by changing the feedback resistors to 50k from 0.026% to 0.033%:

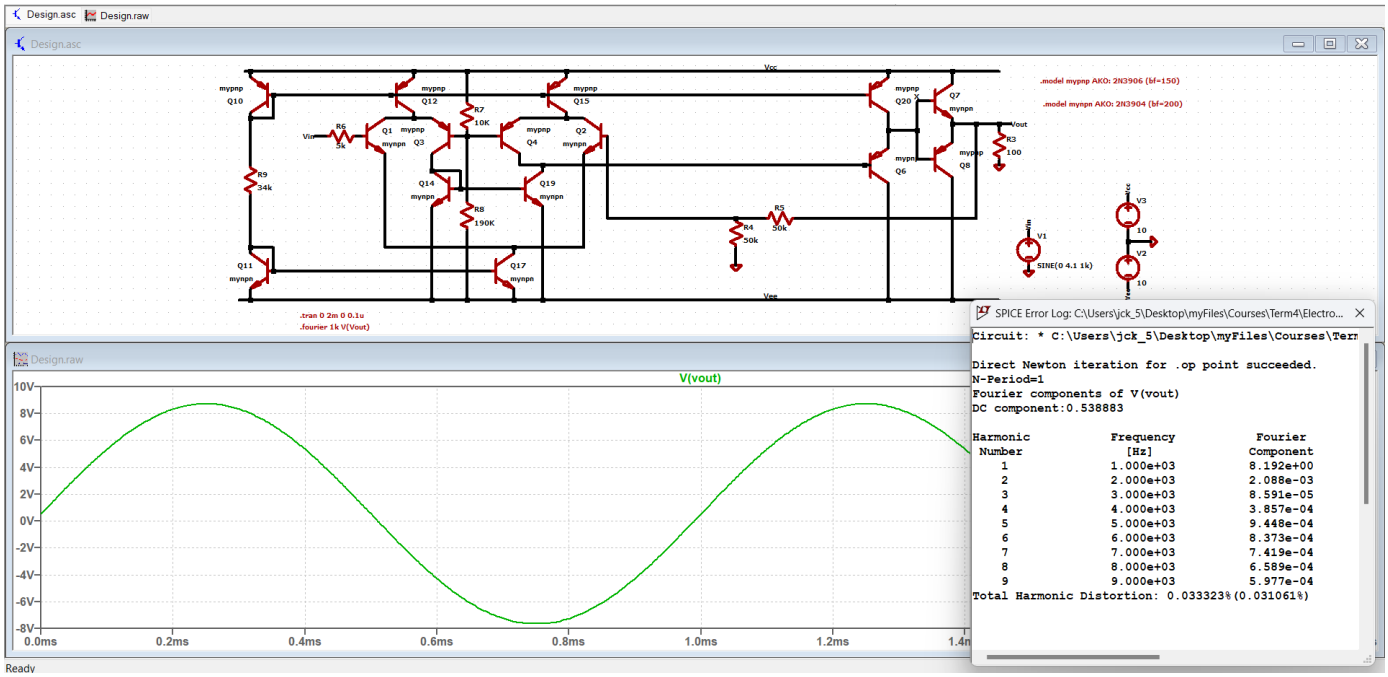

Figure 17: the THD with 50k feedback resistors

VI. explaining the reason 50k feedback resistor creates Distrotion

because with 10k resistors the open loop resistance seen from Q1 and Q2 were the same the differential stage was very symmetrical. by changing to 50k the base resistance of Q2 is now 25k instead of 5k, this makes the differential stage a little bit asymmetric and creates a little amount of distortion.