Electronics 2 Project(part 1) Report

Instructor: Dr. Medi

Sharif University of Technology

LM741 Operational Amplifier first stage analysis

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1 Introduction

1.1 Adder and Subtractor

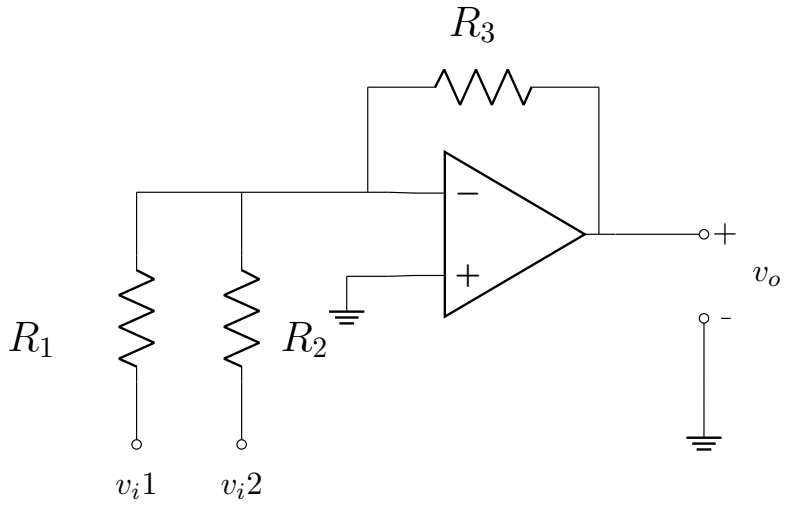

Figure 1: Adder circuit using Op-Amp

by writing KCL at the inverting node of the amplifier we get:

$$v_o = -\frac{R_3}{R_1}v_1 - \frac{R_3}{R_2}v_2$$

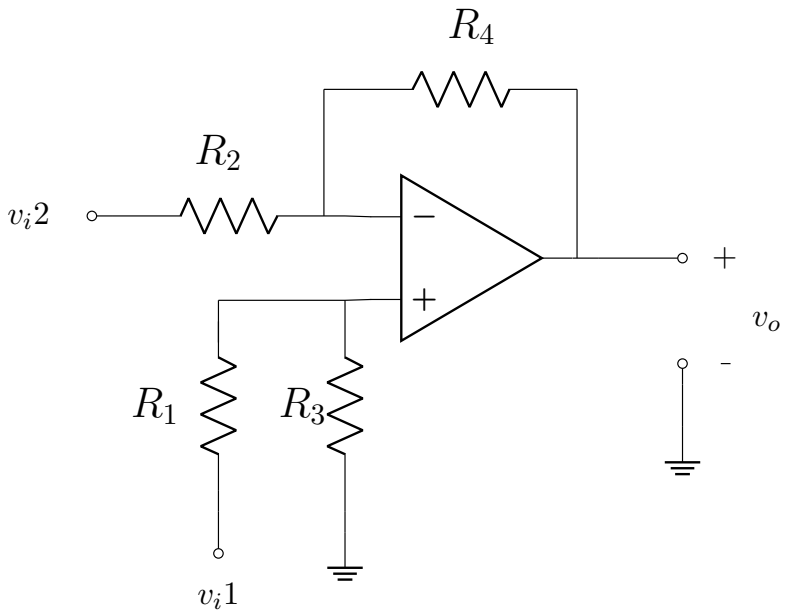

Figure 2: Subtractor circuit using Op-Amp

again by writing KCL at the inverting node of the amplifier and also knowing that the inverting and non-inverting node of the amplifier have the same voltage we get:

$$v_o = \frac{R_3}{R_4(R_1 + R_3)}v_1 - \frac{R_4}{R_2}v_2$$

1.2 Log of a signal

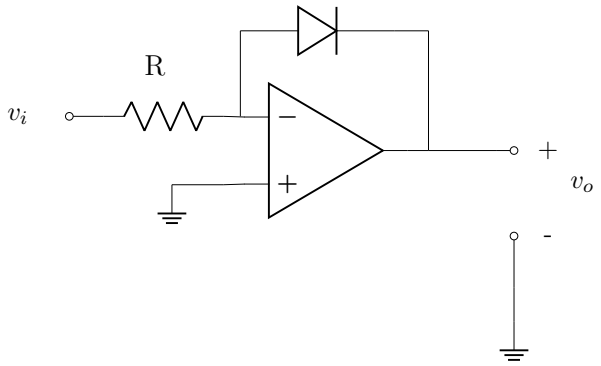

Figure 3: Signal log calculator circuit using Op-Amp

$$i_D = \frac{v_i}{R}$$

$$v_o = -v_T ln(\frac{v_i}{RI_s})$$

1.3 square and triangle wave generator

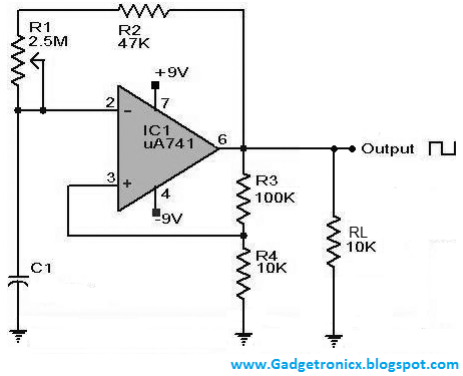

Figure 4: square wave generator using op-amp

Let us assume the voltage at inverting terminal be V2 which equals to the voltage across the capacitor. Also, let us assume the voltage at the non-inverting terminal be V1. The voltage difference between non-inverting and inverting terminal is referred to as differential input voltage and is given by Vin.
At the initial state when the capacitor is fully discharged, the voltage at inverting pin will be zero, i.e. V2 = 0V
Therefore, input differential voltage (Vin) = V1-V2 = V1-0 = V1
When Vin is positive the output is also positive, at this instance, the capacitor starts to charge through resistor R2 towards positive saturation voltage until V1 = V2.
When the voltage at the capacitor increases slightly more than the differential voltage V1.
Negative Vin = V1-V2 (V2 > V1)
Then the output will be switched from positive saturation voltage to negative saturation voltage. In this instance, the capacitor starts to discharge through resistor R2 because V2 becomes greater than Vout. Again, after reaching V2 slightly less than V1 the output will again switch to positive saturation voltage.

This process repeats again and again as a result square wave is generated.

we can easily combine this circuit with an integrator to get a triangular circuit like below figure:

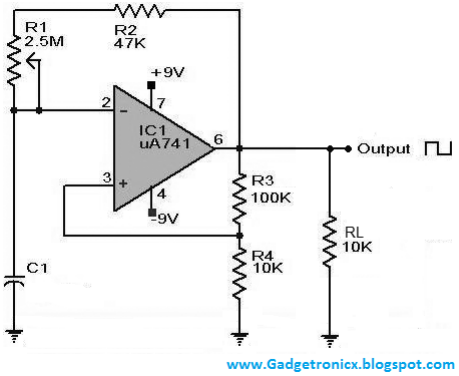

Figure 5: square wave generator using op-amp

1.4 square and triangle wave generator

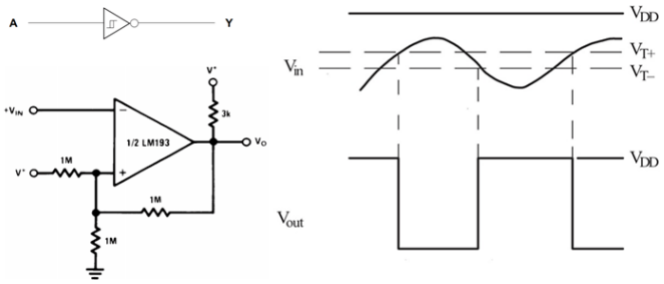

Figure 6: shmitt trigger using op-amp

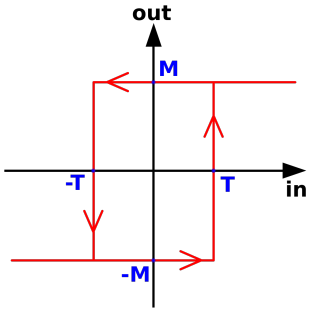

Figure 7: shmitt trigger characterisitc

shmitt trigger uses feedback to compare our input to some voltage $\pm V$ and drop to $-V_{cc}$ when our voltage gets more than V and get to $-V_{cc}$ when the voltage gets less than -V. this circuit has a hysteresis characterisitc.

2 LM741 IC characterisitcs

a)

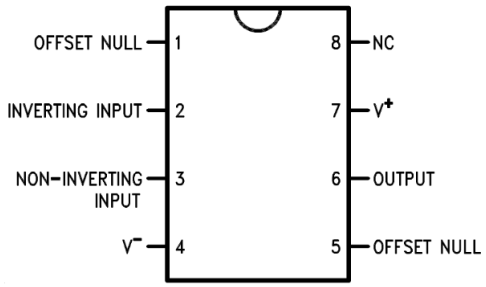

Figure 8: the LM741 IC ports

as it can be seen in the Figure above ports 2 and 3 are the non-inverting and inverting input ports. port 7 and 4 are the ports that we connect Vcc and Vee. and port 6 is the output port. also ports 1 and 5 are for offset null by wich we remove the output unwanted DC value.

b)

this op-amp works with supply voltage $\pm 22V$ and also can get differential input voltage up to $\pm 30V$.
it also uses $60mW$ to $150mW$ of power depending on the amplifier type and can work in temperatures of $-55°C$ to $125°C$

c)

the large signal voltage gain can vary betwenn 20,000 and 200,000. and the input current drift is about 0.5 nA. the input resistance can vary between 300kΩ to 6MΩ in different models and different bias points. the CMRR can vary between 70dB to 95dB.
the circuit can swing $\pm 16V$ and the typical power consumption is about $100mW$.

3 Designing an amplifier circuit

3.1 analyze the different parts of this circuit

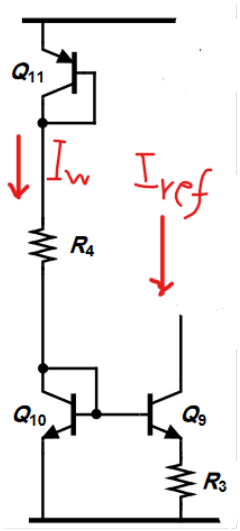

Figure 9: the widlar part of the circuit

we can see that this part of the circuit is a Widlar current source. we derive I_w and I_{ref} here to use them later in synthesis section:

$$I_w = \frac{28.6}{R_4}$$

$$I_{ref} R_3 = v_T ln(\frac{I_w}{I_{ref}})$$

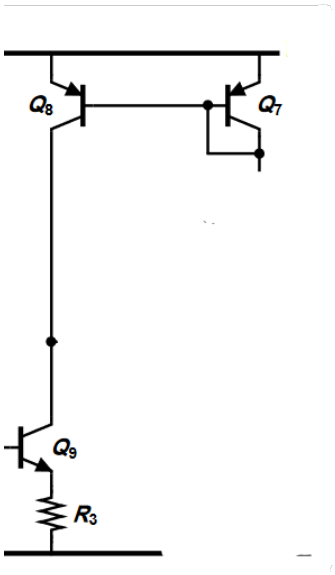

Figure 10: the current mirror for copying I_{ref}

this part only copies I_{ref} to our amplifying section.

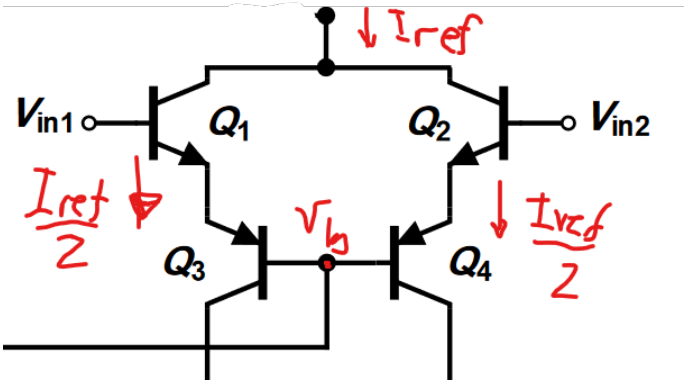

Figure 11: signal input part of the amplifier

first we should point that Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 all have the same $I_C = \frac{I_{ref}}{2}$ so they all have the same g_m and r_e.

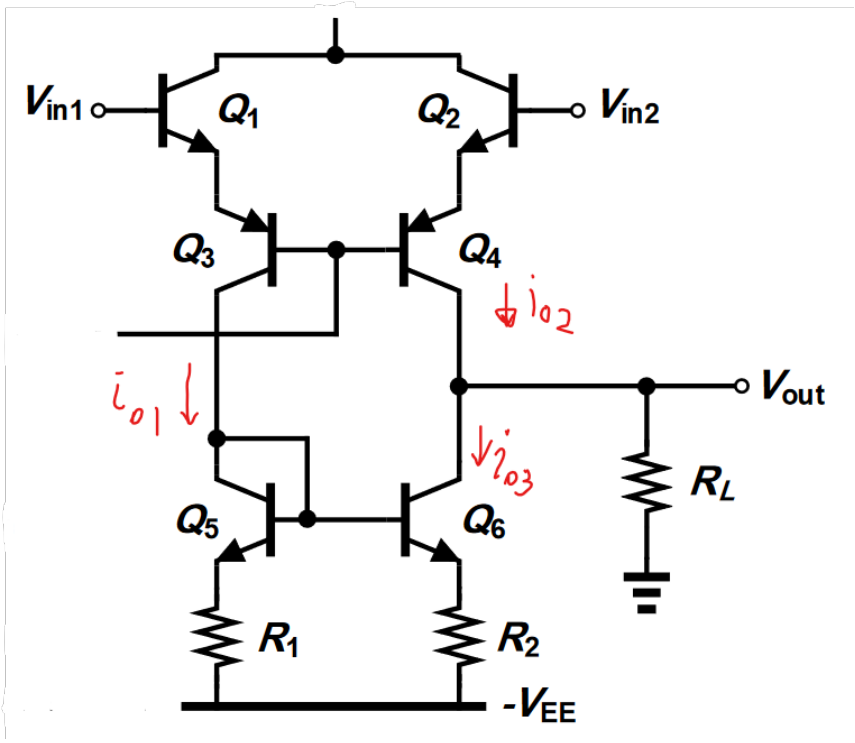

Figure 12: the currents marked on this circuits will be used for calculating the gain

we now start the small signal analysis of now assuming that the input is differential we can consider v_b as GND in small signal.
we can then use the t model for transistors to anlyze this parts half circuits:

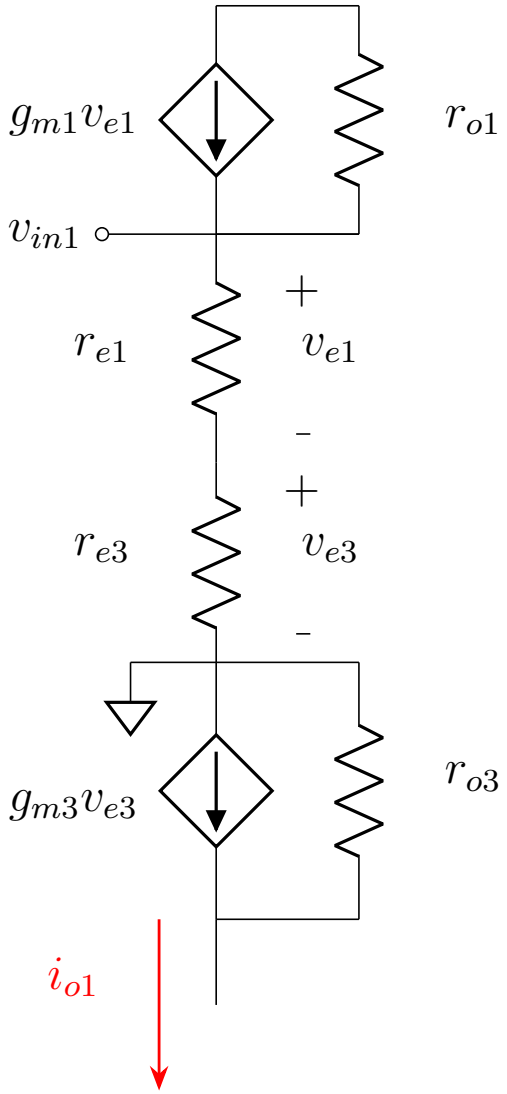

Figure 13: Small signal model of Q_1 and Q_3(same as Q_2 and Q_4 due to symmetry)

*[firstly pay attention that we are going to calculate G_m for this circuit and then multiply it by R_L so remember in all of the steps below the output is assumed short circuit(meaning $R_L = 0$)]

in the above figure we can see:

$$v_{e3} = \frac{r_{e3}}{r_{e3} + r_{e1}} v_{in1} = \frac{1}{2} v_{in}$$

assuming the resistance in i_{o1} being sufficiently small (it can be achieved by choosing an R_1 smaller than r_{o3}) we can say that:

$$i_{o1} = \frac{1}{2} g_{m3} v_{in1}$$

because the output is shorted we can also write:

$$i_{o2} = \frac{1}{2} g_{m4} v_{in2} = -\frac{1}{2} g_{m4} v_{in1}$$

also we can easily see that the input impedance is:

$$R_{in} = 2\beta_n(r_{e1} + r_{e3}) = 4\beta_n(r_{e1}) = 8\beta_n \frac{v_T}{I_{ref}}$$

now Q_5 and Q_6 form a current mirror for copying i_{o1} into i_{o3} their small signal form is:

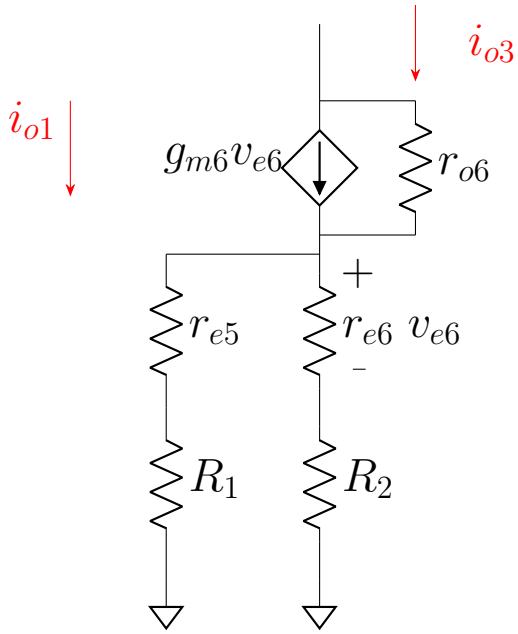

Figure 14: Small signal model of Q_5 and Q_6 currnet mirror

first because output is shorted all of $g_{m6}v_{e6}$ goes to i_{o3}. now we calculate i_{o3}:

$$v_{e6} = i_{o1}\frac{r_{e6}(r_{e5}+R_1)}{r_{e6}+R_2}$$

$$i_{o3} = i_{o1}\frac{r_{e5}+R_1}{r_{e6}+R_2} = \frac{1}{2}g_{m3}\frac{(r_{e5}+R_1)}{r_{e5}+R_2}v_{in1}$$

now we calculate i_{out}:

$$i_{out} = i_{o2} - i_{o3} = -\frac{1}{2}g_{m4}v_{in1} - \frac{1}{2}g_{m3}\frac{(r_{e5}+R_1)}{r_{e5}+R_2}v_{in1}$$

knowing all g_m and r_e are equal:

$$G_m = \frac{i_{out}}{2v_{in1}} = -\frac{1}{4}g_m\frac{2r_e+R_1+R_2}{r_e+R_2}$$

we then calculate the output impedance:

$$R_{out} = ((1+g_m r_{o4})(r_e||r_{\pi 4}))||((1+g_m r_{o6})(R_2||r_{\pi 4})) \simeq (g_m r_{o4} r_e)||(g_m r_{o6}(R_2||r_{\pi 4}))$$

then the final gain is:

$$A_v = G_m(R_L||R_{out}) = -\frac{1}{4}g_m\frac{2r_e+R_1+R_2}{r_e+R_2}(R_L||R_{out})$$

if we set $R_1 = R_2$ we get:

$$A_v = -\frac{1}{2}g_m(R_L||R_{out})$$

and setting $R_1 = R_2$ will increase our common mode rejection but we may or may not do that based on application. we in particular choose to set them equal.

3.2 choosing theoritical values for the amplifier

the input impedance as calculated before is:

$$R_{in} = 8\beta_n \frac{v_T}{I_{ref}} > 2M\Omega \rightarrow I_{ref} < 20\mu A$$

then bounding the gain we have:

$$A_v = -\frac{1}{2} g_m (R_L || R_{out}) \simeq -\frac{1}{4} \frac{I_{ref}}{v_T} R_L > 316 \rightarrow I_{ref} > 31.6\mu A$$

we can see that there is no I_{ref} fitting both conditions thus we choose the I_{ref} giving maximum gain with resistance of $2M\Omega$ meaning $I_{ref} = 20\mu A$ wich gives $A_v = 200$.

now we find the widlar current in way not to consume more than $400mW$:

$$I_w = \frac{28.6}{R_4}$$

$$I_{ref} R_3 = v_T ln(\frac{I_w}{I_{ref}}) \rightarrow R_3 = 3k\Omega I_w = 0.2mA$$

we had freedom in choosing I_w and R_3 but we chose according to maximum power and also not using very high resistances. now for $I_w = 0.2mA$ we should set $R_4 = 143k\Omega$. the choice for R_1 and R_2 pretty much doesn't limit anything so we choose 1.5kΩ for them being near the datasheet.

3.3 Operating point simulation

Transistor	Ic	g_m	r_π	V_{CE}	r_o
Q1	12.75µ	510µ	392.16k	15V	15.69M
Q2	12.75µ	510µ	392.16k	15V	15.69M
Q3	-12.75µ	510µ	196.08k	13.8V	3.92M
Q4	-12.75µ	510µ	196.08k	1.1V	3.92M
Q5	12.56µ	502.4	398.09k	601mV	15.92M
Q6	13.5µ	540µ	370.37k	13.3V	14.81M
Q7	-24µ	960µ	104.17k	590mV	2.08M
Q8	-31.3µ	1.25m	79.87k	16.2V	1.6M
Q9	31.2µ	1.25m	160.26k	13.8V	6.41M
Q10	180µ	7.2m	27.78k	671mV	1.11M
Q11	-180µ	7.2m	13.89k	642.5mV	277.78k

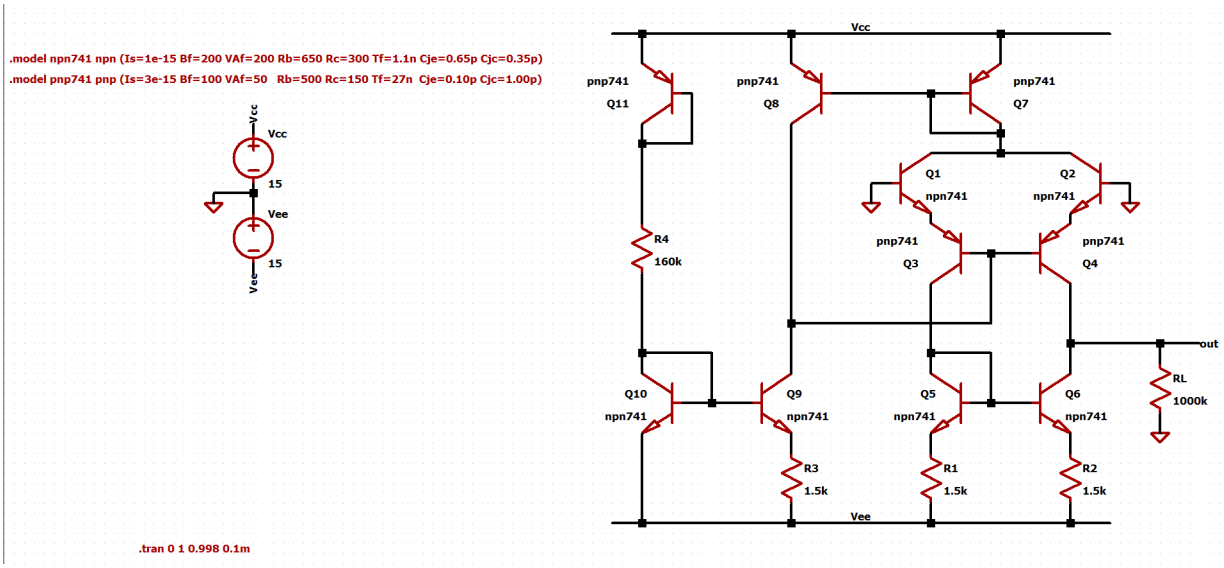

Figure 15: the DC circuit in ltspice

3.4 AC analysis simulation

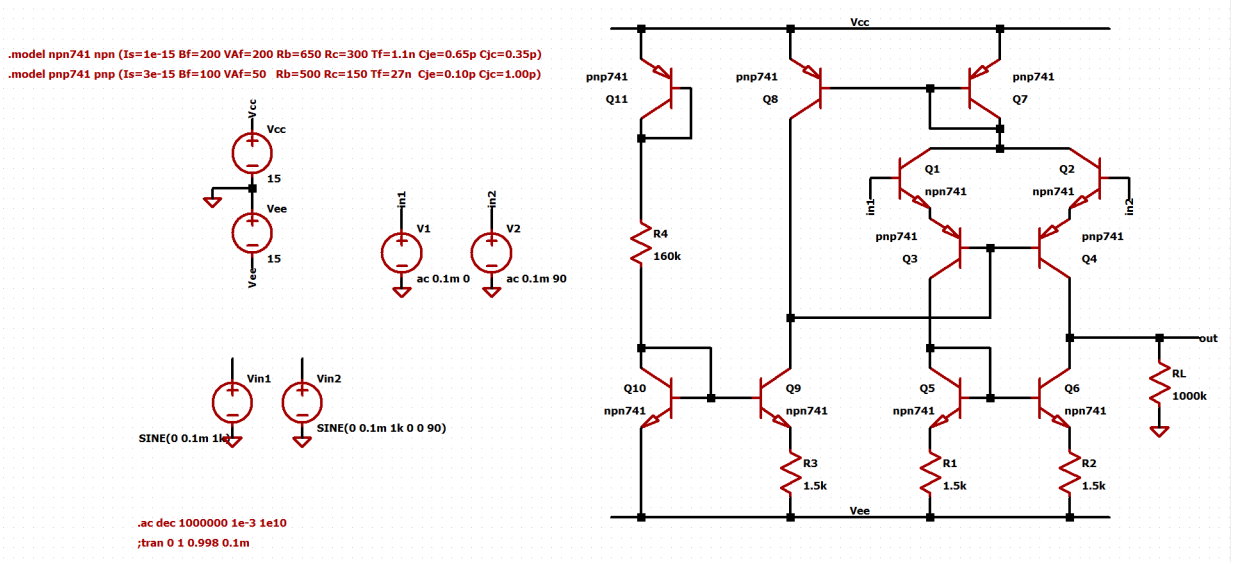

Figure 16: the AC circuit in ltspice

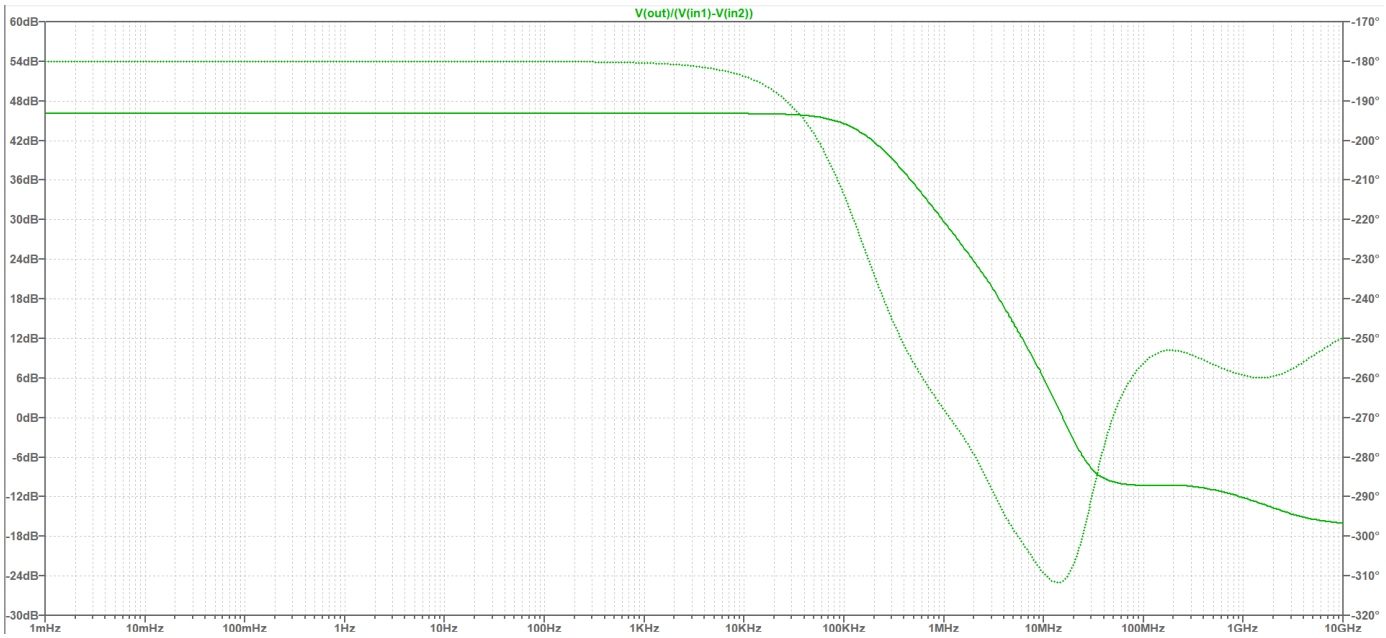

Figure 17: gain in different frequencies

a) the gain was 46.02dB (200) in theory and is about 46dB also in simulation.(though we made small changes in widlar part in simulation due to errors)
b) gain also drops below 3dB at 12.6MHz.
c) unity gain bandwidth is at 15.6MHz.
d)

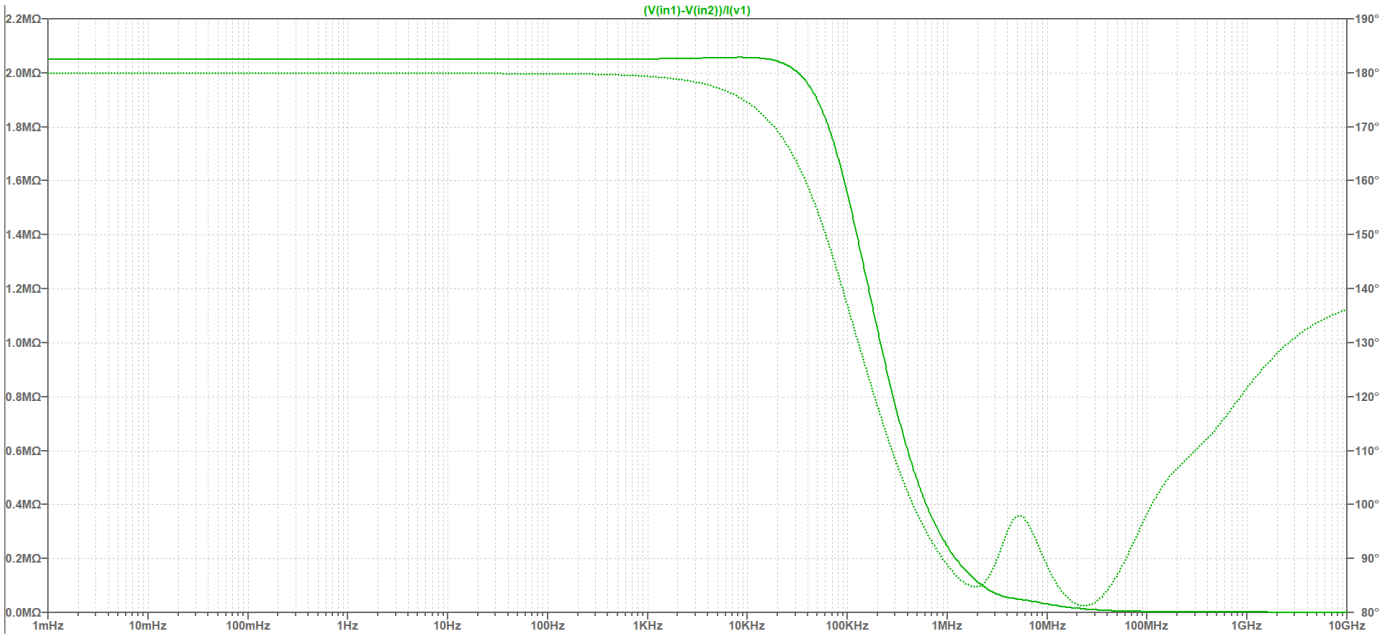

Figure 18: input resistance in different frequencies

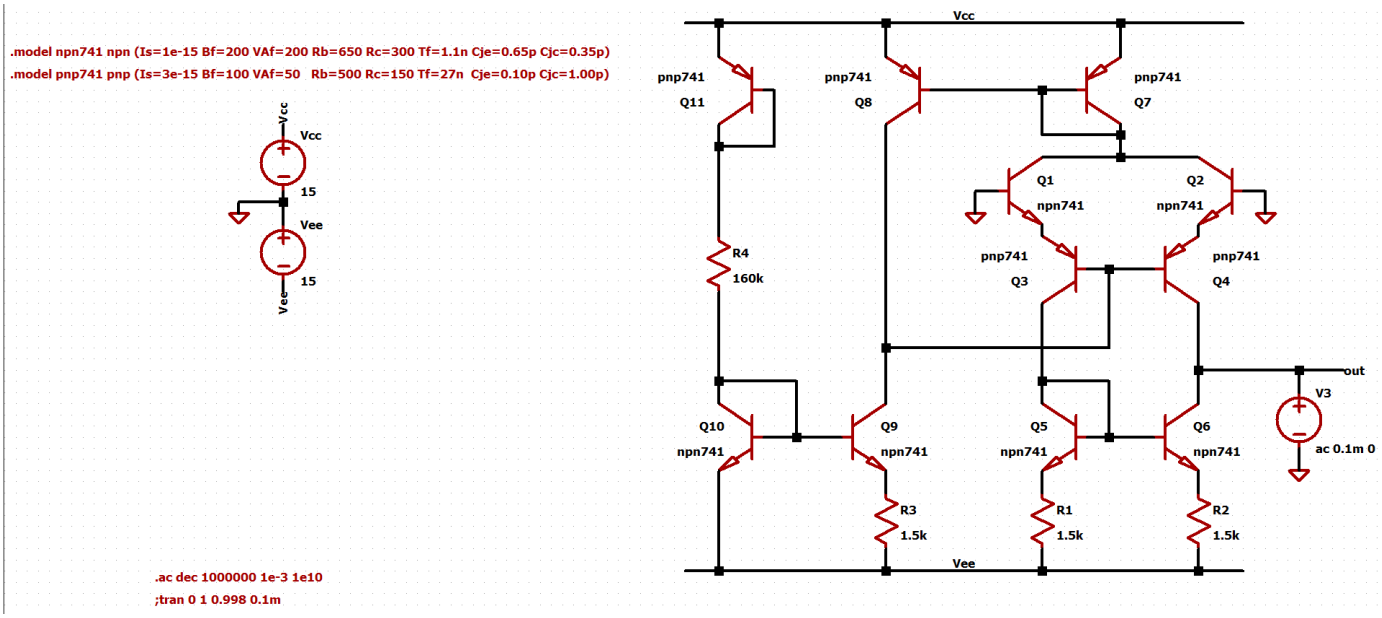

Figure 19: the circuit for seeing output resistance($R_L = \infty$ because it shouldn't be seen in output resistance)

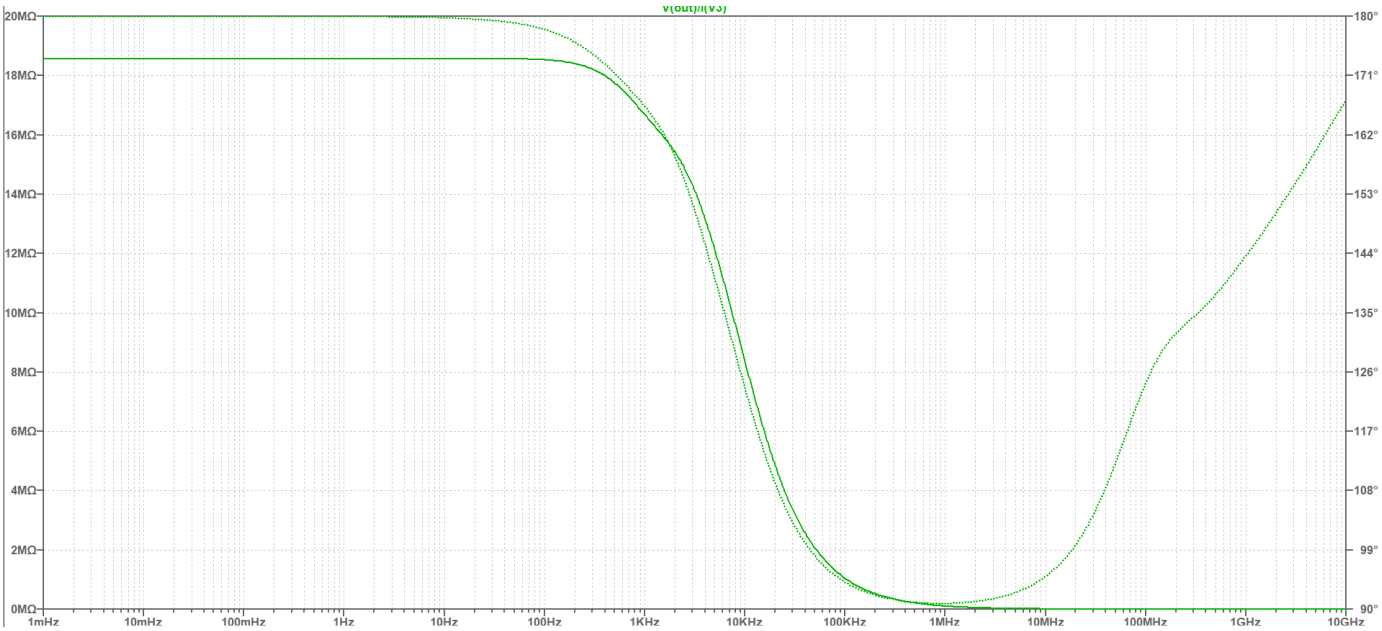

Figure 20: output resistance in different frequencies

we can see that: $R_{in} = 2.1M\Omega$ and $R_{out} = 18.6M\Omega$

e) we again do all the above steps:

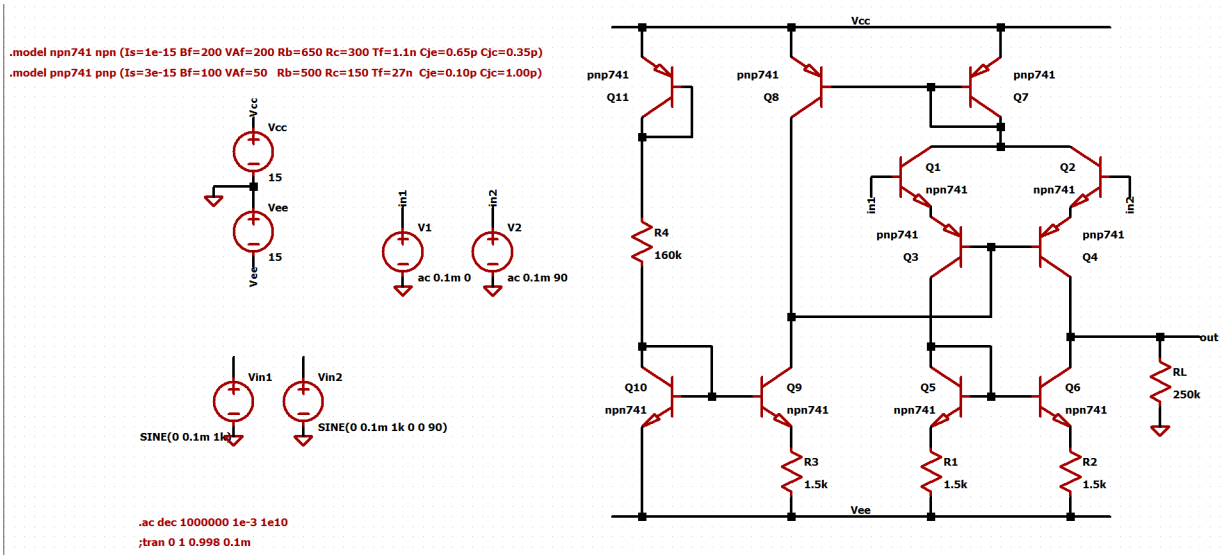

Figure 21: the AC circuit in ltspice(250k)

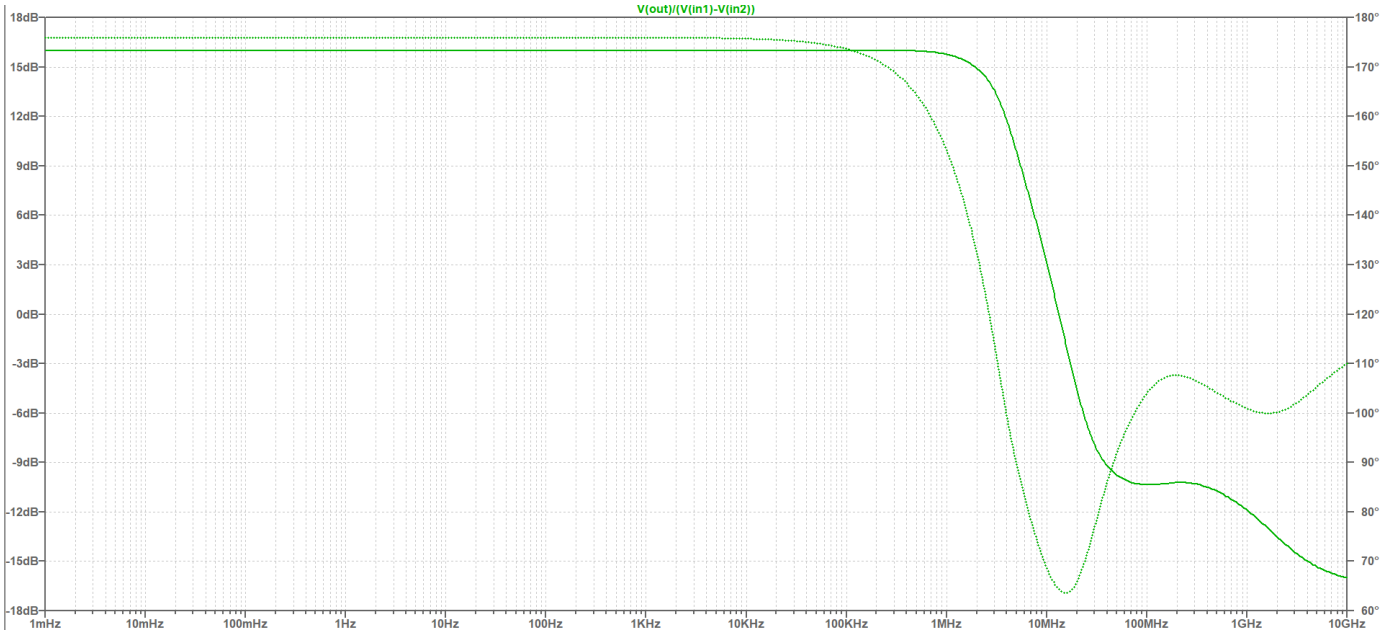

Figure 22: gain in different frequencies(250k)

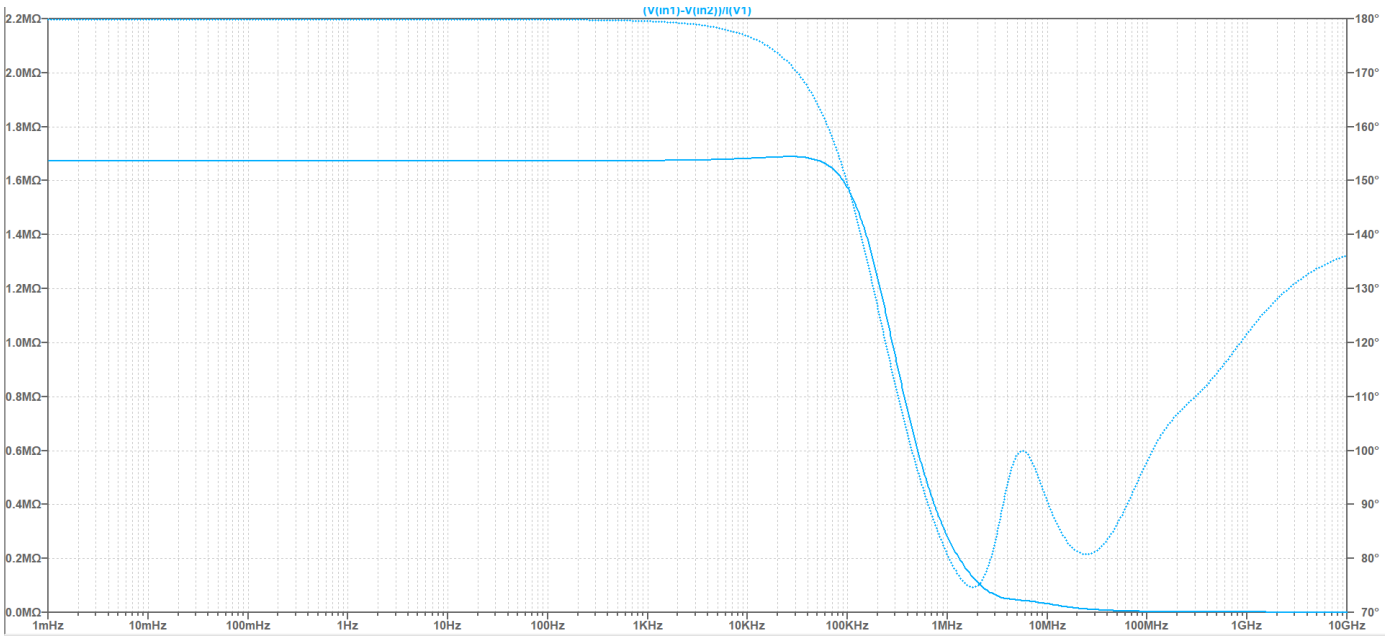

Figure 23: input resistance in different frequencies(250k)

the gain is about 16dB.
the 3dB gain is at 10MHz.
the 0dB gain is 13.3MHz.
the input impedance is at 1.7MΩ.
the output impedance is the same always regardless of the load so it is again 18.6MΩ.

3.5 testing the circuit at 1kHz frequency

a)

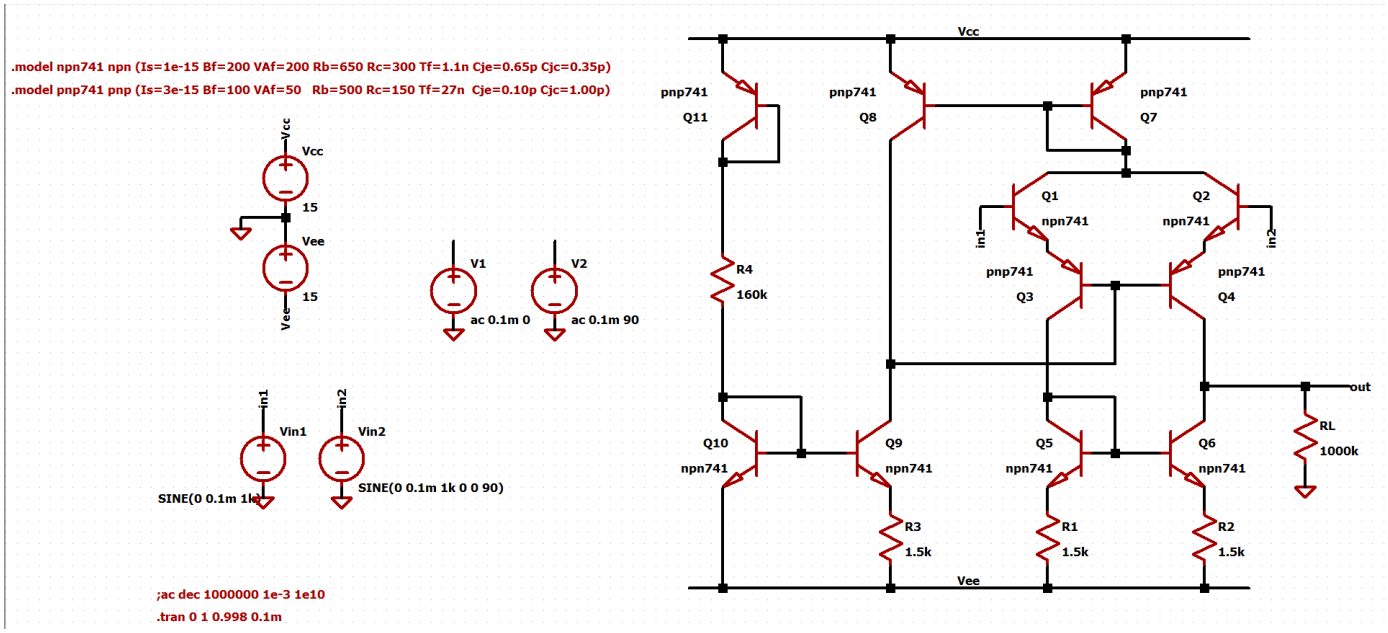

Figure 24: the circuit in 1k transient

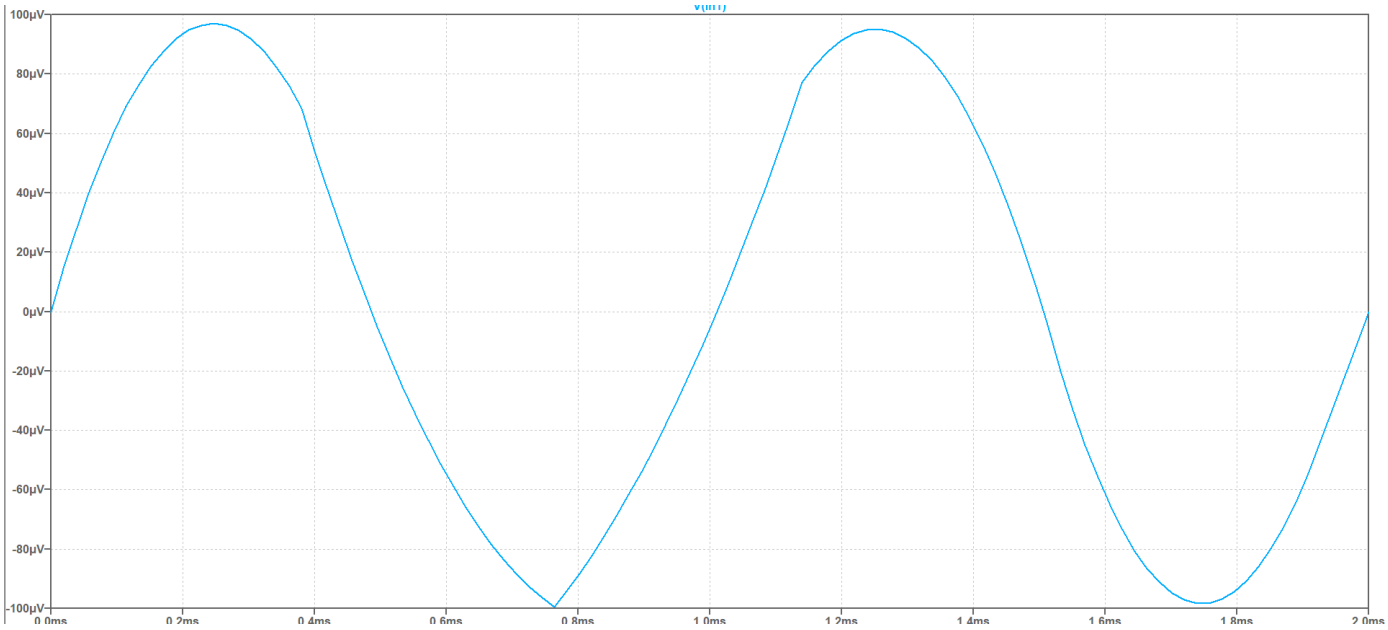

Figure 25: the input(0.1m v_{in1} with 1k frequency)

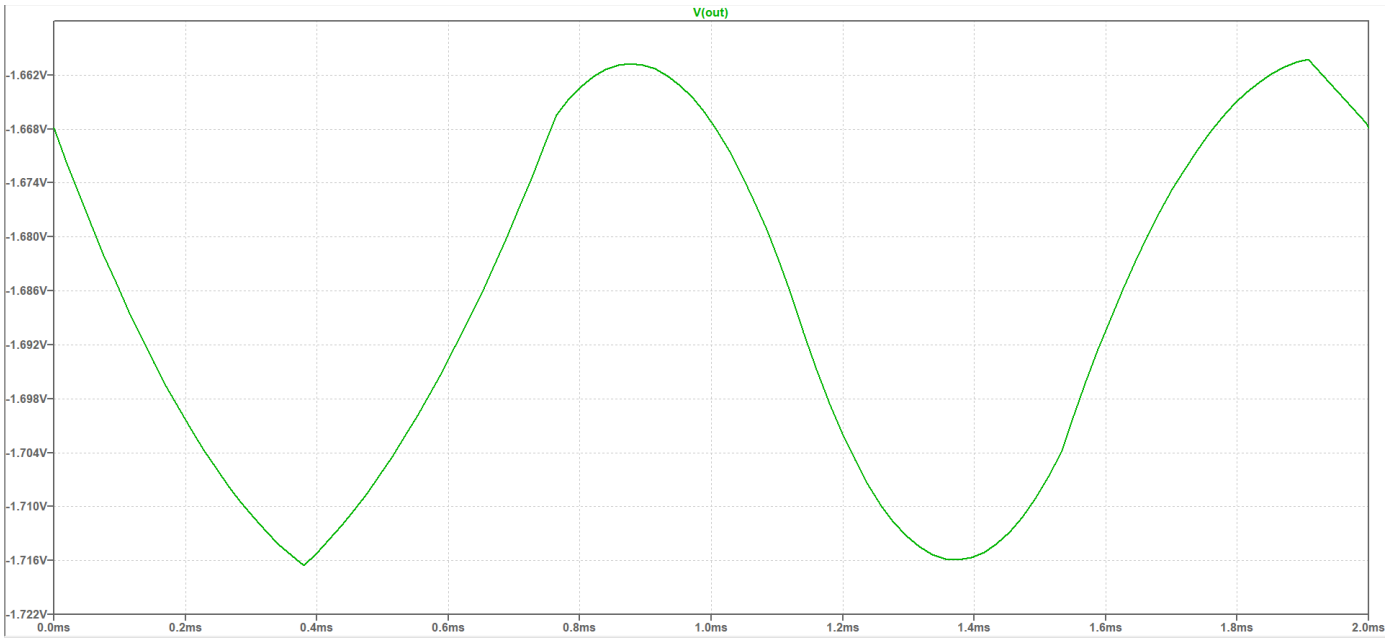

Figure 26: the output to the input with 0.2mV amplitude

it can be seen that the gain is 270 wich agrees with the AC analysis.

b) it can be seen from the figure below that the max swing is between 0 and -15V:

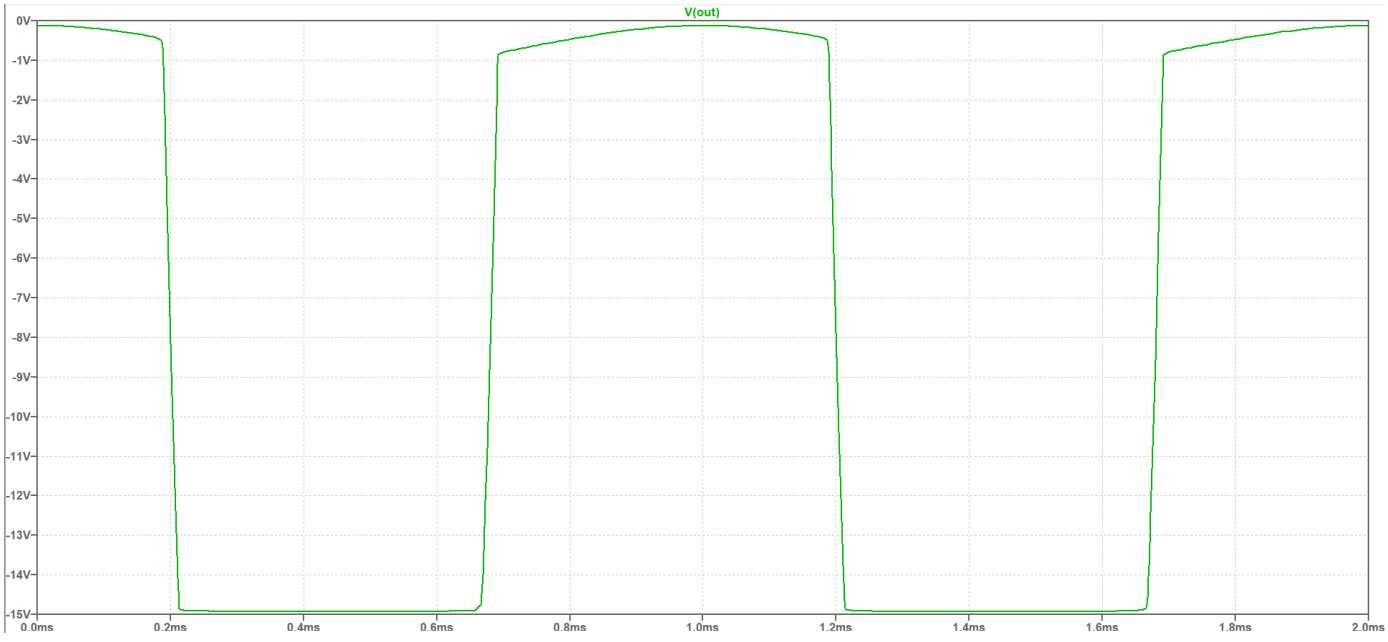

Figure 27: maximum swing of the circuit(given 500mV input)

c)

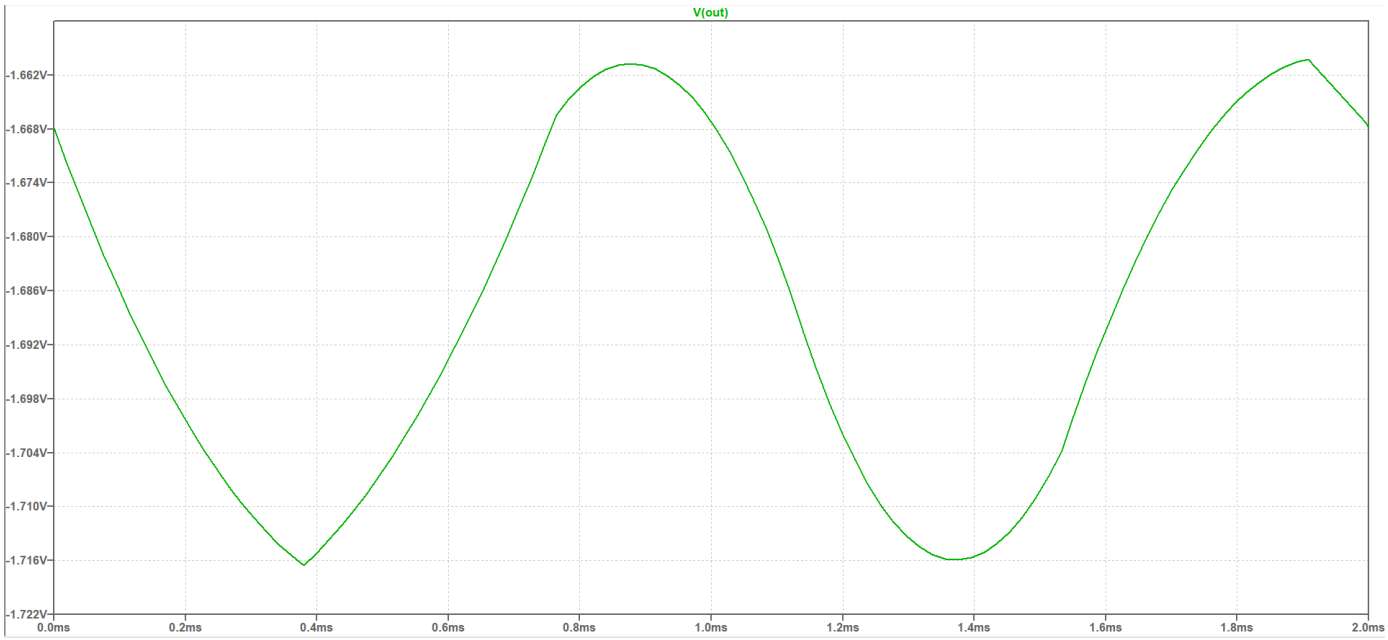

Figure 28: the output to the input with 0.2mV amplitude

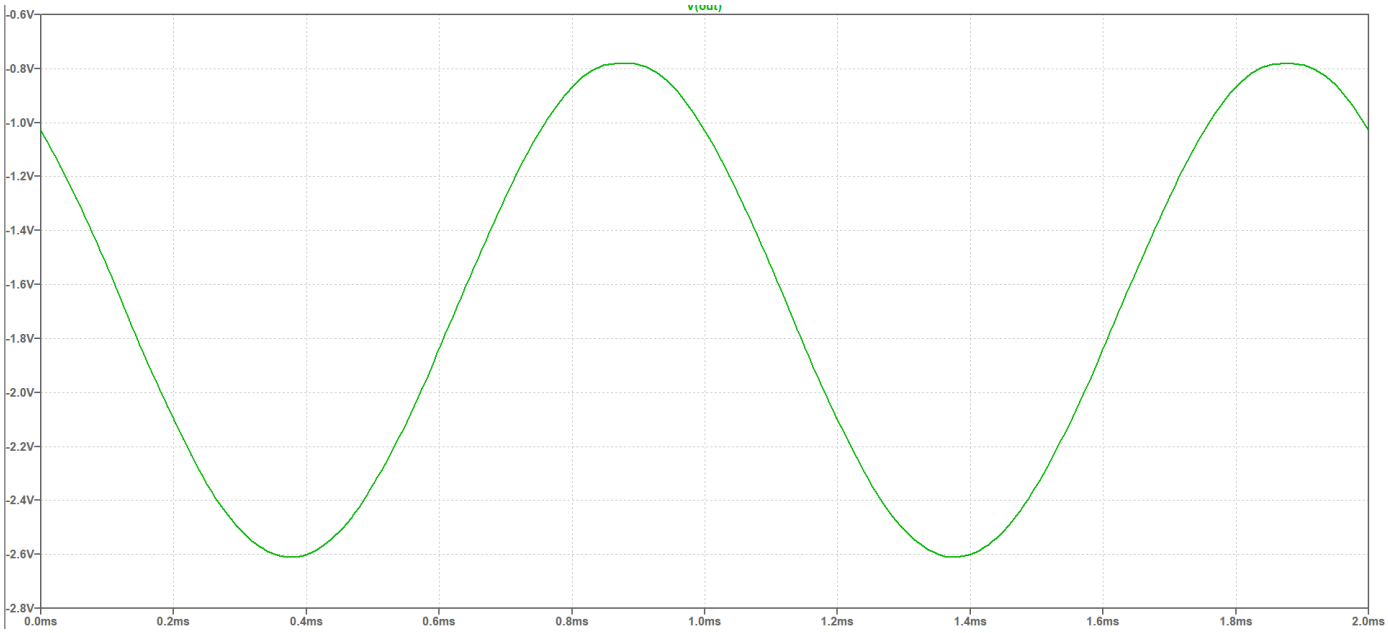

Figure 29: the output to the input with 6.5mV amplitude

d)

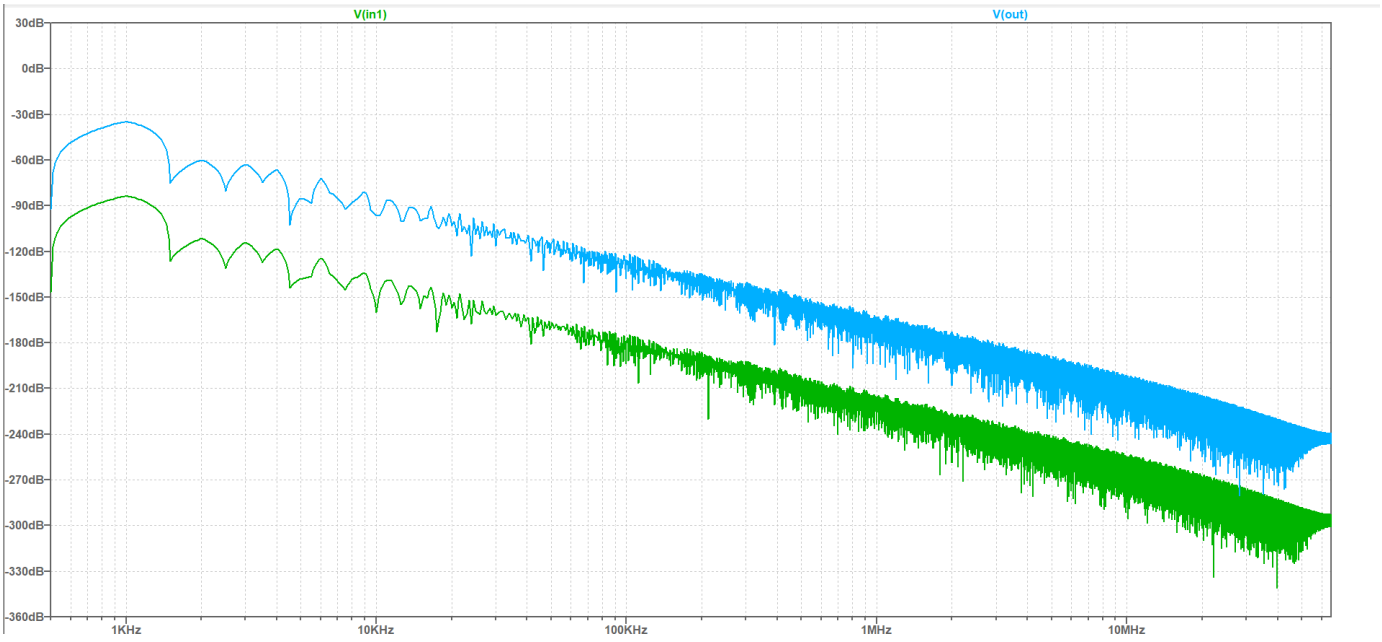

Figure 30: the more linear output fourier

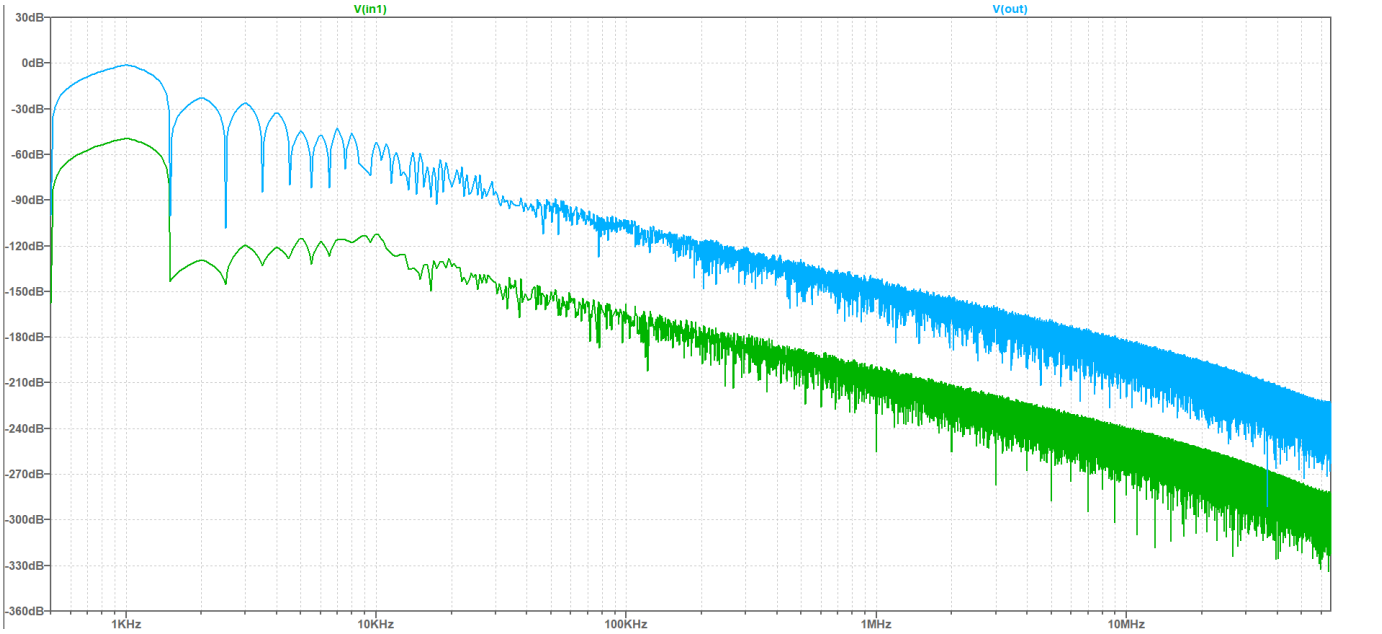

Figure 31: the less linear output fourier

but why the fourier transform changes:
becaue when the signal is small the transistor work more linear and the calculated slope is more accurate but as we make the signal larger more terms in the taylor series of transistor characterisitcs put effect on our signal and change it from the sine wave it was.