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In this project we aim to design and implement the MIPS processor using the pipeline concept.
Full datapath and controller unit has been explained in file **1)DPCU.pdf**

Wired datapath can be observed in figure 1

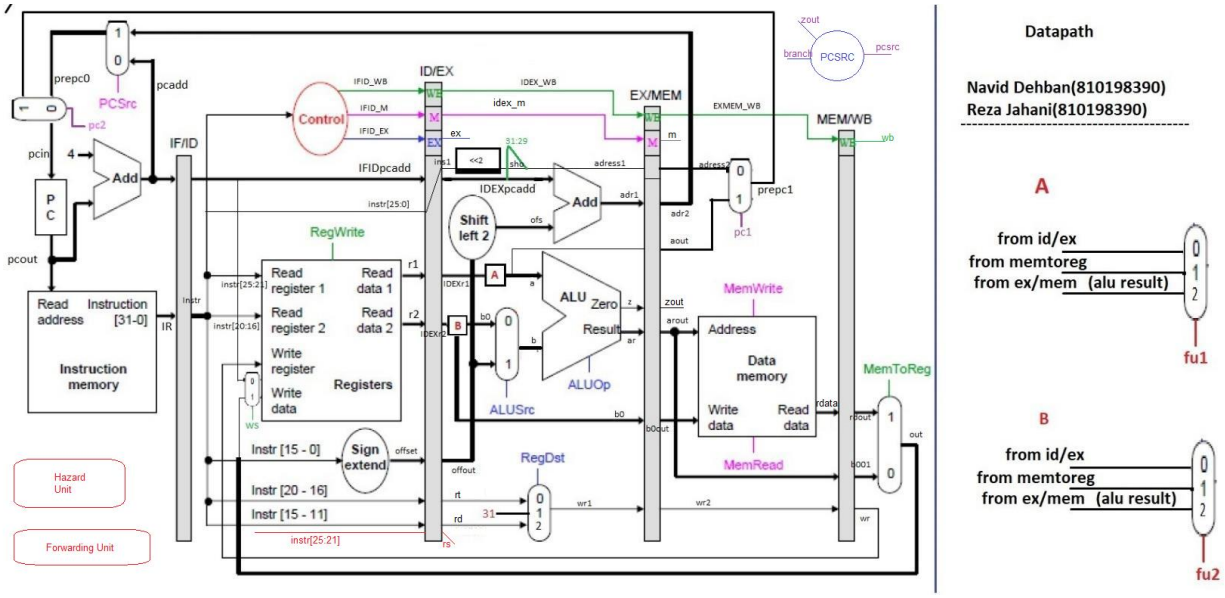

Figure 1: Wired Datapath

In this design we have 2 units detecting data hazards and they also deal with this problem.

Test case which has been used to check the functionality is brought below.

```
addi   R1,R0,1000    //R1=1000
addi   R2,R0,0       //R2=0 counter
LW     R3,R1(0)      //R3=arr[0] keeps the min
addi   R7,R0,0       //R7 index
addi   R4,R0,20      //R4=20
beq    R2,R4,L4        *loop* L3          @
LW     R5,R1(0)      //R5 keeps the min
slt    R6,R3,R5
beq    R6,R0,L2                           @
J      L1                                 @
add    R3,R5,R0    L2                     @
add    R7,R2,R0
addi   R1,R1,4     L1                     @
addi   R2,R2,1
J      L3                                 @
SW     R3,R0(2000)  *endloop*   L4
SW     R7,R0(2004)
```

Figure 2: Assembly Code

```
00000100000000010000001111101000
00000100000000100000000000000000
00001100001000110000000000000000
00000100000001110000000000000000
00000100000001000000000000010100
00010100010001000000000011000100
00001100001001010000000000000000
00000000011001010011000000010000
00010100110000000000000000100100
00011000000000000000000000111100
00000000101000000001100000000001
00000000010000000011100000000001
00000100001000010000000000000100
00000100010000100000000000000001
00011000000000000000000000011001
00010000000000110000011111010000
00010000000001110000011111010100
```

Figure 3: Machine Code

For testing this program we used an array which is

```
mem[1000]<=8;
mem[1004]<=2;
mem[1008]<=3;
mem[1012]<=4;
mem[1016]<=5;
mem[1020]<=6;
mem[1024]<=7;
mem[1028]<=20;
mem[1032]<=1;
mem[1036]<=9;
mem[1040]<=10;
mem[1044]<=11;
mem[1048]<=12;
mem[1052]<=13;
mem[1056]<=14;
mem[1060]<=15;
mem[1064]<=16;
mem[1068]<=17;
mem[1072]<=18;
mem[1076]<=19;
```

Figure 4: Array

As we can observe the minimum element is 1 in index 8. The exact result is gained from the processor written in address 2000 and 2004 in data memory and results can be observed in waveform presented in figure 5

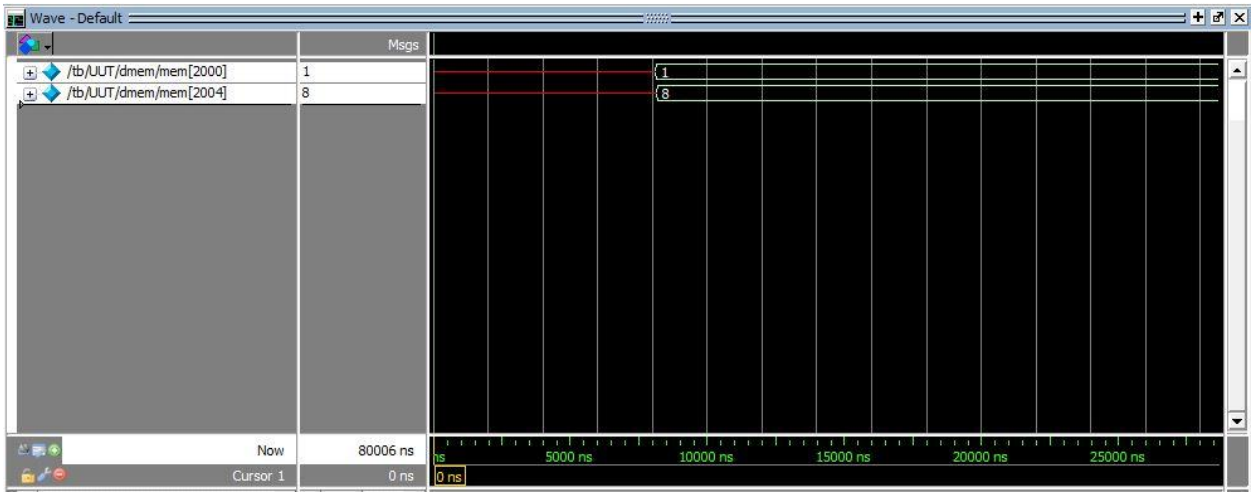

Figure 5: Waveform

- Datapath modules are written in **DP_MODULES.v**
- Controlling modules are written in **CU_MODULES.v**
- The Processing unit is written in **PU.v**