1. Run the code of 2-to 1 MUX (given in presentation, with if-else-if statement) on FPGA board.

2. Use **Behavioral Modeling** (if-else statement) and write the code of 2-to-1 MUX
3. Write the testbench
4. Simulate the testbench and make the analyze of timing diagram, then run the code on FPGA board

5. Run the code of 2-to 4 decoder (given in presentation, with case statement) on FPGA board. –

6. Use **Behavioral Modeling** (if-else statement) and write the code of 2-to-4 decoder (Decoder has 2-bit inputs and 4-bits output) and 8-to-3 encoder (Encoder has 8-bits input and 3-bits output).

7. Write the testbench
8. Simulate the testbench and make the analyze of timing diagram, them run the code on FPGA board