Table 44-2. Standard Instruction Set

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED FILE REGISTER INSTRUCTIONS									
ADDWF	f, d, a	Add WREG and f	1	0010	01da	ffff	ffff	C, DC, Z, OV, N	1
ADDWFC	f, d, a	Add WREG and Carry bit to f	1	0010	00da	ffff	ffff	C, DC, Z, OV, N	1
ANDWF	f, d, a	AND WREG with f	1	0001	01da	ffff	ffff	Z, N	1
CLRF	f, a	Clear f	1	0110	101a	ffff	ffff	Z	
COMF	f, d, a	Complement f	1	0001	11da	ffff	ffff	Z, N	1
DECF	f, d, a	Decrement f	1	0000	01da	ffff	ffff	C, DC, Z, OV, N	1
INCF	f, d, a	Increment f	1	0010	10da	ffff	ffff	C, DC, Z, OV, N	1
IORWF	f, d, a	Inclusive OR WREG with f	1	0001	00da	ffff	ffff	Z, N	1
MOVF	f, d, a	Move f to WREG or f	1	0101	00da	ffff	ffff	Z, N	1
MOVFF	f_s, f_d	Move f_s (12-bit source) to f_d (12-bit destination)	2	1100	$f_sf_sf_sf_s$	$f_sf_sf_sf_s$	$f_sf_sf_sf_s$	None	1, 3, 4
				1111	$f_df_df_df_d$	$f_df_df_df_d$	$f_df_df_df_d$		
MOVFFL	f_s, f_d	Move f_s (14-bit source) to f_d (14-bit destination)	3	0000	0000	0110	$f_sf_sf_sf_s$	None	1, 3
				1111	$f_sf_sf_sf_s$	$f_sf_sf_sf_s$	$f_sf_sf_df_d$		
				1111	$f_df_df_df_d$	$f_df_df_df_d$	$f_df_df_df_d$		
MOVWF	f, a	Move WREG to f	1	0110	111a	ffff	ffff	None	
MULWF	f, a	Multiply WREG with f	1	0000	001a	ffff	ffff	None	1
NEGF	f, a	Negate f	1	0110	110a	ffff	ffff	C, DC, Z, OV, N	1
RLCF	f, d, a	Rotate Left f through Carry	1	0011	01da	ffff	ffff	C, Z, N	1
RLNCF	f, d, a	Rotate Left f (No Carry)	1	0100	01da	ffff	ffff	Z, N	1
RRCF	f, d, a	Rotate Right f through Carry	1	0011	00da	ffff	ffff	C, Z, N	1
RRNCF	f, d, a	Rotate Right f (No Carry)	1	0100	00da	ffff	ffff	Z, N	1
SETF	f, a	Set f	1	0110	100a	ffff	ffff	None	

© 2019-2021 Microchip Technology Inc. and its subsidiaries

.....continued

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
				MSb			LSb		
SUBFWB	f, d, a	Subtract f from WREG with Borrow	1	0101	01da	ffff	ffff	C, DC, Z, OV, N	1
SUBWF	f, d, a	Subtract WREG from f	1	0101	11da	ffff	ffff	C, DC, Z, OV, N	1
SUBWFB	f, d, a	Subtract WREG from f with Borrow	1	0101	10da	ffff	ffff	C, DC, Z, OV, N	1
SWAPF	f, d, a	Swap nibbles in f	1	0011	10da	ffff	ffff	None	1
XORWF	f, d, a	Exclusive OR WREG with f	1	0001	10da	ffff	ffff	Z, N	1
BYTE-ORIENTED SKIP INSTRUCTIONS									
CPFSEQ	f, a	Compare f with WREG, skip if =	1 – 4	0110	001a	ffff	ffff	None	1, 2
CPFSGT	f, a	Compare f with WREG, skip if >	1 – 4	0110	010a	ffff	ffff	None	1, 2
CPFSLT	f, a	Compare f with WREG, skip if <	1 – 4	0110	000a	ffff	ffff	None	1, 2
DECFSZ	f, d, a	Decrement f, Skip if 0	1 – 4	0010	11da	ffff	ffff	None	1, 2
DCFSNZ	f, d, a	Decrement f, Skip if Not 0	1 – 4	0100	11da	ffff	ffff	None	1, 2
INCFSZ	f, d, a	Increment f, Skip if 0	1 – 4	0011	11da	ffff	ffff	None	1, 2
INFSNZ	f, d, a	Increment f, Skip if Not 0	1 – 4	0100	10da	ffff	ffff	None	1, 2
TSTFSZ	f, a	Test f, skip if 0	1 – 4	0110	011a	ffff	ffff	None	1, 2
BIT-ORIENTED FILE REGISTER INSTRUCTIONS									
BCF	f, b, a	Bit Clear f	1	1001	bbba	ffff	ffff	None	1
BSF	f, b, a	Bit Set f	1	1000	bbba	ffff	ffff	None	1
BTG	f, b, a	Bit Toggle f	1	0111	bbba	ffff	ffff	None	1
BIT-ORIENTED SKIP INSTRUCTIONS									
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 – 4	1011	bbba	ffff	ffff	None	1, 2

© 2019-2021 Microchip Technology Inc. and its subsidiaries

.....continued

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
				MSb			LSb		
BTFSS	f, b, a	Bit Test f, Skip if Set	1 – 4	1010	bbba	ffff	ffff	None	1, 2
CONTROL INSTRUCTIONS									
BC	n	Branch if Carry	1 – 2	1110	0010	nnnn	nnnn	None	2
BN	n	Branch if Negative	1 – 2	1110	0110	nnnn	nnnn	None	2
BNC	n	Branch if Not Carry	1 – 2	1110	0011	nnnn	nnnn	None	2
BNN	n	Branch if Not Negative	1 – 2	1110	0111	nnnn	nnnn	None	2
BNOV	n	Branch if Not Overflow	1 – 2	1110	0101	nnnn	nnnn	None	2
BNZ	n	Branch if Not Zero	1 – 2	1110	0001	nnnn	nnnn	None	2
BOV	n	Branch if Overflow	1 – 2	1110	0100	nnnn	nnnn	None	2
BRA	n	Branch Unconditionally	2	1101	0nnn	nnnn	nnnn	None	2
BZ	n	Branch if Zero	1 – 2	1110	0000	nnnn	nnnn	None	2
CALL	k, s	Call subroutine	2	1110	110s	kkkk	kkkk	None	2, 3
				1111	kkkk	kkkk	kkkk		
CALLW	—	Call subroutine using WREG	2	0000	0000	0001	0100	None	2
GOTO	k	Go to address	2	1110	1111	kkkk	kkkk	None	3
				1111	kkkk	kkkk	kkkk		
RCALL	n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	2
RETFIE	s	Return from interrupt enable	2	0000	0000	0001	000s	INTCONx STAT bits	2
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	2
RETURN	s	Return from Subroutine	2	0000	0000	0001	001s	None	2
INHERENT INSTRUCTIONS									
CLRWDT	—	Clear Watchdog Timer	1	0000	0000	0000	0100	$\overline{TO}$, $\overline{PD}$	

© 2019-2021 Microchip Technology Inc. and its subsidiaries

.....continued

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
				MSb			LSb		
DAW	—	Decimal Adjust WREG	1	0000	0000	0000	0111	C	
NOP	—	No Operation	1	0000	0000	0000	0000	None	
NOP	—	No Operation	1	1111	xxxx	xxxx	xxxx	None	3
POP	—	Pop top of return stack (TOS)	1	0000	0000	0000	0110	None	
PUSH	—	Push top of return stack (TOS)	1	0000	0000	0000	0101	None	
RESET	—	Software device Reset	1	0000	0000	1111	1111	All	
SLEEP	—	Go into Standby mode	1	0000	0000	0000	0011	$\overline{TO}$, $\overline{PD}$	
LITERAL INSTRUCTIONS									
ADDFSR	f_n, k	Add FSR (f_n) with literal (k)	1	1110	1000	f_nf_nkk	kkkk	None	
ADDLW	k	Add literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N	
ANDLW	k	AND literal with WREG	1	0000	1011	kkkk	kkkk	Z, N	
IORLW	k	Inclusive OR literal with WREG	1	0000	1001	kkkk	kkkk	Z, N	
LFSR	f_n, k	Load FSR(f_n) with a 14-bit literal (k)	2	1110	1110	$00f_nf_n$	kkkk	None	3
				1111	00kk	kkkk	kkkk		
MOVLB	k	Move literal to BSR<5:0>	1	0000	0001	00kk	kkkk	None	
MOVLW	k	Move literal to WREG	1	0000	1110	kkkk	kkkk	None	
MULLW	k	Multiply literal with WREG	1	0000	1101	kkkk	kkkk	None	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
SUBFSR	f_n, k	Subtract literal (k) from FSR (f_n)	1	1110	1001	f_nf_nkk	kkkk	None	
SUBLW	k	Subtract WREG from literal	1	0000	1000	kkkk	kkkk	C, DC, Z, OV, N	

© 2019-2021 Microchip Technology Inc. and its subsidiaries

.....continued

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
				MSb			LSb		
XORLW	k	Exclusive OR literal with WREG	1	0000	1010	kkkk	kkkk	Z, N	
DATA MEMORY – PROGRAM MEMORY INSTRUCTIONS									
TBLRD*	—	Table Read	2	0000	0000	0000	1000	None	
TBLRD*+	—	Table Read with post-increment	2	0000	0000	0000	1001	None	
TBLRD*-	—	Table Read with post-decrement	2	0000	0000	0000	1010	None	
TBLRD+*	—	Table Read with pre-increment	2	0000	0000	0000	1011	None	
TBLWT*	—	Table Write	2	0000	0000	0000	1100	None	
TBLWT*+	—	Table Write with post-increment	2	0000	0000	0000	1101	None	
TBLWT*-	—	Table Write with post-decrement	2	0000	0000	0000	1110	None	
TBLWT+*	—	Table Write with pre-increment	2	0000	0000	0000	1111	None	

Notes:

1. When a PORT register is modified as a function of itself (e.g., `MOVF PORTB, 1, 0`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
2. If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.
3. Some instructions are multi-word instructions. The extra words of these instructions will be executed as a `NOP` unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.
4. f_s and f_d do not cover the full memory range. 2 MSbs of bank selection are forced to `0b00` to limit the range of these instructions to the lower 4k addressing space.

© 2019-2021 Microchip Technology Inc. and its subsidiaries