Tecnológico de Monterrey, campus Monterrey
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TE2015 Microcontroladores
HW1.2 Case Study: The 8051 Architecture
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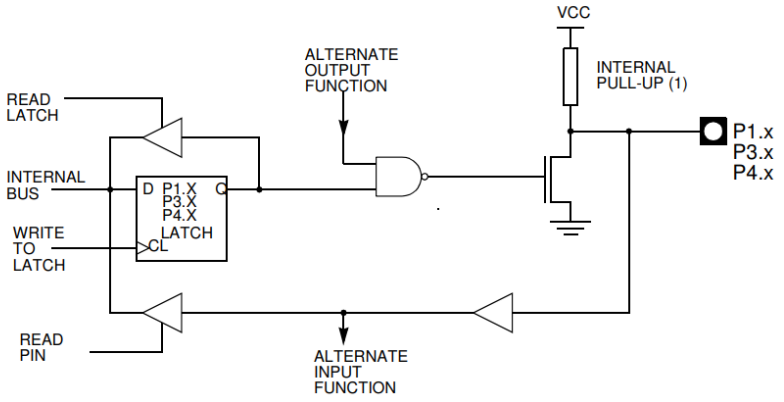
General Purpose Input/Output

Introduction

INTEL's 8051 is an 8-bit microcontroller architecture developed in 1981 and still found in the marked today. One of the currently available microcontrollers based on the 8051 architecture is ATMEL's AT89C51, which datasheet can be found online. In this case study, we will go over some of the 8051's features using the AT89C51 device. Notice that some other devices that share similar architecture can be also found in the market.

According to Figure 1 (page 8) of the AT89C51AC3 microcontroller datasheet, ports 1, 3 and 4 share similar structure, which is shown below:

Figure 1. Port 1, Port 3 and Port 4 Structure



To drive a logic level (0 or 1) as an output of ports 1, 3 and 4, some conditions must be accomplished, as follows (see pin description table on pages 5-7 on the datasheet for further reference):

1. The signal to output is held by INTERNAL BUS and should follow the path towards P1.x, P3.x or P4.x
2. To this to happen, first the LATCH must drive the signal in its input, D, (connected to INTERNAL BUS) towards Q with a clock pulse (CL)
3. Once the INTERNAL BUS signal is transferred to the LATCH output, Q, it is used as one of two inputs of a NAND gate.
4. The second input of the NAND gate is a signal called ALTERNATE OUTPUT FUNCTION. According to the truth table of a NAND gate, if the value of this signal is 0, the output is set to 1 (highlighted in grey in the table below); however, if the value of ALTERNATE OUTPUT FUNCTION is 1, the output of the gate is the inverted value of Q, so is the inverted value of INTERNAL BUS.
5. In this sense, to allow the value of INTERNAL BUS to pass through the NAND gate, ALTERNATE OUTPUT FUNCTION must be set to 1, at the expense that the value to output is inverted.
6. Following the signal path, the output of the NAND gate is used to turn ON (with logic 1) or OFF (with logic 0) the Field Effect Transistor (FET), as it is connected to its Gate terminal. This means that if the value of INTERNAL BUS is 0, the FET's Gate logic value is set to 1, turning ON the transistor; and if INTERNAL BUS is 1, the FET's Gate logic value is 0, turning the transistor OFF.

Q (from Fliop-Flop)	ALTERNATE OUTPUT FUNCTION	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

Table 1: Truth table of the two-input NAND gate.

7. If the FET is OFF, an open circuit can be assumed between the FET's Source and Drain pins, so the pull-up resistor connected between the FET's Source and VCC pulls the pin voltage (P1.x, P3.x or P4.x) up to a logic 1 (hence the name, pull-up resistor). In the opposite case, if the FET is ON, a short circuit is assumed between Source and Drain, driving the pin P1.x, P3.x or P4.x value to a logic 0 (by shorting the pin to ground) and the VCC voltage is entirely absorbed by the pull-up resistor. This means, that the value at INTERNAL BUS is inverted again by the pull-up resistor.

8. This way, the value of INTERNAL BUS value is transferred from the internal data bus of the microcontroller to any pin of ports P1, P3 or P4 as soon as ALTERNATE OUTPUT FUNCTION is set to 1, as shown in the table below:

INTERNAL BUS	ALTERNATE OUTPUT FUNCTION	P1.x, P3.x or P4.x
0	0	0
0	1	0
1	0	0
1	1	1

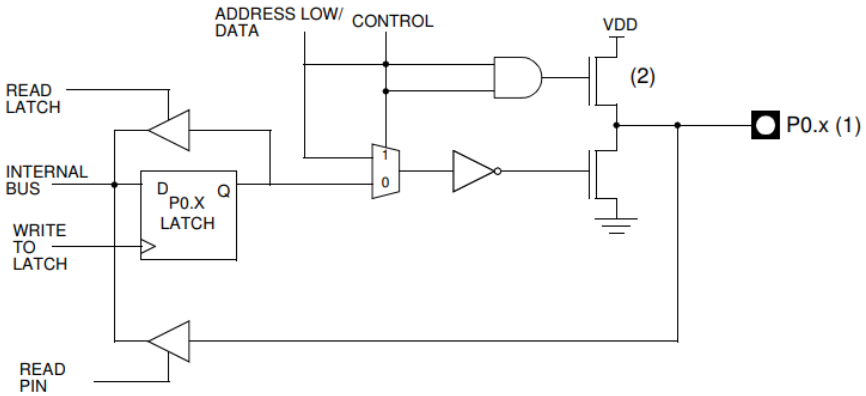
Table 2: Truth table of ports P1, P3 and P4.

Note: Ports P1, P3 and P4 count on a pull-up resistor (a resistor connected between `VCC` and `Drain` of driving FET) to force the logic `1` to `VCC` level when the FET is off.

Activity

1. On the same fashion, describe the path followed by the value of INTERNAL SIGNAL towards P0.x (see Figure 2 of the datasheet). Note that in this case, there is no pull-up resistor pulling the output value to `VCC` for a logic `1`; instead, a FET is used, which is turned on only when both `ADDRESS LOW/DATA` and `CONTROL` signals are high. This is called a *strong pull-up*. However, strong pull-ups of `P0` and `P2` can only be used when these ports are configured as memory buses (`CONTROL = 1`) and not as a GPIO (`CONTROL = 0`), thus in the latter case, `P0.x` and `P2` exhibit an open drain output when a logic 1 set on `INTERNAL BUS`.

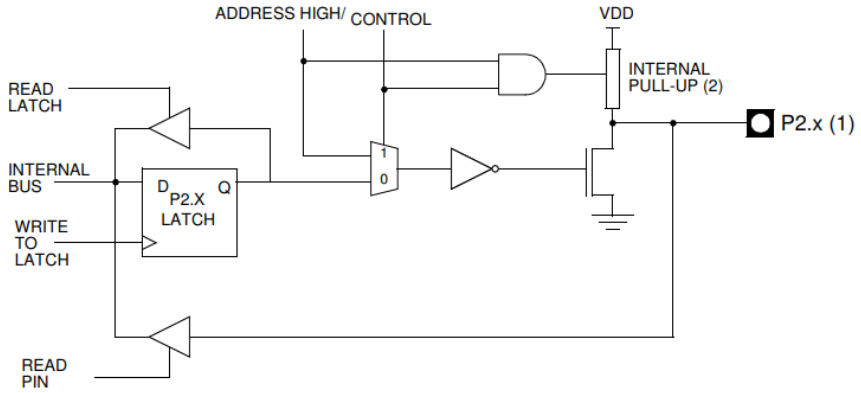
Figure 2. Port 0 Structure



Complement your description with a truth table that shows the change at `P0.x` depending on `INTERNAL BUS`, `ADDRESS LOW/DATA` and `CONTROL` signals (i.e., `ADDRESS LOW/DATA` is one same signal which switches functions to output a memory address or data depending of the port configuration.)

2. Continue with your analysis of the 8051 GPIO but now describe the path followed by the value of INTERNAL SIGNAL towards `P2.x` (Figure 3 of the datasheet). Complement your description with a truth table that shows the change at `P2.x` depending on `INTERNAL BUS`, `ADDRESS HIGH/DATA` and `CONTROL` signals.

Figure 3. Port 2 Structure



3. Considering that ports `P0` and `P2` exhibit open drains when operating as GPIO for the logic `1` case, what do you propose to achieve a logic `1` instead of an open drain when working with GPIO in this configuration?