CIV 2 SM

Reverse Engineering of a High Voltage (HV) Power Supply

Objectives

Given the circuit and functional block diagram of a HV Power Supply you are required to:

1 Analyse the circuit, describe the function of each block and the overall operation of the system;

2 Predict the voltage values and waveforms at various points in the circuit;

3 Test the circuit that has been built;

4 Compare the predicted values with the measured ones.

Report

Each group is required to present a written report on the analysis, measurements and testing of the circuits. The contribution of each member of the group should be clearly indicated in the report.

Log Book Record

Each student is required to keep a log book record of all the work done by the group and these logbooks are to be handed in with the written report.

Safety.

This project involves the analysis and testing of a high voltage power supply of between 3 kV and 5 kV. The design is similar to those used in some of the instruments flown by IRF on space missions. There are some differences such as the size of the board, choice of components, the inclusion of test points in the circuit and the fact that the circuit is NOT encapsulated. This last means that when the circuit is running there are very high voltages at points in the circuit that can be touched. As part of the project you are required to devise procedures for testing the circuit that eliminate this risk. You are not allowed to test the circuit without having had your safety procedures approved by Leif or without supervision by a member of staff and you must then comply with the procedures you have devised when testing the circuit.

Data Sheets

The following information and data sheets are attached:
1 A block diagram of the power supply;
2 A circuit diagram of the power supply;
3 An example of the analysis of one of the circuits;
4 Data sheets for some of the IC's.
Note that all the operational amplifier circuits used in this laboratory work have been covered in the laboratory work 'Basic Operational Amplifier Circuits'.

Component Values

Please check whether the values of the components on the circuit diagram are the same as on the board you have been given as some component values have been changed from those on the circuit diagram. The values on the board are the ones to be used in practise, those on the circuit diagram were the original design ones.

Procedure 1, Circuit Analysis

Some of this will be covered in a discussion on the laboratory work and some in a demonstration to be run to show some finer points. If there is time you should complete this part before testing the circuit in the laboratory.

1.1 **The individual blocks in the block diagram.**
For each of the blocks in the block diagram identify the circuit that it represents.
Examine the circuit and determine what the circuit does.
Estimate the waveforms and voltages at suitable points in the circuit.

1.2 **The over all block diagram.**
Describe the operation of the whole circuit in terms of your block diagram. A number of test points have been included on the board and are shown on the circuit. The voltage values and waveforms at these points should be calculated or estimated and recorded.

1.3 Describe any special voltage or power requirements required for any of the components. For example: the V_{CEO} required for the transistors Q1 and Q2 and in the voltage multiplier ladder the diode and capacitor voltage ratings.

1.4 Devise a circuit test procedure that will prevent anybody touching a high voltage point in the circuit while it is under test. This procedure has to be approved by Leif or David before you are allowed to test the full system.

Procedure 2, Testing the Individual Parts of the System.

2.1 **Safety**
Disable the high voltage part of the circuit by disconnecting the voltage multiplying ladder from the transformer output. That is remove capacitor C4.

2.2 Connect the 5 Volt and the ± 12 Volt supplies to the board but **NOT** the 30 Volt supply.

2.3 **The Oscillator.**
Observe and record the voltages and the waveforms at the output of the oscillator and across capacitor C1 using the oscilloscope.
Measure the minimum and maximum frequency of the oscillator by varying the potentiometer R2.

2.4 **The Pulse Generator.**
Record the relationship between the input waveform and the two output waveforms using the oscilloscope.

The rest of the circuit is part of a feedback loop so needs to be tested in the following way with the voltage multiplying ladder still disconnected, that is C4 removed.

2.5 **Output Voltage Sample and Output Voltage Monitor.**
To test this circuit a dc voltage needs to be applied between the 500 MΩ and the 220 kΩ resistors and the output voltage of the two circuits monitored. The 500 MΩ will ensure that the voltage multiplier does not affect the measurements.
Ground the junction of the two resistors and measure the voltages at the outputs of the two circuits.
Apply a dc voltage of +1.5 Volts to the junction of the two resistors and measure the voltages at the outputs of the two circuits. Check that varying the voltage varies the two output voltages as expected. Leave the +1.5 Volts connected to the junction.
Calculate the dc gain of each circuit.

2.6 **Input Reference Voltage and Power Control.**
In this circuit the Input Reference Voltage is represented by connection J1 and the potentiometer R6.
Apply dc voltages of +5 Volts to J1 and +1.5 Volts to the junction as in 5 above.
Examine and record how the output voltage at Test Point 3, TP3, varies as the potentiometer R6 is altered and as the value of the voltage applied to the junction is altered.

2.7 **Power Control and Power Switch.**
Set the voltage at the junction of the two resistors at +1.5 Volts as in 5 above and apply the +5 Volts to J1.
Observe the voltages and waveforms at Test Point 2, TP2, (or Test Point 4, TP4,) and Test Point 3, TP3, using the oscilloscope.
Adjust the potentiometer, R6 to set the voltage at TP3 to a negative voltage of around -5 Volts.
Record from the oscilloscope the voltages and waveforms at the test points being observed, TP2 and TP3.
Record how the voltages and waveforms at the test points being observed vary with changes in the two voltages being applied to the circuit.
Return to the conditions where the voltage at test point 3 is about -5 Volts.

2.8 **Power Switch and Transformer.**
Check that the voltage multiplying ladder is disabled, that is capacitor C4 has been removed.
Observe with the oscilloscope the voltages and waveforms at test points TP1 and TP2.
With the voltages applied to the circuit as in 7 above also connect the 30 Volt to the board. This will allow the two power transistors to drive the transformer in a push pull arrangement.
It is now necessary to tune the oscillator so that the push-pull pulses are at the resonant frequency of the transformer. This is done by observing the waveform at test point 1 and varying the oscillator frequency to give a maximum in the waveform at test point 1 that is also at the same frequency as the push-pull pulses. Note very similar results can be obtained with the pulses at half the transformer resonant frequency. Record these results including the oscillator frequency.

Procedure 3 High Voltage System Test.

To test the operation of the HV supply you MUST follow the procedures that have been approved by either Leif or David.
This testing phase MUST be done under supervision by a member of staff, in the laboratory.

3.1 **Initial Conditions.**
Turn all the supplies to the board OFF.
Remove the connection and the supply to the junction of the two resistors, the 500 MΩ and the 220 kΩ.
Replace the capacitor, C4, between the transformer and the ladder network.
Check that the board is set up as in 1.8 above.
Apply the 5 Volt and the ±12 Volt supplies.

3.2 **Initial Test.**
Apply the 30 Volt supply to the board and measure the HT Voltage using the High Voltage Probe and a meter. Record the value of the HT Voltage.
Adjust the oscillator frequency to give maximum HT Voltage.

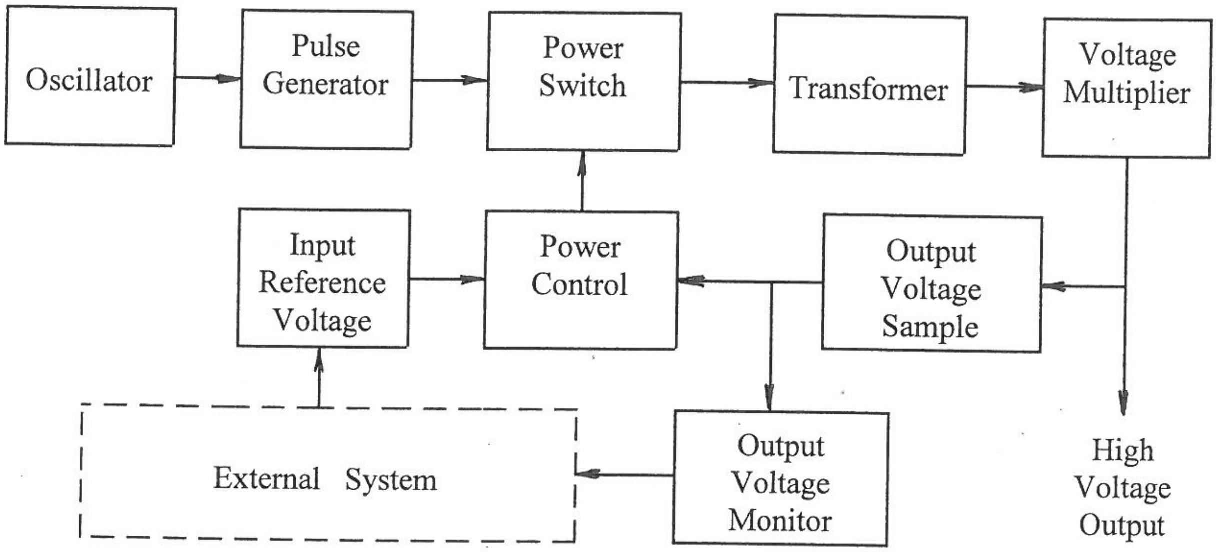
3.3 **Variation of Output Voltage.**
Alter the input reference voltage using potentiometer R6 to find the maximum and minimum values of HT Voltage.

Results

Compare the results with the analysis you have recorded.

HT Power Supply Block Diagram

Figure 1, Block Diagram of the HT Power Supply.

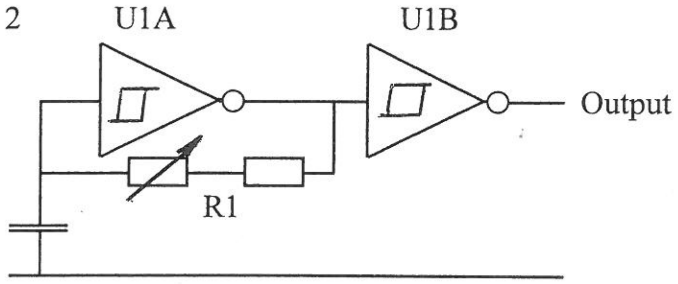


The Oscillator Circuit

As an example of the circuit analysis take the block labelled 'Oscillator' this represents the circuit of Figure 2.
For this circuit you should:

1 Identify the type of gates used.
2 Describe the operation of the circuit.
3 Derive an expression for the frequency of operation of the circuit.
4 Describe or sketch the expected output wave form.
5 State the range of frequency that will be obtained at the output using the variable resistor.

Figure 2

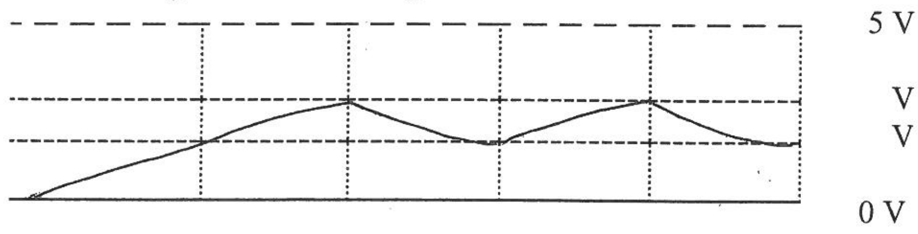


1 The gates are type 74HC14.
These are Inverting Gates with Schmitt Trigger Inputs.
There are 6 of them in the same IC package.

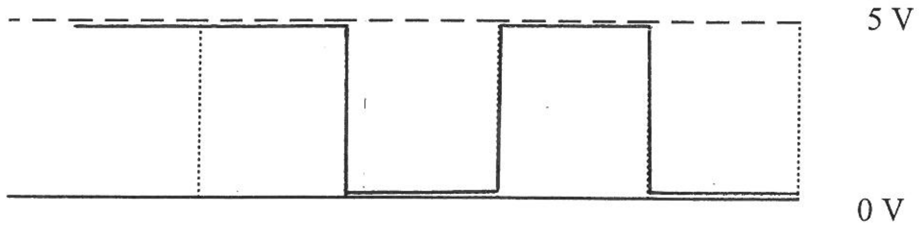
The supply voltage is +5 Volts. The data sheets give values for 4.5 V and 6 Volts so you will have to interpolate between these.
Thus at 5 Volts the thresholds are: positive-going = negative-going =

and the output voltages are: Logic HIGH = Logic LOW =

At the input of the first gate U1A the voltage levels are:



At the output the resulting voltages are:



The period of each pulse is given by the time taken for the C1 R1 circuit to charge or discharge from one threshold level to the other.

The equation for a charge of a capacitor through a resistor is:

$$v = V\left[1 - e^{-\frac{t}{CR}}\right] \qquad \text{-----} \quad 1$$

Where v is the voltage across the capacitor C,
V is the voltage difference between the start and the voltage it is charging from
and CR is the time constant of the circuit.

Ignoring the first cycle then in the above case:
the start voltage is the lower threshold voltage, =

The voltage it is charging from is the output voltage, =

Therefore V is the difference in voltage, =

The time of the rising period, t, is the time to rise from the lower threshold voltage to the upper threshold voltage so:

Voltage, v =

The period is time t, so rearrange equation 1 to give:

$$e^{-\frac{t}{CR}} = \frac{V}{V - v}$$

$$t = C\,R \ln\left[\frac{V}{V - v}\right]$$

Substituting figures gives:

Similarly for the other period. $v = V e^{-\frac{t}{CR}}$ ---- 2 $\quad or \quad t = C\,R \ln \frac{V}{v}$

In this case V =

And v =

Substituting figures gives:

Total period is

So the frequency is

DC CHARACTERISTICS

Type 74HC14

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −20 μA	2.0	1.9	2.0	–	V
		I_O = −20 μA	4.5	4.4	4.5	–	V
		I_O = −20 μA	6.0	5.9	6.0	–	V
		I_O = −4.0 mA	4.5	3.98	4.32	–	V
		I_O = −5.2 mA	6.0	5.48	5.81	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA	2.0	–	0	0.1	V
		I_O = 20 μA	4.5	–	0	0.1	V
		I_O = 20 μA	6.0	–	0	0.1	V
		I_O = 4.0 mA	4.5	–	0.15	0.26	V
		I_O = 5.2 mA	6.0	–	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	–	0.1	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	6.0	–	–	2.0	μA
T_{amb} = −40 to +85 °C							
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −20 μA	2.0	1.9	–	–	V
		I_O = −20 μA	4.5	4.4	–	–	V
		I_O = −20 μA	6.0	5.9	–	–	V
		I_O = −4.0 mA	4.5	3.84	–	–	V
		I_O = −5.2 mA	6.0	5.34	–	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA	2.0	–	–	0.1	V
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 20 μA	6.0	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.33	V
		I_O = 5.2 mA	6.0	–	–	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	–	1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	6.0	–	–	20	μA

TRANSFER CHARACTERISTICS

Type 74HC

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C; note 1							
V_{T+}	positive-going threshold	Figs 7 and 8	2.0	0.7	1.18	1.5	V
			4.5	1.7	2.38	3.15	V
			6.0	2.1	3.14	4.2	V
V_{T-}	negative-going threshold	Figs 7 and 8	2.0	0.3	0.52	0.90	V
			4.5	0.9	1.40	2.00	V
			6.0	1.2	1.89	2.60	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	Figs 7 and 8	2.0	0.2	0.66	1.0	V
			4.5	0.4	0.98	1.4	V
			6.0	0.6	1.25	1.6	V
T_{amb} = −40 to +85 °C							
V_{T+}	positive-going threshold	Figs 7 and 8	2.0	0.7	–	1.5	V
			4.5	1.7	–	3.15	V
			6.0	2.1	–	4.2	V
V_{T-}	negative-going threshold	Figs 7 and 8	2.0	0.3	–	0.90	V
			4.5	0.90	–	2.00	V
			6.0	1.20	–	2.60	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	Figs 7 and 8	2.0	0.2	–	1.0	V
			4.5	0.4	–	1.4	V
			6.0	0.6	–	1.6	V
T_{amb} = −40 to +125 °C							
V_{T+}	positive-going threshold	Figs 7 and 8	2.0	0.7	–	1.5	V
			4.5	1.7	–	3.15	V
			6.0	2.1	–	4.2	V
V_{T-}	negative-going threshold	Figs 7 and 8	2.0	0.30	–	0.90	V
			4.5	0.90	–	2.00	V
			6.0	1.2	–	2.60	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	Figs 7 and 8	2.0	0.2	–	1.0	V
			4.5	0.4	–	1.4	V
			6.0	0.6	–	1.6	V

Note

1. All typical values are measured at T_{amb} = 25 °C.

Type 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Fig.9	4.5	–	20	34	ns
t_{THL}/t_{TLH}	output transition time	see Fig.9	4.5	–	7	15	ns
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Fig.9	4.5	43	–	–	ns
t_{THL}/t_{TLH}	output transition time	see Fig.9	4.5	19	–	–	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Fig.9	4.5	–	–	51	ns
t_{THL}/t_{TLH}	output transition time	see Fig.9	4.5	–	–	22	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

TRANSFER CHARACTERISTIC WAVEFORMS

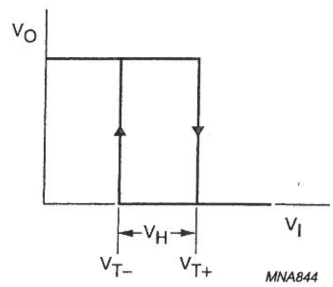
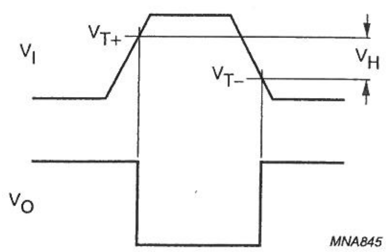


Fig.7 Transfer characteristic.



V_{T+} and V_{T-} are between limits of 20% and 70%.

Fig.8 The definitions of V_{T+}, V_{T-} and V_H.

FAIRCHILD
SEMICONDUCTOR™

October 1987
Revised January 2004

CD4017BC • CD4022BC
Decade Counter/Divider with 10 Decoded Outputs • Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BC and CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power Fan out of 2 driving 74L
  TTL compatibility: or 1 driving 74LS
- Medium speed operation: 5.0 MHz (typ.)
  with 10V V_{DD}
- Low power: 10 µW (typ.)
- Fully static operation

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

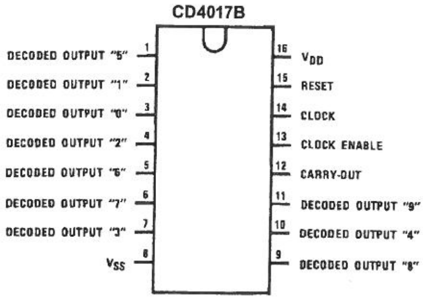
Ordering Code:

Order Number	Package Number	Package Description
CD4017BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4017BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4022BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4022BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

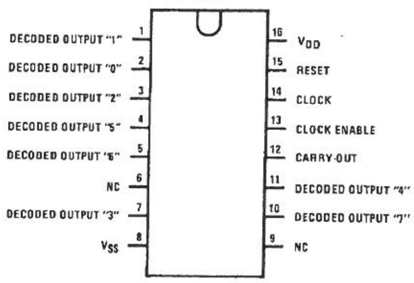
Connection Diagrams

CD4017B



Top View

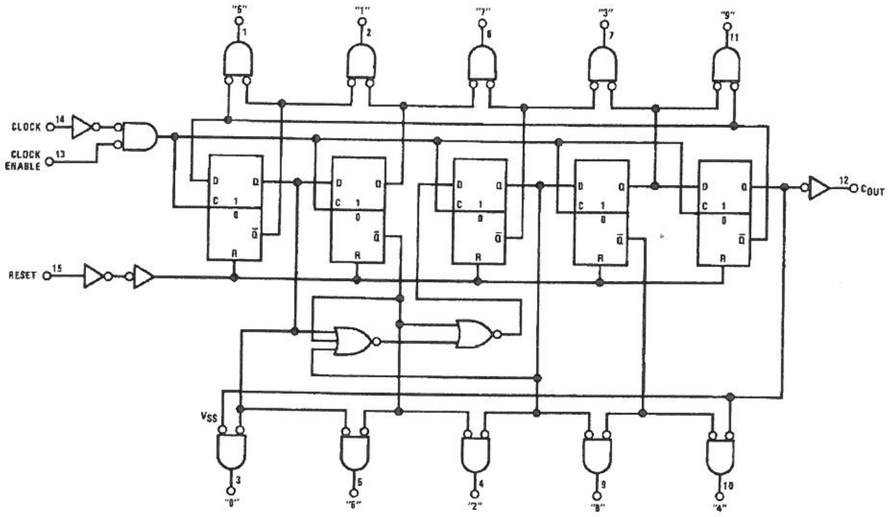
CD4022B



Top View

Logic Diagrams

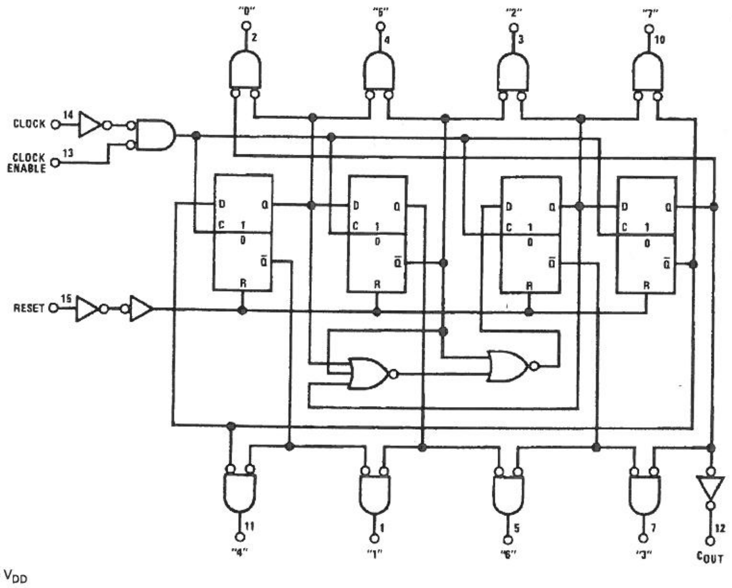
CD4017B



Terminal No. 8 = GND

Terminal No. 16 = V_{DD}

CD4022B

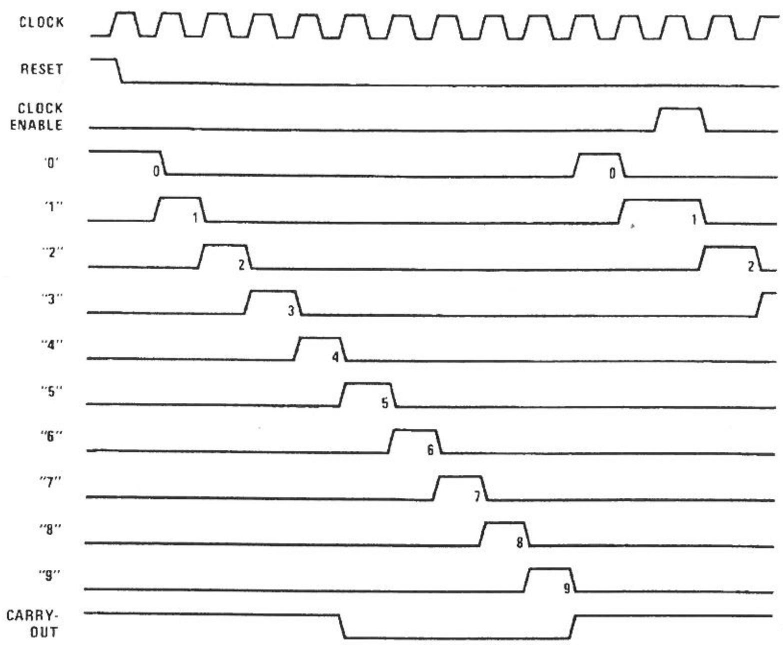


Terminal No. 16 = V_{DD}

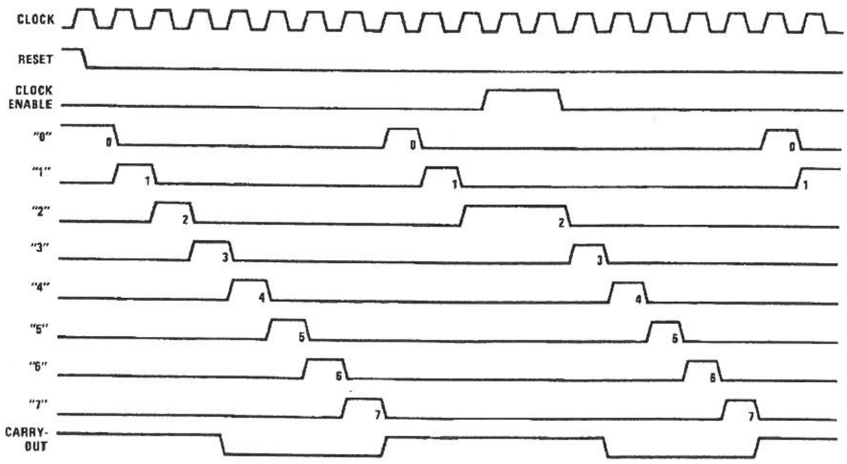
Terminal No. 8 = GND

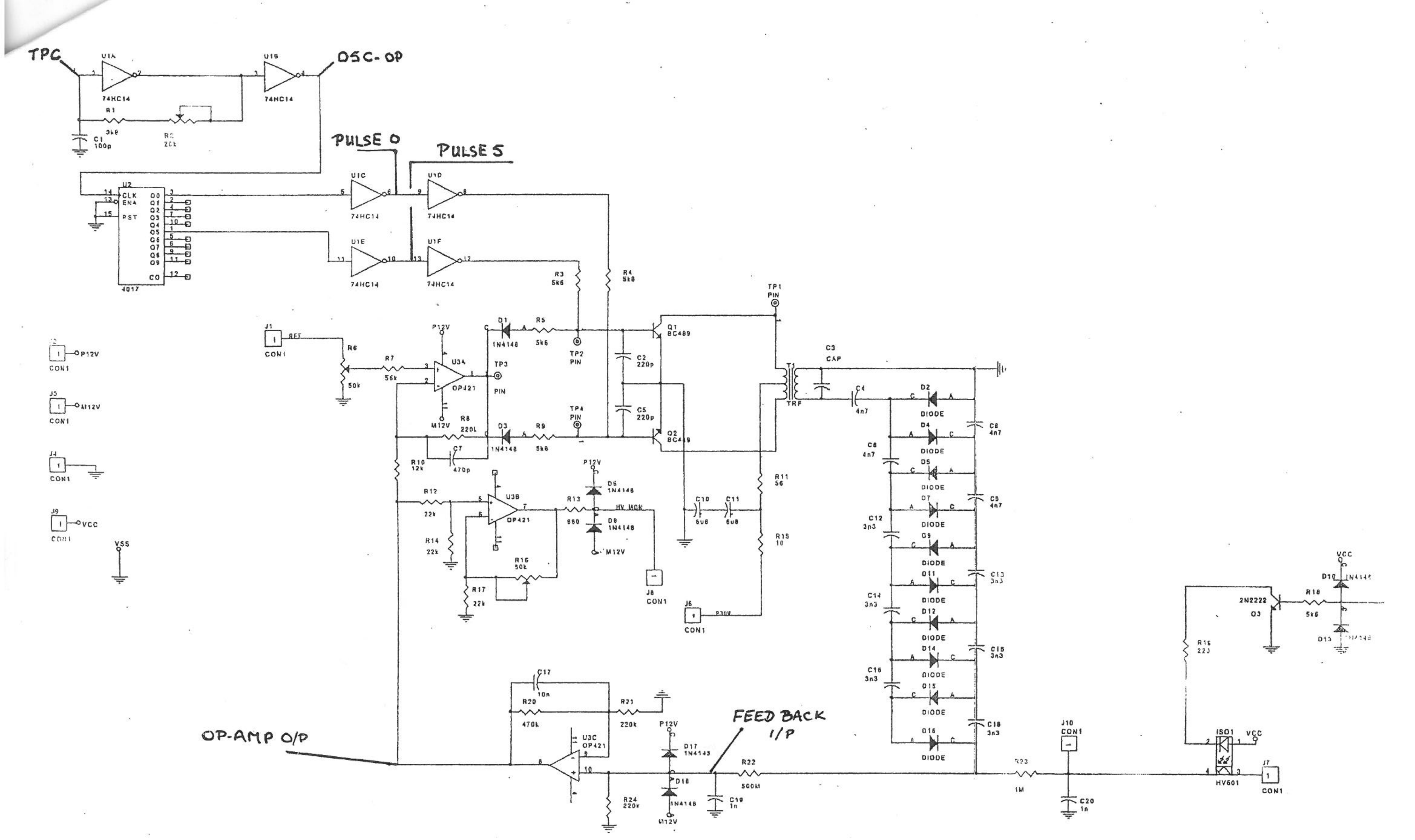
Timing Diagrams

CD4017B



CD4022B





TPC
OSC-OP
PULSE 0
PULSE 5
OP-AMP O/P
FEED BACK I/P
U1A
U1B
U1C
U1D
U1E
U1F
74HC14
U2
4017
R1
3k9
C1
100p
R2
20k
J1
CON1
REF
R6
50k
R7
56k
U3A
OP421
U3B
U3C
TP1
TP2
TP3
TP4
PIN
D1
D3
1N4148
R5
5k6
R9
R3
R4
Q1
Q2
BC489
C2
C5
220p
C3
CAP
C4
4n7
T1
TRF
R8
220L
C7
470p
R10
12k
R12
22k
R14
R13
680
D6
D8
HV MON
R16
50k
R17
J8
C10
C11
6u8
R11
56
R15
10
J6
P30V
J2
P12V
J3
M12V
J4
J9
VCC
VSS
DIODE
C17
10n
R20
470k
R21
220k
R24
D17
1N4143
D18
C19
1n
R22
500M
R23
1M
J10
C20
R19
22J
ISO1
HV601
J7
Q3
2N2222
R18
5k6
D10
D13