

## NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
  - A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES  
610-60527-01\_03.ZIP
  - B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
  - C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
  - D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
  - E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
  - F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

## 2 DIELECTRIC MATERIAL:

- A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).
- B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
- C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS, IF SPECIFIED. 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
- D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

## 3. DRILLING:

- A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+,.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
- B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

## 4. SOLDER MASK:

- A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
- B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
- C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

## 5. MARKING:

- A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
- B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
- C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

## 6. ELECTRICAL TEST:

- A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB+, DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
- B. ALL PCBs SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
- C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

## 7 FINAL FINISH:

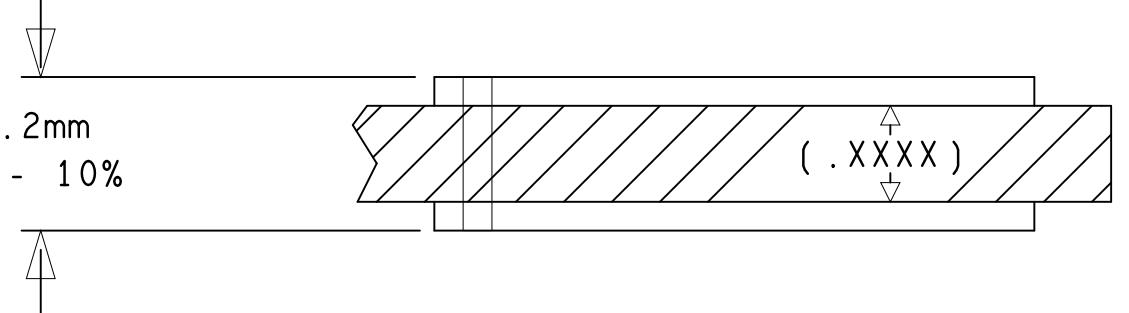
- A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

## 8. IMPEDANCE:

- A. IMPEDANCE CALCULATIONS ARE NOT REQUIRED.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBs SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

## STACK-UP



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	CPW SPACE	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	CPW SPACE
L01 - TOP	1/2 OZ	--	-----	-----	-----	-----	-----
L02 - BOTTOM	1/2 OZ	--	-----	-----	-----	-----	-----

		CYPRESS		EMBEDDED IN TOMORROW	
198 CHAMPION COURT SAN JOSE, CA 95134 (408) 943-2600		TITLE PCB FABRICATION, CY8CPROTO-063-BLE PSoC6 PROTOTYPING KIT			
ALLEGRO FILE: 600-60527-01_03.BRD		SIZE CAGE CODE CY P/N <b>D</b> - 610-60527-01			
SEE BOM NEXT ASSY		SEE BOM USED ON <b>2</b>		DO NOT SCALE DRAWING APPROVALS DATE DRAWN PRAO 09/18/18 ENGINEER TARE 09/18/18 CHECKER -	
APPLICATION		MATERIAL		FINISH <b>7</b>	
THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO CYPRESS SEMICONDUCTOR AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHEN SUCH USER POSSESSES AUTHORIZATION FROM CYPRESS		QA - PROJ. ENG. -		SCALE 1/1 SHEET 1 OF X REV 03	

8

7

6

5

4

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2

1

D

D

C

C

D

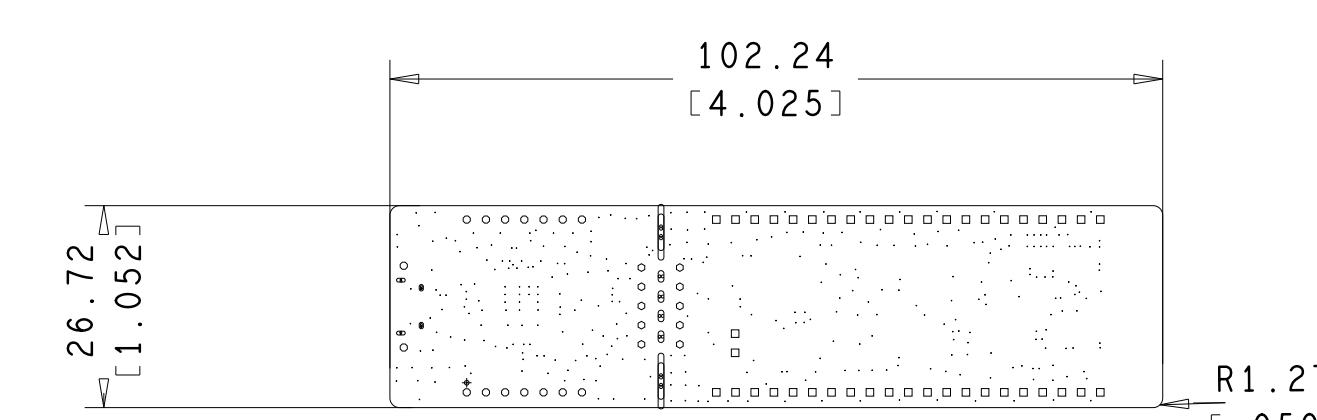
D

B

B

A

A



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN INCHES				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
+	0.0079	+0.0020/-0.0079	PLATED	351
□	0.0394	+0.0030/-0.0030	PLATED	44
○	0.0400	+0.0030/-0.0030	PLATED	10
○	0.0402	+0.0030/-0.0030	PLATED	16
◎	0.0335x0.0216	+0.0030/-0.0030	PLATED	2
(GA)	0.0453x0.0197	+0.0030/-0.0030	PLATED	2
◎	0.0600x0.0300	+0.0020/-0.0020	NON-PLATED	4
‡	0.2400x0.0300	+0.0020/-0.0020	NON-PLATED	4

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SIZE	CAGE CODE	CY P/N
D	-	610-60527-01
SCALE	SHEET	REV
1/1	2	03

COMPUTER GENERATED DRAWING  
DO NOT CHANGE MANUALLY