SwRI CCD Small Satellite Readout System (MDE F25-13)

Actions

Task Name	Status	Assigned To	Date
Change various “Demonstration” verification types to “Test”. Whatever requires a quantifiable value is a “Test”	Complete	Jae	4/3/2025
Define the comms protocol we’re using in requirements (from ICD)	Complete	Javier	4/3/2025
Change “develop” to “utilize” for the comms requirement	Complete	Cody	4/3/2025
Update Slide 10 to current design (bidirectional communication, etc.)	Complete	Cody	4/3/2025
Remove anything from the blue box in slide 10 except for the name of our project	Complete	Cody	4/3/2025

Actions

Task Name	Status	Assigned To	Date
Update Concept of Operations: remove shutter	Complete	Yifu	4/3/2025
Update Concept of Operations: make “start” signal more explicit	Complete	Yifu	4/3/2025
Update Concept of Operations: remove “image processing”	Complete	Yifu	4/3/2025
Update Concept of Operations: don’t send signal (it’s requested async). Image is placed in a buffer	Complete	Yifu	4/3/2025
Remove shutter from subsystem diagram	Complete	Cody	4/3/2025
Complete Soldering Training and Lab Swipe Access	Complete	Team	4/3/2025

Actions

Task Name	Status	Assigned To	Date
CCD Subsystem Diagram: add how the voltage dividers will go high and low using the MOSFETs	Complete	Cody	4/3/2025
CCD Subsystem Diagram: Complete subsystem layout for CDR	Complete	Cody	4/3/2025
System Sequencing Diagram: add commands found in ICD	Complete	Javier	4/3/2025
System Sequencing Diagram: add logic for “idle” and “sleep” functions	Complete	Javier	4/3/2025
System Sequencing Diagram: change “person” icon to “spacecraft”	Complete	Yifu	4/3/2025

Actions

Task Name	Status	Assigned To	Date
Class Diagram: Show parameters for functions	Complete	Javier	4/3/2025
Class Diagram: remove compression and other unnecessary blocks	Complete	Yifu	4/3/2025
Class Diagram: expand each box with specifics for CDR	Complete	Javier	4/3/2025
Class Diagram: change “Data Reorganization” to “Data Storage”	Complete	Yifu	4/3/2025
Trade Studies: need to be made with later replacing with space-rated parts in mind	Complete	Cody	4/3/2025

Actions

Task Name	Status	Assigned To	Date
Cost Table: add estimated PCB costs to the table	Complete	Cody	4/3/2025
Cost Table: use more of the available $500-750 budget	Complete	Cody	4/3/2025
System Testing: choose a specific speed to test CCD at to make design easier	Complete	Jae	4/3/2025
System Testing: no need to test with a light filter, can test with LEDs on a bench	Complete	Jae	4/3/2025
System Testing: emulator for comms testing needs to be added to the WBS in “Testing Support”	Complete	Javier	4/3/2025

Actions

Task Name	Status	Assigned To	Date
System Testing: add TVAC testing to our schedule. Have a bake out schedule	Complete	Team	4/3/2025
System Testing: make sure we know how to clean our board before entering the TVAC	Complete	Team	4/3/2025
System Testing: get to know how our specific chamber works (constraints, how to feed wires through). Get an actual tour and as much info as possible on the TVAC chamber	Complete	Team	4/3/2025
System Testing: add active temp readout through thermistors to the board	Complete	Cody	4/3/2025

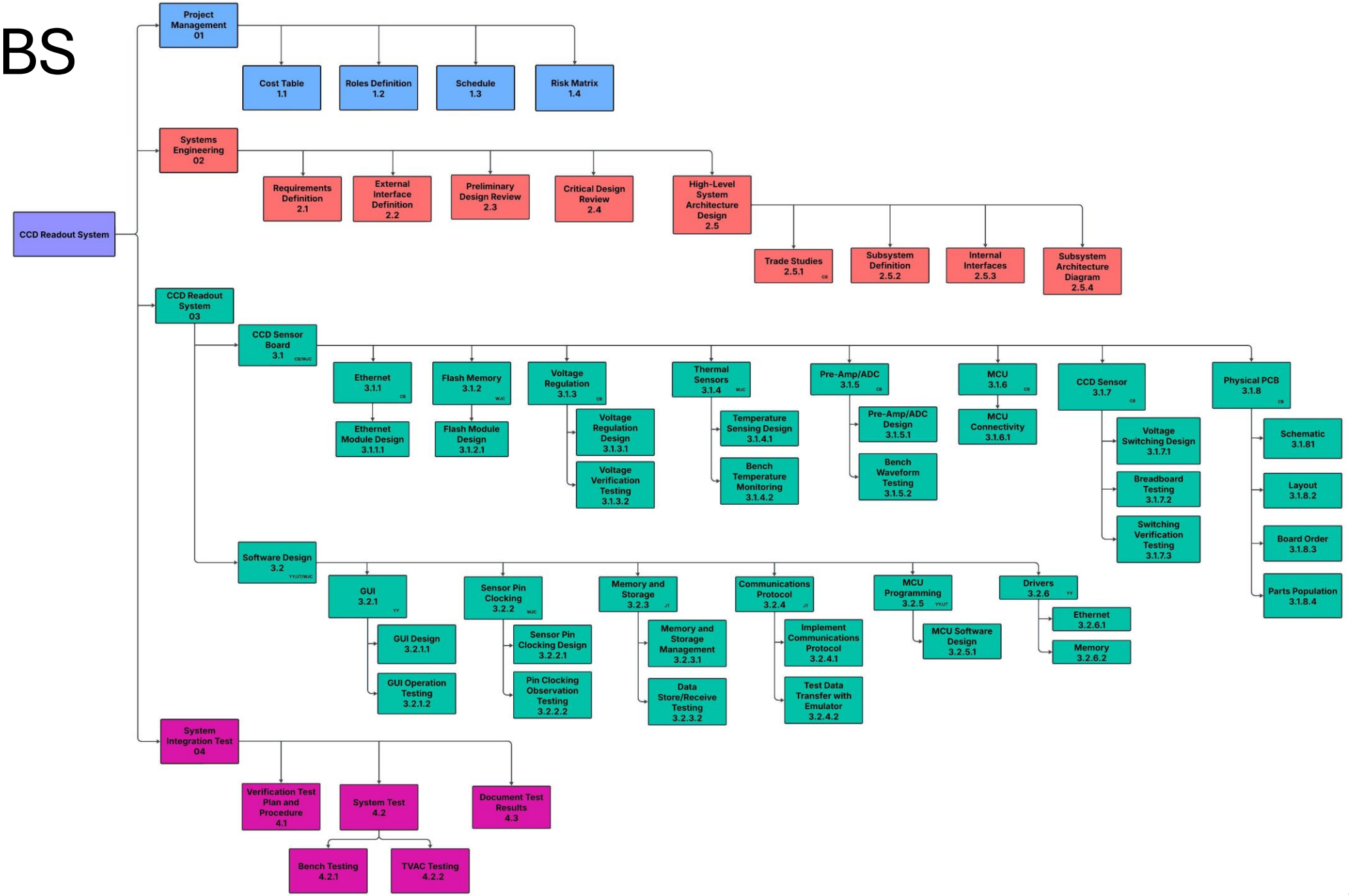
Actions

Task Name	Status	Assigned To	Date
System Testing: noise testing comes before putting it in the TVAC. Short CCD connections to board ground	Complete	Javier	4/3/2025
Project Schedule: detailed design needs to be built out for CDR	Complete	Cody	4/3/2025
Risk Mitigation: need to find a way to mitigate almost certain risks, nothing should be in the red in terms of probability. Re-Assess risks until we have good enough procedures to reduce their probability of occurring	Complete	Jae	4/3/2025

Actions

Task Name	Status	Assigned To	Date
Parts Ordering: Start ordering parts that will take long shipping times.	Partially Complete	Team	4/3/2025
Documents for the customer: Prepare a document that the team and VT isn't responsible if the CCD is damaged	Partially Complete	Cody	4/3/2025

WBS



VIRGINIA TECH

Project Requirements

: Updated

Functional	***Verification Type***
1. Shall be operational between -55C and 35C	Test : Temperature
2. Shall survive between -65C and 45C	Test : Temperature
3. Shall generate image	Test : Image
4. Shall be clocked by a microprocessor	Demonstration
5. Must have at least a 12-bit ADC	Analysis
6. Must have temperature sensing	Analysis
Performance	
1. Shall not generate more than 3 electrons of read noise	Analysis
Compliance	
1. All code must be written in Python	Demonstration
2. Operation and commands must adhere to ICD	Demonstration
Environmental	
1. Shall stay operational in harsh space conditions	Test : Temperature

Project Requirements cont.

Power 1. Shall be powered by a 28V wired connection 2. Shall not consume more than 5W 3. Shall have DC voltage regulation(i)	***Verification Type*** Demonstration Test: Power Test: Volts
Mechanical 1. Total system shall not be larger than 1/2U 2. Shall not be made of more than 3 boards 3. Boards must have 8-32 mm mounting holes 4. Shall use the CCD sensor provided	Analysis Inspection Inspection Demonstration
Input/Output 1. Shall have pre-amping for the analog signal produced from the CCD sensor 2. Shall use Ethernet for data transfer 3. Shall implement existing UDP for interacting with the host computer	Test: Volts Demonstration Test: Test Cases

i: Voltage biasing for 29V, 25V, 17V, 12V, 10V, 9.5 V, 3.3V, 3V

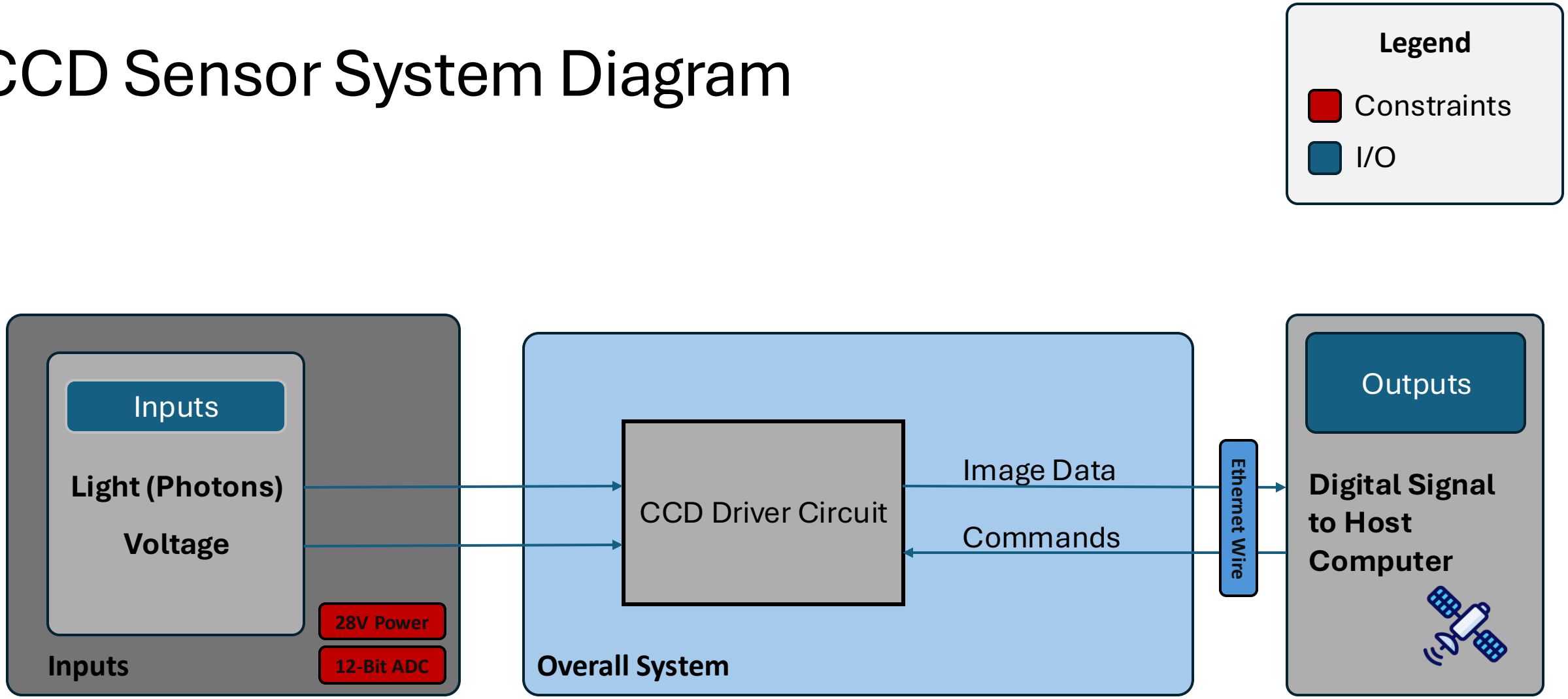
Project Requirements cont.

Testing 1. Shall test the functionality of the prototype in a thermal vacuum chamber	***Verification Type*** Test: Temperature
Schedule 1. Shall finish prototype design by April 20th	Demonstration
Reliability 1. Shall use commercial/automotive hardware to build prototype	Demonstration

Nice to Have

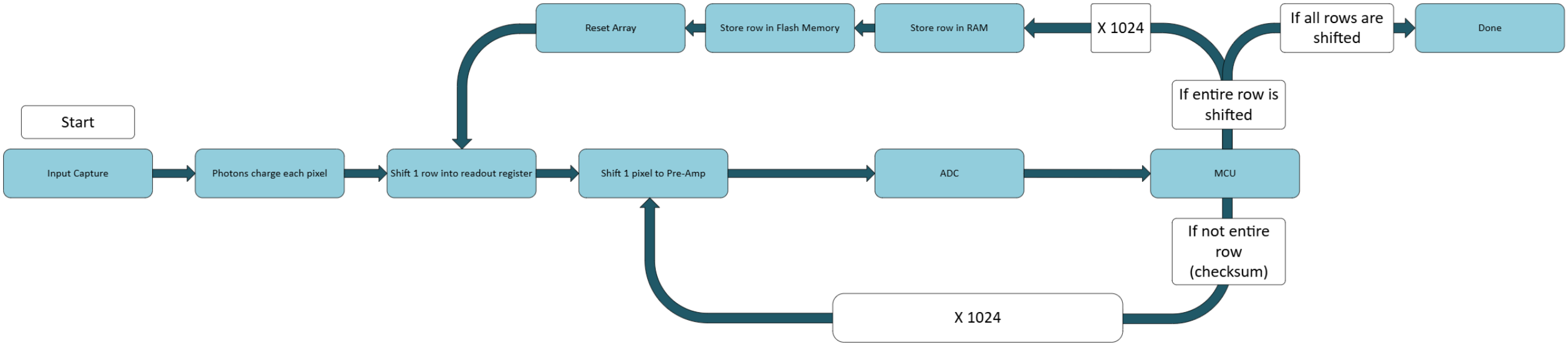
Design 1. Should use a 16-bit ADC (as opposed to 12-bit)	Demonstration

CCD Sensor System Diagram



VIRGINIA TECH

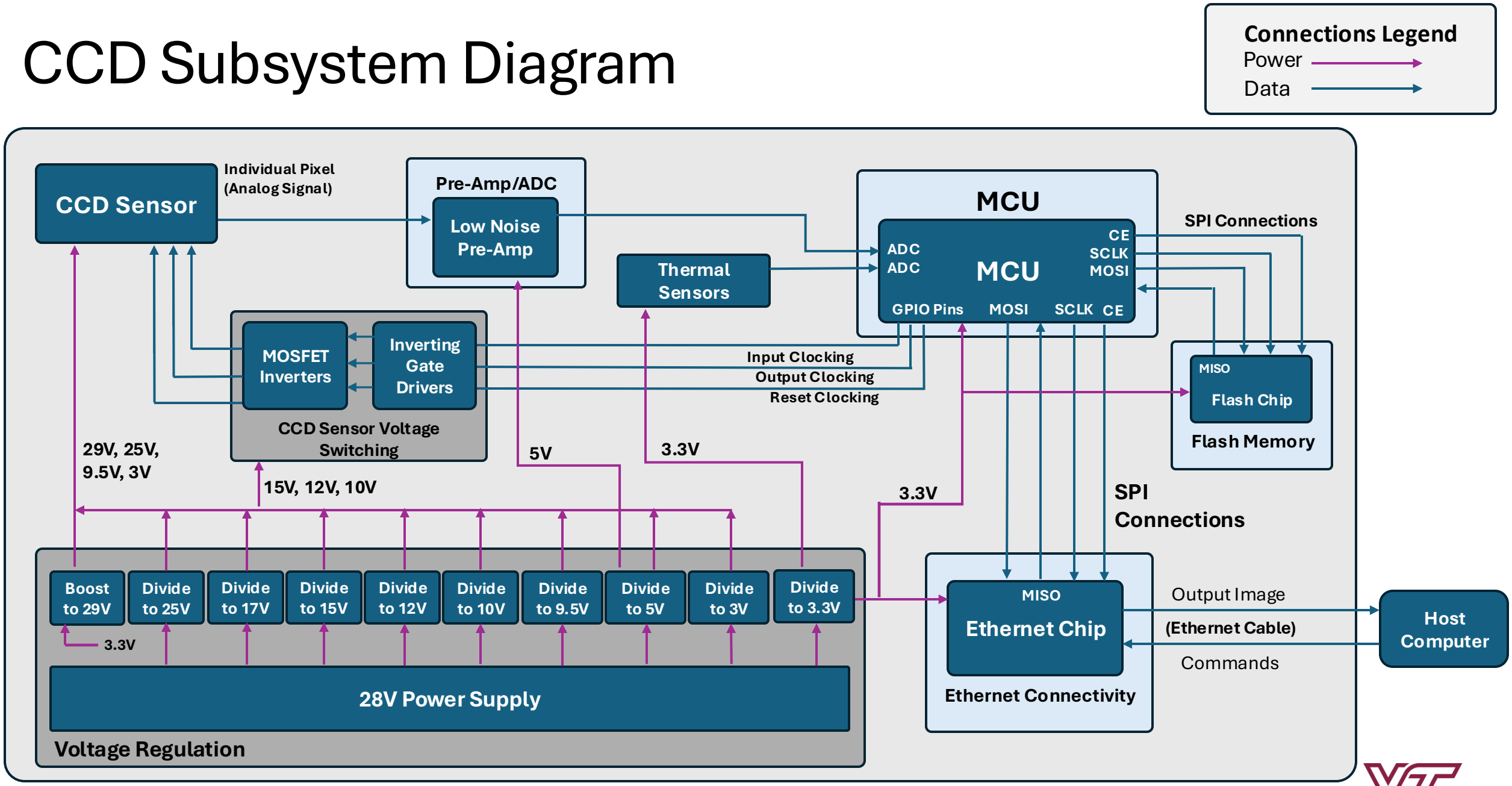
Concepts of Operations



VIRGINIA TECH

Hardware Subsystems

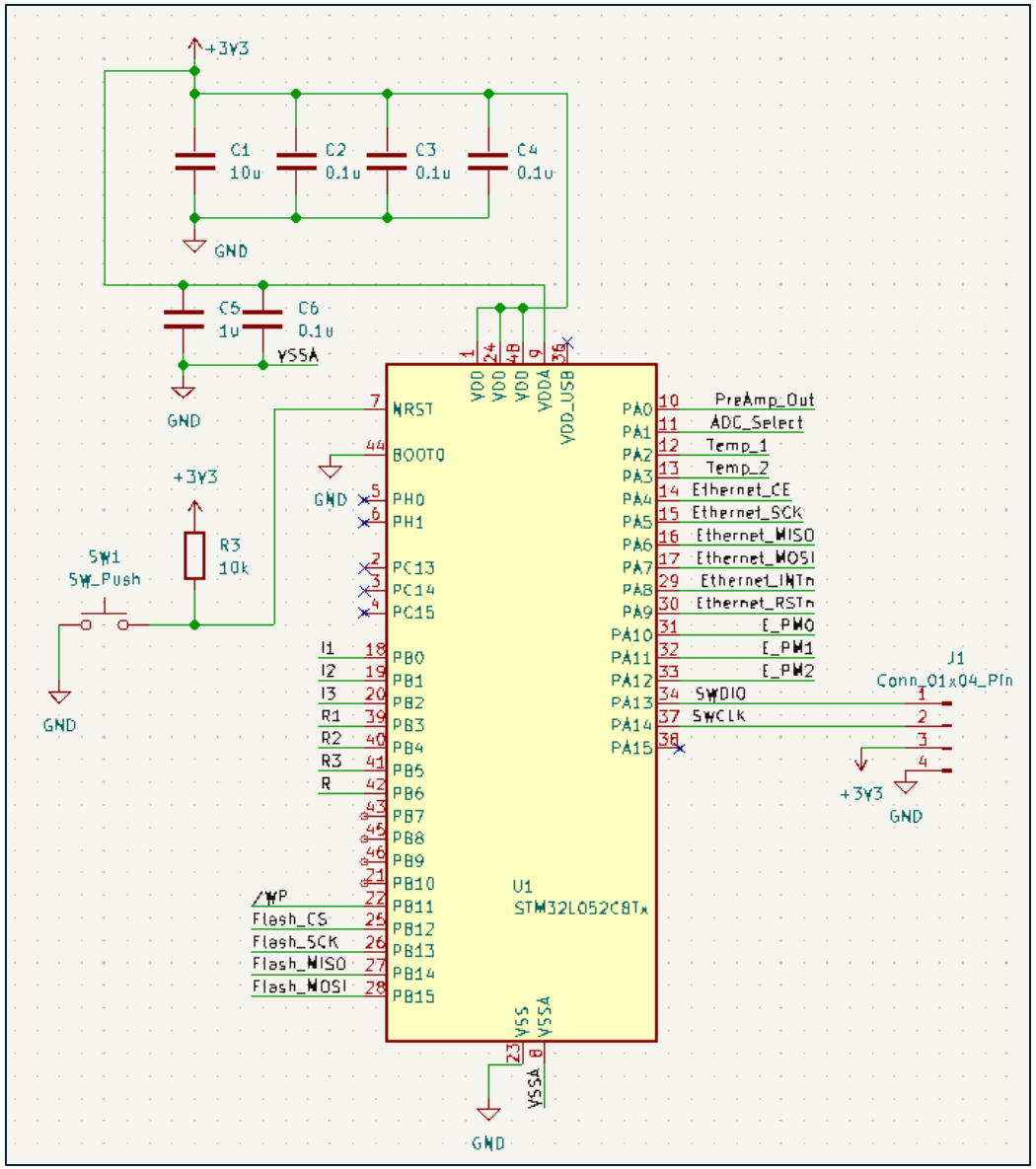
CCD Subsystem Diagram



VIRGINIA TECH

PCB Schematics and Simulations

PCB Schematic: MCU, Preamp, and Memory



Labeled Connections to:

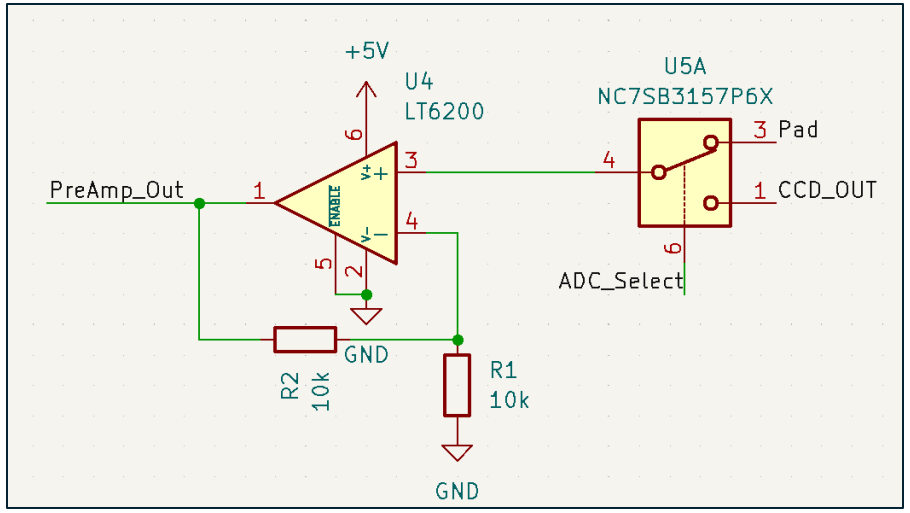
- Pre-Amp
- Temperature Sensors 1 and 2
- Ethernet Module (W5500)
- SWD Debug Pins
- Flash Memory Chip
- Gate Driver Inputs

Other Connections:

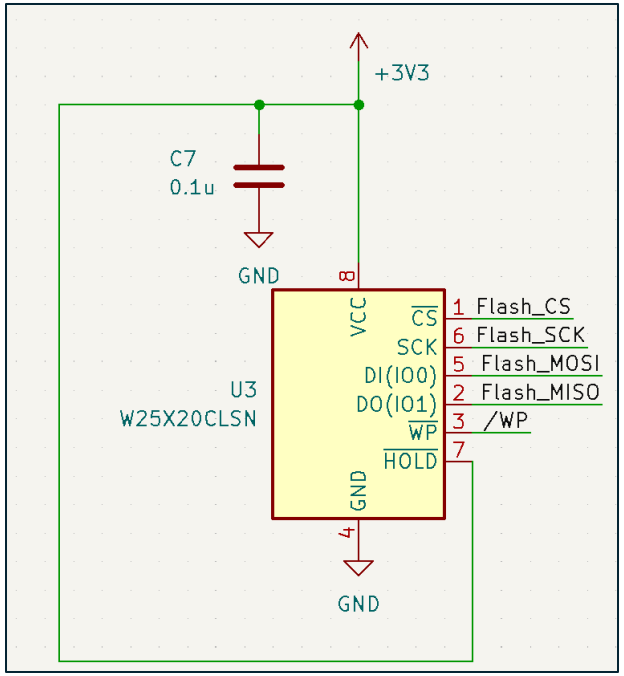
- VDD and decoupling capacitors
- Push Button with a Pull-Up Resistor for Reset
- Boot0 pulled low for normal booting

VIRGINIA TECH

PCB Schematic: Preamp and Flash Memory



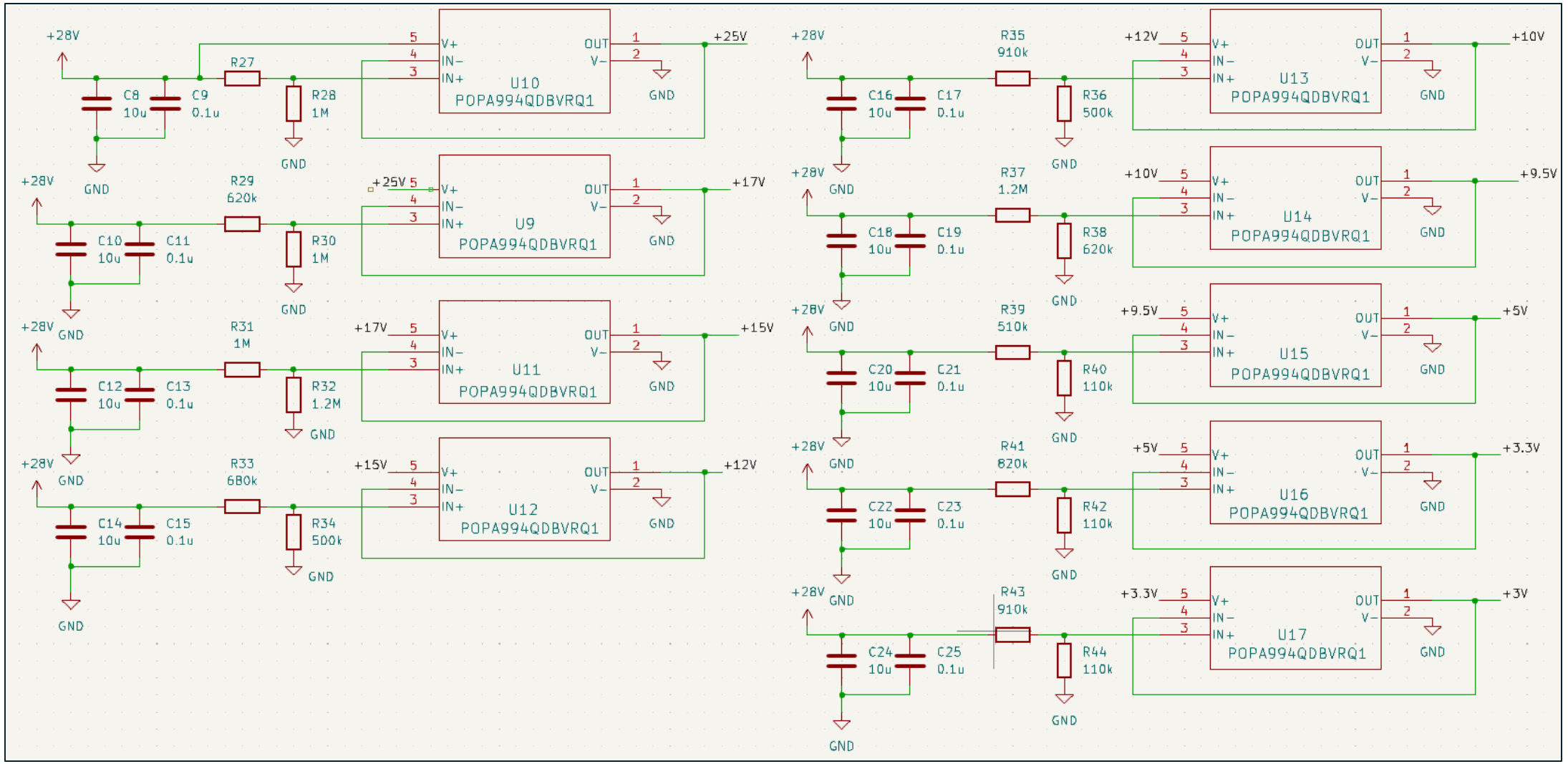
- Amplifier with a Gain of 2
- Positive input is connected to a 2x1 MUX, which is connected to a pad, and the CCD output
- The select pin for the MUX is connected to a GPIO pin on the MCU



- 1Gbit Flash Memory
- Pins connected to the second SPI channel on the MCU

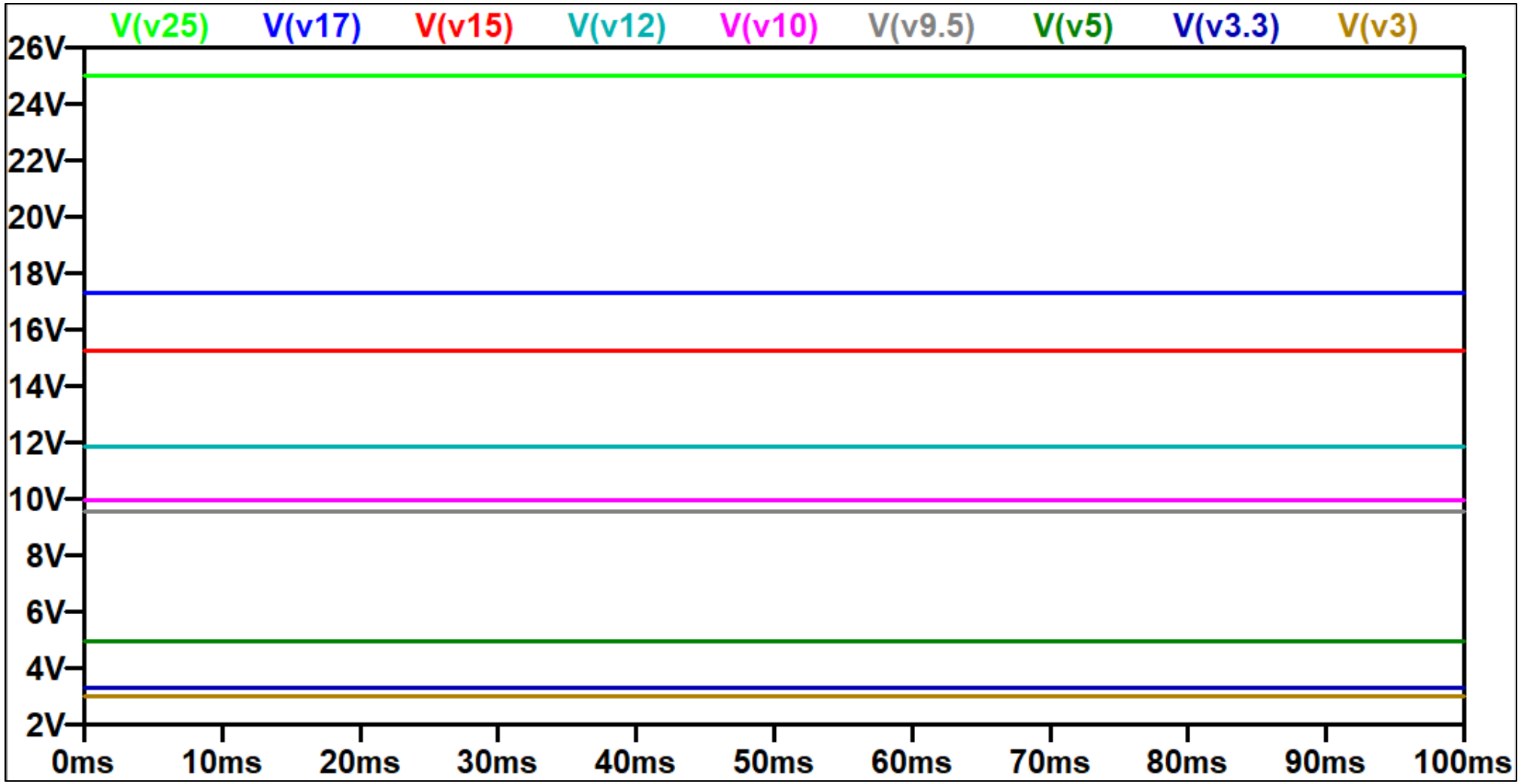
VIRGINIA TECH

PCB Schematic: Power Regulation (Voltage Dividers)



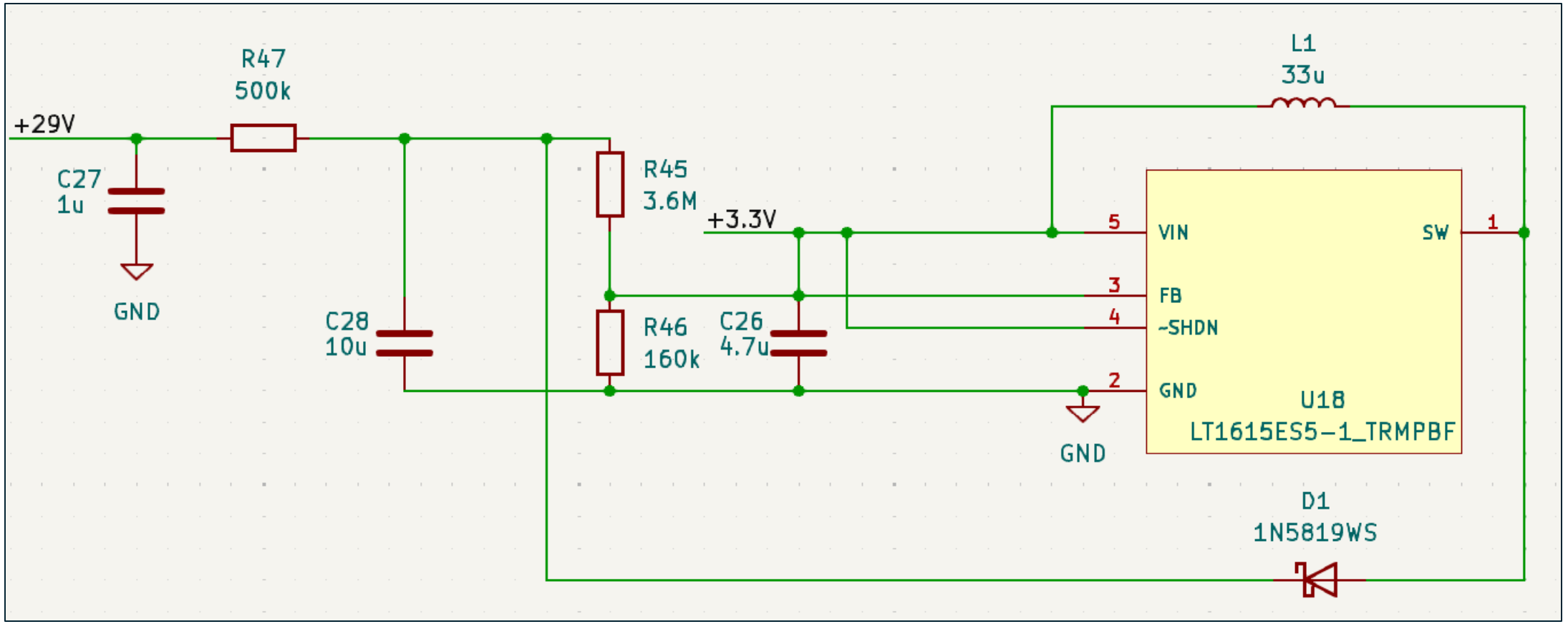
VIRGINIA TECH

Hardware Simulation: Voltage Dividers



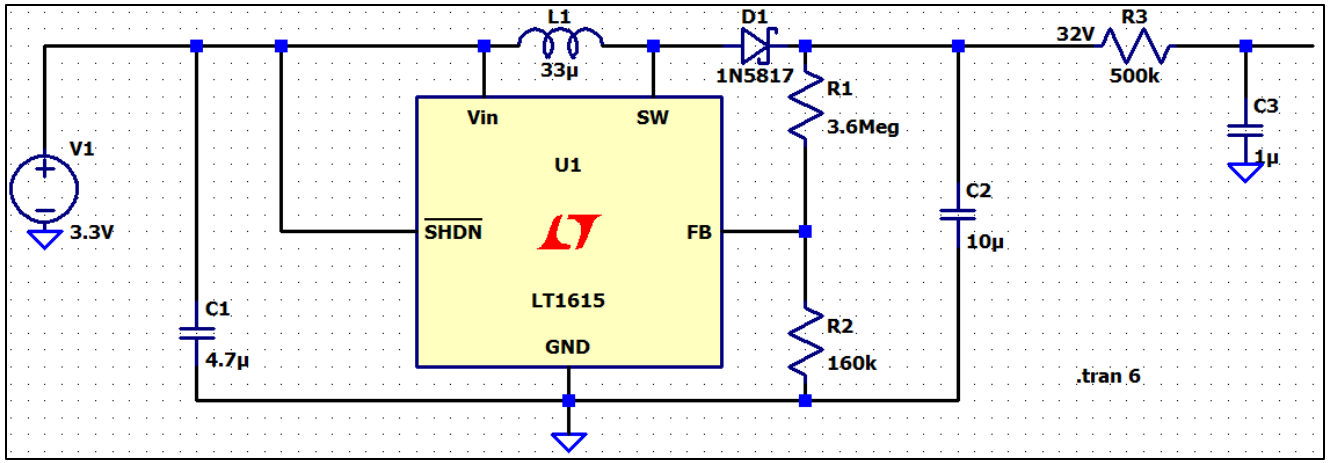
VIRGINIA TECH

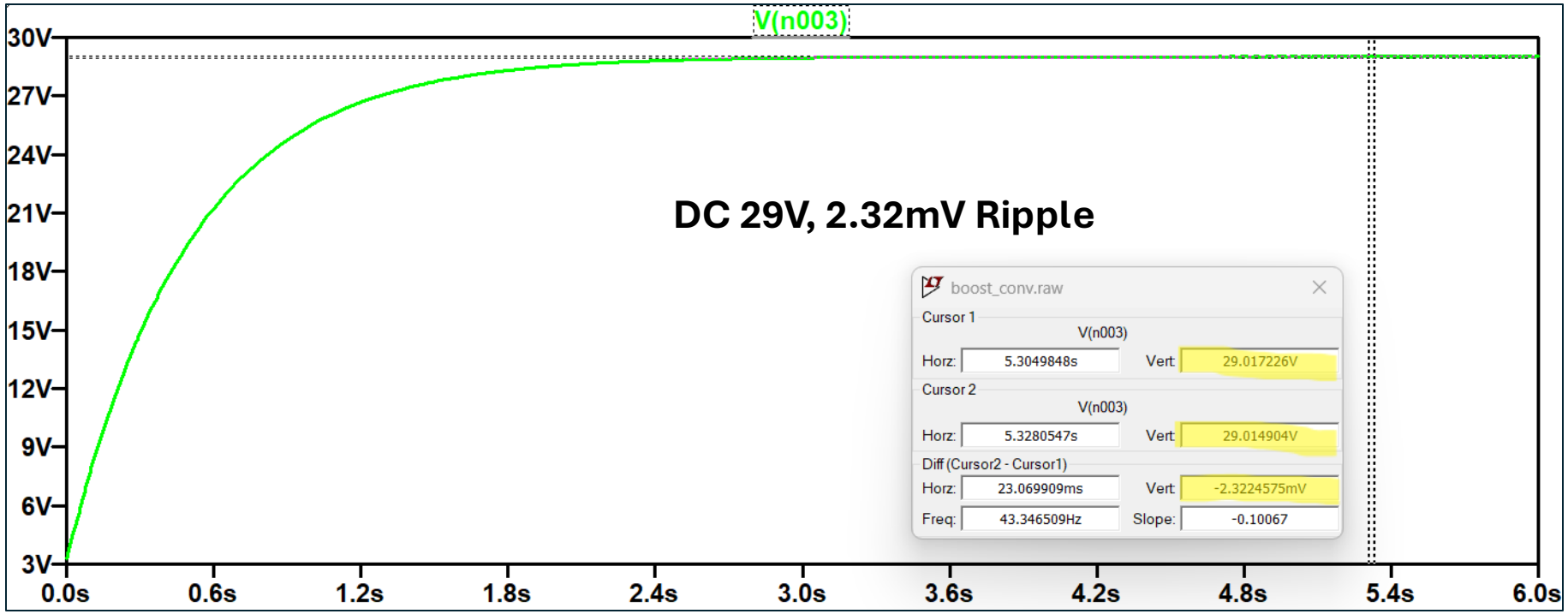
PCB Schematic: Power Regulation (Boost Converter)



VIRGINIA TECH

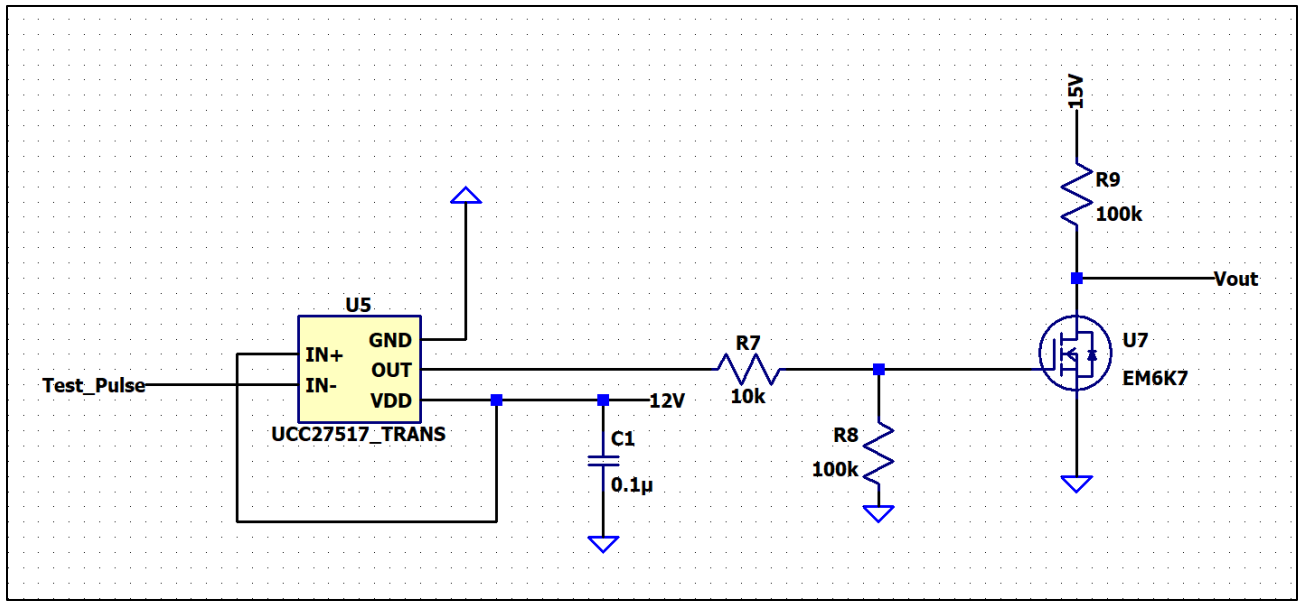
Hardware Simulation: Boost Converter to 29V

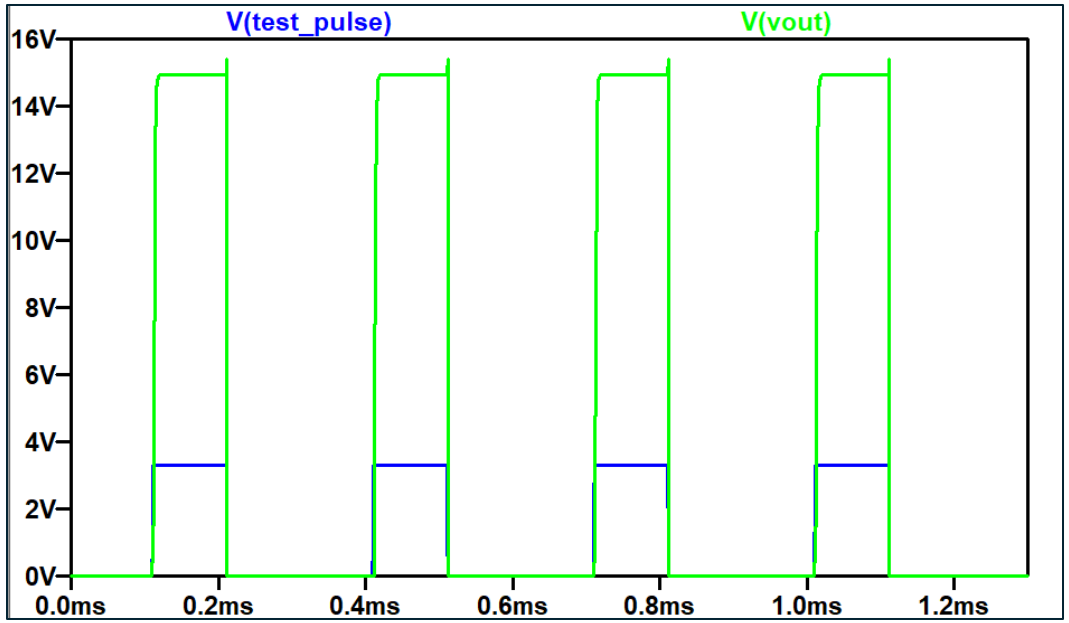




VIRGINIA TECH

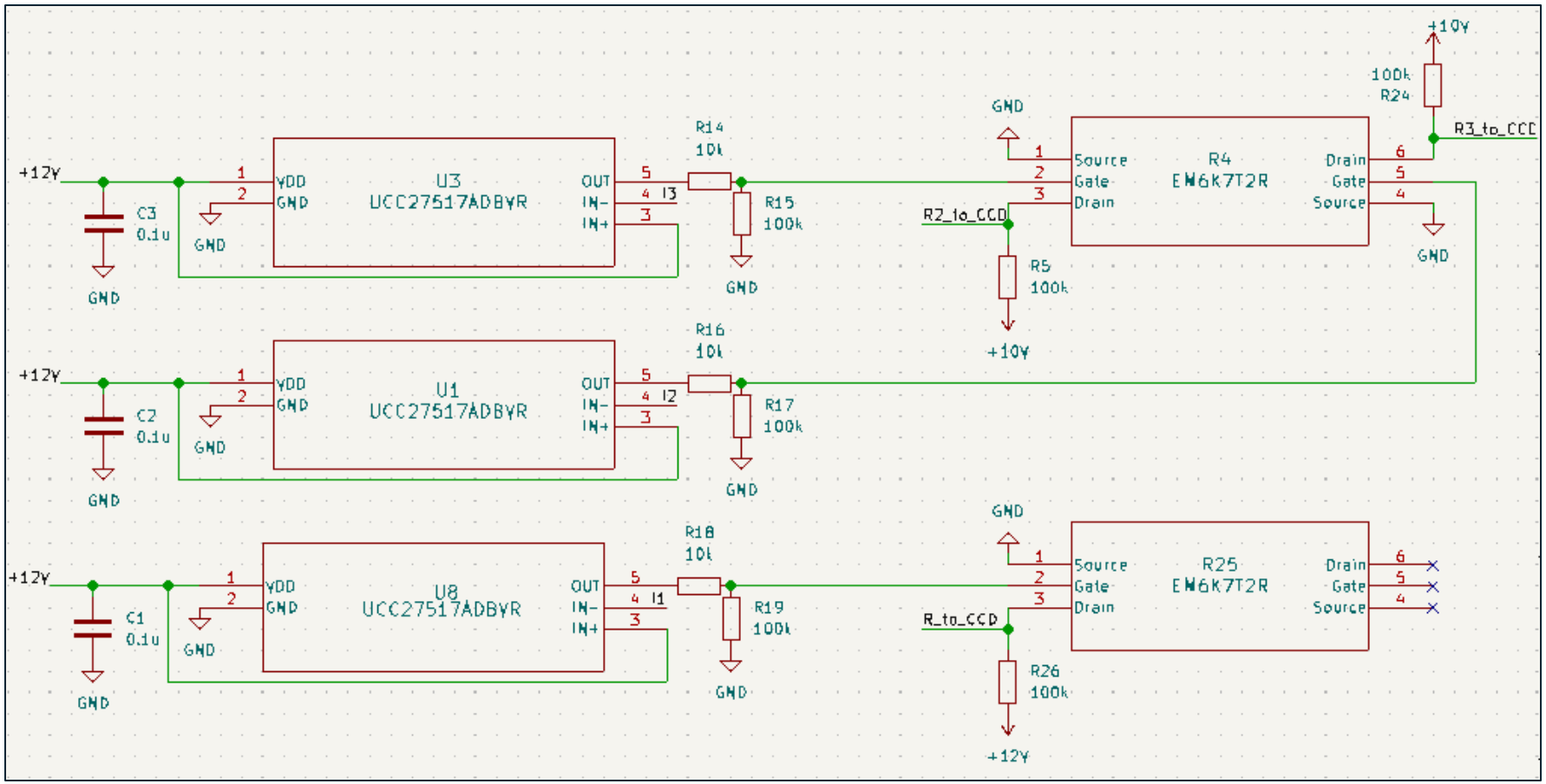
PCB Schematic: MOSFET Switching (One Switch)





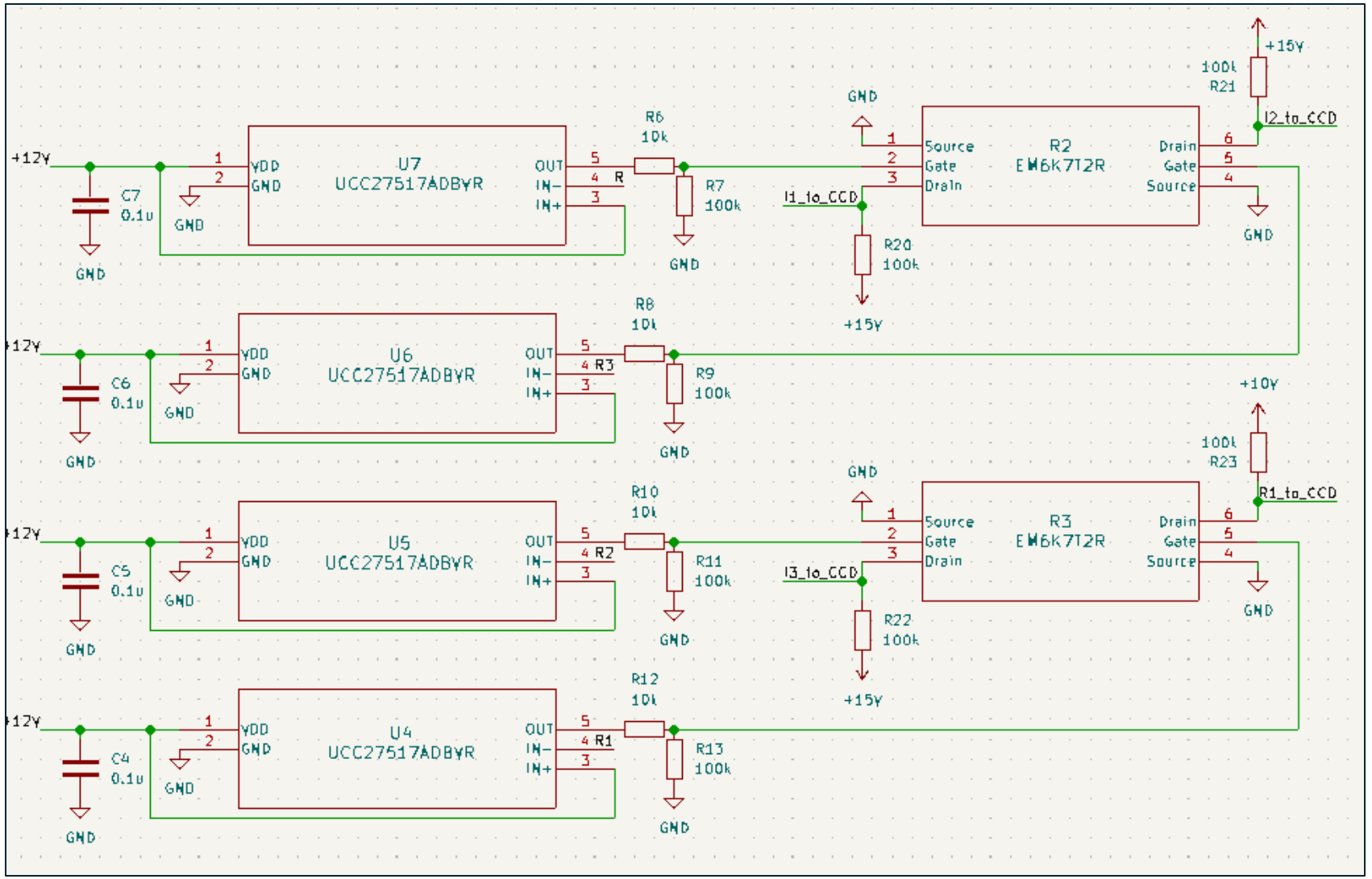
VIRGINIA TECH

PCB Schematic: MOSFET Switching (Section 1)



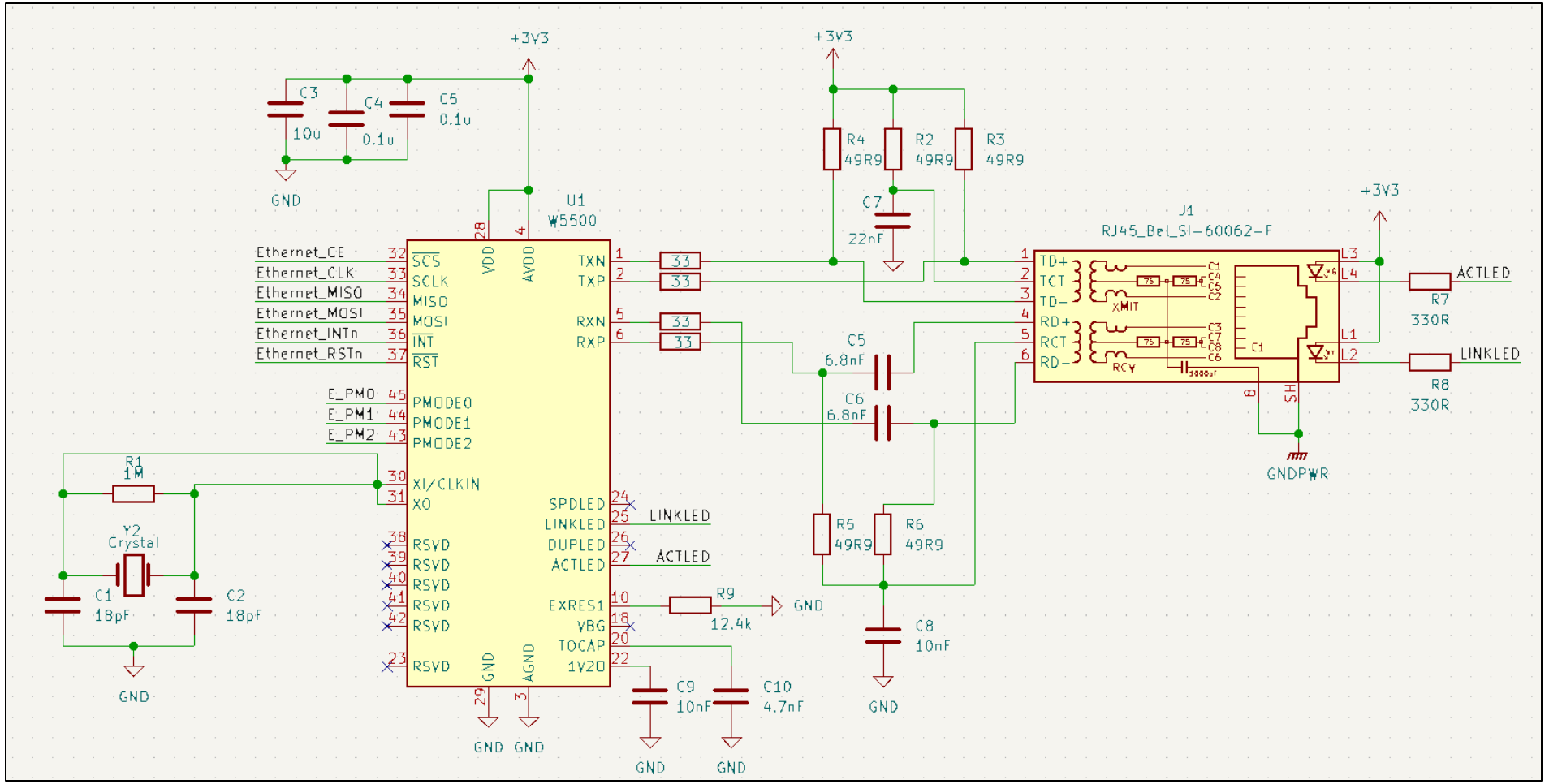
VIRGINIA TECH

PCB Schematic: MOSFET Switching (Section 2)



VIRGINIA TECH

PCB Schematic: Ethernet Module



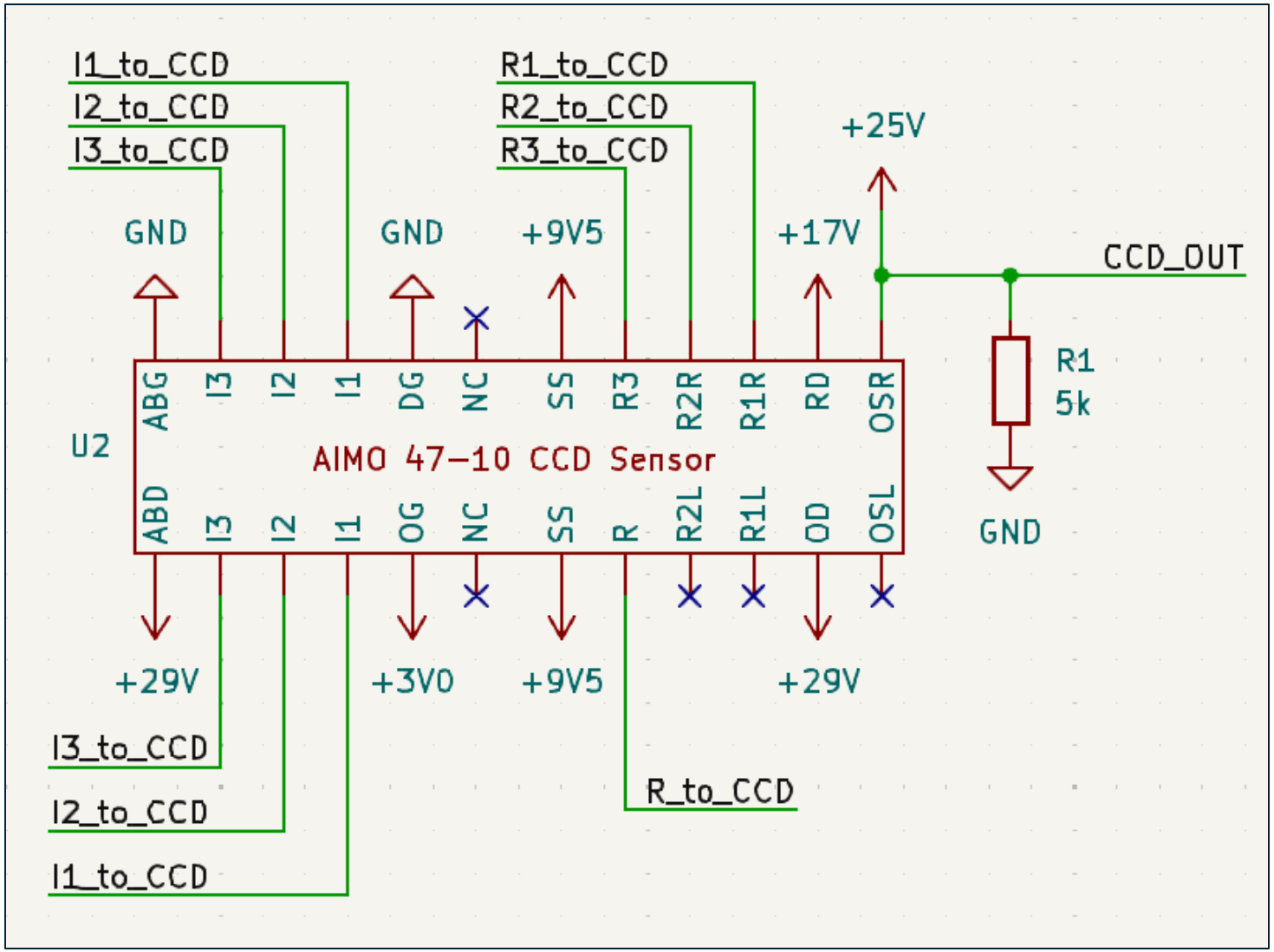
Connections to MCU are labeled on the left side

The RJ45 connector has integrated magnetics

The crystal oscillator in the bottom left is 25MHz

VIRGINIA TECH

PCB Schematic: CCD Sensor

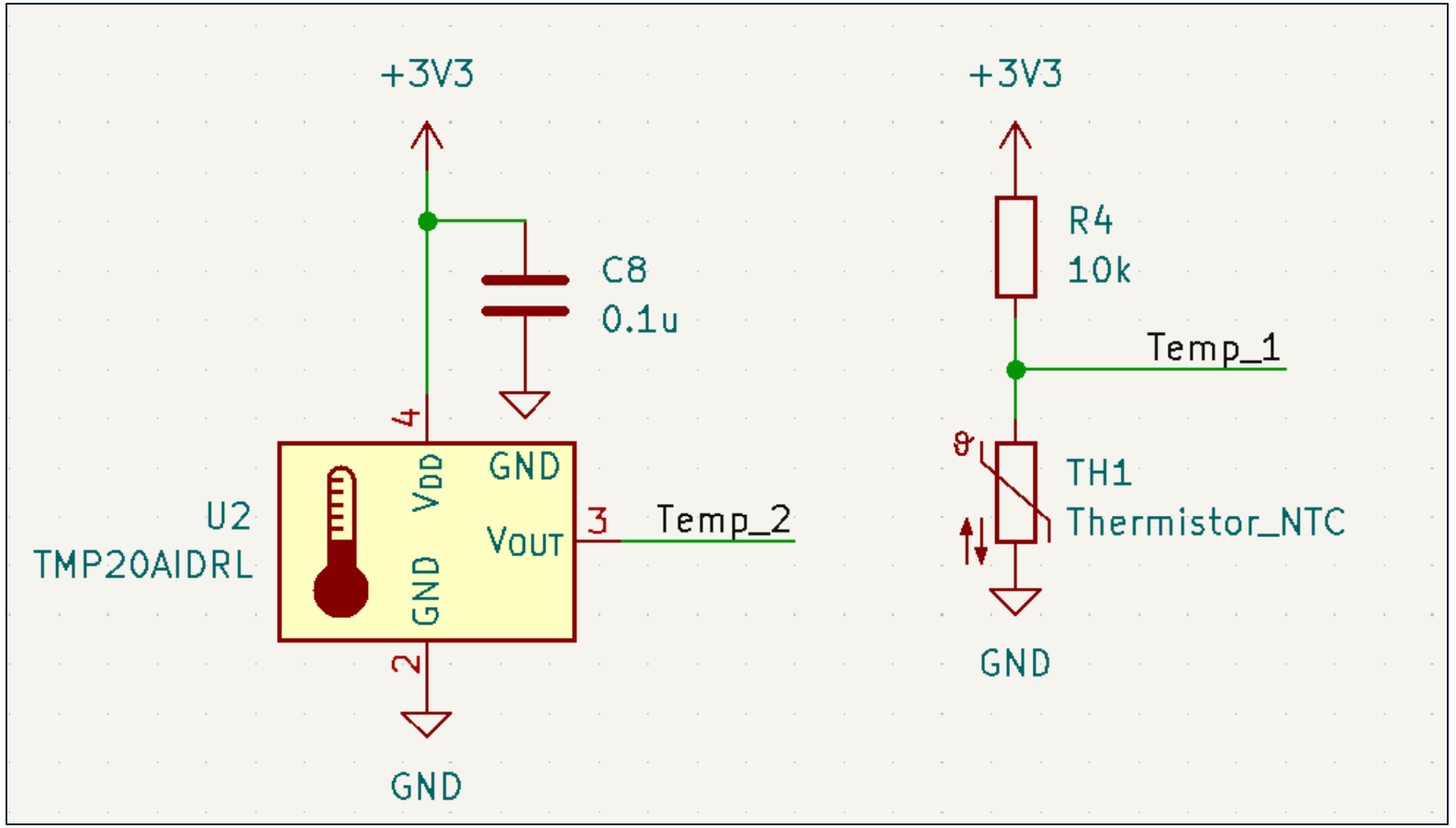


Signal names come from switching outputs created on slides **23** and **24**, and from the MCU schematic on slide **18**

Voltage values come from the voltage regulation outputs from slides **19** and **21**

VIRGINIA TECH

PCB Schematic: Thermal Sensors



Temp_1: Environment Temperature Measurement with Thermistor

Temp_2: Board Temperature Measurement with SMD Component

VIRGINIA TECH

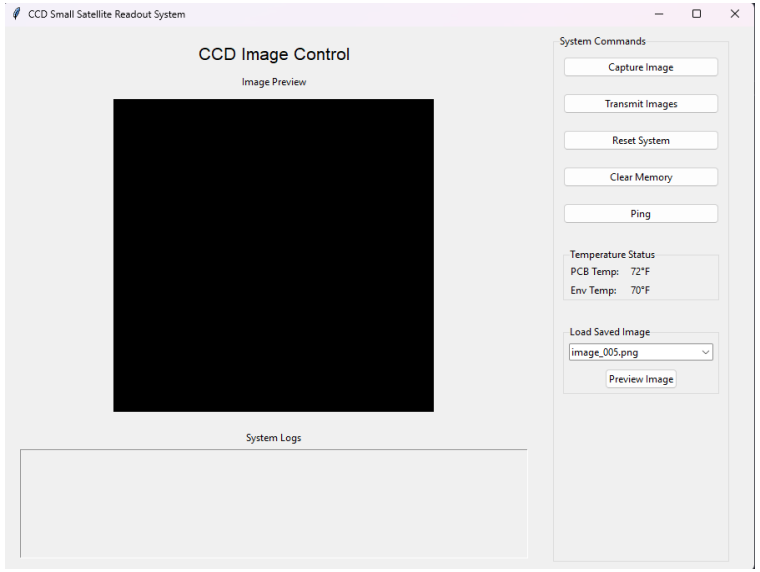
Cost Table

Item	Purpose	Quantity	Unit Price	Total Price
STM32L073CZT6	MCU	1	$5.03	$5.03
LT6200	Low-Noise ADC Preamplifier	1	$6.33	$6.33
W5500 Chip	Used to transmit data from the MCU through SPI to an ethernet cable	1	$4.99	$4.99
EM6K7	MOSFETS used for voltage switches	4	$0.58	$2.32
UCC27517	MOSFET Gate Drivers	7	$1.16	$8.12
TMP20AIDRLR	SMD Temperature Sensor	1	$0.97	$0.97
OPA2994	36V Rail-to-Rail Op-Amps	9	$2.35	$21.15
W25N01GVZEIG	1 Gbit Flash Memory	1	$3.10	$3.10
PCBs	Physical PCBs	5	~$8	~$40
LT1615	Boost Converter Switch	1	$7.40	$7.40
RJ45 Connector	Ethernet connector with integrated magnetics	1	$7.15	$7.15
		Total		**$101.57**

Software Subsystems

Subsystem Overview

- GUI
  - Emulation of satellite interaction with the CCD



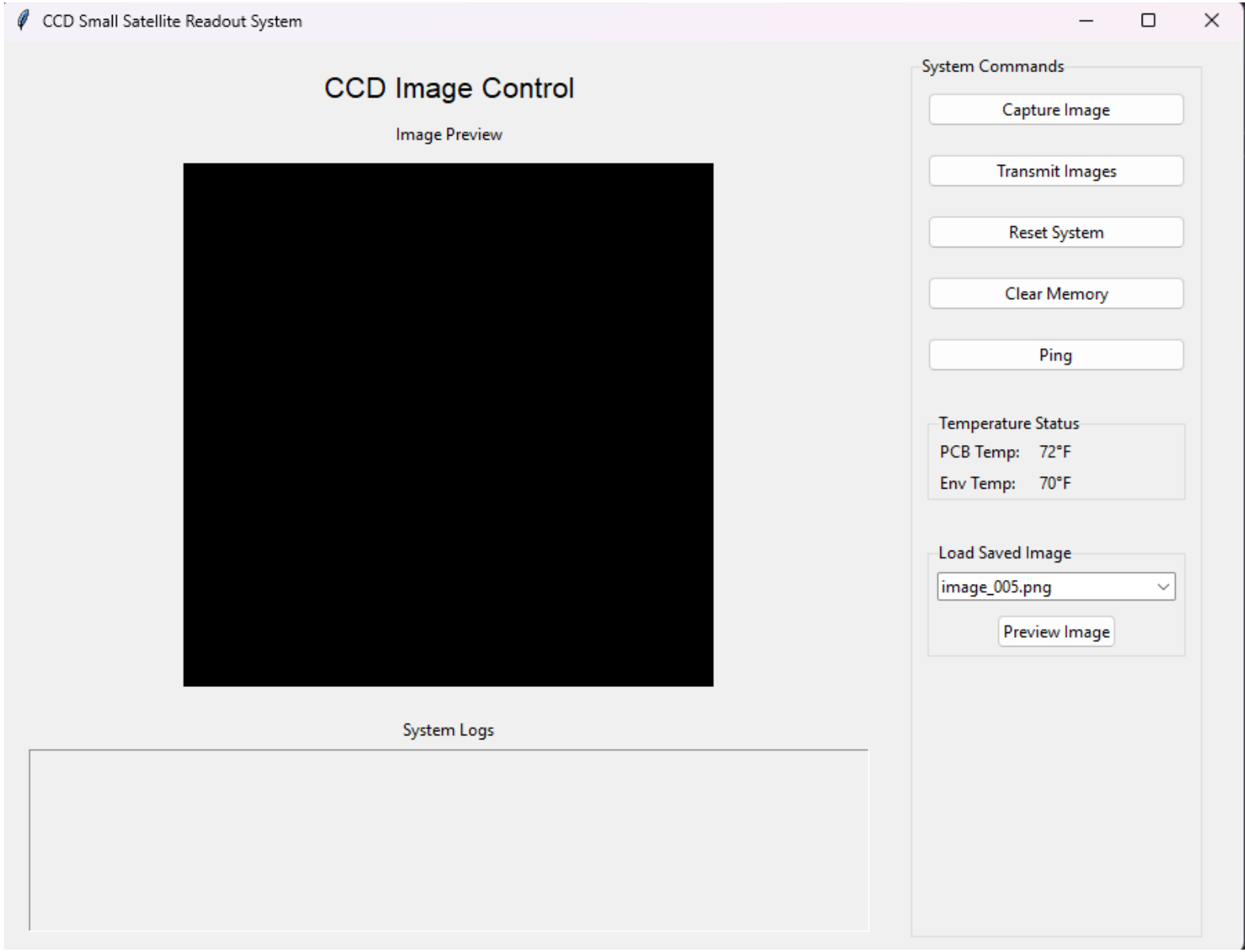
- Ethernet
  - Mode of communication and data transfer
  - W5500 Ethernet Chip with RJ45

- MCU
  - Microcontroller using Micro python to facilitate protocol
  - STM32L073CZT6

VIRGINIA TECH

GUI functionality

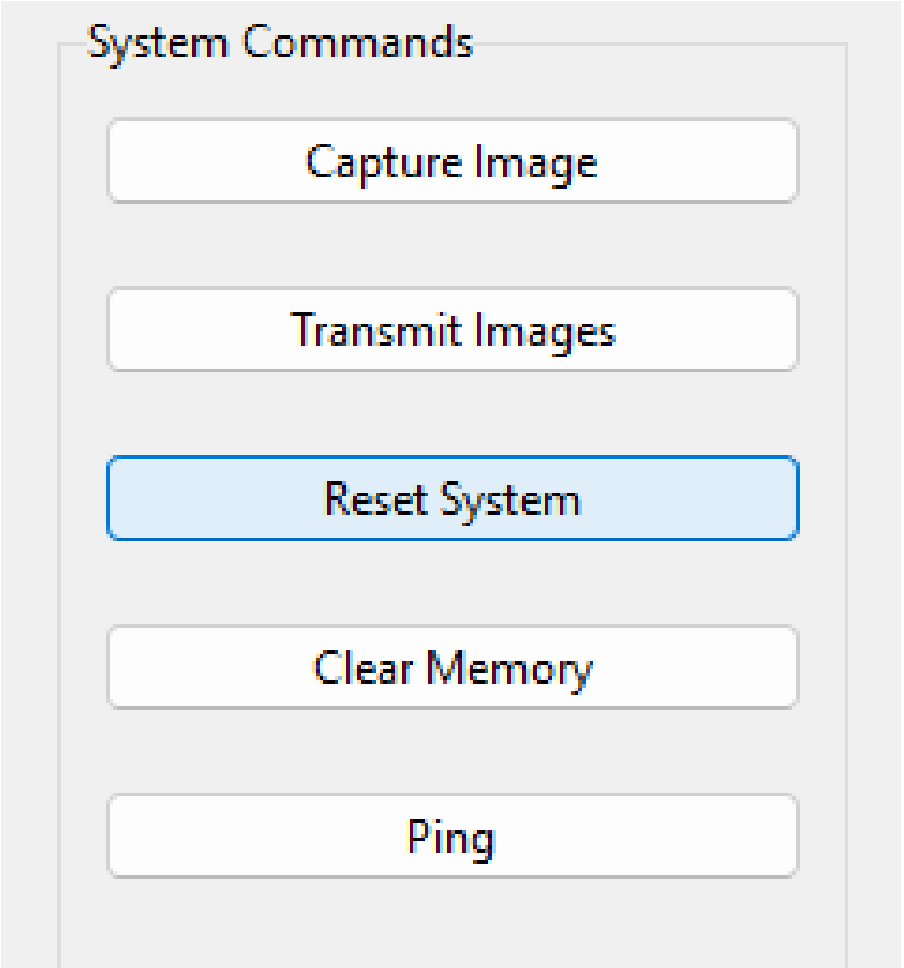
- Image portrayal
  - Section where greyscale image is shown
- Command Buttons
  - Buttons used for sending commands
- Logging Interface
  - Feedback logging and system state logging
- Temperature Readout
  - Constantly reads out PCB temperature and environment temperature



VIRGINIA TECH

Self-Imposed Commands

- Capture Image
  - Store image data and headers from ccd sensor into external flash memory
- Transmit Image(s)
  - Transmits images stored in external flash memory through ethernet bus
- Reset System
  - Clears memory, resets system to initial state
- Clear Memory
  - Clears Flash memory without resetting full system
- Ping
  - Tests if PCB is alive and connected through ethernet



VIRGINIA TECH

Command Packet Format

- Command ID (1 byte)
  - Capture Image = 0x01
  - Transmit Images = 0x02
  - Reset System = 0x03
  - Clear Memory = 0x04
  - Ping = 0x05
- Reserved (7 bytes)
  - Set to 8 bytes for future integration and consistency

Logging Packet Format

- Message Type (1 byte)
  - Info = 0x10
  - Warning = 0x11
  - Error = 0x12
  - PCB Temperature = 0x13
  - Environment Temperature = 0x14
- Reserved (1 byte)
- Length (1 byte)
  - Length of text in bytes
- ASCII Text (n bytes)

Image Data Packet Format

- Packet Type (1 byte)
  - Image transfer = 0x20
- Image ID (4 bytes)
  - This lets satellite know which image this chunk belongs to
- Chunk Offset (4 bytes)
  - Indicates the byte position in the image that the chunk starts from
- Payload Length (n bytes)
  - Total Length of payload
- Checksum (4 bytes)
- Image data (n bytes)

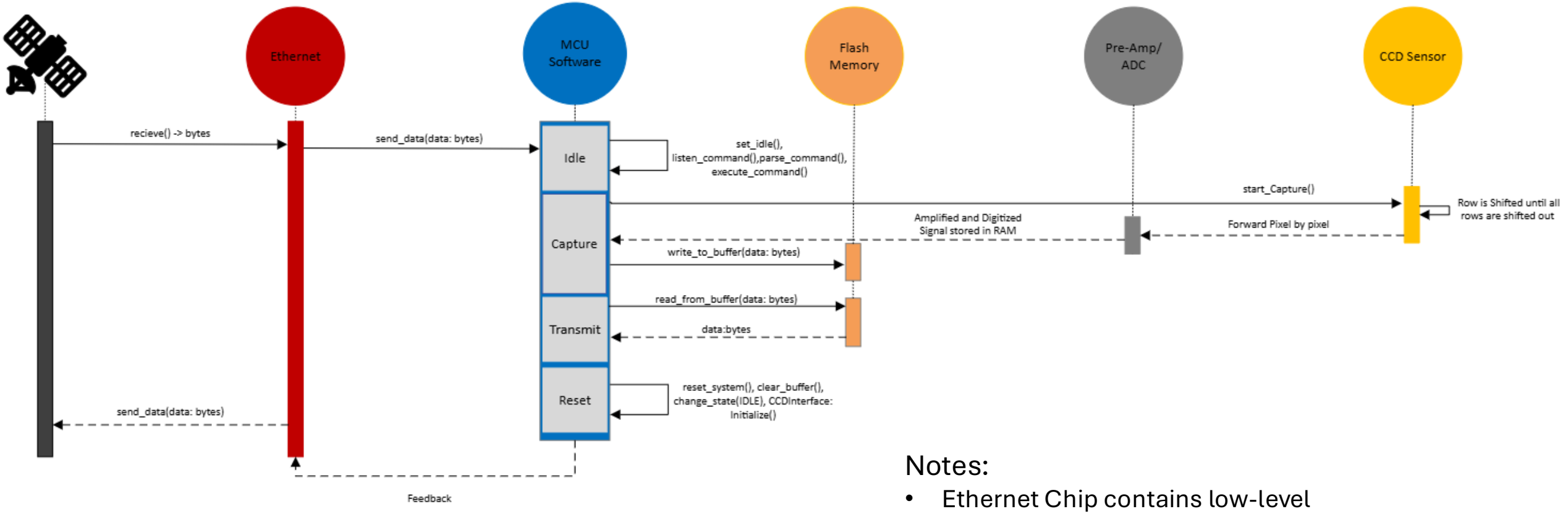
Data Formats

- Metadata (16 bytes)
  - Image ID
  - Image Size (Bytes)
  - Checksum
  - Reserved
- Pixel format
  - 16-bit pixel (2 bytes)
  - 4 LSB's are Zero Padded

XXXXXXXXXXXX0000

VIRGINIA TECH

Software Subsystem Sequencing Diagram

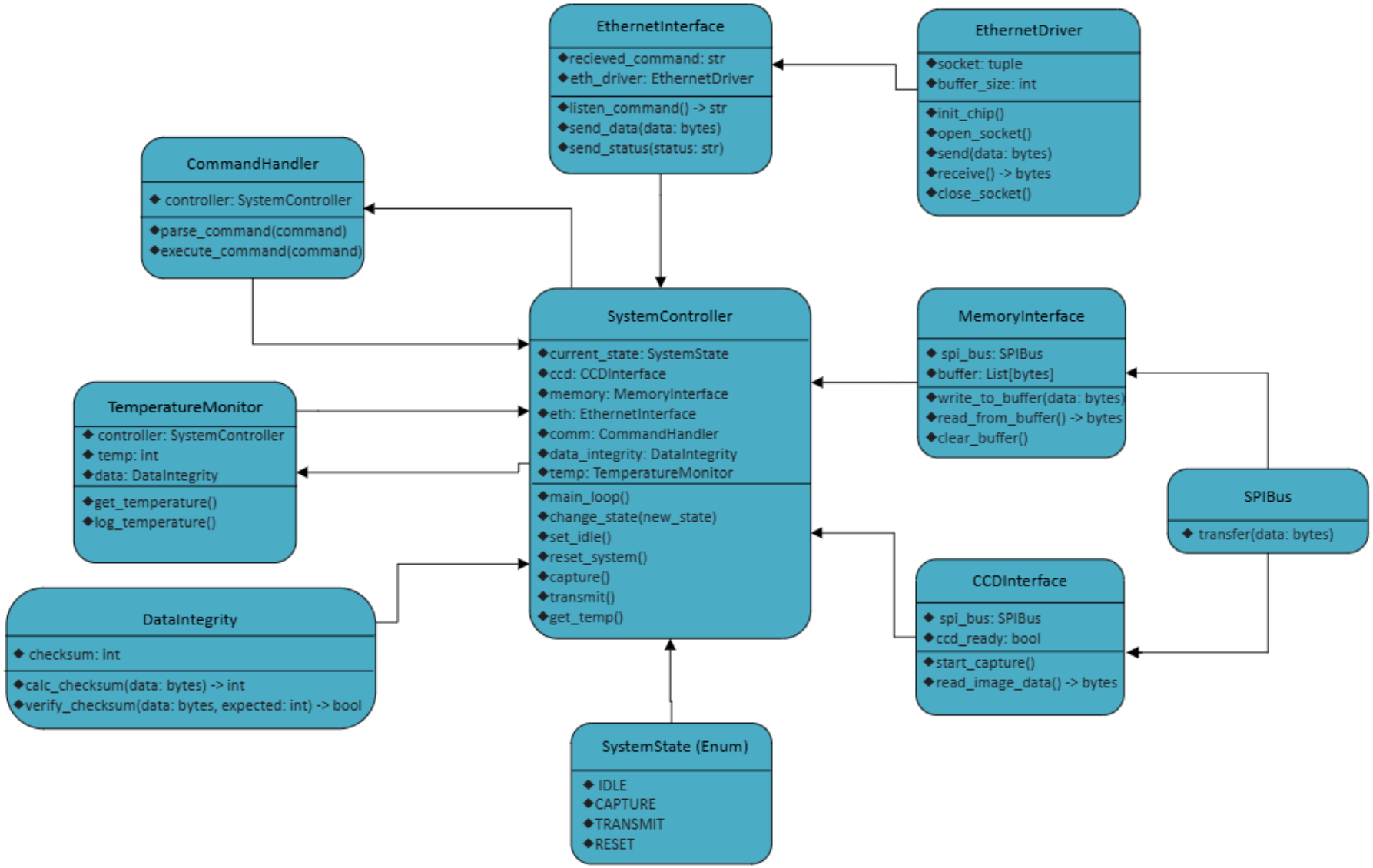


Notes:

- Ethernet Chip contains low-level drivers while MCU contains higher level Networking implementations
- Satellite represents Run script/ client script on satellite

VIRGINIA TECH

Software Class Diagram



Notes:

- Modular Design
- System Controller class main software interface
- Low level Ethernet firmware lives on ethernet chip while TCP/IP stack or higher-level networking firmware exists on MCU

VIRGINIA TECH

ICD Adhering

To Be Provided:

- Run Script
  - Bash Script that runs instance of camera module
    - Can be executed in BASH terminal or Systemd service
- Disk cleanup script
  - Bash Script that manages cleaning up image files on local Pleiades storage
- Systemd file
  - Used by Systemd for running the camera instance as a Linux service
    - Currently running on Ubuntu 22.04
- Update crontab to perform disk cleanup
  - Task scheduling for the disk cleanup script need to be updated using crontab
  - Images are saved to local storage as uncompressed Portable Network Graphics

./CCD_Run –m $mac_address –o $output_path

Subsystem Testing

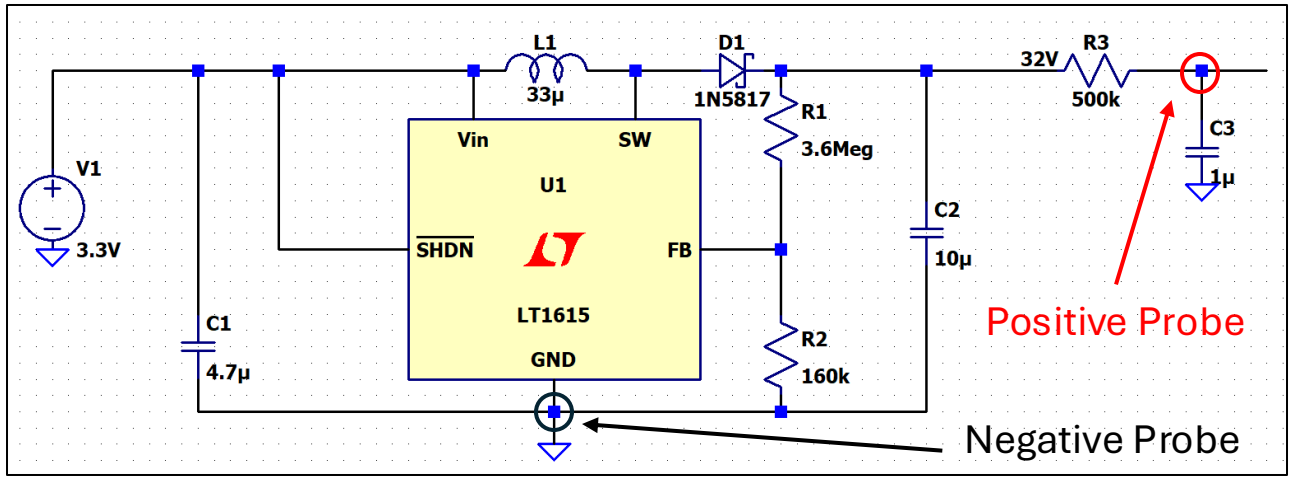
Voltage Verification Testing

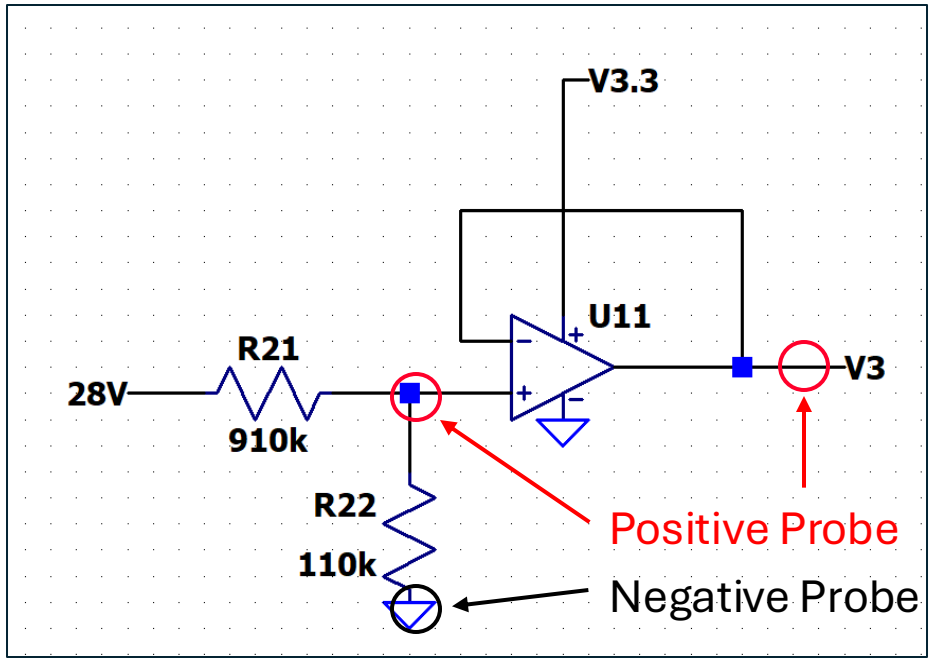
Required Materials:

- 28V Board Power
- PCB
- DMM or Oscilloscope

Testing Procedure:

1. Once the board is plugged into the 28V power supply, we'll use a multimeter to test the output voltage levels of the boost converter and each voltage divider
2. Make sure that the output of the voltage divider and voltage buffer are the same





VIRGINIA TECH

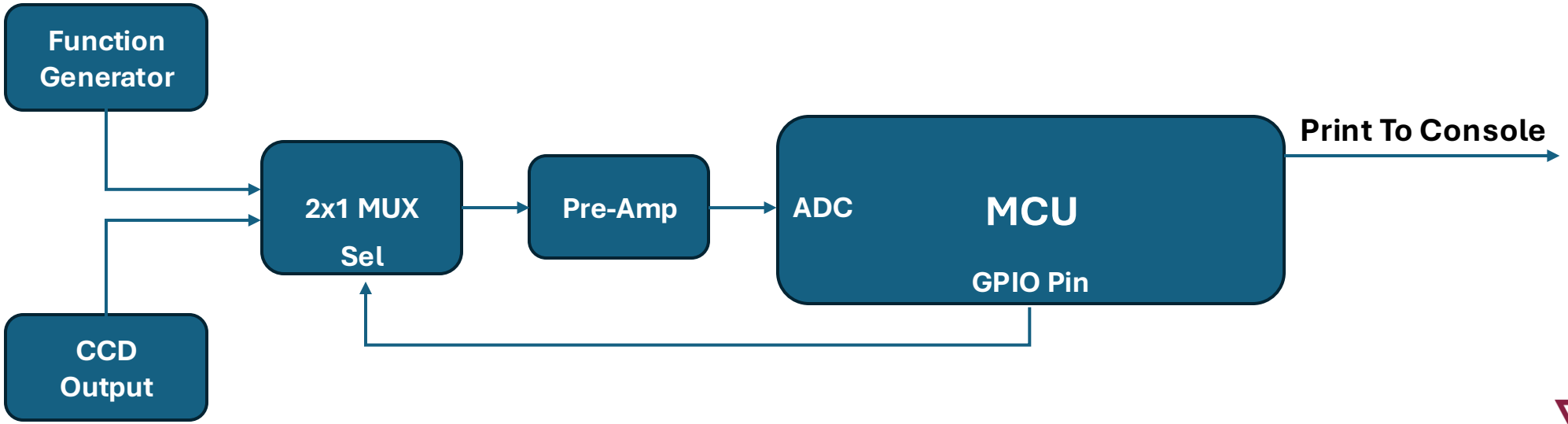
Bench Waveform Testing

Required Materials:

- 28V Board Power
- PCB
- Function/Wave Generator
- Laptop to Program/Debug MCU
- IDE for Programming/Console Output

Testing Procedure:

1. Apply voltage through function generator
2. Signal goes through MUX, to Pre-Amp, to ADC
3. Digital signal is printed to the console



VIRGINIA TECH

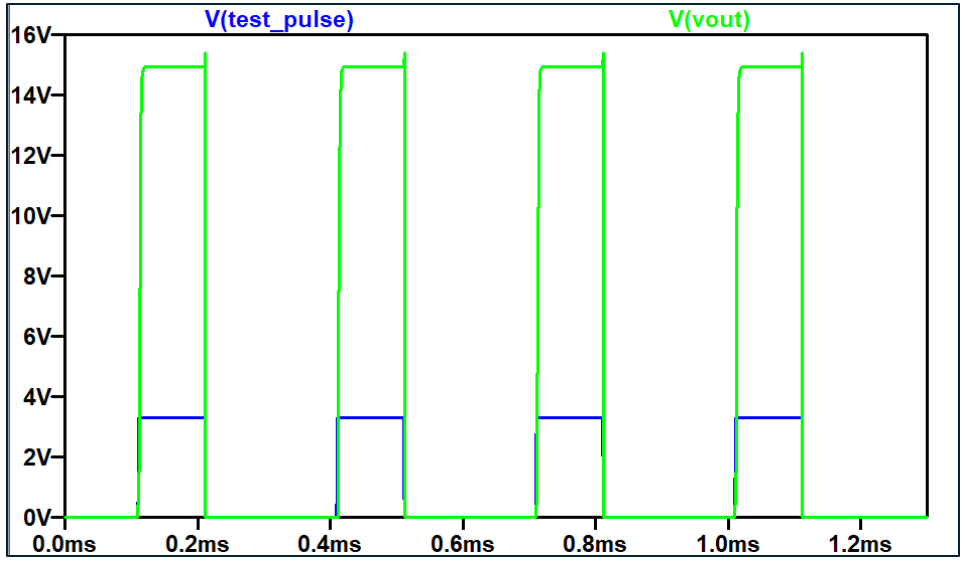
Switching Verification and Pin Observation Testing

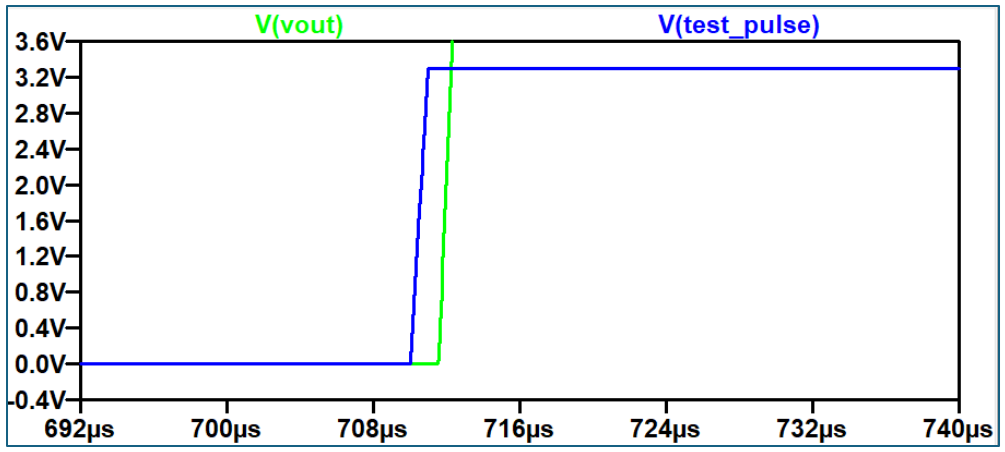
Required Materials:

- 28V Board Power
- PCB
- Oscilloscope
- Software to control the timing outputs for the CCD sensor

Testing Procedure:

1. Flash the development board with the software to control the timing outputs for the CCD sensor
2. With the oscilloscope, probe the input pins of the CCD sensor.
3. Run the program and see if the timing diagrams for the pin matches up with the planned-out timing scheme





VIRGINIA TECH

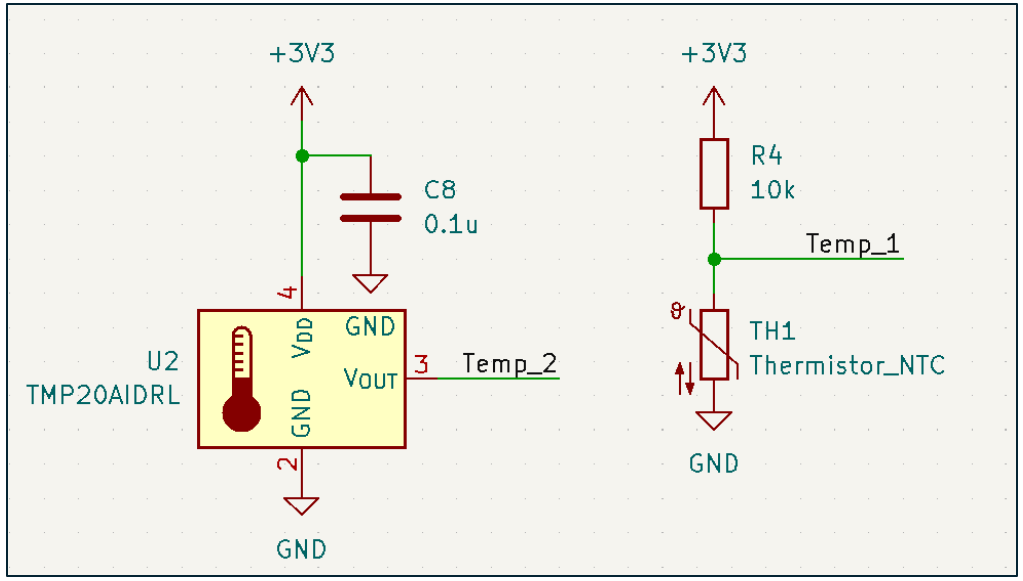
Bench Temperature Monitoring

Required Materials:

- 28V Board Power
- PCB
- Laptop to Program/Debug MCU
- IDE for Programming/Console Output
- Thermometer

Testing Procedure

1. Read the temperature sensor voltages through the MCU's ADC
2. Convert those voltages to temperatures in Celsius using the Steinhart-Hart equation
3. Compare to the thermometer's room reading



Steinhart-Hart Equation

$$\frac{1}{T} = A + B\ln(R) + C[\ln(R)]^3$$

VIRGINIA TECH

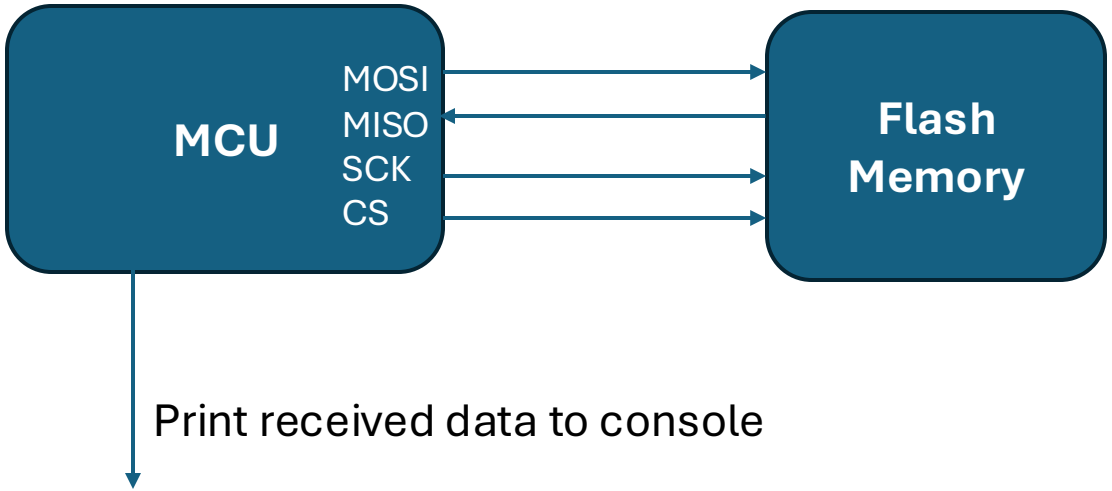
Data Store/Receive Testing

Required Materials:

- 28V Board Power
- PCB
- IDE for Programming/Console Output

Testing Procedure:

1. Send data from the MCU through SPI to the flash chip
2. Retrieve the sent data from the flash module and print to console to verify it's unchanged



VIRGINIA TECH

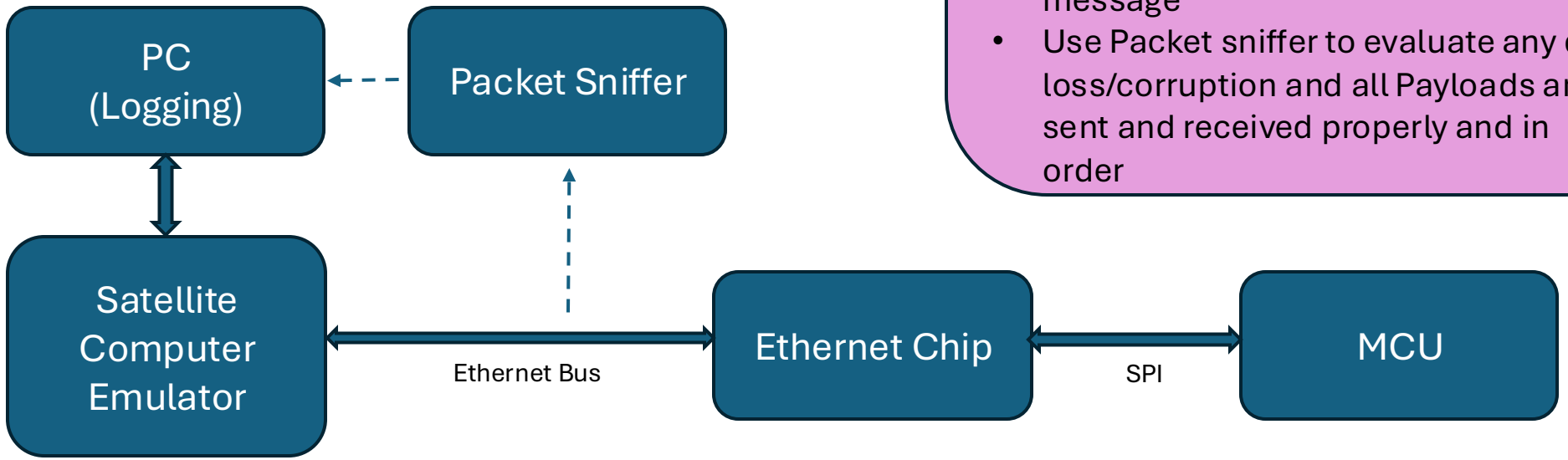
Testing Data Transfer and GUI Operations

Required Materials:

- Packet Sniffer (Wireshark)
- 28 V Power
- Completed GUI with satellite emulator functionality)
- Completed PCB

Testing Procedure:

- Send Custom UDP Payload through ethernet bus to W5500
- Ethernet chip communicates correct command to MCU and MCU responds with correct logging for chosen command to GUI
- Logging on GUI should show logged message
- Use Packet sniffer to evaluate any data loss/corruption and all Payloads are sent and received properly and in order



VIRGINIA TECH

System Testing

Noise Level Testing Diagram

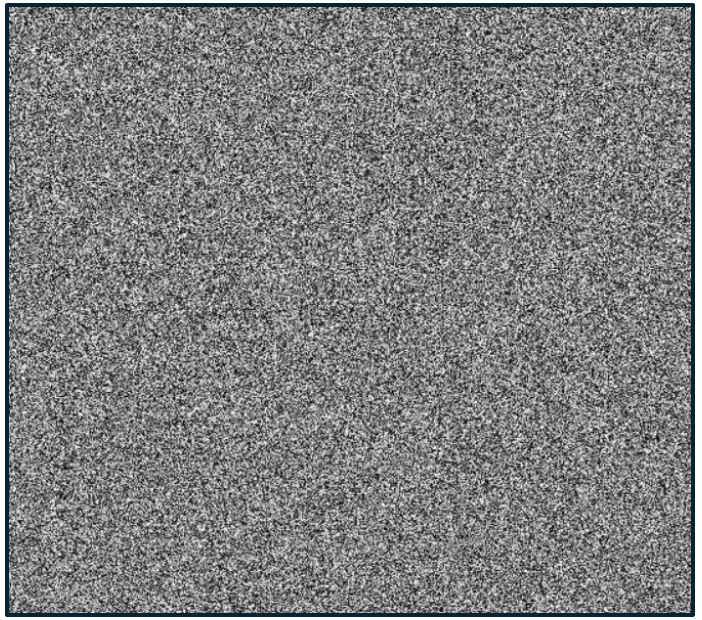
Noise Level Testing:

Required Materials:

- 28 V Power
- Grounded CCD Pin Slots
- Completed GUI with satellite emulator functionality

Testing Procedure:

- Ground the PCB's CCD pins connections
- Capture and receive an image through the GUI
- Take the standard deviation of each pixel's value (looking for less than 3 electrons of read noise)



Grounded Image Sample

VIRGINIA TECH

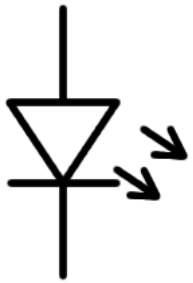
Bench Testing

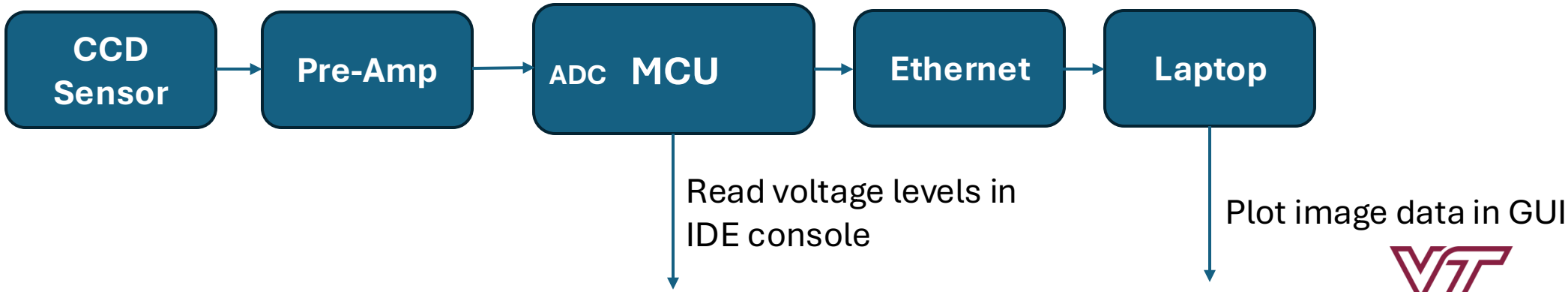
Required Materials:

- LED
- 28V Board Power
- PCB
- Laptop
- IDE for Programming and
- Ethernet Cable
- Completed GUI with satellite emulator functionality

Testing Procedure:

- Turn on the LED in front of the CCD sensor
- Press “Take Image” on GUI
- Validate if the voltage levels are as expected through the IDE console
- Press “Receive Image/Buffer” on GUI
- Validate the accuracy of the image posted in the GUI





VIRGINIA TECH

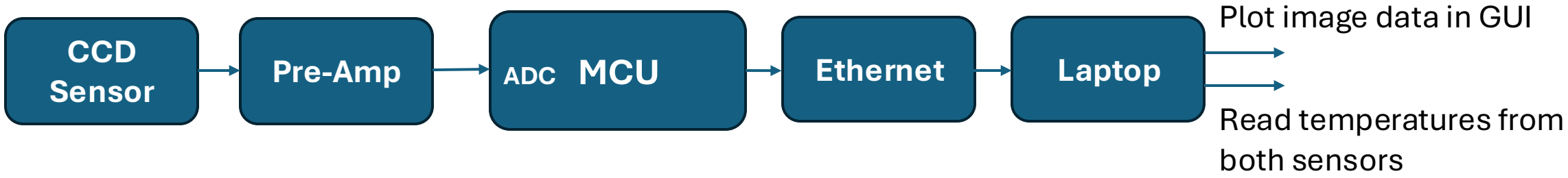
TVAC Testing

Required Materials:

- PCB
- Thermal Vacuum Chamber
- 28V Power
- Ethernet Cable
- Completed GUI with satellite emulator functionality

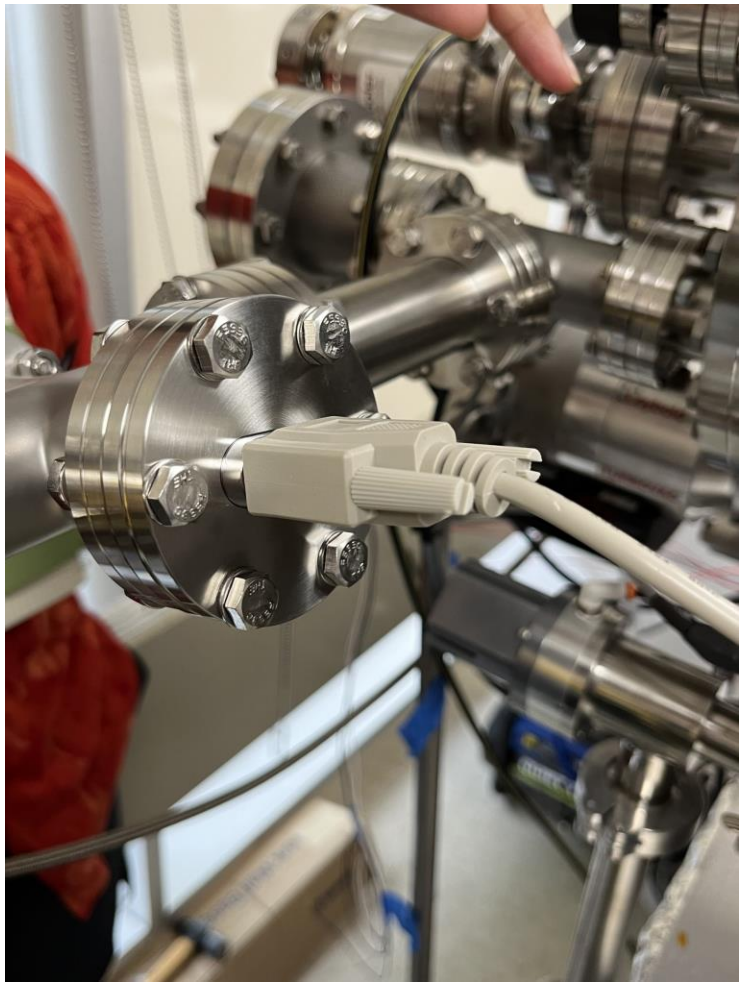
Testing Procedure:

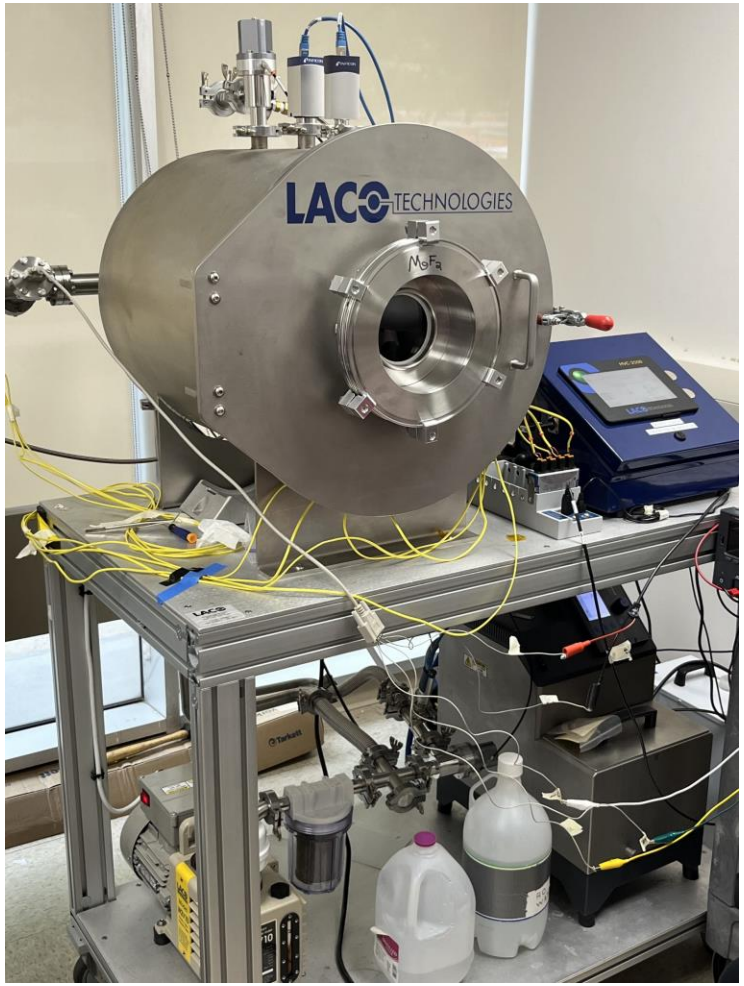
- Bakeout PCB
- Operate vacuum within operating temperatures (-40C to 85C)
- Test taking images inside the TVAC chamber
- Read temperature from both sensors



VIRGINIA TECH

Thermal Vacuum Chamber





VIRGINIA TECH

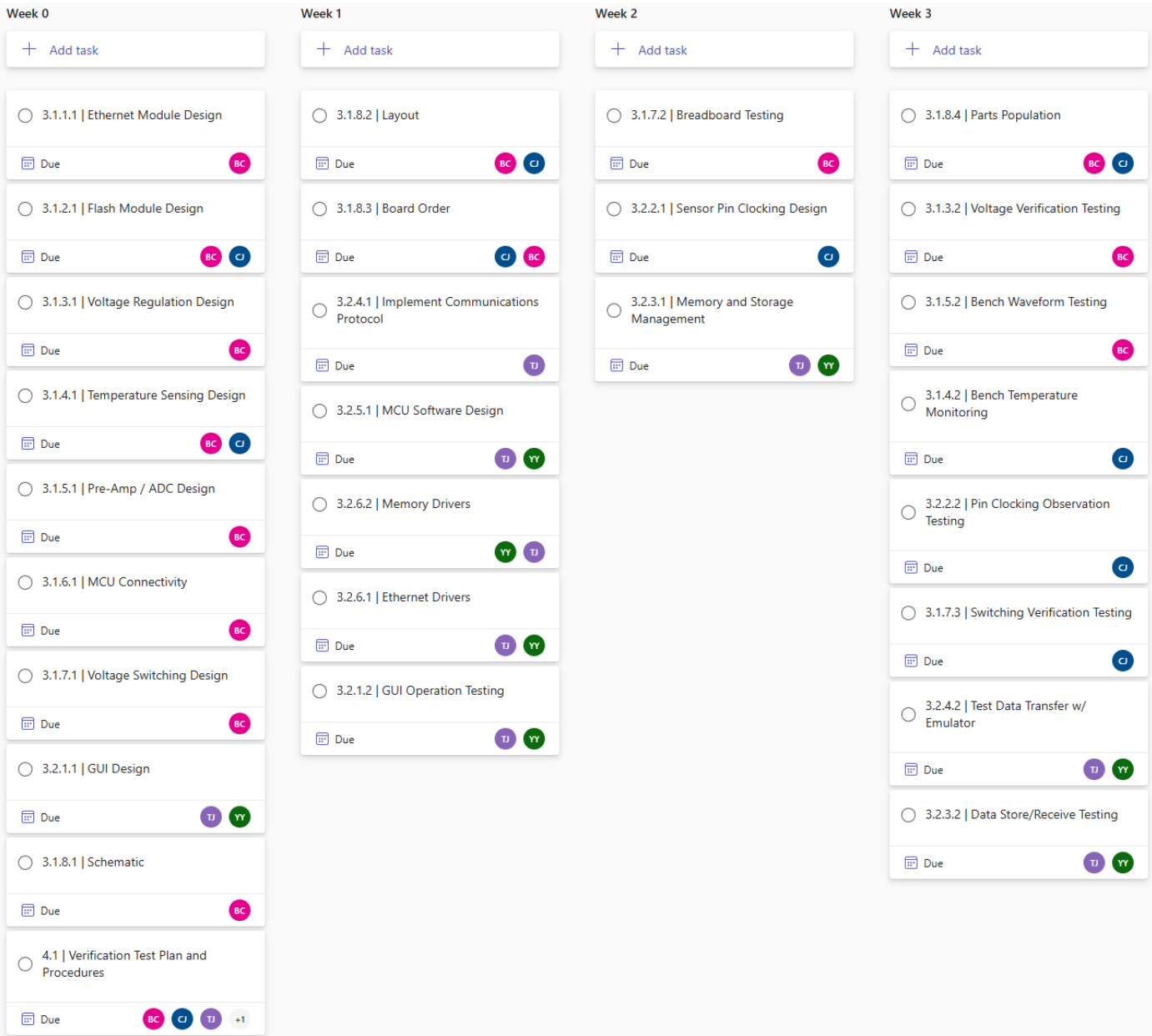
Project Schedule and Risks

Updated Project Schedule

	Task Name	Start	Finish	Predecessors	Duration
1	1 Project Management	Sat 2/1/25	Wed 11/12/2		40.8 wks
2	1.1 Cost Table	Tue 2/18/25	Fri 3/28/25		29 days
3	1.2 Roles Definition	Sat 2/1/25	Wed 2/5/25		4 days
4	1.3 Schedule	Sat 2/1/25	Wed 4/16/25		54 days
5	1.4 Risk Matrix	Mon 2/17/25	Sun 3/30/25		31 days
6	2 Systems Engineering	Sun 2/16/25	Wed 4/30/25		54 days
7	2.1 Requirements Definiton	Sun 2/16/25	Fri 2/28/25		11 days
8	2.2 External Interface Definition	Mon 3/3/25	Wed 3/26/25	7	18 days
9	2.3 Preliminary Design Review	Wed 2/19/25	Wed 4/2/25	2,3,4,5,7,8	31 days
10	2.4 Critical Design Review	Wed 4/2/25	Wed 4/30/25	9,13	21 days
11	2.5 High-Level System Architecture Design	Mon 2/17/25	Tue 6/10/25		82 days
12	2.5.1 Trade Studies	Mon 2/17/25	Mon 2/17/25		1 day
13	2.5.2 Subsystem Definition	Thu 4/3/25	Tue 6/10/25	9	49 days
14	2.5.3 Internal Interfaces				
15	2.5.4 Subsystem Architecture Diagram	Mon 2/17/25	Mon 2/17/25		1 day
16	3 CCD Readout System	Sun 2/16/25			
17	3.1 CCD Sensor Board	Sun 3/16/25		8	
18	3.1.1 Ethernet Connectivity	Wed 6/11/25	Thu 6/12/25	13	2 days
19	3.1.1.1 Ethernet Module Design				
20	3.1.2 Flash Memory	Wed 6/11/25	Wed 6/11/25	13	1 day
21	3.1.2.1 Flash Module Design				
22	3.1.3 Voltage Regulation	Wed 6/11/25	Thu 6/12/25	13	2 days?
23	3.1.3.1 Voltage Regulation Design	Wed 6/11/25	Wed 6/11/25		1 day?
24	3.1.3.2 Voltage Verification Testing	Thu 6/12/25	Thu 6/12/25	23	1 day?
25	3.1.4 Thermal Sensors	Wed 6/11/25	Fri 6/13/25	13	3 days?
26	3.1.4.1 Temperature Sensing Design	Wed 6/11/25	Wed 6/11/25		1 day
27	3.1.4.2 Bench Temperature Monitoring	Thu 6/12/25	Thu 6/12/25	26	1 day?
28	3.1.5 Pre-Amp/ADC	Sun 3/16/25	Sun 3/16/25	13	1 day?
29	3.1.5.1 Pre-Amp/ADC Design	Sun 3/16/25	Sun 3/16/25		1 day?
30	3.1.5.2 Bench Waveform Testing	Mon 3/17/25	Mon 3/17/25	29	1 day
31	3.1.6 MCU	Mon 6/16/25	Mon 6/16/25		1 day?
32	3.1.6.1 MCU Connectivity	Mon 6/16/25	Mon 6/16/25	20,22,25,28,33	1 day?
33	3.1.7 CCD Sensor Voltage Switching	Mon 3/17/25	Wed 6/11/25		63 days?
34	3.1.7.1 Voltage Switching Design	Wed 6/11/25	Wed 6/11/25	13	1 day?
35	3.1.7.2 Breadboard Testing	Mon 3/17/25	Mon 3/17/25	34	1 day?
36	3.1.7.3 Switching Verification Testing	Tue 3/18/25	Tue 3/18/25	35	1 day?
37	3.1.8 Physical PCB	Tue 6/17/25	Tue 9/16/25		66 days?
38	3.1.8.1 Schematic	Tue 6/17/25	Tue 6/17/25	18,20,22,25,28,33,31	1 day?
39	3.1.8.2 Layout	Fri 9/12/25	Fri 9/12/25	38	1 day?
40	3.1.8.3 Board Order	Mon 9/15/25	Mon 9/15/25	39	1 day?
41	3.1.8.4 Parts Population	Tue 9/16/25	Tue 9/16/25	40	1 day?
42	3.2 Software Design	Sun 2/16/25			
43	3.2.1 GUI	Sun 2/16/25	Thu 2/20/25	13	1 wk?
44	3.2.1.1 GUI Design	Sun 2/16/25	Thu 2/20/25		5 days
45	3.2.1.2 GUI Operation Testing	Fri 2/21/25	Fri 2/21/25	44	1 day?
46	3.2.2 Sensor Pin Clocking	Sun 2/16/25	Thu 2/27/25	13	2 wks?
47	3.2.2.1 Sensor Pin Clocking Design	Sun 2/16/25	Thu 2/20/25		1 wk
48	3.2.2.2 Pin Clocking Observation Testing	Fri 2/21/25	Fri 2/21/25	47	1 day?
49	3.2.3 Memory and Storage	Sun 2/16/25	Tue 2/18/25	13	3 days?
50	3.2.3.1 Memory and Storage Managemer	Sun 2/16/25	Mon 2/17/25		2 days
51	3.2.3.2 Data Store/Receive Testing	Tue 2/18/25	Tue 2/18/25	50	1 day?
52	3.2.4 Communications Protocol	Sun 2/16/25	Thu 2/20/25	13	1 wk?
53	3.2.4.1 Implement Communications Protc	Sun 2/16/25	Thu 2/20/25		1 wk
54	3.2.4.2 Test Data Transfer with Emulator	Fri 2/21/25	Fri 2/21/25	53	1 day?
55	3.2.5 MCU Programming	Fri 2/28/25	Fri 2/28/25		1 day?
56	3.2.5.1 MCU Software Design	Fri 2/28/25	Fri 2/28/25	46,49,52	1 day?
57	3.2.6 Drivers	Sun 2/16/25		13	
58	3.2.6.1 Ethernet				1 wk
59	3.2.6.2 Memory				5 days
60	4 System Integration Testing	Sun 2/16/25			
61	4.1 Verification Test Plan and Procedure	Wed 6/11/25	Tue 6/17/25	7,8,13	1 wk
62	4.2 System Test	Sun 2/16/25	Thu 3/13/25	61	4 wks
63	4.2.1 Bench Testing	Wed 6/18/25	Tue 7/1/25	61,41	2 wks
64	4.2.2 TVAC Testing	Wed 7/2/25	Tue 7/15/25	63	2 wks
65	4.3 Document Test Results	Wed 7/16/25	Tue 7/29/25	64,63	2 wks

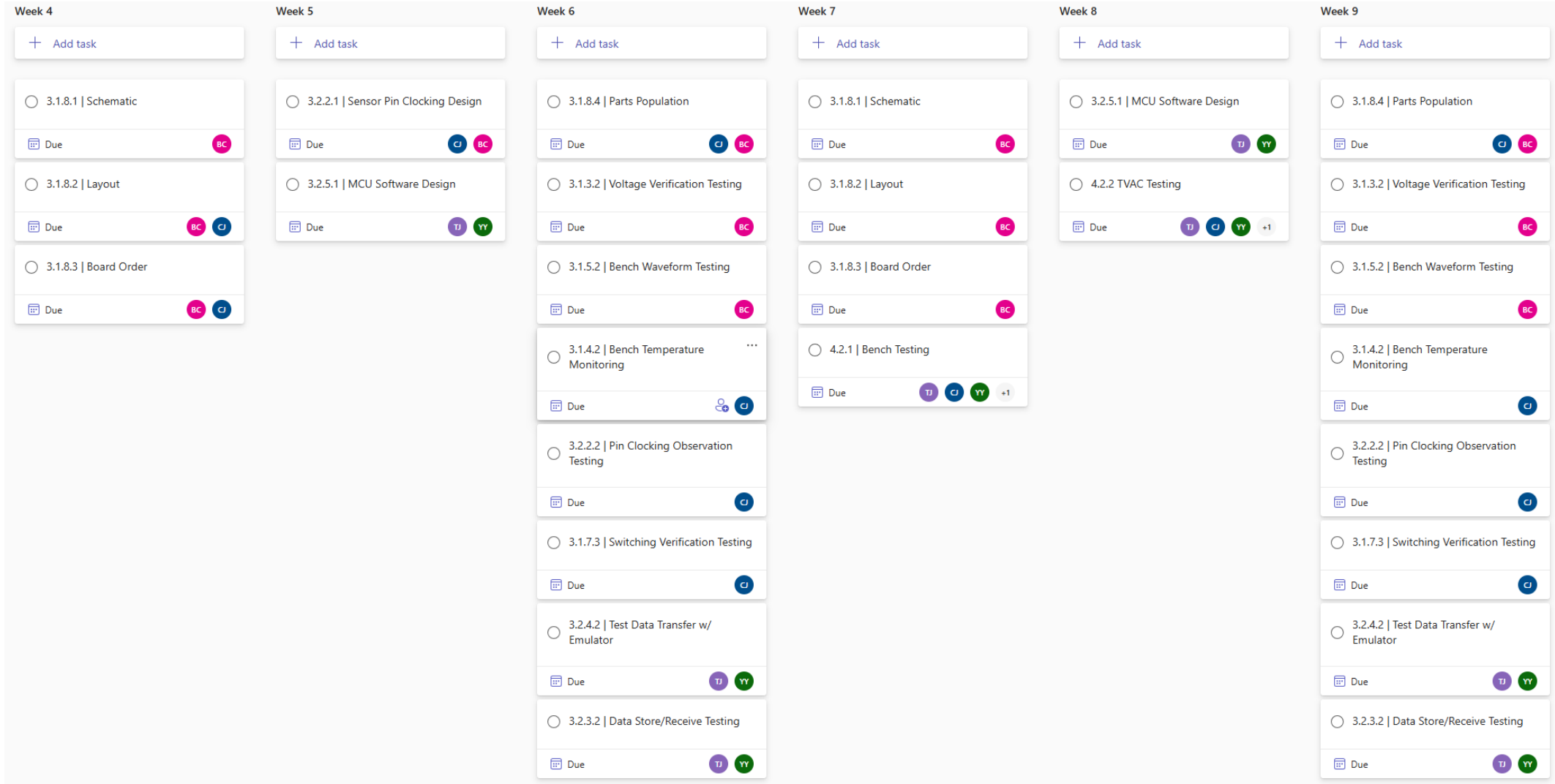
VIRGINIA TECH

Sprint Board



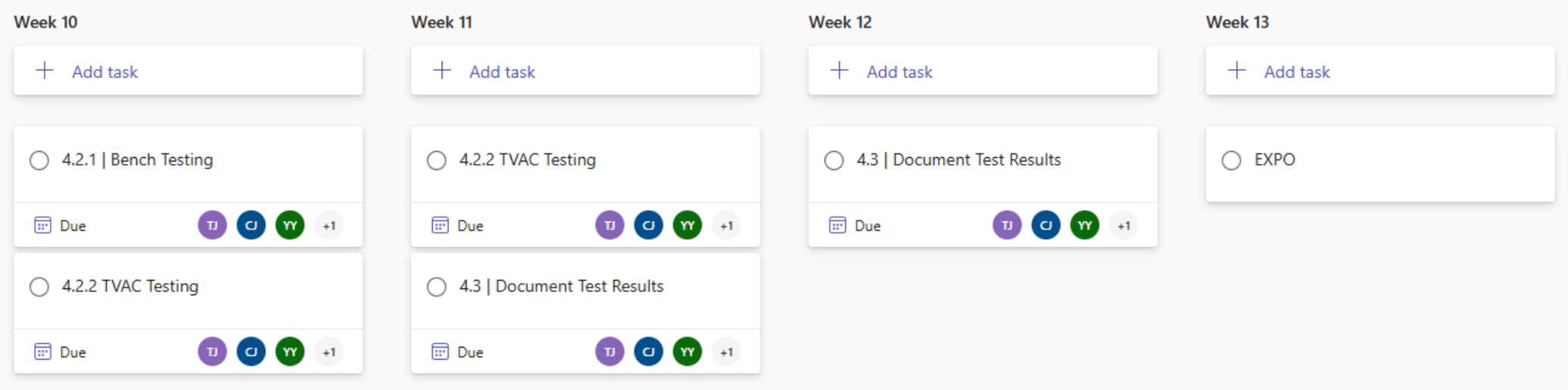
VIRGINIA TECH

Sprint Board cont.



VIRGINIA TECH

Sprint Board cont.

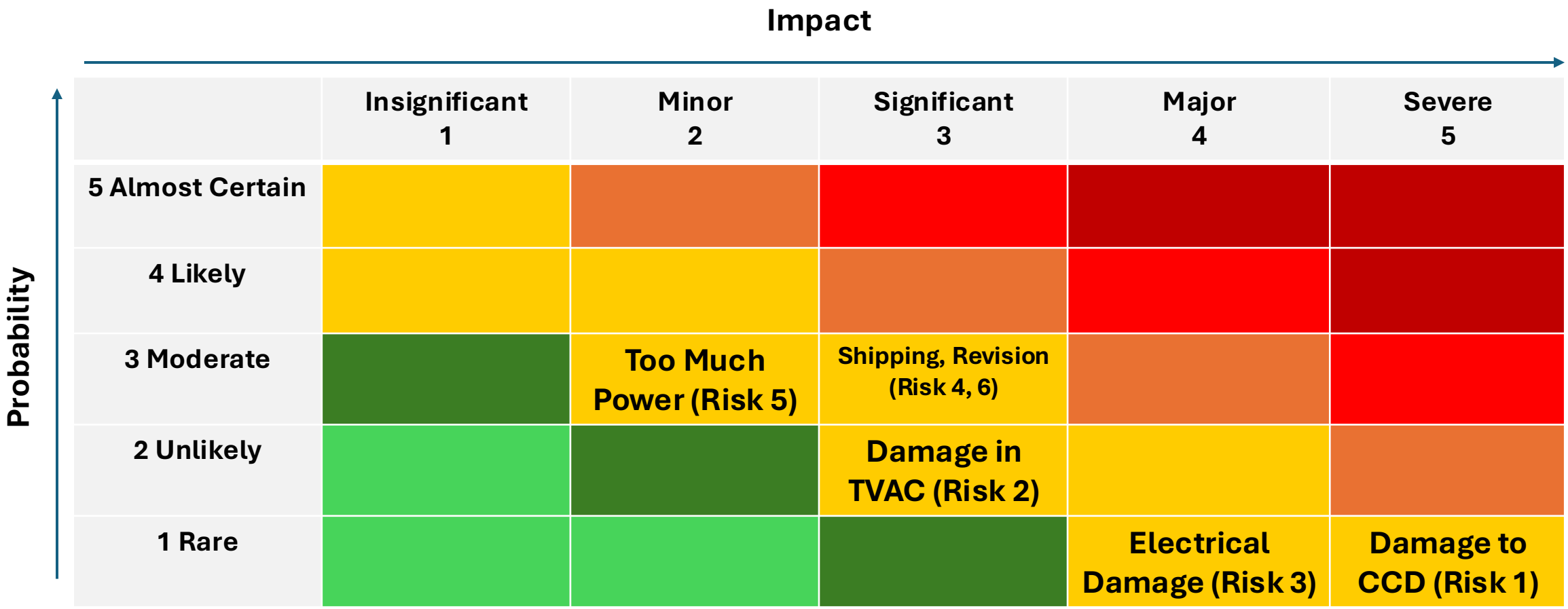


VIRGINIA TECH

Risk Identification/Mitigation

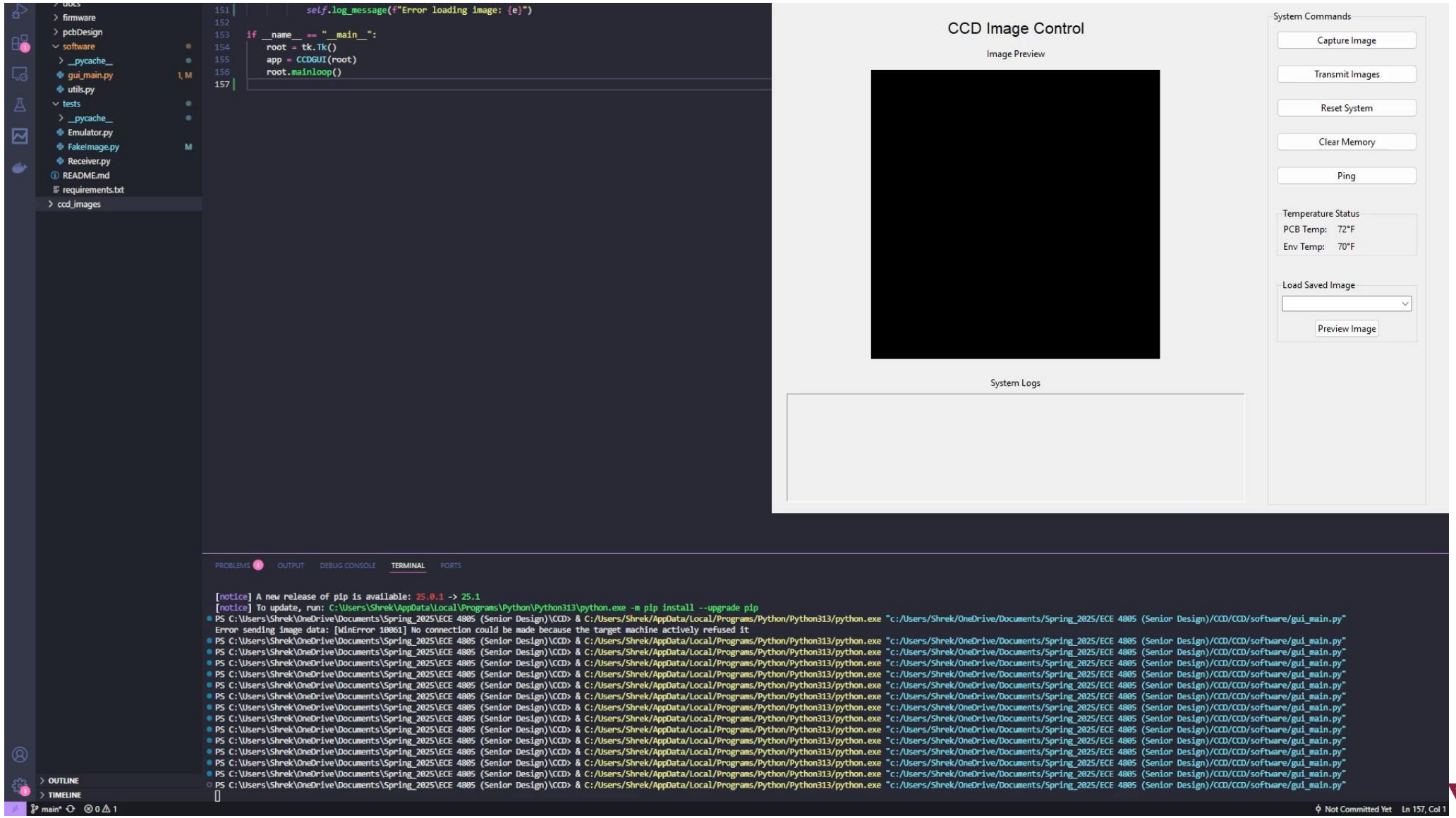
Risk No	Related Risk	RISK	Severity	Probability	Mitigations
1	2	Damage the CCD sensor	High	Low	- Handle the CCD sensor in a cleanroom environment - Use ESD protection - Follow manufacturer handling guidelines.
2	1	Damage circuit components while testing in T-VAC	Medium	Low	- Perform pre-test functional checks - Use appropriate thermal cycling procedures - Monitor temperature and pressure conditions closely
3	1,2	Electrical damage due to incorrect power supply connections	High	Low	- Implement overvoltage and overcurrent protection - Verify connections before powering up- - Use proper grounding techniques.
4	1, 2, 3	Shipping delays	Medium	Medium	- Finalize designs early and order as soon as we're confident. Our first prototype is most likely going to work exactly how we want it to, so we must redesign quickly to be able to order more parts/PCBs early.
5	N/A	Our circuit uses too much power	Low	Medium	- Ensure more careful design choices and planning so that the circuit consumes less than 5W
6	4, 5	Revisions to the first prototype or PCB design	Medium	Medium	- Make various prototype designs to compensate for other designs not working

Risk Matrix Mitigation



VIRGINIA TECH

Demo



VIRGINIA TECH

Blank Actions

Task Name	Status	Assigned To	Date
Concept of Operations: “reset array” needs to specify resetting RAM array, not Flash array	Incomplete	Javier, Yifu	5/1/2025
Concept of Operations: there needs to be a decision tree for “if entire row is shifted”	Incomplete	Javier, Yifu	5/1/2025
Concept of Operations: because we have no shutter, add a CCD reset step before each new cycle	Incomplete	Javier, Yifu	5/1/2025
Voltage Regulation: inject noise in simulations to better model an actual circuit	Incomplete	Cody	5/1/2025
Boost Converter: remove this entirely, it isn’t needed	Incomplete	Cody	5/1/2025

Blank Actions

Task Name	Status	Assigned To	Date
MOSFET Switching: try to minimize the voltage peak from the inverter output	Incomplete	Cody	5/1/2025
CCD Sensor Clocking: review the summing well of the CCD and see if it also needs clocking	Incomplete	Jae	5/1/2025
Ethernet Module: breadboard the ethernet section before we put it on a PCB	Incomplete	Cody	5/1/2025
Thermal Sensing: select a target accuracy for the sensors	Incomplete	Jae	5/1/2025

Blank Actions

Task Name	Status	Assigned To	Date
Cost Table: review the PCB cost and update according to the temperature rated material we're going to use	Incomplete	Cody	5/1/2025
GUI Functionality: explain more clearly what "reset system" is actually resetting (RAM, Flash, etc.)	Incomplete	Javier	5/1/2025
GUI Functionality: add a "reset CCD sensor" button for resetting the CCD before every operation	Incomplete	Javier	5/1/2025
Image Data Packet Format: checksum should come after "image data"	Incomplete	Javier, Yifu	5/1/2025

Blank Actions

Task Name	Status	Assigned To	Date
Software Subsystem Sequencing: need to define what happens when the system receives a warning or an error, then reflect that in the diagram	Incomplete	Javier, Yifu	5/1/2025
Software Subsystem Sequencing: ConOps also needs to reflect errors and aborts	Incomplete	Yifu	5/1/2025
Software Subsystem Sequencing: define what constitutes an error or a warning	Incomplete	Javier	5/1/2025

Blank Actions

Task Name	Status	Assigned To	Date
Software Subsystem Sequencing: this can be incorporated in the original diagram, but consider making a Soft Subsystem Sequencing diagram that defines anomaly situations (aborts, etc.)	Incomplete	Javier, Yifu	5/1/2025
Class Diagram: update based projected changes on warnings and aborts, ConOps, and Image Data Packet Format	Incomplete	Yifu	5/1/2025
Temperature Sensing: consider RTD or PTRs for temperature sensing	Incomplete	Cody, Jae	5/1/2025

Blank Actions

Task Name	Status	Assigned To	Date
Noise Level Testing: check our current method to make sure we know how we're going to get the electron read noise from this test	Incomplete	Team	5/1/2025
CCD Image Testing: instead of using the CCD sensor immediately for image testing, consider injecting analog inputs through the Pre-Amp to simulate a CCD input	Incomplete	Cody, Jae	5/1/2025
TVAC Testing: make sure we have a harness for our PCB for when we use the TVAC chamber	Incomplete	Team	5/1/2025

Blank Actions

Task Name	Status	Assigned To	Date
Sprint Board: breadboarding should come before board order	Incomplete	Cody, Jae	5/1/2025
Sprint Board: possibly move board order back a week or two to ensure time for breadboard testing	Incomplete	Cody, Jae	5/1/2025
Sprint Board: add soldering to our schedule	Incomplete	Cody, Jae	5/1/2025
System Testing: add how each system test is checking for some requirement. Use specific actions from the WBS and link them with certain tests	Incomplete	Team	5/1/2025

Thank You!