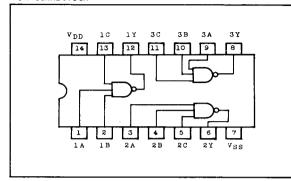
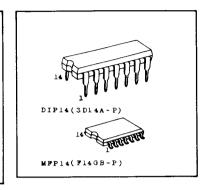
C²MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC40H010P/F

TC40H010 TRIPLE 3-INPUT NAND GATE

PIN CONNECTION





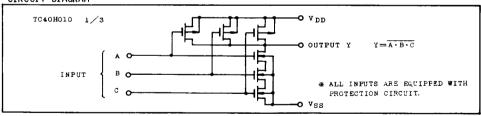
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	$V_{SS}-0.5 \sim V_{SS}+10$	v
Input Voltage	VIN	$V_{SS}-0.5 \sim V_{DD}+0.5$	v
Output Voltage	VOUT	V _{SS} -0.5 ~ V _{DD+0.5}	v
Input Current	IIN	±10	m.A.
Power Dissipation	PD	300(DIP)/180(MFP)	mW
Storage Temperature	Tstg	-65 ~ 150	°C
Lead Temp./Time	Tsol	260°C·10 sec	

TRUTH TABLE

OUTPUTS		NPUTS	I
Y	С	В	A.
Н	L	L	L
Н	Ţ	L	H
H	L	H	L
н	L	H	H
Н	Ή	L	L
Н	Н	L	н
н	Н	H	L
	Н	н	н

CIRCUIT DIAGRAM



RECOMMENDED OPERATING CONDITIONS (VSS=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	=	2.0	-	8.0	V
Input Voltage	VIN	_	0	-	v _{DD}	v
Operating Temperature	Topr	_	-40	-	85	°C

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TC40H010P/F

ELECTRICAL CHARACTERISTICS (VSS=0.0V)

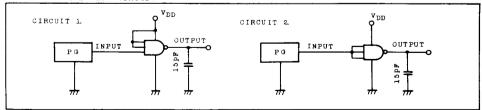
CHARACTERISTIC		SYMBOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
High Lev Output		v _{ОН}	I _{OUT} < 1 _μ A V _{IN} =V _{SS} , V _{DD}	5	4.95	-	4.95	5.0	•	4.95	-	v
Low Leve Output		V _{OL}	$ ^{\mathbf{I}_{OUT}} _{<1_{\mu}A}$ $v_{\mathbf{IN}}=v_{\mathbf{DD}}$	5	_	0.05	-	0.0	0.05		0.05	v
High Le		IOH	V _{OH=4.6} V V _{IN} =V _{SS} ,V _{DD}	5	-0.52	-	-0.44	-	-	-0.36	-	
Low Level		IOL	V _{OL=0.4V} V _{IN} =V _{DD}	5	1.4	_	1.1	-	-	0.8	-	m.A.
Input	"H" Level	VIH	IOUT <1µA	5	4.0	_	4.0	-	-	4.0	-	
Voltage	"L" Level	VIL	V _{OUT=0.5V} V _{OUT=4.5V}	5	_	1.0	-	-	1.0	-	1.0	V
Input	"H" Level	IIH	VIH=8.0V	8	-	0.3	-	10-5	0.3	-	1.0	
Current	"L" Level	IIL	V _{IL=0.0V}	8	_	-0.3	-	-10-5	-0.3	-	-1.0	μА
Quiescen Supply C		IDD	*V _{IN} =V _{SS} ,V _{DD}	5	-	2.0	-	10-3	2.0	-	10.0	μA

^{*} All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, VSS=0.0V, CL=15pF)

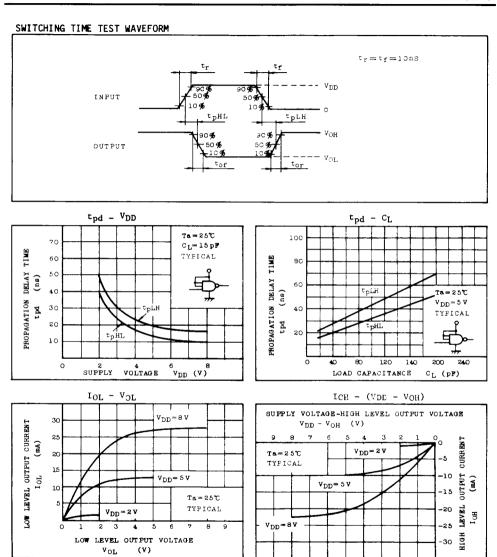
CHARACTERISTIC		SYMBOL	TEST CONDITION	ADD(A)	MIN.	TYP.	MAX.	UNIT	
Output Rise Time		tor	Circuit 1	5	-	25	40		
Output Fall Time		tof	Circuit 1	5	-	14	30	ns	
Propagation	(Low-High)	tPLH	Circuit 1	5	-	21	32		
Delay Time	(High-Low)	tpHL	Circuit 1	5	-	15	23		
Propagation	(Low-High)	tpLH		5	-	12	20	ns	
Delay Time	(High-Low)	tpHL	Circuit 2	5	-	17	26		
Input Capacitance		CIN			_	5	-	pF	

SHITCHING TIME TEST CIRCUIT



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