NXP Semiconductors
Application Note

Document Number: AN12171
Rev. 0, July 2018

Using the Power Management Controller block (PMC) self-tests on the MPC574xP

by: NXP Semiconductors

1 Introduction

The MPC5744P device targets chassis and safety applications, which require a high Automotive Safety Integrity Level (ASIL). All devices in this family are built around a safety concept based on delayed lock step core, targeting an ISO26262 ASIL-D (Design) integrity level.

A requirement of the standard is to detect the accumulation of latent defects. To meet this requirement the MPC5744P has the ability to execute PMC self-test procedures.

The PMC self-test can be performed on the device's embedded voltage detectors.

Additionally, there is "SafeAssure" Functional Safety program to reduce the development effort required by customers to meet ISO26262. As part of this program, NXP provides an MPC5744P safety manual to advice users on how to configure the MPC5744P to obtain ISO26262 ASIL D compliance.

2 Objective

This application note introduces PMC self-tests on the MPC574xP and explains how to configure and use PMC self-test features of the MPC574xP. After reading this application note the user should:

- Understand the PMC self-tests features that are available for MPC574xP
- Understand the difference between default (HW), SW triggered and single voltage detector VD test
- Be able to develop application strategies for deploying SW triggered testing
- Be able to develop application strategies for deploying single VD testing
- Understand when different PMC self-tests takes place

This application note also provides example for PMC self-test configurations that can be directly implemented by the user. The example is provided in the software package that accompanies this document and is also explained in detail.

To aid in understanding of this document and software package, user should obtain the MPC574xP Reference and Safety manuals from the NXP website.

Contents

3 Overview of PMC self-test

The term Built-In Self-Test (BIST) is used to describe on-chip hardware mechanisms that can be used to detect latent faults within the MCU. The BIST allows the MCU to conduct periodic self-tests to identify faults. The results of these self-tests (HW triggered self-test, software triggered VDs self-test and software triggered single VD self-test) can then be used by the MCU to handle the faults and ensure that the device remains in a safe state.

3.1 PMC self-test

The PMC self-test implements an LVDs/HVD test mechanism for use in satisfying safety goals. The digital block assists and controls the analog block during its performance of the self-test.

3.2 PMC clocking

Digital part of PMC module is clocked by PBRIDGE clock. PBDRIGE clock can run up to 50 MHz supplied from FMPLL module.

NOTE

Minimum PBRIDGE clock for correct test functionality is 16 MHz.

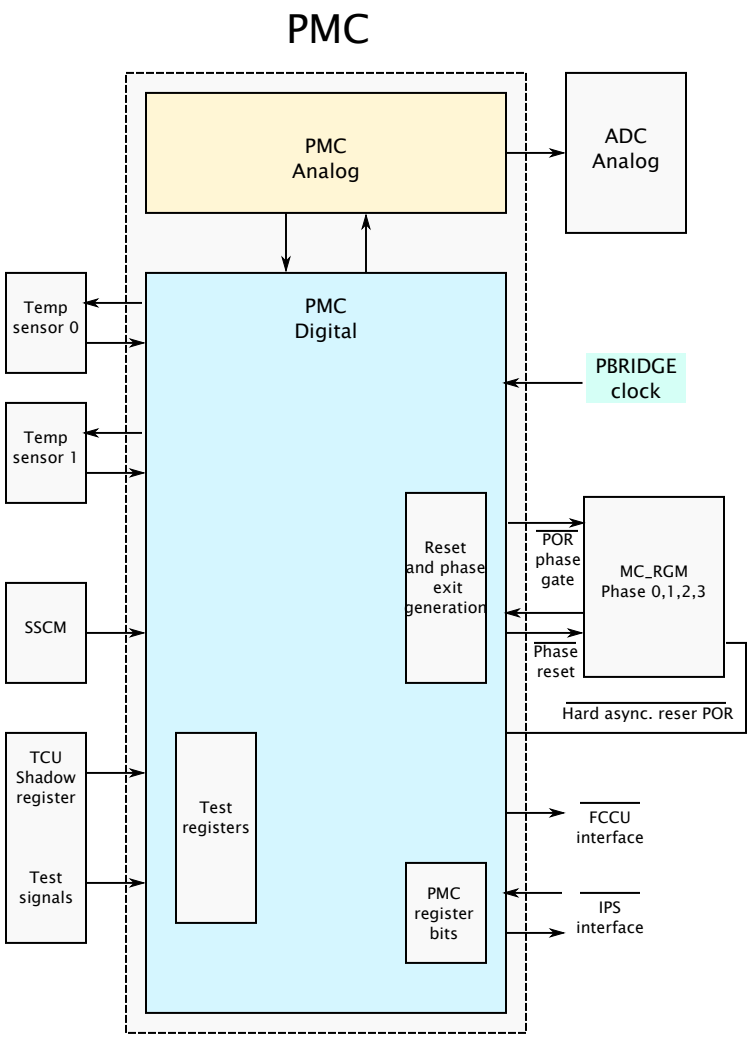

Figure 1. PMC block diagram

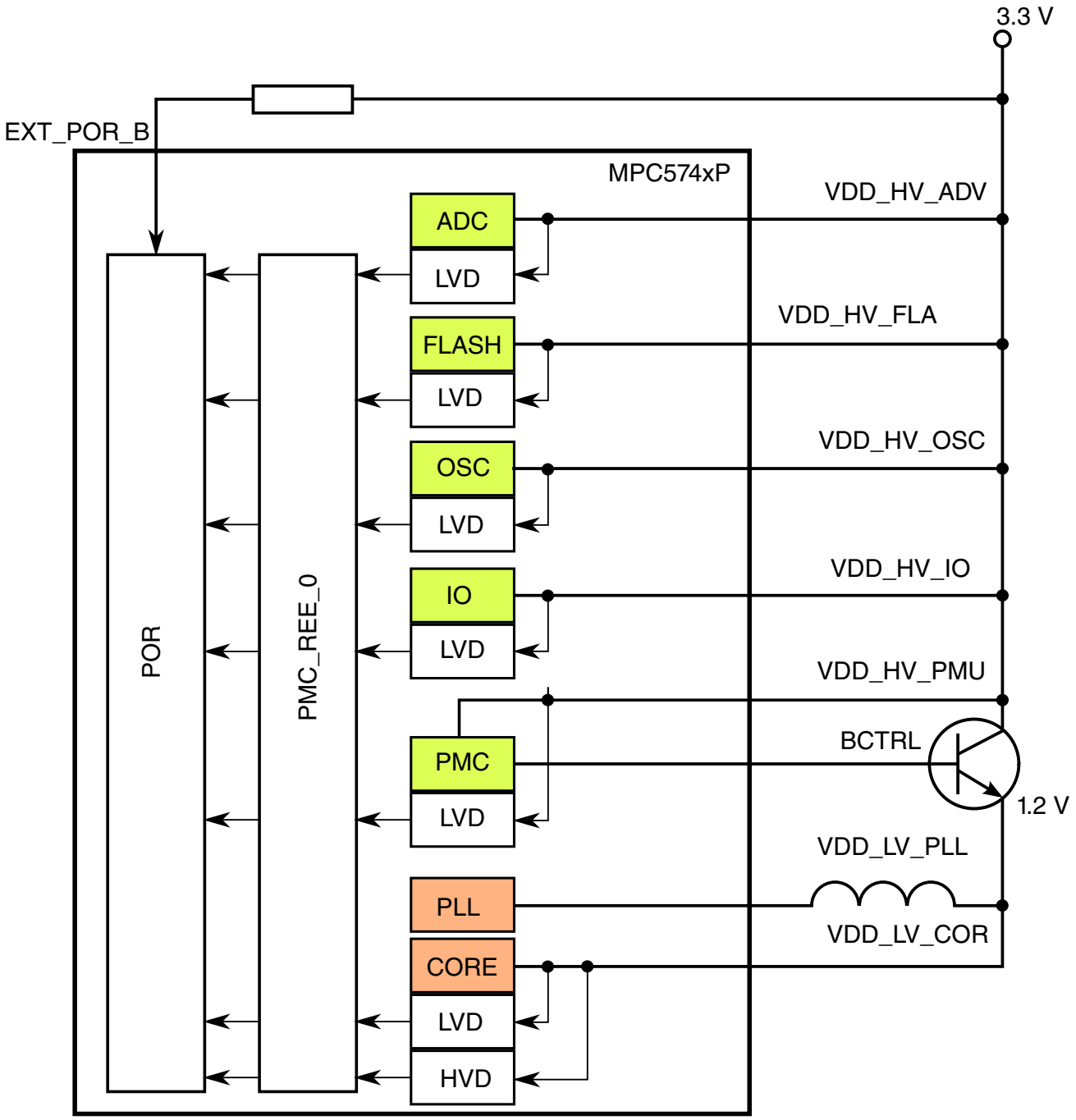

Figure 2. PMC self-test principle

3.3 Hardware triggered self-test

The self-test is always performed during startup (power on). The self-test starts during the phase 3 MC_RGM state, when the SSCM has completed reads from the flash memory (that is, asserts 'sscm_done' signal). A watchdog counter monitors the execution time of each voltage test duration. Watchdog default timeout value is 8 µs.

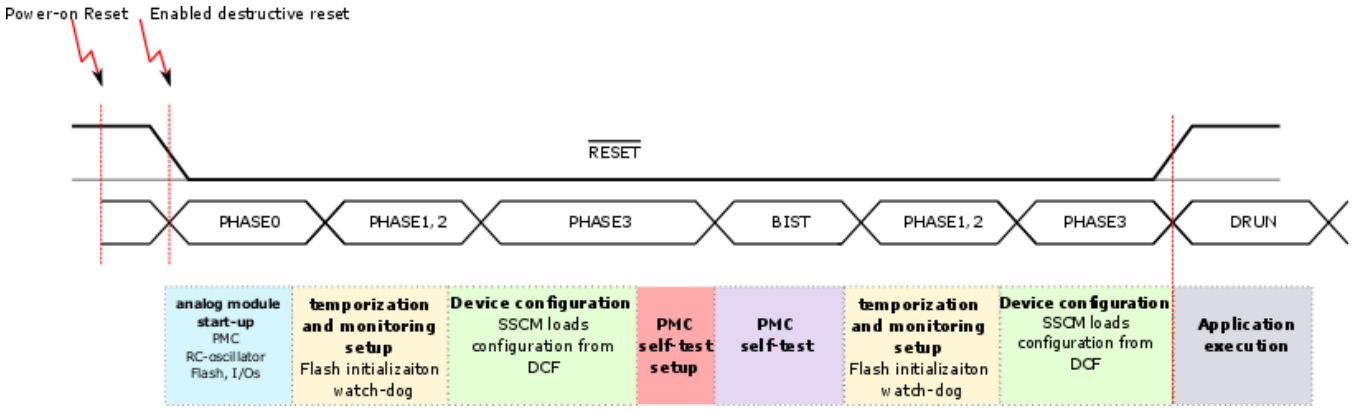

Figure 3. Default mode self-test execution

3.4 Software triggered self-test

This is PMC self-test triggered from user application to verify the functionality of LVDs/HVD. Its execution depends on application needs. Self-test can be triggered repeatedly in time intervals or run just once.

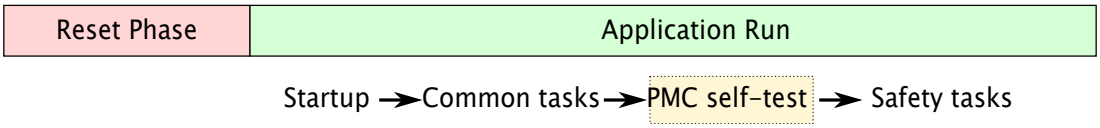

Figure 4. Software triggered self-test

3.5 Single VD test

Single VD test offers the possibility to execute only selected PMC self-test. This self-test can be executed only from user application.

User can execute following single VD test based on the PMC_VD_UTST[CTRL] settings:

- LVD_CORE
- HVD_CORE
- LVD_VDDREG
- LVD_FLASH
- LVD_ADC
- LVD_OSC
- LVD_IO
- LVD_CORE_HOT

There are two LVD trigger points in the device for 1.2 V core supply. One at the hot point deep inside the die and other at cold point is at the pad. Each of them is trimmed separately. The reason of the two LVDs is the IR drop in the design (to have LVDs at two ends of the die).

3.6 Self-test time window (STTW)

STTW is time-window used to monitor duration of self-test for each LVD/HVD. It is very important to set STTW correctly. While time-window is active (test is started) reset reaction on LVD/HVD events are masked. After time-window expired the reset reactions are again active even if test is still ongoing. The device is reset if reset is enabled in PMC_REE_0] and POR or VOR flag is set in MC RGM (reset generation module) because the time-window expired while the test is still active. ST_RESULT flag in PMC_VD_UTST register are cleared (self-test failed). This bit can be modified by the HW self-test which is running during device startup.

Self-test duration set in STTW depends on power supply and clock for its digital part. The average time for one single LVD/HVD self-test is 8 µs. However, this time depends on power supply parameters. If the power supply is not strong enough, this time will be longer.

NOTE

8 µs is typical value, which heavily depends on the supply level, which is being sensed. If the supply is ramping very slowly the response time can be really slow, moreover there is dependency on the temperature and supply level.

STTW value for HW PMC self-test (executed during reset) is set at 0x7F. This is programed in NXP factory and stored in factory DCF records. Self-test during reset is running with 16 MHz IRC clock therefore 0x7F(-> 0x7F/16[us]= 8 µs) is sufficient timeout.

NOTE

SW triggered self-test duration must be calculated properly for correct operation.

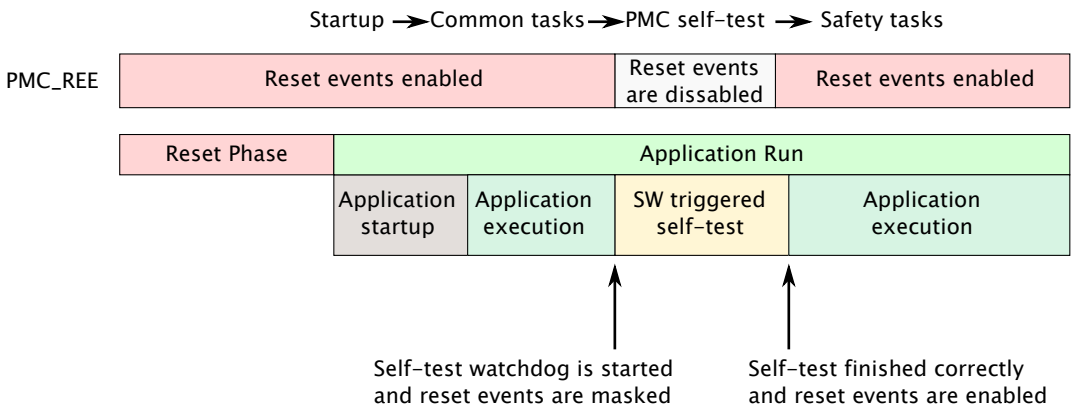

Figure 5. PMC_REE behavior during self-test

4 HW triggered self-test

This is full PMC self-test and it is executed during reset phase 3. There is no possibility to disable PMC HW triggered self-test (default mode). This test is configured via factory programmed DCF records which user has no possibility to modify.

5 SW triggered self-test

SW triggered self-test is started from user application code. User must ensure correct configuration of SW self-test to prevent unintended resets.

Steps to configure SW triggered self-test:

1. Set test mode to default

```
PMC.VD_UTST.B.ST_ MODE = 0x0; /* default mode */
```

2. Clear result bit - The result bits needs to be cleared by writing 1. During clearing the bit be sure that the mode is configured to default

```
PMC.VD_UTST.B.ST_RESULT = 0x1; /* write 1 to clear results */
```

3. Set watchdog timeout – if the test fails, slightly adjust the calculated value as power supply is probably not strong enough. Refer to note in section Self-test time window (STTW) on page 6.

```
PMC.STTW.R = 0x19A; /* configure watchdog */
```

4. Select SW triggered self-test mode

```
PMC.VD_UTST.B.VD_ST_CTRL = 0x0; /* Full self-test */
```

5. Start PMC SW triggered self-test

```
PMC.VD_UTST.B.ST_MODE = 0x1; /* SW triggered self-test */
```

After the self-test finishes (PMC_VD_UTST[ST_DONE is set]) its execution user can read test results in PMC_VD_UTST[ST RESULT].

5.1 Calculating STTW timeout

STTW is supplied by PBRIDGE clock.

Calculation example:

PBRIDGE clock = 50 MHz

1 PMC test = ~8 µs

STTW = PBRIDGE [MHz] * PMC test [us]= 50 MHz * 8 µs = 400 = 0x190h

The STTW timeout is valid for single voltage test, and it is restarted after each single test of SW triggered self-test. SW triggered self-test contains 8 single voltage tests.

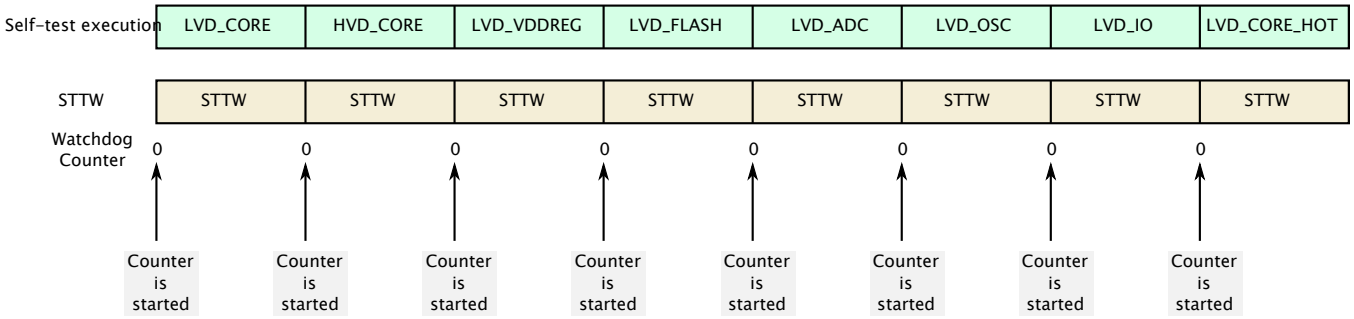

Figure 6. STTW behavior during Software triggered VDs self-test execution

6 Single VD test

In time-critical application user has possibility to execute only selected self-test via Single VD test method. This feature is available for all software triggerable voltage tests which are listed in section Single VD test on page 5.

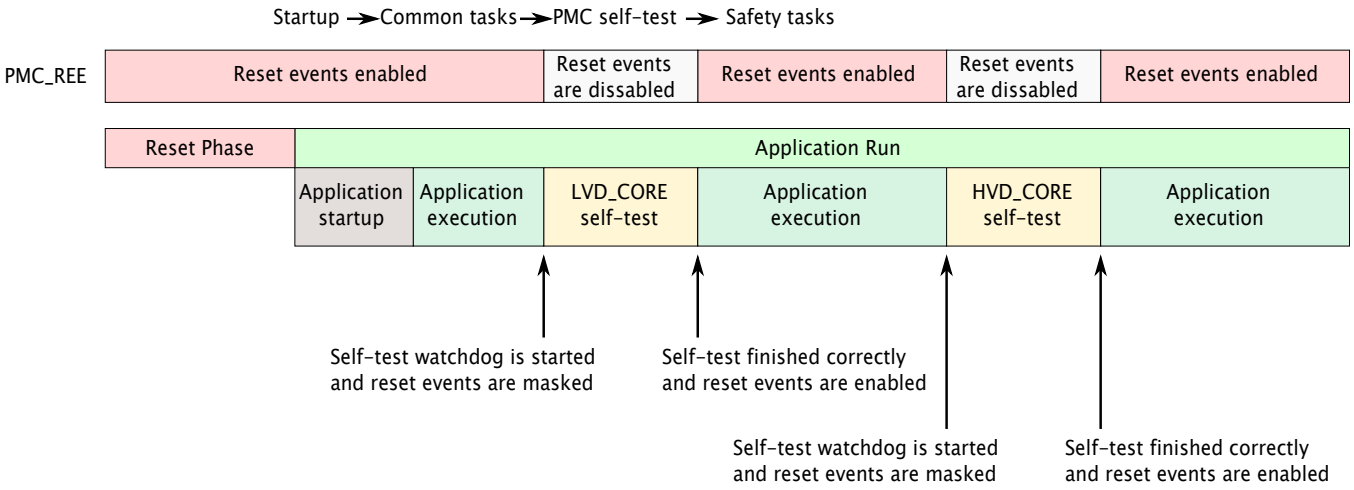

Figure 7. Example of Single VD test execution

Steps to configure Single VD test:

1. Set test mode to default

   ```
   PMC.VD_UTST.B.ST_MODE = 0x0; /* default mode */
   ```

2. Clear result bit - The result bits need to be cleared by writing 1. During clearing the bit be sure that the mode is configured to default.

   ```
   PMC.VD_UTST.B.ST_RESULT = 0x1; /* clear results */
   ```

3. Set watchdog timeout - if the test fails, slightly adjust the calculated value as power supply is probably not strong enough. Refer to note Self-test time window (STTW) chapter 3.6

   ```
   PMC.STTW.R = 0x19A; /* configure watchdog */
   ```

4. Select SW triggered self-test mode. Make sure that configured mode is default.

   ```
   PMC.VD_UTST.B.VD_ST_CTRL = 0x3; /* Single VD test as indicated by the VD_UTST bits */
   ```

5. Start PMC Single VD self-test

   ```
   PMC.VD_UTST.B.ST_MODE = 0x2; /* start Single VD test */
   ```

After the self-test finishes (PMC_VD_UTST[ST_DONE is set]) its execution user can read test results in PMC_VD_UTST[ST RESULT].

6.1 Calculation of STTW timeout

STTW is supplied by PBRIDGE clock.

Calculation example:

PBRIDGE clock = 50 MHz

1 PMC test = ~8 µs

STTW = PBRIDGE [MHz] * PMC test [us] = 50 MHz * 8 µs = 400 = 0x190h

The STTW timeout is valid for single VD test. The STTW timer is started each time when Single VD test is started.

7 References

- MPC574 4P Reference Manual (document MPC5744PRM)

A PMC SW triggered self-test

A.1 PMC SW triggered self-test

Example 1:

```
void PMC_single_self_test(void)
{
    /* 1. set mode to default*/
   PMC.VD_UTST.B.ST_MODE = 0x0;         /*default mode */
   /* 2. clear result bit*/
   PMC.VD_UTST.B.ST_RESULT = 0x1;      /* write 1 to clear results */
   /* 3. Set STTW - the watchdog counter is reset after every voltage test, so the value is
same for SW test and single VD test*/
   PMC.STTW.R = 0x19A;                  /* 0x19Ah */
   /* 4. Full selt-test*/
   PMC.VD_UTST.B.VD_ST_CTRL = 0x0;     /* Full self-test */
   /* 5. configure self-test mode bits for testing of LVDs and HVDs */
   PMC.VD_UTST.B.ST_MODE = 0x1;    /*  SW triggered self-test */
}
```

A.2 PMC single VD test

Example 2:

```
void PMC_single_self_test(void)
{
    /* Program DCF records to disable LVD reset reactions before test execution */
    /* PMC self-test is running from PBRIDGE_CLK*/

    /* 1. set mode to default */
    PMC.VD_UTST.B.ST_MODE =0x0;         /*default mode */
    /* 2. clear result bit*/
    PMC.VD_UTST.B.ST_RESULT = 0x1;      /* write 1 to clear results*/

    /* 3. set watchdog timeout*/
    /* 1 SW test last ~8us*/
    /* PBRIDGE_CLK = 50MHz */
    /* 1 SW test => 8us * PBRIDGE_CLK = 8 * 50 =400us = ~0x190h */
    /* this is dependent on power supply, it is always good to have a slight reserve */
    /* Value in PMC STTW is valid for 1 SW test*/
    PMC.STTW.R = 0x19A;        /* 0x19Ah */


    /* 4. Select self-test*/
    /* Single VD test as indicated by the VD_UTST bits */
    PMC.VD_UTST.B.VD_ST_CTRL = 0x3;
    /* 5. configure self-test mode bits for testing Single VD test */
    PMC.VD_UTST.B.ST_MODE = 0x2;  /* start Single VD self-test */
}
```

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Document Number: AN12171
Rev. 0, July 2018