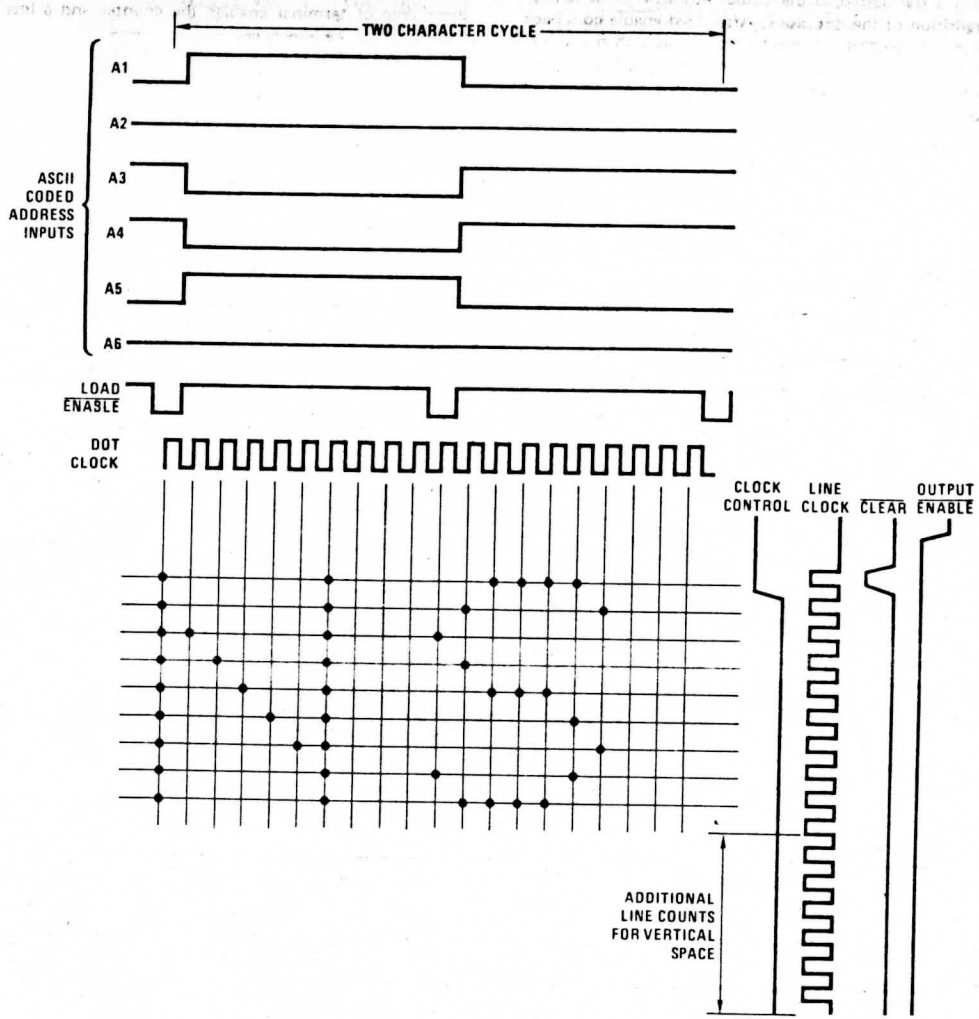
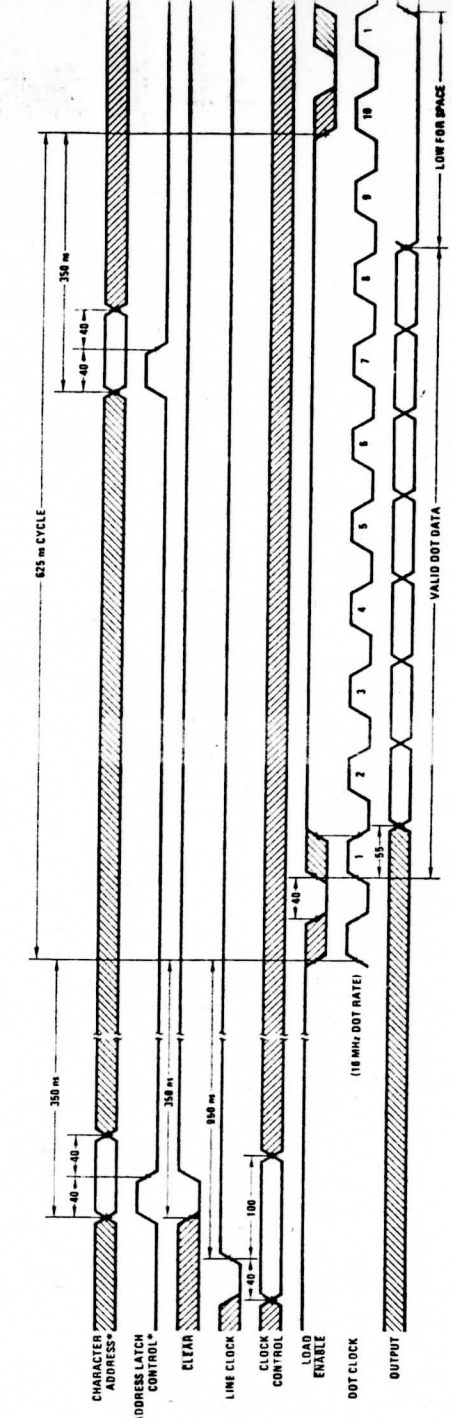


FIGURE 3. Example of Two Character Display Timing



*Shown here for operation with dynamic memory. For static memory operation the address latch control would be tied high and the character addresses would be stable between each address change occurring 350 ns before the high-to-low transition of Load enable.

FIGURE 4. Typical System Timing Waveform