1. SFR are not cacheable because they correspond to physical hardware on the pic 32.

2. 8 bit fields, after reset trisc15- trisc12 are implemented to 1, and Trisc4-trisc1 are implemented to 1

3. Processor.o is machine code that tells the physical memory addresses of sfrs

4. This is because the prefetch module gets 4 lines ahead of the program, so it needs the ability to get 4x the amount of data per clock cycle. This means it must take 128 bits.