DAC YF

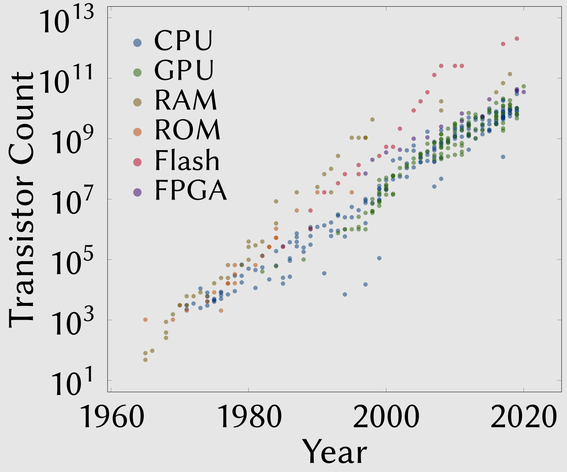
Advanced Node Physical Design and Attack

Haocheng Li and Prof. Evangeline F. Y. Young, The Chinese Univ. of Hong Kong

DESIGN AUTOMATION CONFERENCE 57
FROM CHIPS TO SYSTEMS – LEARN TODAY, CREATE TOMORROW

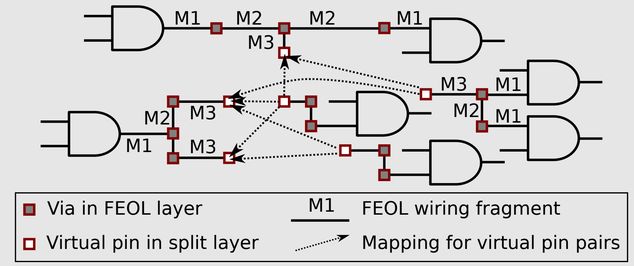
Introduction

Moore's Law claims a doubling of transistor count for every two years. The advancement of technology nodes brought new crucial problems to automated physical design like having complicated rule checking, multi-row standard cells, and globalized manufacturing. Cell implementations with mixed height result in difficulties during placement. We need to reserve more space to accommodate resolution enhancement techniques (RETs), and detailed routing has to handle these spacing rules. Globalized manufacturing increases the risk that the manufacturer may steal the intellectual properties (IPs) by overproducing the chips or even inserting Trojans inside.



Split Manufacturing

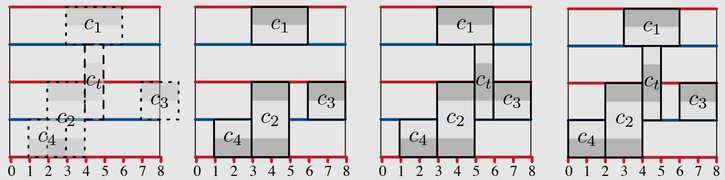
Available FEOL, cell library, layout database.



Correct Connection Rate

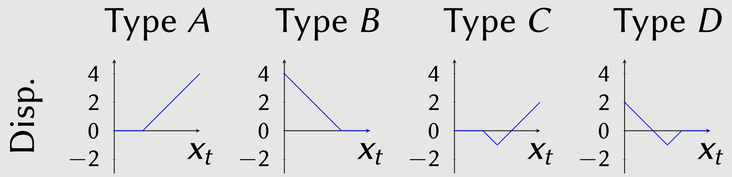
$$CCR = \frac{\sum_{i=1}^{m} c_i x_i}{\sum_{i=1}^{m} c_i}. \quad (1)$$

Detailed Placement



(a) GP (b) Placed Cells (c) MLL (d) MGL

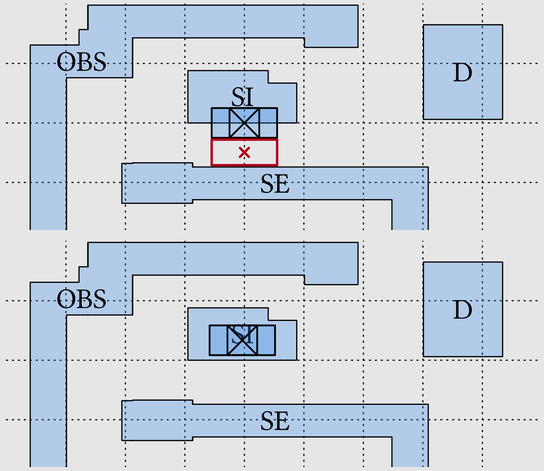
Displacement Curves



Detailed Routing

Pin SI has no violation-free same-layer access point.

Connect SI to upper-layer access points with an off-track via.



Attack Framework