PIN DIAGRAM

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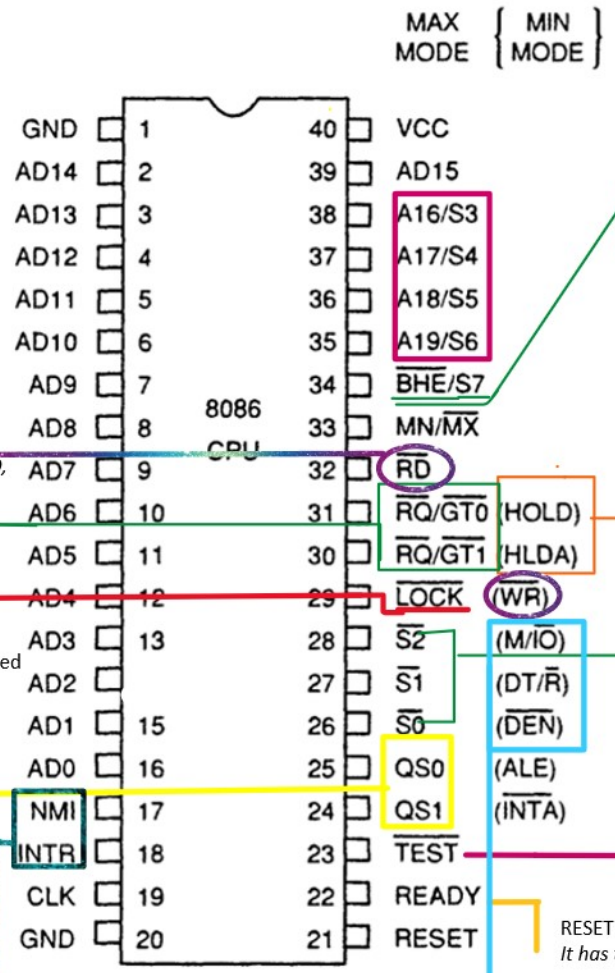

$\overline{BHE}$	A_0	Indication
0	0	Whole word
0	1	Upper byte from or to odd address
1	0	Lower byte from or to even address
1	1	None

BHE (BUS HIGH ENABLE)
Activates the significant byte

ADDRESS/ STATUS PINS

S6 = *LOGIC 0*
(denotes the processor is in low state, in control of external device)

S5 = IF *flag register status*
At each cycle this is updated and denotes w interrupt is enable.

S3,S4 = *segment access*
S7 = *logic 1*

S4	S3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

READ: *for output, that the processor is reading active during T2 and T3 cycles. tristate during hold acknowledge.*

WRITE: microprocessor is writing, similar to READ,

RQ/ GT, request for access, grant request by other processors in multipurpose

LOCK: when prefixed with an instruction, LOCK ADD B,C , avoids the external buses taking control till the instruction is implemented

USED FOR DMA(DIRECT MEMORY CONTROL)
HOLD *is from DMA to x86 for control*
HLDA *is the acknowledgement.*

DMA: *for any peripherals interest in using the memory of microprocessor, without it's interference. All buses are in external control.*

STATUS signals. For timing and control of buses.
Passive when ready is inactive.

Status Signal			Machine Cycle
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive/Inactive

QS0, QS1 The status of queue is given by these for external monitoring

Queue status		Queue operation
QS_1	QS_0	
0	0	No operation
0	1	First byte of an opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

Examined by 'WAIT'. If low, execution continues. If high, processor waits or is idle

RESET: *when active, processor terminates all the activities. It has to be high for at least 4 clock cycles.*

From memory or I/O that it's acknowledged or is ready to perform.

NON MASKABLE INTRRRUPT
INTERRUPT REQUEST (maskable interrupt)

M/$\overline{IO}$ - to enable the acceess of memory or input/output
DT/$\overline{R}$ – *control direction of data, whether recieving or transmitting*
$\overline{DEN}$ – *enable pin that the data can be transmitted or recieved*