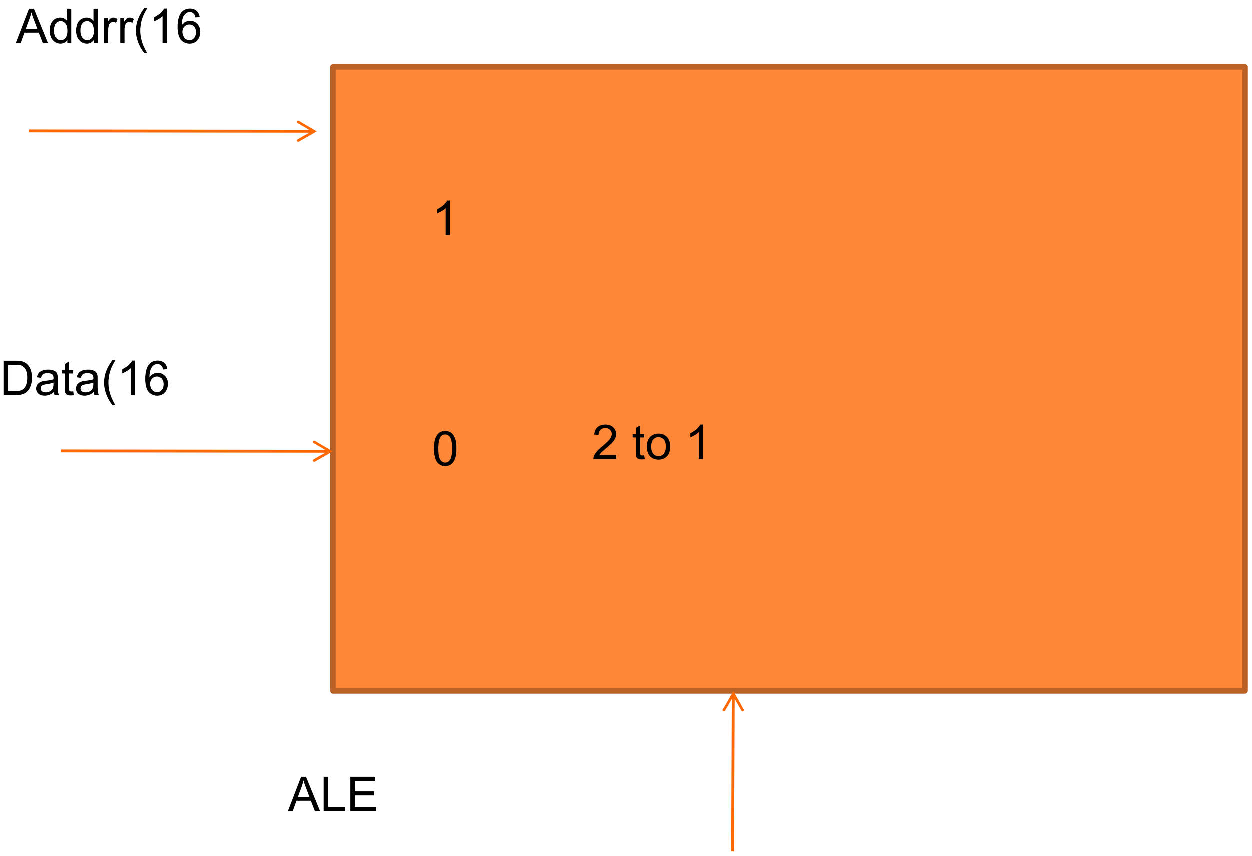
16 BIT MICROPROCESSOR 8086

FEATURES OF 8086 MICROPROCESSOR

- 16 bit microprocessor(data), 40 pin ,DIP(Dual in line package
- 20 address lines i.e 2^20=1MB memory addressed.
- 1MB =1000KB(decimal)
- 1MB=1024KB(Binary)
- No. of address lines =n
- No. of addresses =N
- N=2^n
- Uses the concept of **segmented memory. 8086 able to address a memory capacity of 1** megabyte and it is byte organized. This 1 megabyte memory is divided into 16 logical segments. Each segmentcontains 64 kbytes of memory.
- Arithmetic operation on 8 bit or 16 bit signed or unsigned data including multiplication and division.
- Operate in single processor or multiprocessor(8087)
- It has multiplexed address and data bus AD0-AD15 & A16-A19
- It requires single phase clock with 33% duty cycle to provide internal timing.
- Prefetches up to 6 instruction bytes from memory and queues them in order to speed up the processing.
- 8086 supports 2 modes of operation

  a. Minimum mode(single processor)

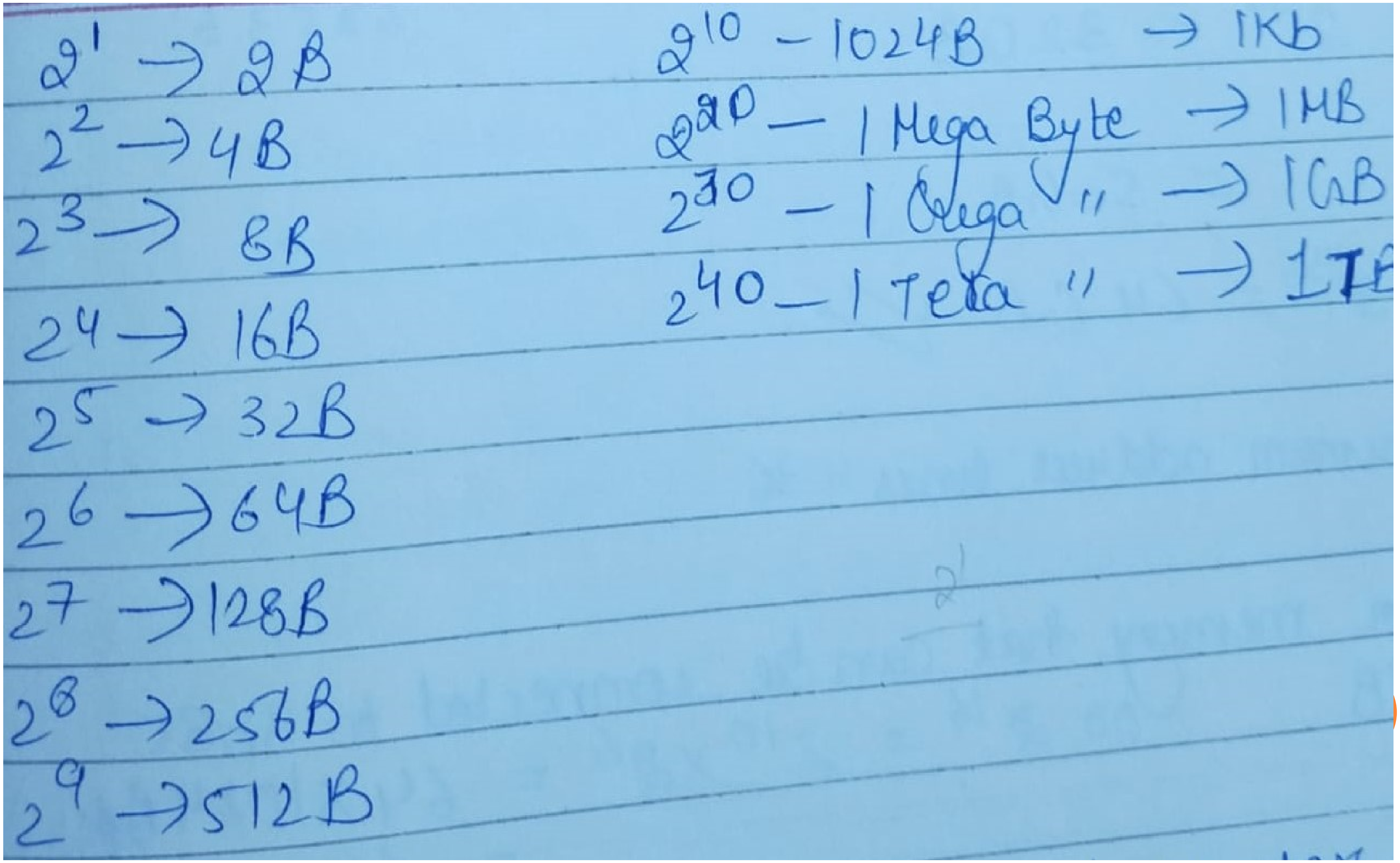
  b. Maximum mode.(multiple processors)


Addrr(16
1
Data(16
0
2 to 1
ALE

- 1s –Time period
- Logic 1 -.33s
- Logic -.67s
- Duty cycle=Ton(Logic 1)/Total TP

64kb
64kb

MEMORY SIZE



$2^{1} \rightarrow 2B$

$2^{2} \rightarrow 4B$

$2^{3} \rightarrow 8B$

$2^{4} \rightarrow 16B$

$2^{5} \rightarrow 32B$

$2^{6} \rightarrow 64B$

$2^{7} \rightarrow 128B$

$2^{8} \rightarrow 256B$

$2^{9} \rightarrow 512B$

2^{10} - 1024B → 1Kb

2^{20} — 1 Mega Byte → 1MB

2^{30} — 1 Gega " → 1GB

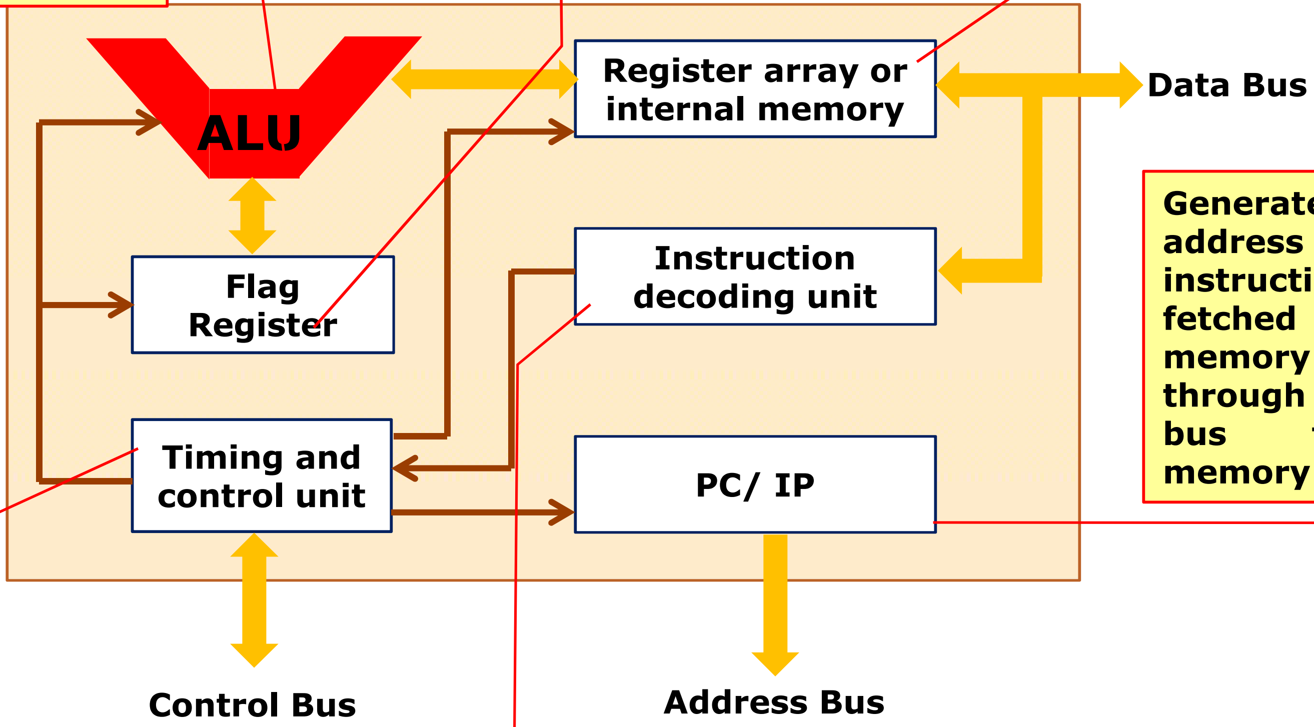
2^{40} — 1 Tera " → 1TB

FUNCTIONAL BLOCKS

Computational Unit; performs arithmetic and logic operations

Various conditions of the results are stored as status bits called flags in flag register

Internal storage of data

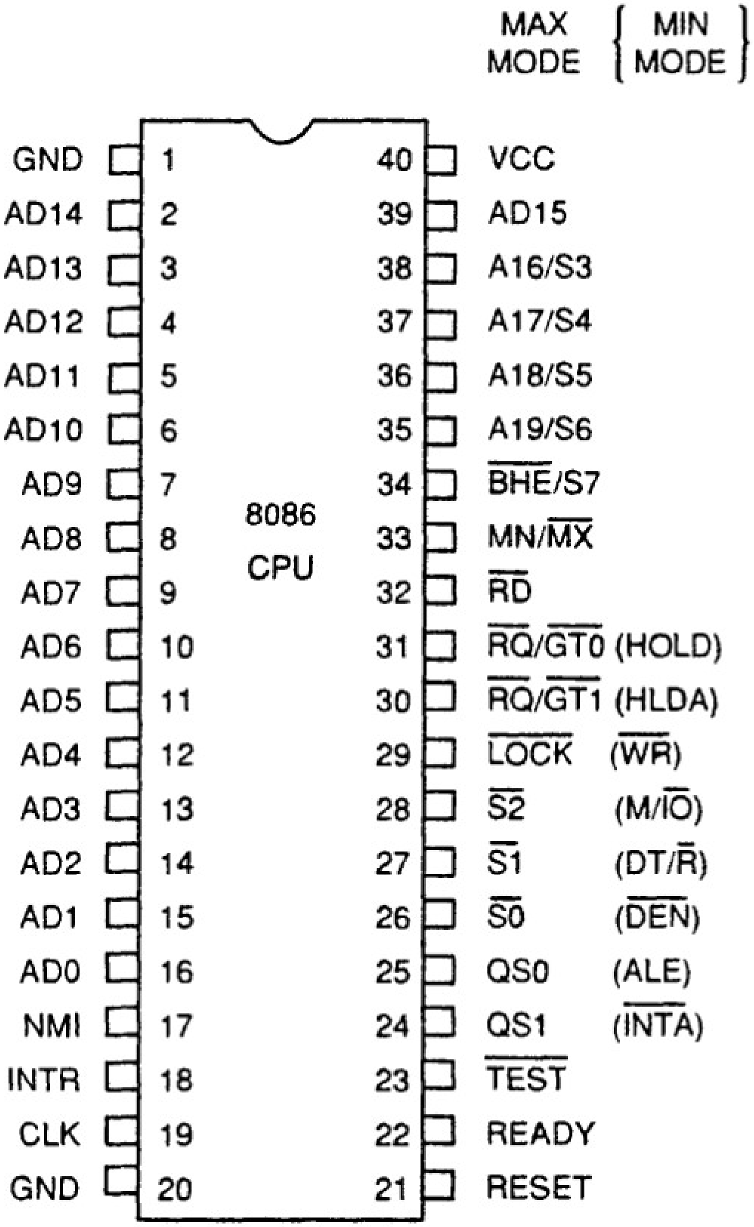


Generates the address of the instructions to be fetched from the memory and send through address bus to the memory

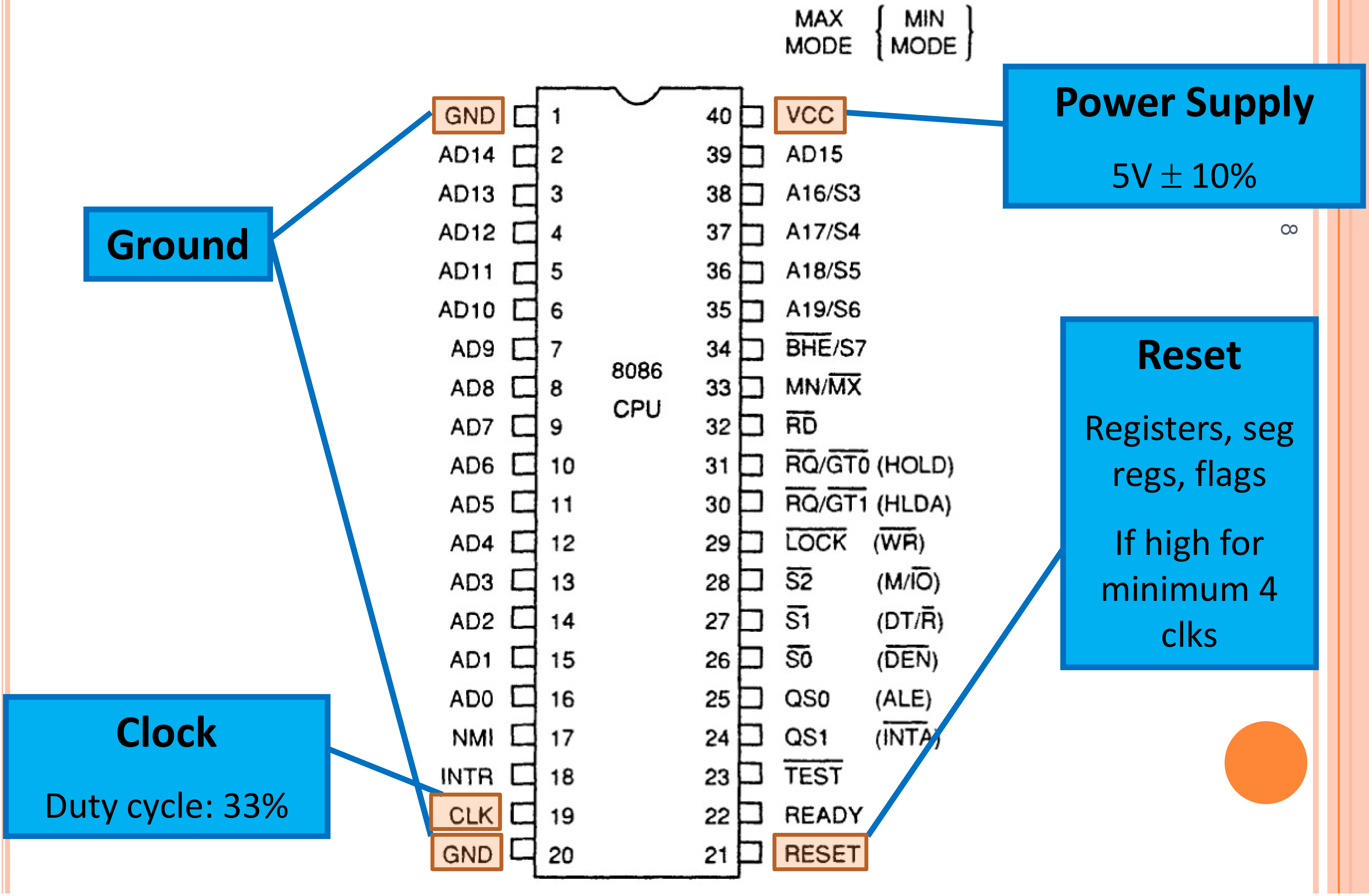
Generates control signals for internal and external operations of the microprocessor

Decodes instructions; sends information to the timing and control unit

INTEL 8086 - Pin Diagram



INTEL 8086 - Pin Details



Power Supply

5V ± 10%

Ground

Reset

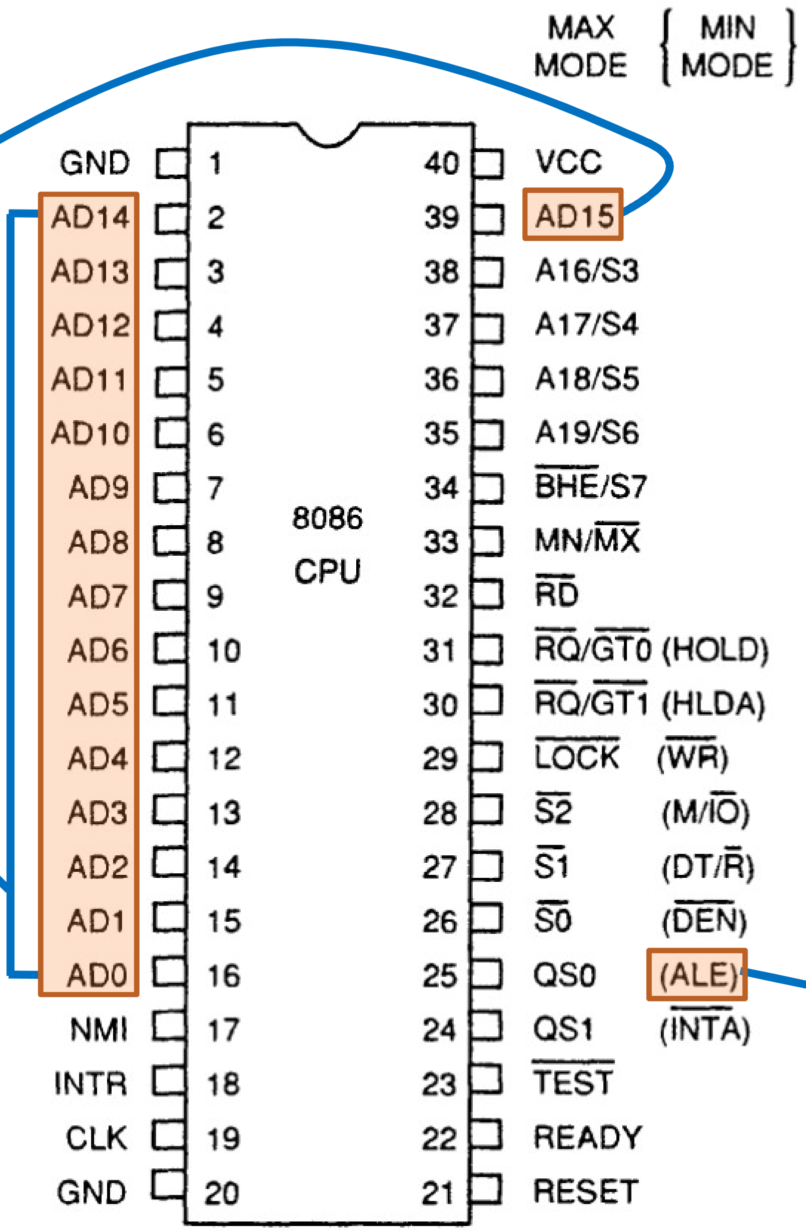
Registers, seg regs, flags

If high for minimum 4 clks

Clock

Duty cycle: 33%

INTEL 8086 - Pin Details



Address/Data Bus:

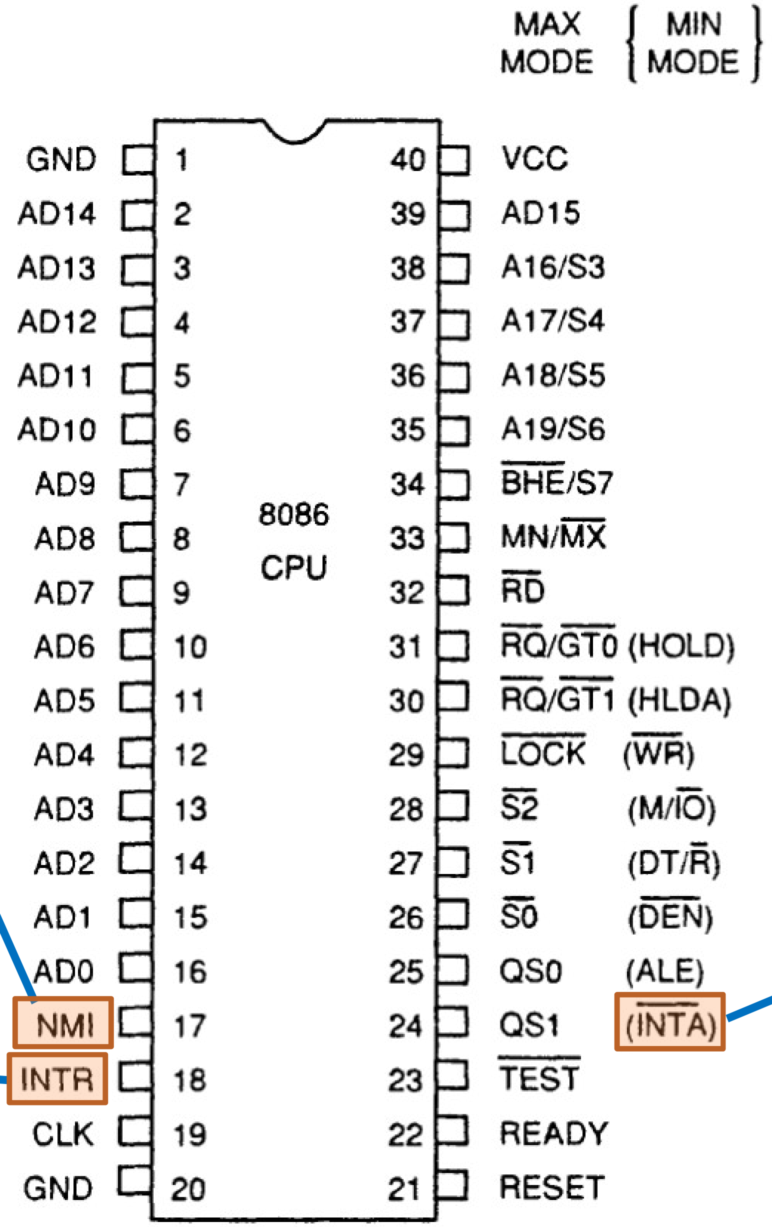
Contains address bits A_{15}-A_0 when ALE is 1 & data bits D_{15} – D_0 when ALE is 0.

Address Latch Enable:

When high, multiplexed address/data bus contains address information.

INTEL 8086 - Pin Details

INTERRUPT



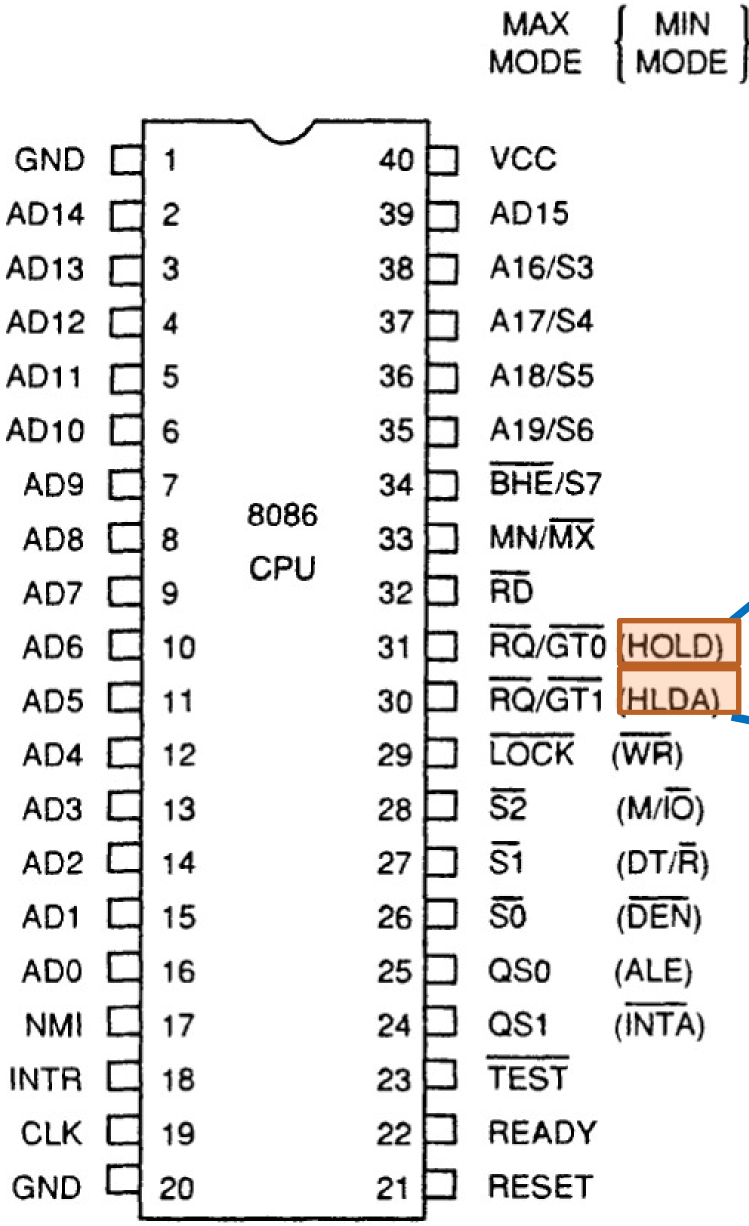
Non - maskable interrupt(which cannot be ignored) positive edge triggered input

Interrupt request(high level-triggered, maskable interrupt request signal)

Interrupt acknowledge

(Low active output in response to INTR)

INTEL 8086 - Pin Details



Direct Memory Access

Hold(Active high i/p signal From DMA controller to processor for control on system buses)

Hold acknowledge(signal by the processor to the bus master requesting the control of the bus through HOLD.

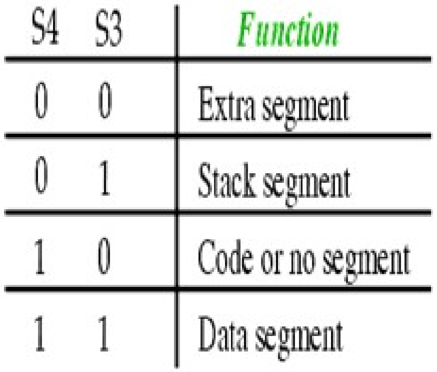
Acknowledge is asserted high, when the processor accepts HOLD.)

INTEL 8086 - Pin Details

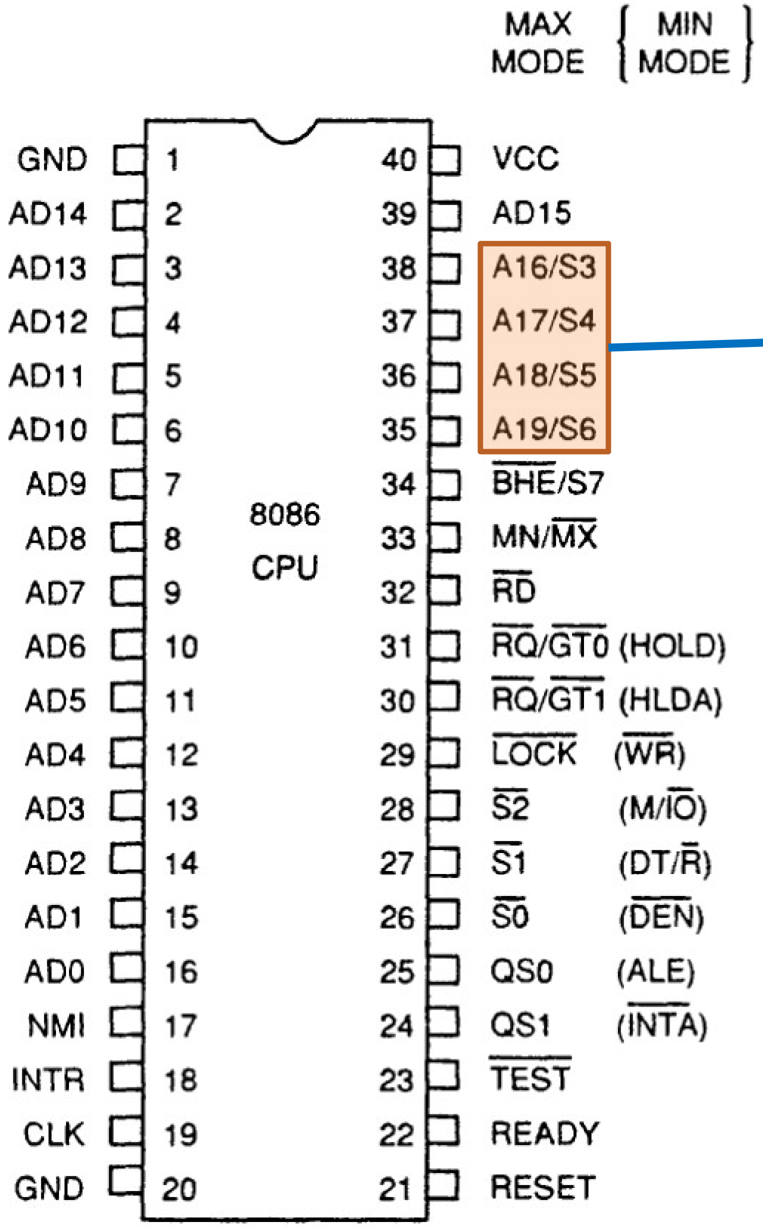
S6: Logic 0.

S5: Indicates condition of IF flag bits.

S4-S3: Indicate which segment is accessed during current bus cycle:



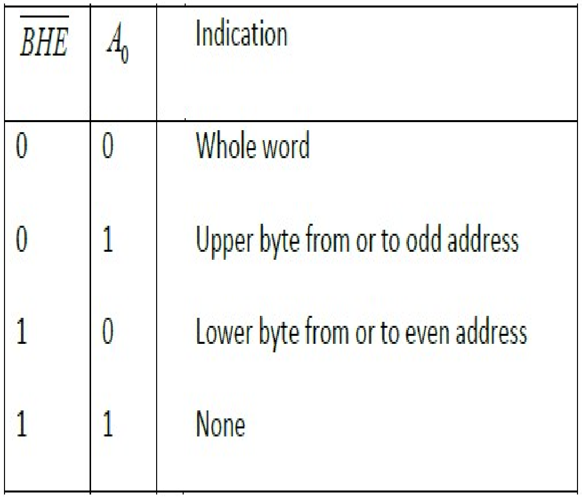
S4	S3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment



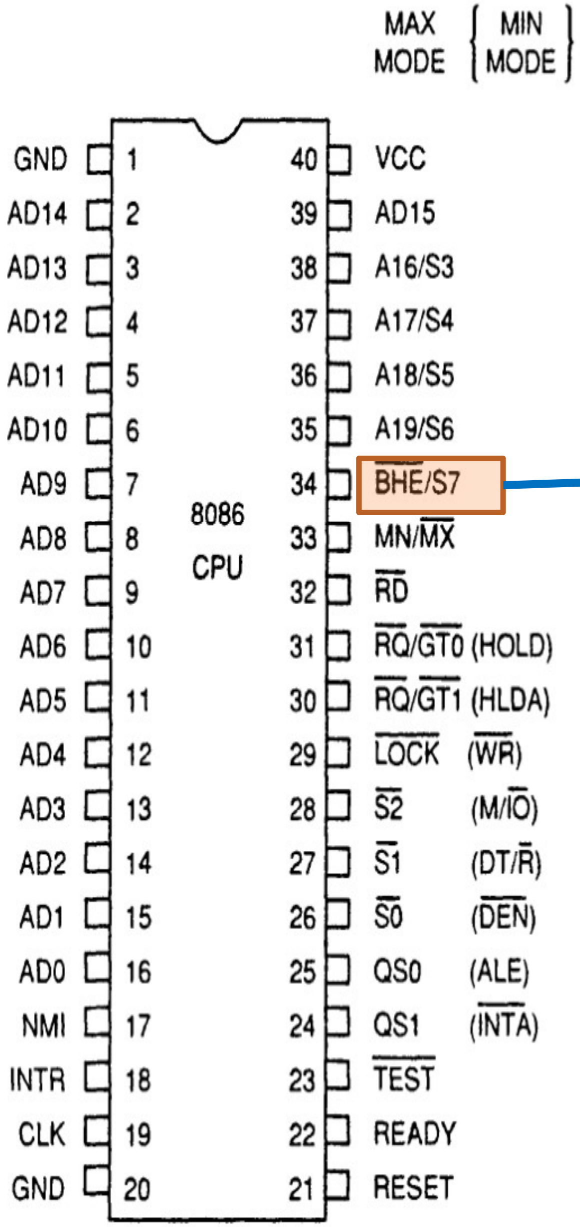
Address/Status Bus

Address bits A_{19} – A_{16} & Status bits S_6 – S_3

INTEL 8086 - Pin Details



$\overline{BHE}$	A_0	Indication
0	0	Whole word
0	1	Upper byte from or to odd address
1	0	Lower byte from or to even address
1	1	None



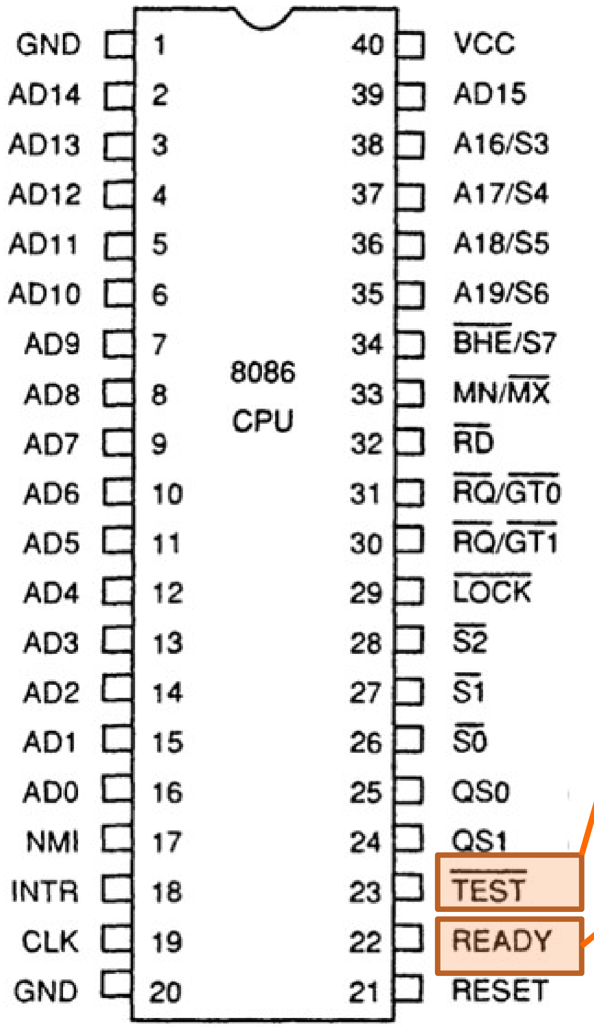
MAX MODE
MIN MODE
8086 CPU
GND 1 — 40 VCC
AD14 2 — 39 AD15
AD13 3 — 38 A16/S3
AD12 4 — 37 A17/S4
AD11 5 — 36 A18/S5
AD10 6 — 35 A19/S6
AD9 7 — 34 $\overline{BHE}$/S7
AD8 8 — 33 MN/$\overline{MX}$
AD7 9 — 32 $\overline{RD}$
AD6 10 — 31 $\overline{RQ}/\overline{GT0}$ (HOLD)
AD5 11 — 30 $\overline{RQ}/\overline{GT1}$ (HLDA)
AD4 12 — 29 $\overline{LOCK}$ ($\overline{WR}$)
AD3 13 — 28 $\overline{S2}$ (M/$\overline{IO}$)
AD2 14 — 27 $\overline{S1}$ (DT/$\overline{R}$)
AD1 15 — 26 $\overline{S0}$ ($\overline{DEN}$)
AD0 16 — 25 QS0 (ALE)
NMI 17 — 24 QS1 ($\overline{INTA}$)
INTR 18 — 23 $\overline{TEST}$
CLK 19 — 22 READY
GND 20 — 21 RESET

Bus High Enable/S7

Enables most significant data bits $D_{15} – D_8$ during read or write operation.

S_7: Always 1.

INTEL 8086 - PIN DETAILS



TEST(Pin No. 23)

-This i/p is examined by 8086 wait instruction

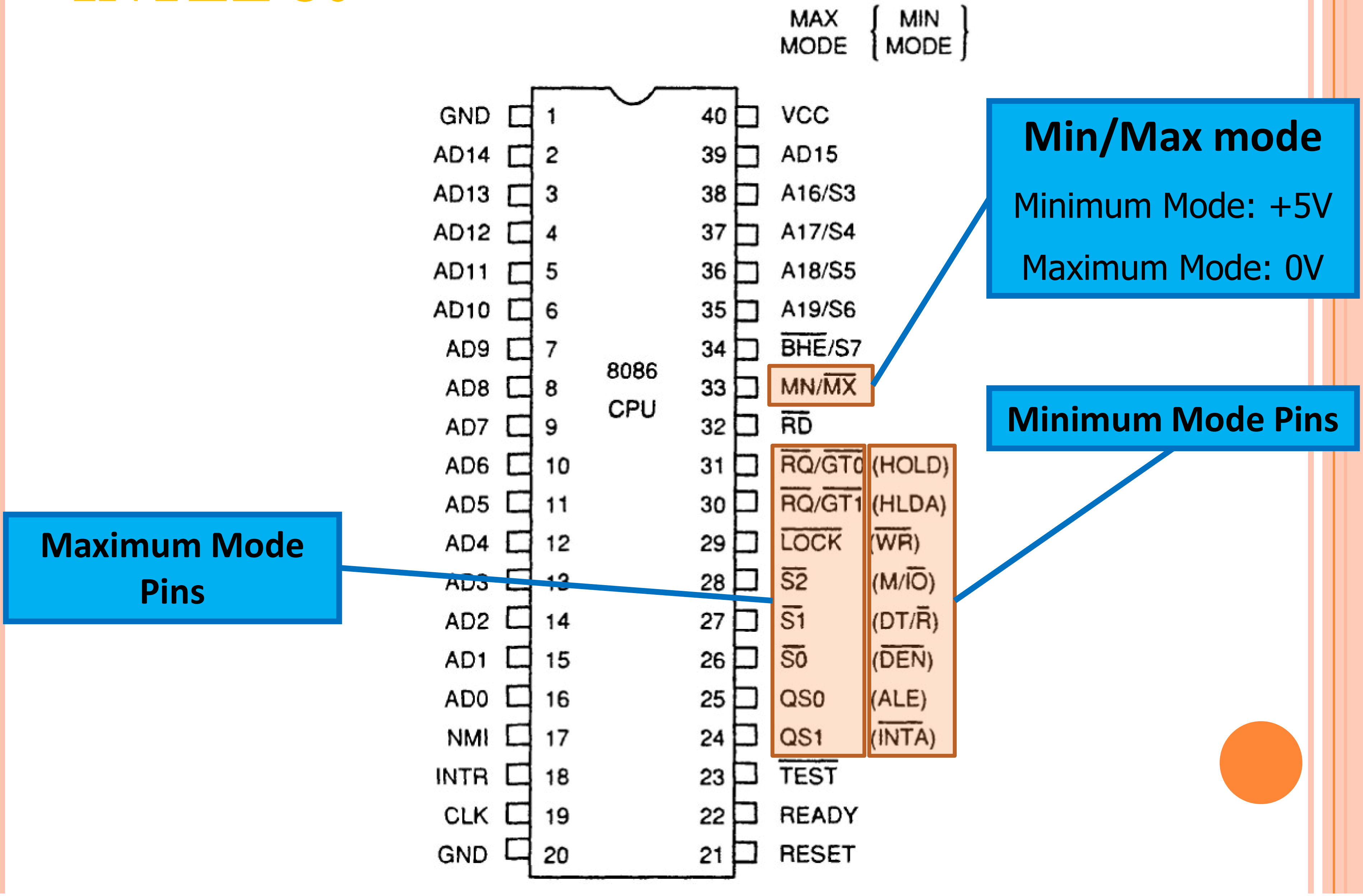
-If TEST i/p → low -→ execution continued --→ if not then processor enter /wait in idle state

Ready (pin no-22)

-When high--→ carry out it normal operation

-When low -→ freezes it's bus & enters a wait state

INTEL 8086 - Pin Details



Min/Max mode

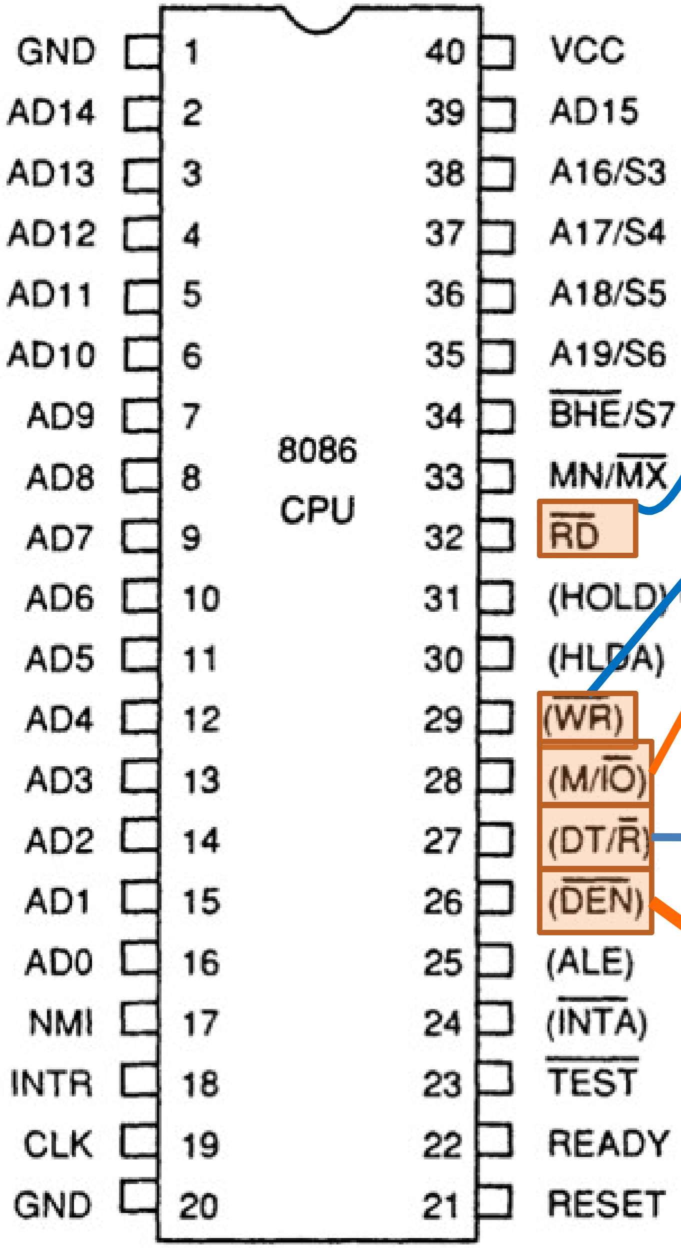
Minimum Mode: +5V

Maximum Mode: 0V

Minimum Mode Pins

Maximum Mode Pins

Minimum Mode- Pin Details



Read Signal

(The signal is used for read operation. It is an output signal.It is active when low)

Write Signal(asserted low Whenever processor writes data to memory or I/O port)

$M/\overline{IO}$

Used to differentiate memory access and I/O access. For memory reference instructions, it is high. For IN and OUT instructions, it is low.

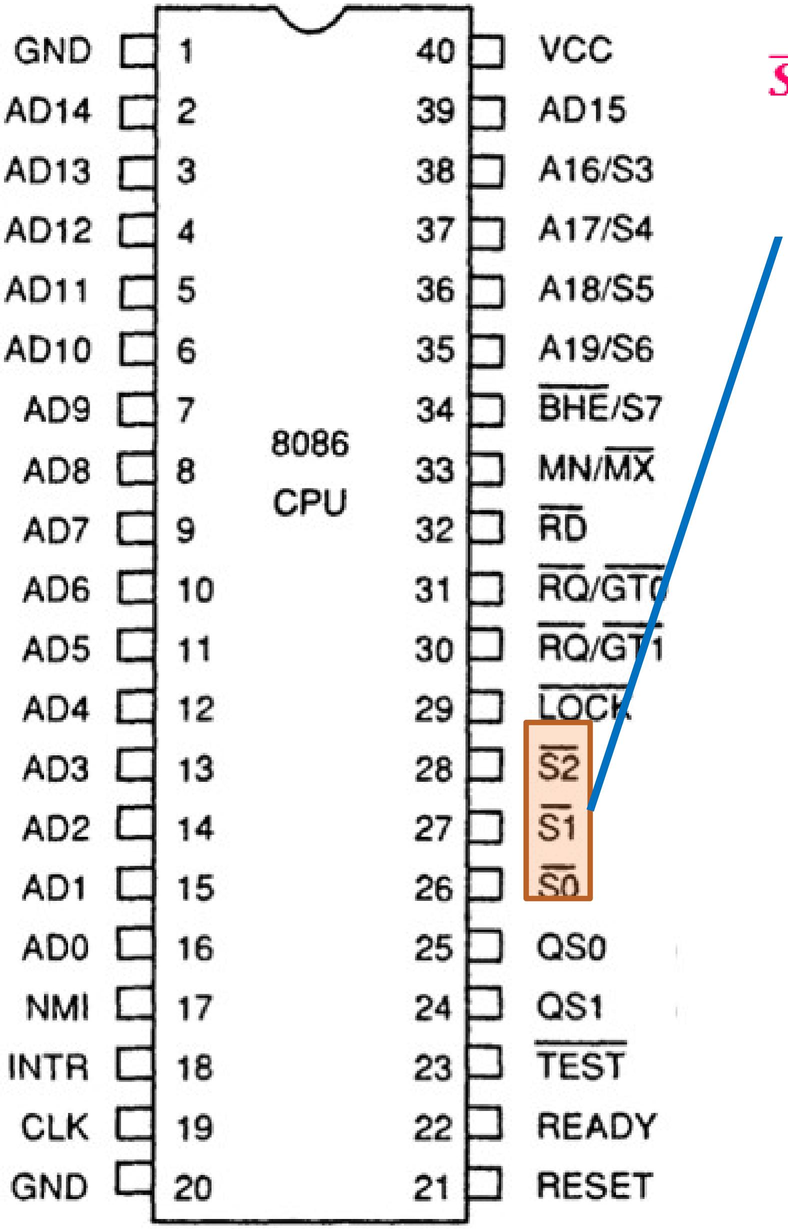
$DT/\overline{R}$

Data Transmit/ Receive) Output signal from the processor to control the direction of data flow through the data transceivers
High-data transmission, low-receiving data

$\overline{DEN}$

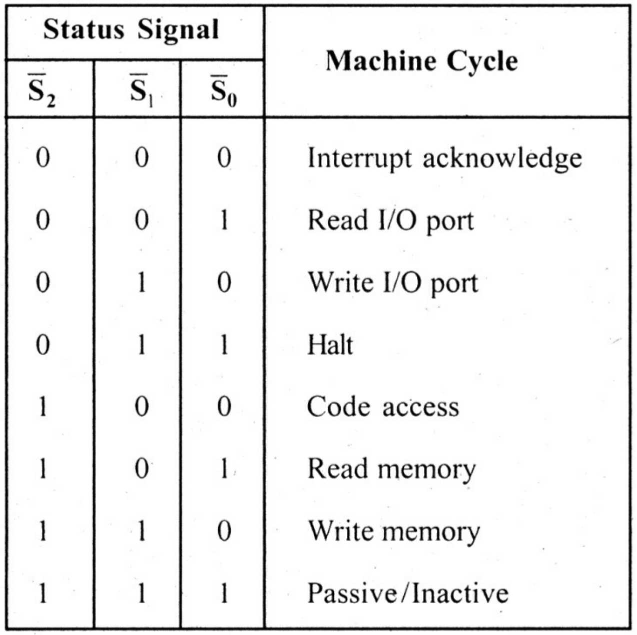
(Data Enable) Output signal from the processor used a out put enable for the transceivers.
It informs the transceivers that the processor is ready tc send or receive data.)

Maximum Mode - Pin Details



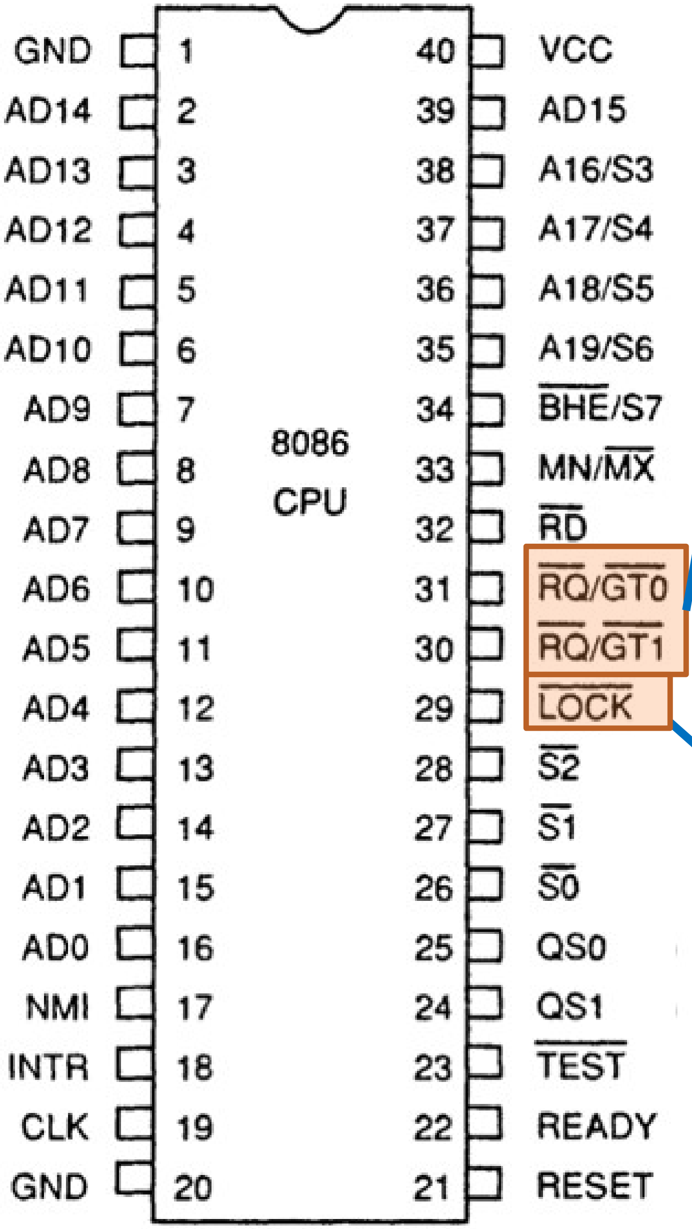
$\overline{S_0}, \overline{S_1}, \overline{S_2}$

Status signals; used by the 8086 bus controller to generate bus timing and control signals. These are decoded as shown.



Status Signal			Machine Cycle
$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive/Inactive

Pin Details

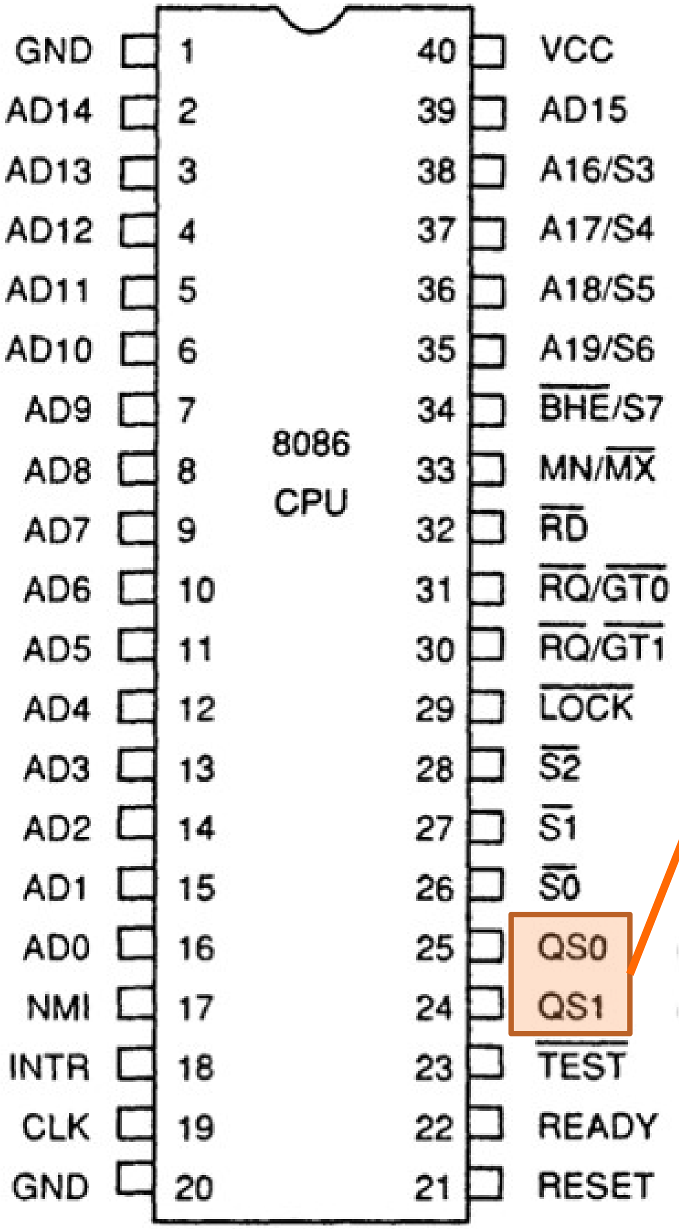


DMA Request/Grant

$\overline{RQ}/\overline{GT_0}$, $\overline{RQ}/\overline{GT_1}$	(**Bus Request/ Bus Grant**) These requests are u by other local bus masters to force the proces to release the local bus at the end of processor's current bus cycle. These pins are bidirectional. The request on $\overline{GT_0}$ will have higher priority thar $\overline{GT_1}$

$\overline{LOCK}$	An output signal activated by the LOCK instruction. Remains active until the completion of instruction prefixed by LOCK. The 8086 output low on the $\overline{LOCK}$ pin executing an instruction prefixed by LOC <u>prevent other bus masters from gaining cont the system bus.</u>

Maximum Mode - Pin Details

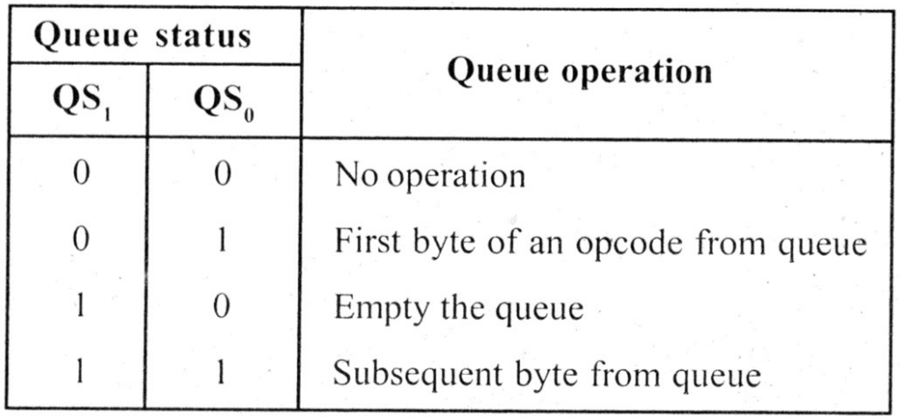


$\overline{QS_0}$, $\overline{QS_1}$

(Queue Status) The processor provides the stat of queue in these lines.

The queue status can be used by external device track the internal status of the queue in 8086.

The output on QS_0 and QS_1 can be interpreted shown in the table.



Queue status		Queue operation
QS_1	QS_0	
0	0	No operation
0	1	First byte of an opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue