SEM 2 – 5 (RC 07 – 08)

F.E. (Sem. – II) Examination, May/June 2010
BASIC ELECTRONICS ENGG.
(RC in 2007-08)

Duration: 3 Hours Total Marks : 100

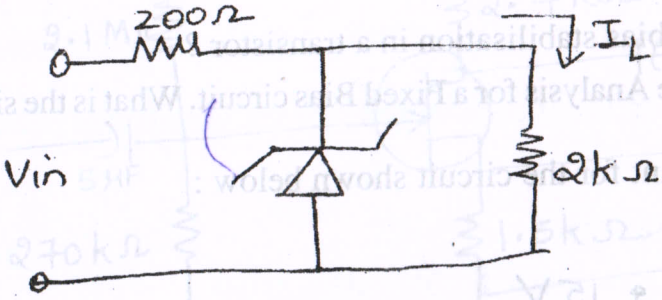
Instructions : *1) Attempt **any** 5 questions selecting at least **one** from **each** Module.*
*2) **Assume** suitable data only **if necessary**.*

MODULE – I

1. a) Draw the V-I characteristics of a p-n junction diode. Explain the piecewise linear equivalent circuit of a diode. **6**

   b) Explain the phenomenon of avalanche and zener breakdown in a diode. **6**

   c) Over what range of i/p voltage will the zener circuit shown maintain 30 V across the 2 kΩ load assuming that series resistance R = 200Ω. Zener current rating is 25 mA. **6**

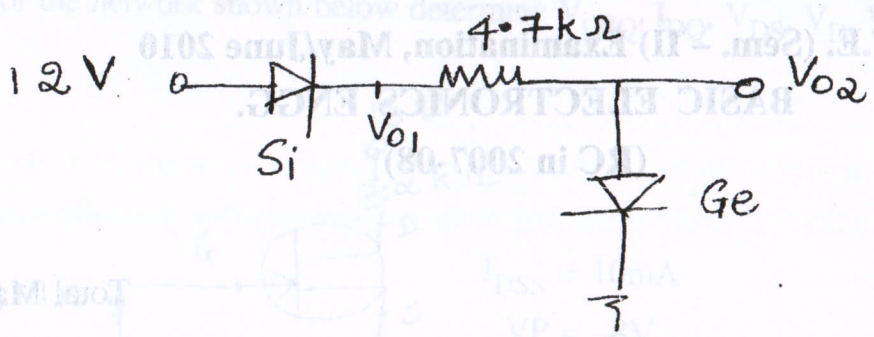


   d) What are the advantages of using a silicon diode over germanium diode ? **2**

2. a) With neat diagram explain the working of center-tapped full wave rectifier. Derive the expressions for Ripple factor, Ratio of rectification and T.U.F. **8**

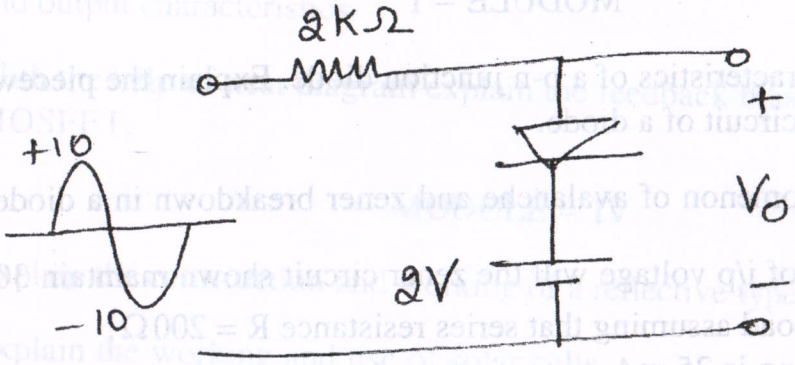
P.T.O.

b) Determine V_{01} and V_{02} for the network shown below : 4



c) A diode having internal resistance $R_f = 20\Omega$ is used for half ware rectification. The applied voltage at the input of the rectifier is $v = 50 \sin \omega t$ and $R_L = 800\Omega$. Find I_m, I_{dc}, I_{rms}, η, V_{dc} and T.U.F. 5

d) Determine the output for the following circuit for the input shown : 3



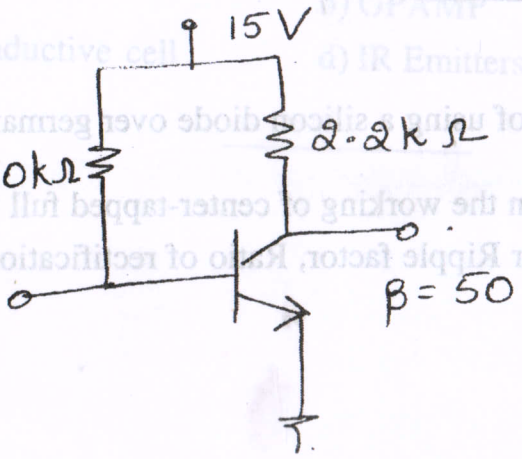
MODULE – II

3. a) Explain the CE configuration of a npn transistor. Draw the input and output characteristics. 6

b) What is the need for bias stabilisation in a transistor ? 4

c) Explain the Load Line Analysis for a Fixed Bias circuit. What is the significance of a load line. 5

d) Determine the Q point for the circuit shown below : 5



4. a) Explain the voltage divider biasing method for a transistor. **6**

b) Determine the stability factor $S(I_{co})$ for the emitter stabilised bias. **8**

c) Determine the stability factor $S(V_{BE})$ and change in I_C from 25°C to 100°C if corresponding V_{BE} are 0.65 and 0.48 respectively for the following bias arrangements :

a) Fixed bias $R_B = 240\ k\Omega$ and $\beta = 100$

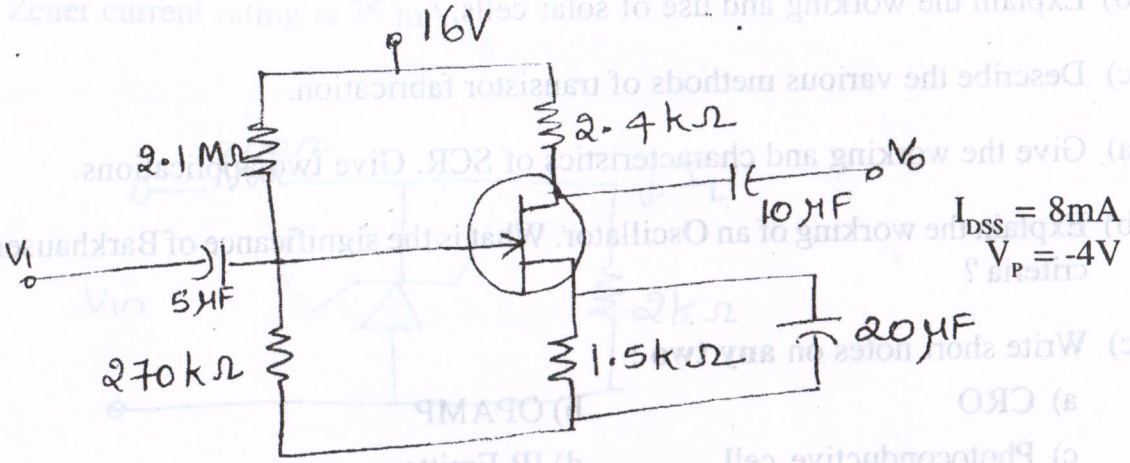
b) Emitter bias with $R_B = 240\ k\Omega$, $R_E = 1\ k\Omega$, $\beta = 100$

c) Emitter bias with $R_B = 47\ k\Omega$, $R_E = 4.7\ k\Omega$, $\beta = 100$ **6**

MODULE – III

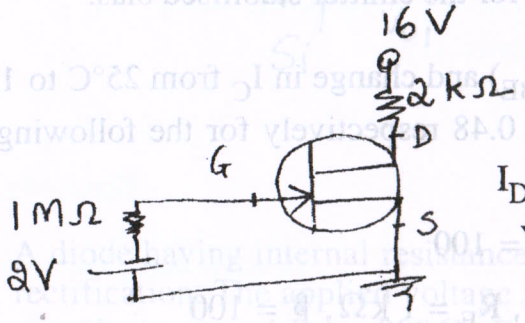
5. a) Explain the working and characteristics of a enhancement type n-channel MOSFET. **6**

b) Determine I_{DQ}, V_{GSQ}, V_D, V_S, V_{DS} and V_{DG} for the network shown below : **8**



c) With the help of neat diagram explain the self bias configuration of a JFET. **6**

6. a) For the network shown below determine V_{GSQ}, I_{DQ}, V_{DS}, V_D, V_G and V_S. **8**



I_{DSS} = 10mA

VP = –8V

b) Explain the working of a n-channel JFET. Draw the transfer characteristics and output characteristics. **7**

c) With the help of neat diagram explain the feedback biasing arrangement of a MOSFET. **5**

MODULE – IV

7. a) Explain the construction and working of a reflective type field effect LCD. **8**

b) Explain the working and use of solar cells. **6**

c) Describe the various methods of transistor fabrication. **6**

8. a) Give the working and characteristics of SCR. Give two applications. **7**

b) Explain the working of an Oscillator. What is the significance of Barkhausen's criteria ? **7**

c) Write short notes on **any two** : **6**

a) CRO b) OPAMP

c) Photoconductive cell d) IR Emitters.