SEM 2 – 5 (RC 07-08)

F.E. (Semester – II) (Revised in 2007-08) Examination, Nov./Dec. 2014
BASIC ELECTRONICS ENGINEERING

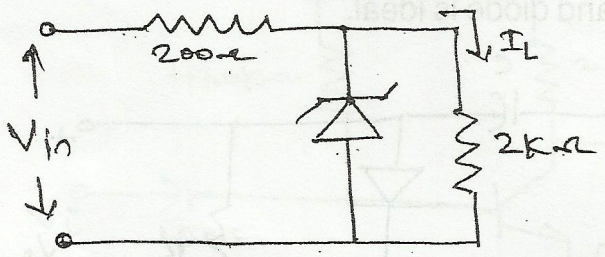
Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer **any 5** questions, selecting atleast **one** from **each** Module.*
*2) Make suitable assumptions **wherever** necessary.*

MODULE – I

1. a) Explain the effect of temperature on V I characteristics of diode. 4

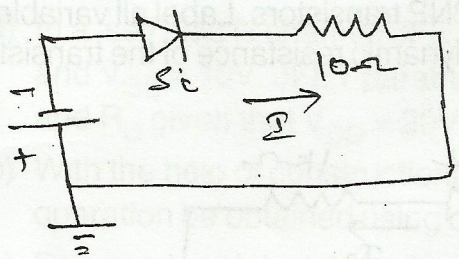
   b) Over what range of input voltage will zener circuit shown maintain 30V across 2KΩ load assuming series resistance R = 200Ω. Zener rating is 25mA. 6



   c) Why SI is preferred over Ge. 2

   d) Sketch a curve showing how the dynamic resistance of SI diode varies with voltage across the diode from 0V to 1V without using actual valves for resistance. Indicate cut in voltage and explain its significance in determining diode resistance. 5

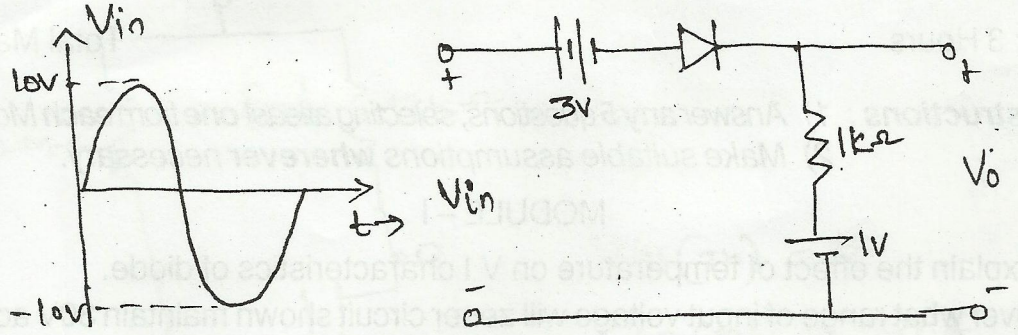
   e) Determine current I for the given configuration using approximate diode model. 3



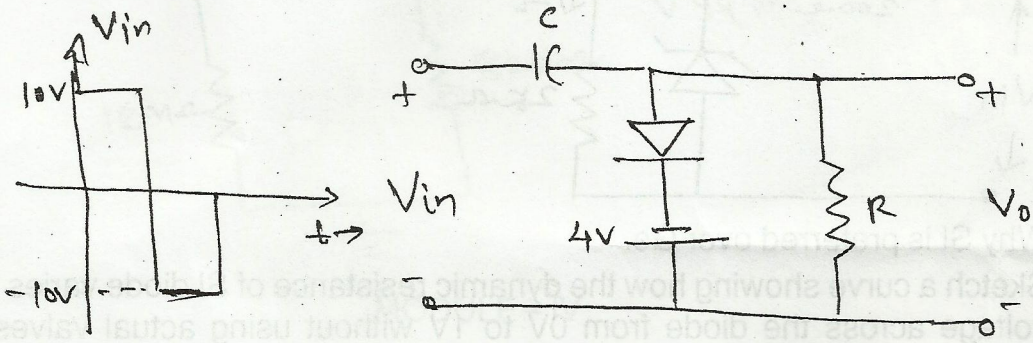
2. a) Explain why it is necessary to use filter in a power supply with the help of waveforms. Show the variation of output voltage with three different valves of capacitances. 5

   b) In a bridge rectifier R_1 = 1KΩ and each diode has a forward biased resistance rf = 10Ω. The voltage across each half of the secondary winding is 22 sin ωt. Determine :
   1) Im
   2) Idc
   3) Irms
   4) Ripple factor 5

c) Determine the output waveform for the following circuit for the input shown. Assume ideal diode. 4



d) Determine the output waveform for the following clamper circuit assuming RC time constant is very large and diode is ideal. 3

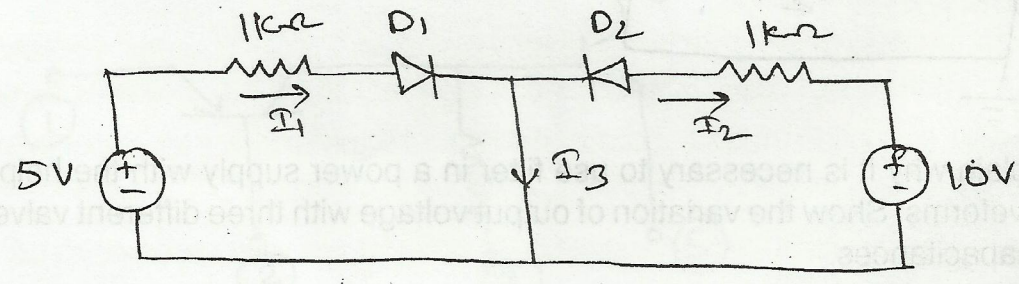


e) Draw and explain the operation of half wave voltage doubler. 3

MODULE – II

3. a) Sketch typical CB input characteristics for PNP transistors. Label all variables. Outline the procedure for calculating input dynamic resistance of the transistor at a given point from these curves. 7

b) 6



Prove with the help of above circuit that transistor action cannot be achieved by connecting two back to back diodes.

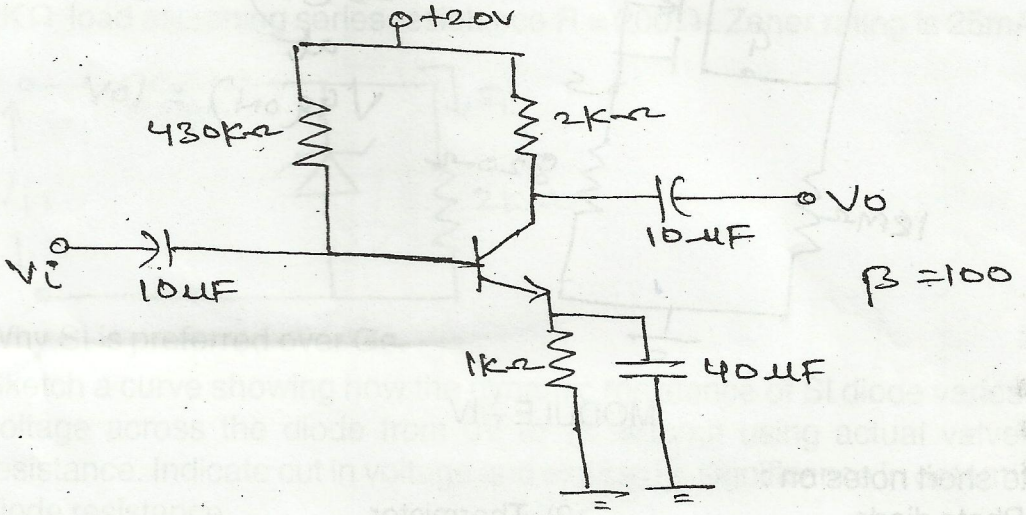
c) Explain how CE configuration can be used as an amplifier. Also explain why CE configuration is most widely used. 7

4. a) Draw collector current response of switching transistor. Define the various time intervals involved. 7

b) What is thermal run away and how it can be controlled using biasing techniques ? 5

c) For the given emmitter bias network determine. 8

a) I_B b) I_C
c) V_{CE} d) V_C
e) V_E f) V_B
g) V_{BC} h) I_{Csat}.



MODULE – III

5. a) In a self bias N channel JFET, the operating point is to be set at $I_D = 1.5$ mA and $V_{OS} = 10$V. JFET parameters are $I_{DSS} = 5$mA and $V_P = -2$V. Find R_s and R_D given that $V_{DD} = 20$V. 8

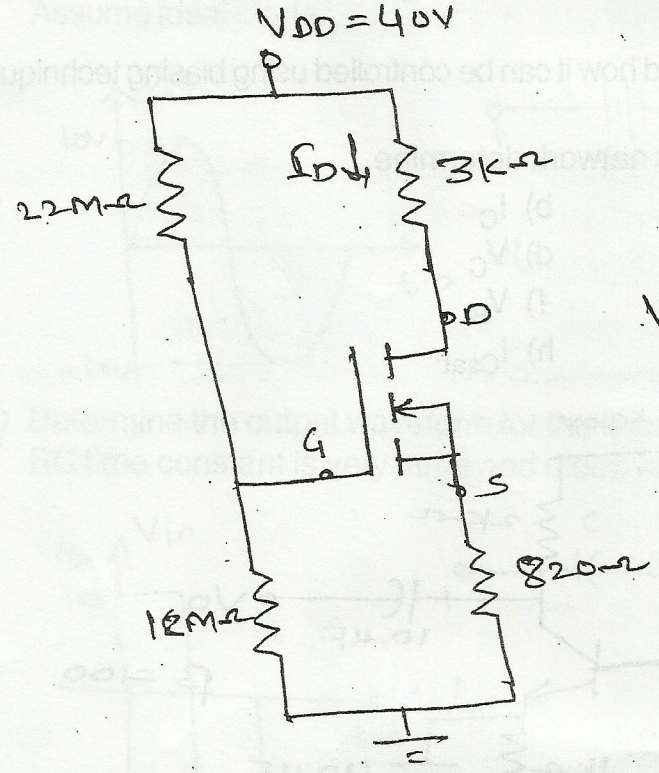
b) With the help of constructional diagram explain CMOS inverter. Can this operation be obtained using depletion type MOSFET ? Justify your answer. 6

c) Draw and explain output characteristics and transfer curve for depletion type PMOS. How can be the transfer curve obtained from output characteristics ? 6

6. a) Draw and explain drain characteristics of N channel enhancement type MOSFET. 7

b) Give atleast 3 precautions to be observed when handling a MOSFET that does not have any built in gate protection. 3

c) For the circuit shown in fig. Calculate V_G, I_D, V_{GS}, V_{DS}. 10

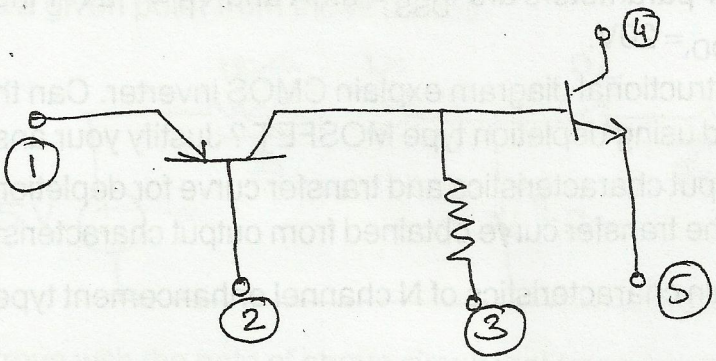


MODULE – IV

7. a) Write short notes on : 8
   1) Photo diode 2) Thermistor.

   b) Draw and explain internal block diagram of OPAMP. 6

   c) Design the monolithic I_C to implement the following schematic. Figure below shows the circuit to be built using monolithic approach. 6



8. a) Draw and explain the working of reflective type field effect LCD. What changes will you bring about to invert the display ? 7

   b) Draw and explain electron gun assembly in CRO. 7

   c) Explain the working of SCR using two transistor equivalent circuit. 6