F.E. (Semester – II) Examination, May/June 2013
BASIC ELECTRONIC ENGINEERING
(Revised 2007-08)

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer **five** questions, choosing atleast **one** from **each** Module.*
*2) Assume any additional data, if **required**.*
*3) Graph papers will be provided on **request**.*

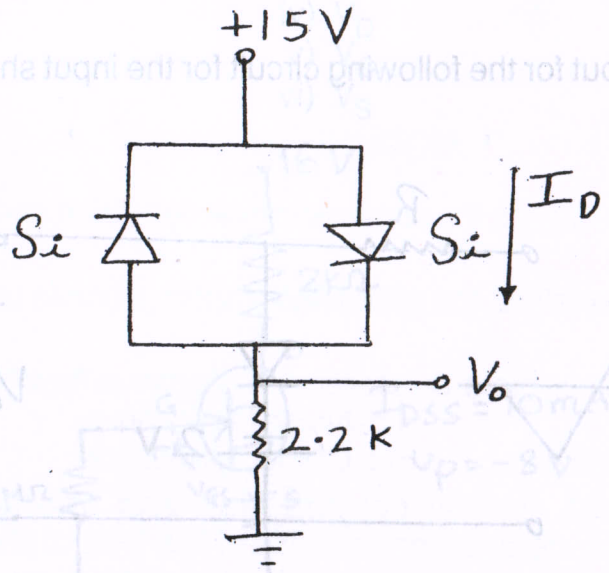
MODULE – I

1. a) Draw the V-I characteristics of a p-n junction diode and show how the dynamic resistance of the diode can be determined. **4**

   b) Differentiate between Zener breakdown and Avalanche breakdown. **4**

   c) What is transition capacitance of a diode ? Explain where it is used. **4**

   d) Find V_O and I_D for the given circuit. **2**



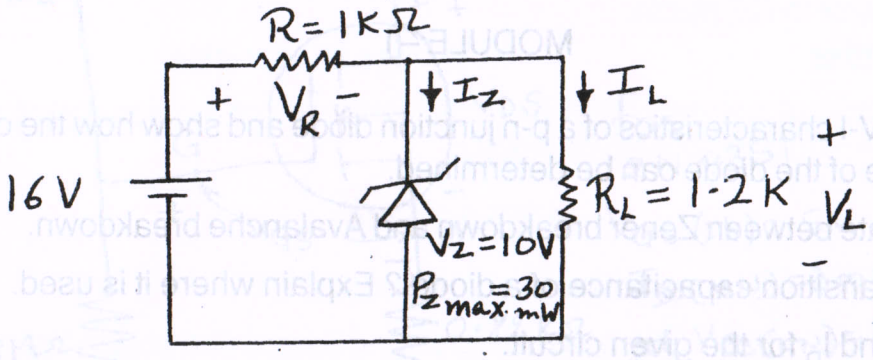
   e) Derive the transformer utilization factor for a half-wave rectifier and compare its value with that of a full-wave bridge rectifier. **6**

2. a) In a center-tap full wave rectifier, $R_L = 1\ k\Omega$ and each diode has a forward biased dynamic resistance $r_f = 10\ \Omega$. The voltage across each half of the secondary winding = 220 sin ωt. Determine :

   i) I_m ii) I_{dc} iii) I_{rms} iv) ripple factor **5**

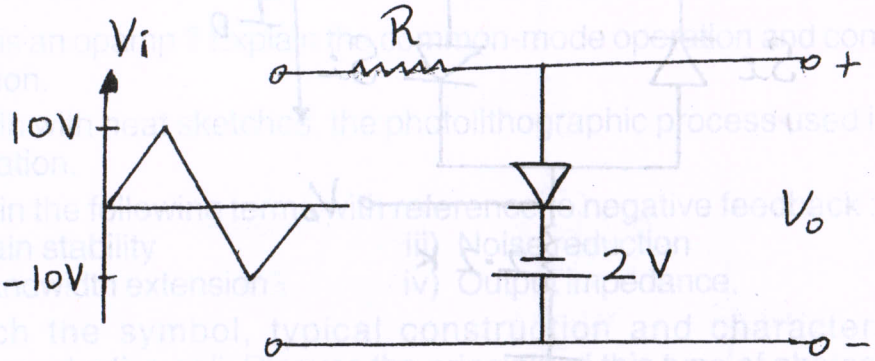
   b) Draw the circuit and input and output waveforms of a capacitor filter. Discuss the effect of the resistance and capacitance values chosen, on the output waveform. **4**

   c) For the Zener diode network shown, determine V_L and I_Z. **3**



   d) With the help of a neat diagram, explain the working of an unbiased positive clamper and draw the input and output waveforms for a 12 V_{p-p} sinusoidal input. **5**

   e) Determine the output for the following circuit for the input shown. Assume ideal diode. **3**



MODULE – II

3. a) Distinguish between the emitter, base and collector regions of a transistor. Derive the relationships between the current gains of Common Base (CB) and Common Emitter (CE) transistors. **6**

b) With the help of a circuit and waveforms, explain how a transistor can be used as an amplifier. Obtain the expression for voltage gain. 8

c) Draw the circuit setup and explain how the static input characteristics of a CE (pnp) transistor are plotted. 6

4. a) Using neat sketches and equations, explain how the graphical load line analysis is employed to determine the operating point for a CE (npn) transistor having emitter bias resistor. 6

b) With neat diagrams, analyze the following BJT biasing configurations using suitable mathematical expressions and compare the two techniques. Assume the transistor in CE mode.

i) Fixed Bias ii) Voltage Divider Bias. 8

c) With the help of a sketch, define the time intervals of a pulse waveform encountered in a switching transistor. 6

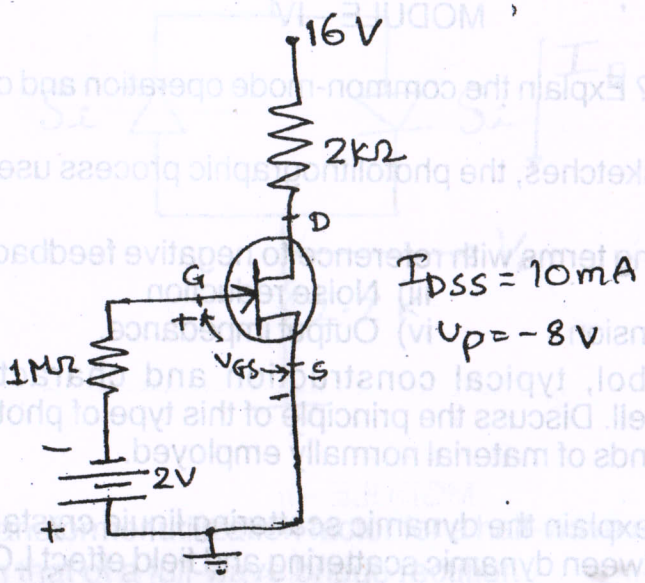
MODULE – III

5. a) i) Draw the basic construction of a p-channel JFET.

ii) Apply the proper biasing between drain and source and sketch the depletion region for $V_{GS} = 0V$ and $V_{DS} > 0$. 7

b) Determine the following for the network of fig. below : 7

i) V_{GSQ}
ii) I_{DQ}
iii) V_{DS}
iv) V_D
v) V_G
vi) V_S



c) Sketch the transfer and drain characteristics of an n-channel depletion type MOSFET with $I_{DSS} = 12$ mA and $V_P = -8$ V for a range of $V_{GS} = -V_P$ to $V_{GS} = 1$ V. 6