Total No. of Printed Pages:4

F.E. Semester-II (Revised Course 2007-08)
EXAMINATION OCTOBER 2020
Basic Electronics Engineering

[Duration : Two Hours] **[Total Marks :60]**

Instructions:- 1) Answer THREE FULL QUESTIONS with ONE QUESTION from ANY THREE MODULES.
2) Make suitable assumption, if required.

Module – I

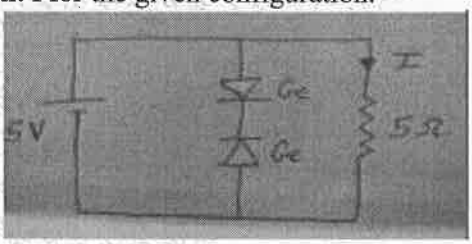
Q1. a) Explain the formation of the depletion region in a pn diode. **(4)**

b) Plot the V – D characteristics of a pn junction diode and define static resistance from the curve. How does reverse satination cement vary with temperature? **(5)**

c) Briefly explain the concept of transition and diffusion capacitances associated with pn diode and draw the relevant graph illustrating how there capacitances vary with the applied bias. **(6)**

d) Discuss the Zener breakdown mechanism. What the effect is of increased in temperature on zener breakdown voltage? **(5)**

Q2 a) Determine the current I for the given configuration. **(2)**



2 b) A voltage v=7.1 sinwt is applied across each half of the secondary winding of a centre tapped full wave rectifier. Assuming ideal diodes, if the resistance of the half secondary winding is 1.5Ω and the load resistance is 1K Ω, determine:
i) DC voltage
ii) Peak and DC current
iii) DC power delivered to the load. **(4)**

2 c) Discuss the effect of resistance and capacitance values chosen on the output waveform of a C-filter. **(2)**

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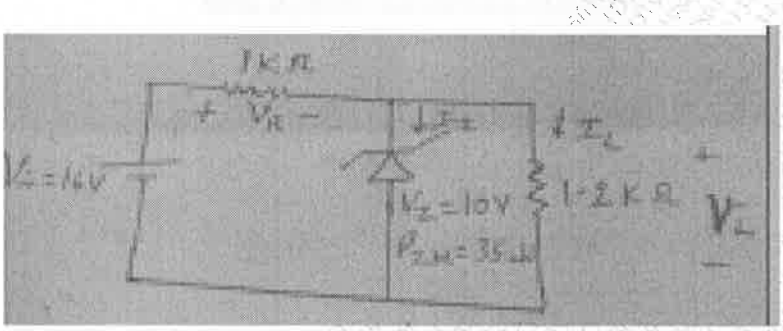
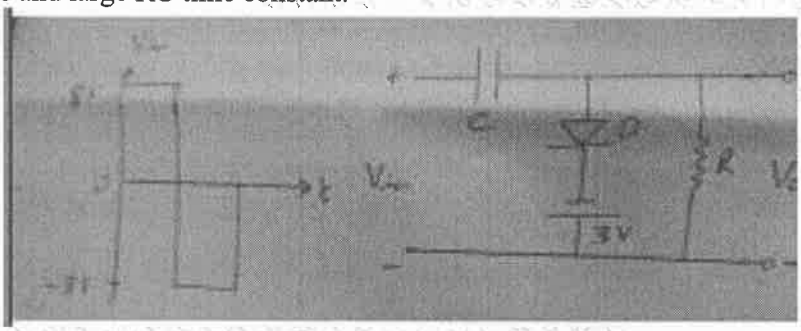
2 d) For the given zener diode network, find V_L, V_R and I_Z **(3)**



2 e) Draw and explain the circuit of a negative clipper with output waveform. **(2)**

2 f) Determine the output waveform for the following clamper circuit assuming ideal diode and large RC time constant. **(4)**



2 g) Draw the circuit diagram and waveforms of a halfwave Voltage Doubler **(3)**

Module – II

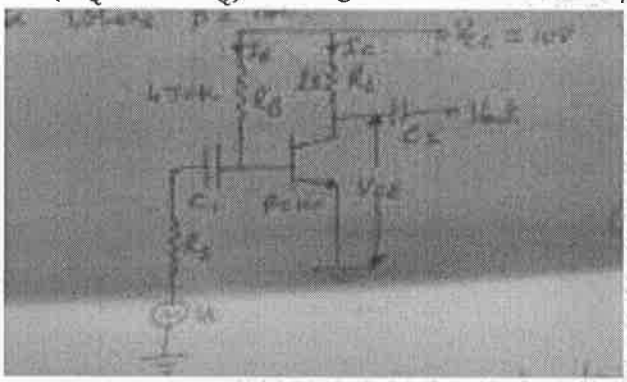
Q3 a) When the emitter current of a transistor is changed by 1mA, its collector current changes by 0.995 mA. Calculate
i) Its common base current gain $\propto$
ii) Its common emitter current gain β. **(4)**

3 b) Draw the laboratory (circuit) setup of a CB pnp transistor and explain how the static output characteristics are plotted. Find the output resistance from the curves. **(8)**

3 c) Explain how a CE transistor can be used as an amplifier. **(6)**

3 d) Identify and label the limits of operation on the output characteristics of a CE amplifier **(2)**

4 a) Find the Q-point (IC_Q and VCE_Q) for the give si transistor where $\beta = 100$ **(6)**



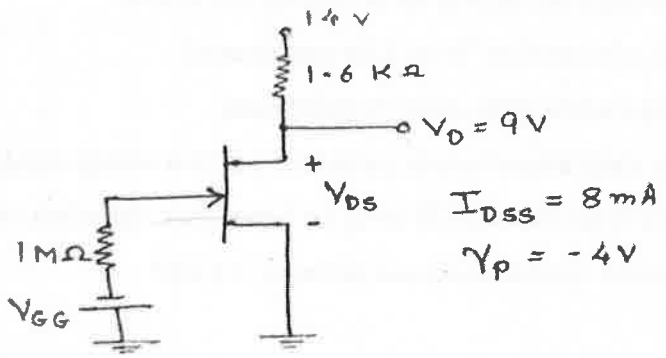
4 b) What is the need for bias stabilization? Define Stability Factor S. Which bias circuit has the highest 'S' factor? Derive it. **(8)**

4 c) With the help of a sketch, define the time intervals of a pulse waveform encountered in a switching transistor. **(6)**

Module – III

Q5. a) With the help of a neat diagram, explain the operation of a n- channel JFET. Show the internal depletion region and explain their shapes. **(8)**

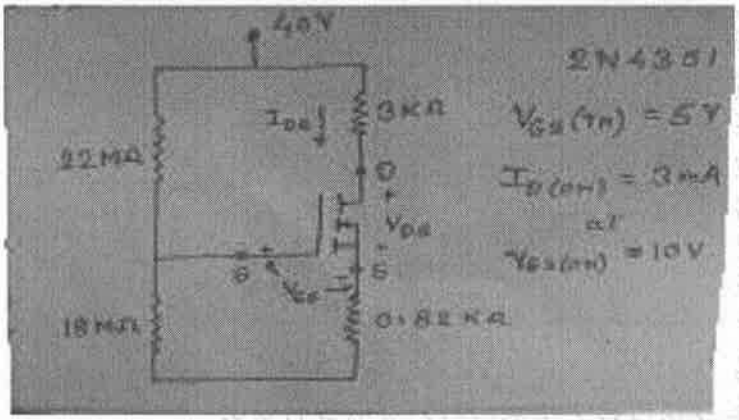
b) For fired bias Configuration given below. Determine V_{DS}, V_{GG} and V_{GSQ} by using graphical approach:
Given: $V_D = 9V, I_{DSS} = 8mA, V_P = -4V$



(7)

c) Explain why JFET is called a voltage controlled device? A p-Channel JFET has device parameter of $I_{DSS} = 6$ mA and $V_P = +6V$ and $V_P = +6V$.
Sketch transfer characteristics. **(5)**

Q6. a) Determine I_{DQ}, V_{GSQ} and V_{DS} for the Circuit shown below: **(8)**



b) Differentiate between the following:
i) BJT and JFET
ii) DMOSFET and EMOSFET **(4)**

c) If gate to source voltage is n-channel DMOSFET is made more positive, does drain Current increase beyond I_{DSS} or it decrease?
Justify your answer with reason. **(4)**

d) Explain with the help of a diagram the basic CMOS operation. **(4)**

Module – IV

Q7. a) Explain various steps involved in fabrication of Monalithic ICs. **(10)**

b) Draw and explain the internal block diagram of OPAMP. **(6)**

c) Explain Nyguist criterion. What is its significance? **(4)**

Q8. a) Explain dark current with respect to photodiode. **(4)**

b) Explain the application of photo conductive cell in a voltage regulator. **(5)**

c) Describe the behaviour of SCR using the 2 transistor equivalent circuit. **(6)**

d) How is internal synchronization is achieved in CRO? **(5)**