SEM 2 – 5 (RC 07 – 08)

F.E. (Semester – II) (RC) Examination, Nov./Dec. 2016
BASIC ELECTRONICS ENGINEERING

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Attempt **any five** questions with atleast **one** question from **each** Module.*
*2) Assume suitable data **if necessary**.*
*3) **Neat** diagrams should be drawn **wherever** necessary.*
*4) Figures to the **right** indicate **full** marks.*

MODULE – I

1. a) With the help of a neat diagram of a V/I characteristic, explain the working of a PN junction diode. Also explain the following terms :
   i) Reverse saturation current
   ii) Cut-in or knee voltage of the diode. **7**

   b) Differentiate between Zener and Avalanche breakdown. **3**

   c) Find V_o for the circuit. Given in Fig. 1 (c) **4**

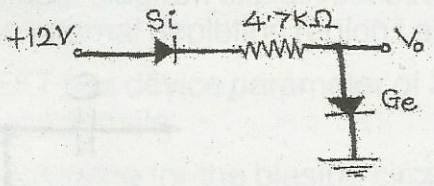

Fig. 1(c)

   d) With the help of neat diagram, explain the working of a Half Wave Voltage Doubler. Draw input and output voltage waveforms. **6**

2. a) For the Zener diode network given in Fig. 2(a), determine V_L, V_R, I_Z, P_Z. Given V_i is 16 V, R_L is 3 KΩ , V_Z is 10 V and P_{ZM} is 30 mW. **5**

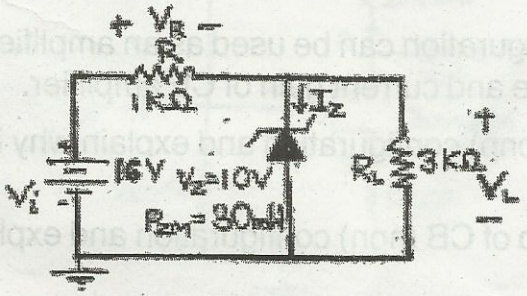

Fig. 2(a)

b) The turns ratio of a transformer used in a half wave rectifier is n1 : n2 = 10 : 1. The primary is connected to the power mains : 220 V, 50 Hz. Assuming the diode resistance in forward bias to be zero, calculate :

i) dc voltage across the load

ii) dc current through the load of 2.2 KΩ

iii) PIV of the diode. 5

c) Determine the output for the following circuit with the input waveform shown in Fig. 2(c). 5

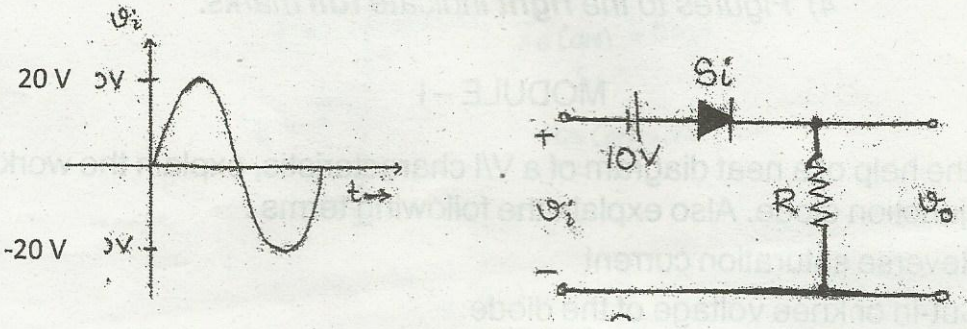

Fig.2(c)

d) Sketch the output waveform for the circuit shown in Fig. 2(d). 5

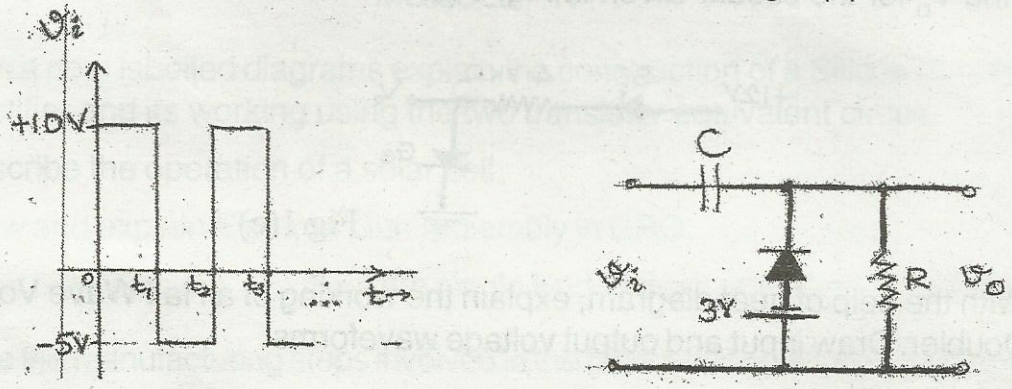

Fig.2(d)

MODULE – II

3. a) Explain how CE configuration can be used as an amplifier. Also derive the expression for voltage and current gain of CE amplifier. 7

b) Draw CC transistor (pnp) configuration and explain why it is not used as a voltage amplifier. 3

c) Draw the circuit setup of CB (npn) configuration and explain its output characteristics. 7

d) Explain why two back to back connected diodes cannot be used as a transistor. 3

4. a) For the biasing circuit shown in Fig. 4 (a) determine : 6

i) I_b ii) V_c iii) I_c

iv) V_e v) V_{ce} vi) V_b

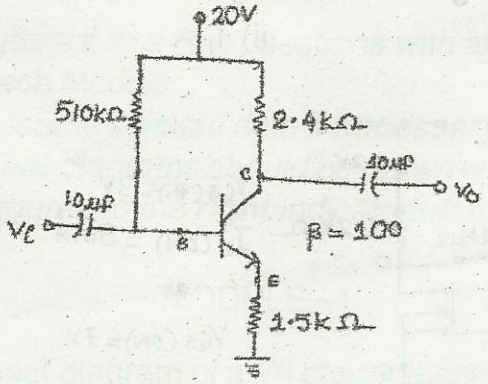

Fig.4(a)

b) Derive the stability factor $S(I_{CO})$ for Emitter stabilized bias circuit. 8

c) Explain the working of a transistor as a switch. 6

MODULE – III

5. a) With the help of neat diagram explain construction and operation of n channel JFET. Show the internal depletion regions and explain their shapes. 8

b) A P-channel JEFT has device parameter of $I_{DSS} = 9$ mA and $V_p = 5$V. Sketch the transfer characteristic. 4

c) Determine the following for the biasing circuit given in Fig. 5(c) : 8

i) V_{GSQ} ii) I_{DQ}

iii) V_{DS} iv) V_S

v) V_G

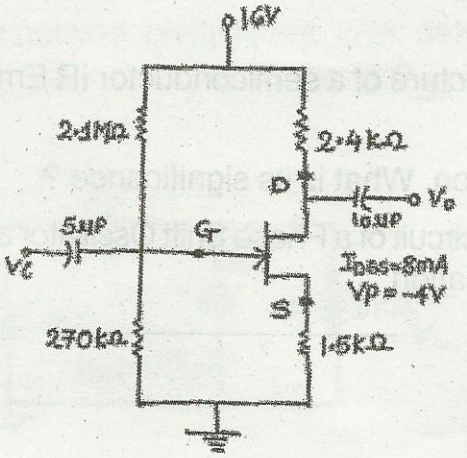

Fig.5(c)

6. a) With the help of neat sketches explain construction and output characteristic of n channel depletion type MOSFET. 8

   b) Write a short note on CMOS as an inverter. 6

   c) Determine the following for the biasing circuit given in Fig. 6(c). 8

      i) V_{GSQ} ii) I_{DQ}

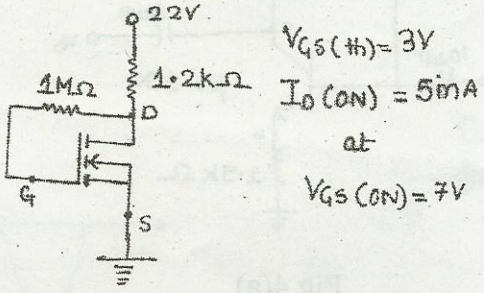

Fig.6(c)

MODULE – IV

7. a) With a neat labelled diagrams explain the construction of a Silicon Controlled Rectifier and its working using the two transistor equivalent circuit. 6

   b) Describe the operation of a solar cell. 4

   c) Draw and explain Electron Gun Assembly in CRO. 6

   d) What is an op-amp ? Explain the single Ended input operation of an op-amp. 4

8. a) Give the manufacturing steps involved in the fabrication of diode in a Monolithic IC. 5

   b) Draw the general structure of a semiconductor IR Emitter diode and explain its working. 5

   c) Define Nyquist criterion. What is its significance ? 5

   d) Draw and explain the circuit of a Phase Shift Oscillator and write the expression for frequency of oscillation. 5