FE215

Total No. of Printed Pages:3

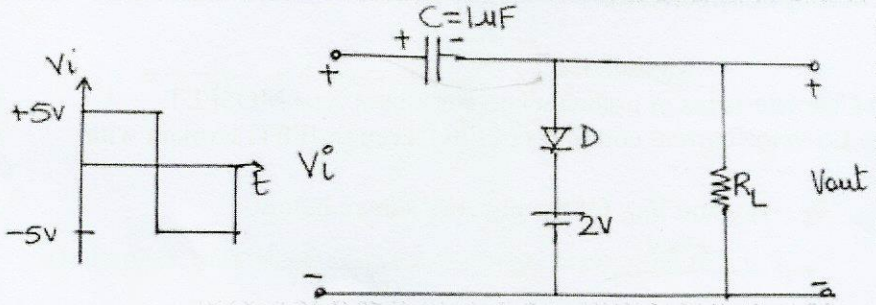
F.E. Semester-II (Revised Course 2007-2008)
EXAMINATION MAY/JUNE 2019
Basic Electronic Engineering

[Duration : Three Hours] **[Max. Marks : 100]**

Instructions:
1. Attempt any five questions choosing at least one question from each module.
2. Assume suitable data only if necessary.

Module I

Q.1 a) Explain Load line analysis and find the point of operation on the diode characteristics. **06**
b) Show that the maximum Rectification Efficiency of a Half wave Rectifier is 40.6%. **10**
c) Sketch the output waveform for the circuit show in fig below assuming RC time constant is very large and diode is ideal. **04**



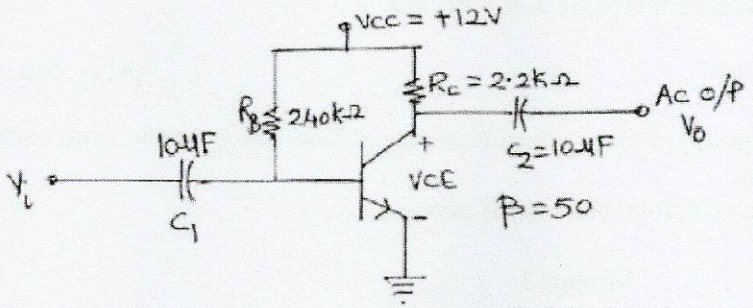
Q.2 a) Explain the following terms i) Transition Capacitance ii) Diffusion capacitance **04**
b) In a center tap full wave rectifier RL = 1 KΩ and each diode has a forward biased dynamic resistance rf = 10 Ω. The voltage across each half of the secondary winding is 220sinwt. Determine 1m, ldc, lrms and ripple factor. **05**

c) Explain why it is necessary to use a voltage regulator circuit in the power supply. **06**
d) Draw V-I characteristics of PN junction diode. Explain Piecewise linear equivalent circuit of a diode. **05**

Module II

Q.3 a) What is the need for biasing a transistor. Explain any one technique of transistor biasing. **08**
b) Draw the circuit setup of Common base (NPN) transistor configuration and explain how its input and output characteristics are plotted. **08**
c) What do you mean by stabilization of operating point? Explain the reasons why stabilization of Q point is necessary. **04**

Q.4 a) Determine the following for the network given in fig a) I_{BQ} and I_{CQ} b) V_{CEQ} c) V_B and V_C d) V_{BC} **06**



b) Explain the amplifying action of Bipolar junction Transistor. **05**

c) Draw the circuit setup and explain how the static input characteristics of a CE transistor are plotted. **05**

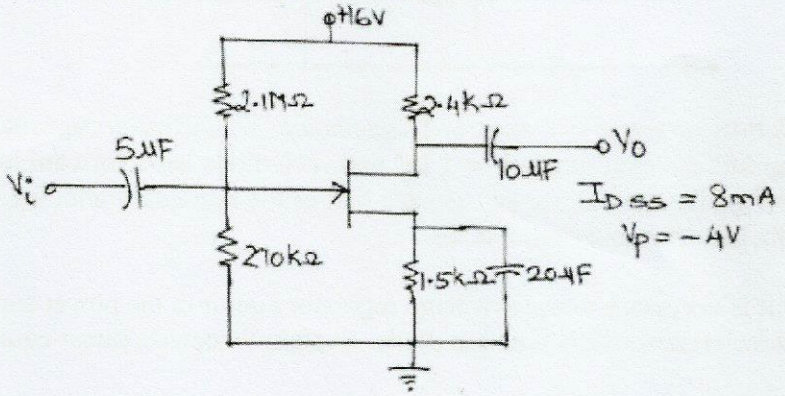
d) Explain Fixed bias BJT biasing configuration. **04**

Module III

Q.5 a) Draw and explain Drain Characteristics of n-channel enhancement type MOSFET **06**

b) Even after Pinch off Condition the current continues to flow through JFET. Explain with relevant diagrams. **06**

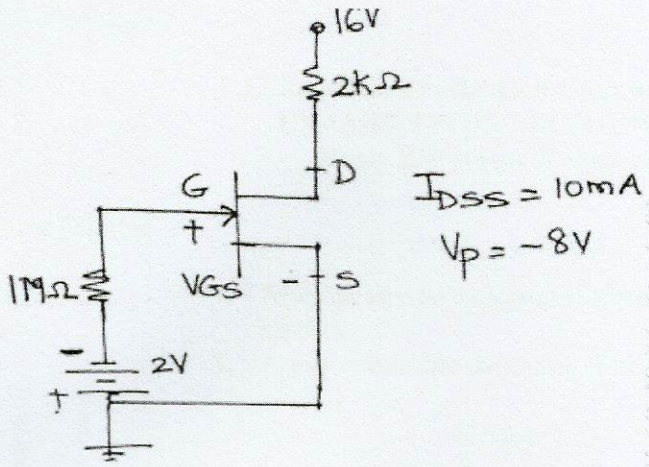
c) Determine I_{DQ}, V_{GSQ}, V_D, V_S, V_{DS} and V_{DG} for the network shown below. **08**



Q.6 a) Explain the operation of an N-channel JFET. Show the internal depletion regions and explain their shape. **08**

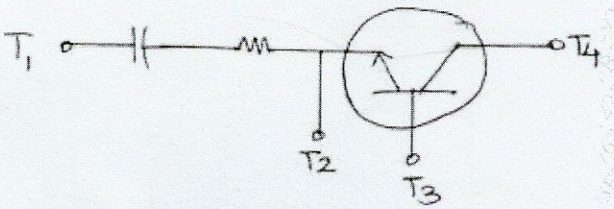
b) Explain with the help of diagram the basic CMOS operation. **06**

c) Determine the following for the network shown in fig below i) V_{GSQ} ii) I_{DQ} iii) V_{DS} iv) V_D v) V_G vi) V_S **06**



Module IV

Q.7	a)	Write short notes on (Any two) i) Solar cell ii) IR emitter iii) Thermistor	**08**
	b)	Design a monolithic IC to implement the following schematic	**06**



	c)	Explain with block diagram the trigger operation of CRO.	**06**
Q.8	a)	Draw and explain Internal block diagram of OP-AMP	**05**
	b)	Explain the working of SCR using two transistor equivalent circuit.	**05**
	c)	Draw and explain the working of Reflective type field effect LCD.	**06**
	d)	Draw and explain Electron gun assembly used in CRO	**04**