SEM 2 – 5 (RC 07-08)

F.E. (Semester – II) (RC) Examination, May/June 2016
BASIC ELECTRONICS ENGINEERING

Duration : 3 Hours

Total Marks : 100

Instructions : *1) Answer **any five** questions with **atleast one** question from **each** Module.*
*2) Assume suitable data **if necessary**.*
*3) **Neat** diagrams should be drawn **wherever** necessary.*
*4) Figures to the **right** indicate **full** marks.*

MODULE – I

1. a) Explain the construction and working of a PN junction diode with necessary diagrams. **8**

   b) Why is Silicon preferred over Germanium for semiconductor device fabrication ? **2**

   c) Find V_0 for the circuit given in Fig. 1 (c). **4**

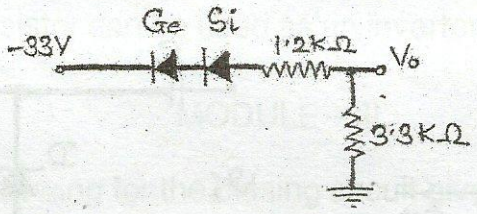

Fig. 1 (c)

   d) With the help of neat diagram, explain the working of a Full Wave Voltage Doubler. Draw the waveform for input and output voltage. **6**

2. a) Determine the range of values of V_i that will maintain the Zener diode in the ON state for the circuit shown in Fig. 2 (a). **5**

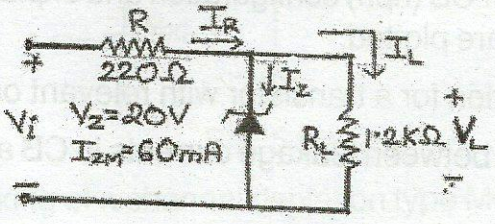

Fig. 2 (a)

b) Draw a Center tapped Full wave rectifier circuit and derive the expression for : **5**

i) Ratio of rectification ii) Transformer Utilization factor.

c) Determine the output for the following circuit shown in Fig. 2 (c). **5**

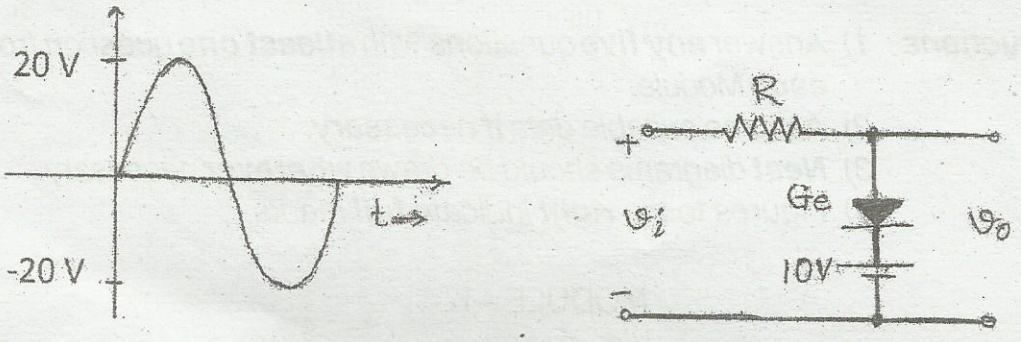

Fig. 2 (c)

d) Sketch the output waveform for the circuit shown in Fig. 2 (d). **5**

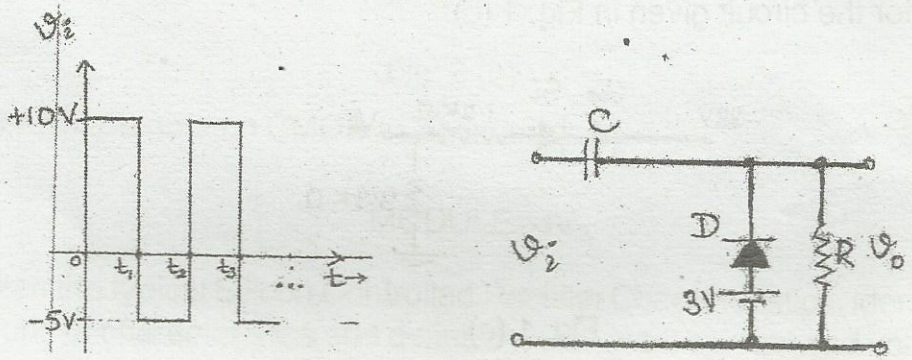

Fig. 2 (d)

MODULE – II

3. a) Draw the circuit setup of CB (npn) configuration and explain how its input and output characteristics are plotted. **7**

b) Explain limits of operation for a transistor with relevant output characteristic. **5**

c) Derive the relationship between leakage currents in CB and CE transistor configuration. **4**

d) Calculate the values of collector current and emitter current for a transistor with $\alpha_{dc} = 0.98$ and $I_{CBO} = 5\mu$ A. The base current is measured as 100μ A. **4**

4. a) Derive the stability factor $S(I_{CO})$ for Fixed bias circuit. 4

b) For the biasing circuit given in Fig. 4 (b) determine : 6

i) I_b ii) V_c iii) I_c iv) V_e v) V_{ce} vi) V_b.

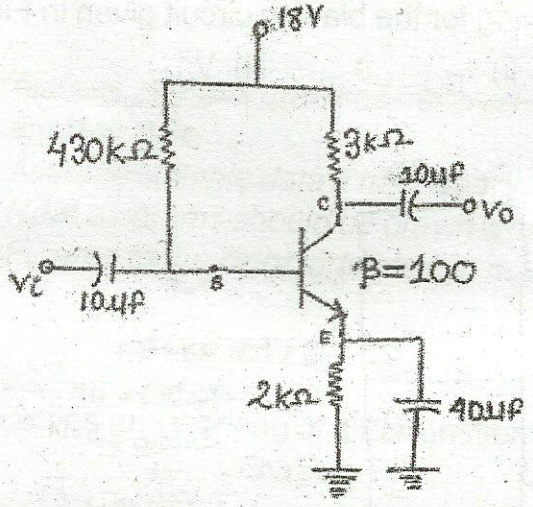

Fig. 4 (b)

c) What is the need for biasing a transistor ? 4

d) Explain how transistor can be used as an inverter ? 6

MODULE – III

5. a) Determine the following for the biasing circuit given in Fig. 5 (a) : 5

i) V_{GSQ} ii) I_{DQ} iii) V_{DS} iv) V_S v) V_D.

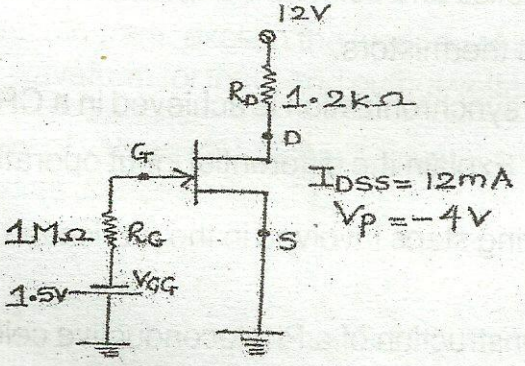

Fig. 5 (a)

b) Explain the working of n channel depletion type MOSFET. Also draw output and transfer characteristics for n channel depletion type MOSFET. 8

c) With the help of neat diagram and set of equations explain the self-bias circuit of JFET. 7

6. a) In general comment on the polarity of various voltage and direction of currents for an n channel JFET versus P channel JFET, with the help of neat labeled sketches. 6

b) Determine the following for the biasing circuit given in Fig. 6 (b). 8

i) V_{GSQ} ii) I_{DQ} iii) V_{DS}.

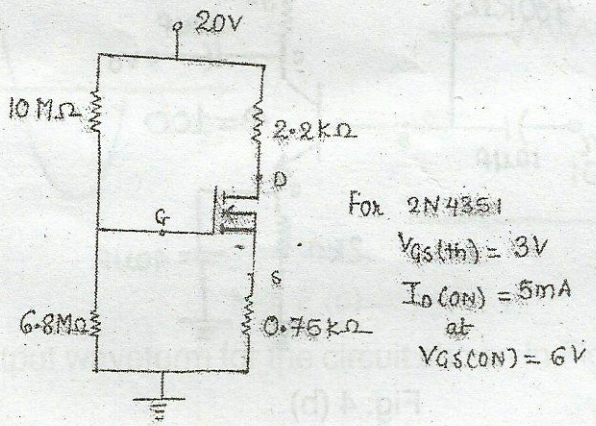

Fig. 6 (b)

c) Write a short note on CMOS as an inverter. 6

MODULE – IV

7. a) Sketch the typical Silicon Controlled Rectifier Characteristics, identify all the regions of characteristics and define the important current and voltage levels. 6

b) Write a short note on thermistors. 4

c) Explain how internal synchronization is achieved in a CRO. 6

d) What is an op-amp ? Explain the differential input operation of an op-amp. 4

8. a) Give the manufacturing steps involved in the fabrication of resistors in Monolithic IC. 5

b) Draw the symbol, construction of a Photoconductive cell and explain its principle of operation. 5

c) With neat diagrams, explain the working of reflective type Field Effect LCD. 5

d) Draw the circuit of a Wein bridge oscillator and write the expression for frequency of oscillation. 5