SEM 2 – 5 (RC)

F.E. (Semester – II) (Revised in 2007-08) Examination, November 2010
BASIC ELECTRONICS ENGG.

Duration : 3 Hours | Total Marks : 100

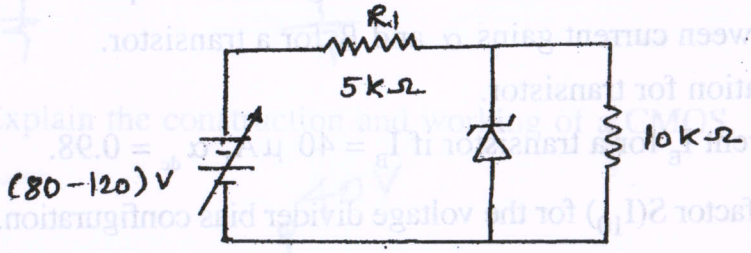
Instructions : *1) Attempt **any five** questions selecting at least **one** from **each** Module.*
*2) **Assume** suitable data only **if** necessary.*

MODULE – I

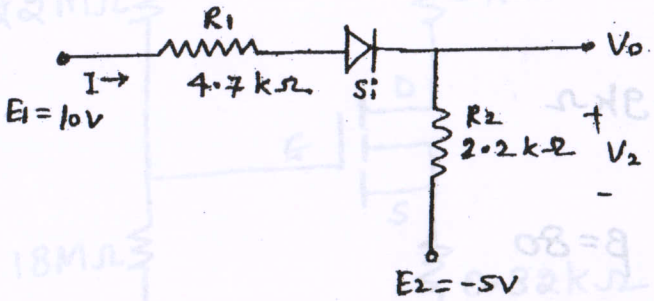
1. a) Explain the effect of temperature on reverse saturation current and threshold voltage of diode. **2**

b) Explain how to determine the dynamic resistance of p-n junction diode with the help of neat diagram. **2**

c) Determine maximum and minimum value of zener diode current for the circuit shown below if zener has $V_z = 50$ V. **4**



d) Determine the values of I, V_1, V_2 and V_0 for the given network : **6**



e) Explain the working of a half wave rectifier. Derive the expression for ripple factor, ratio of rectification and T.U.F. of the half wave. **6**

P.T.O.

2. a) In center-tapped full wave rectifier load resistance R_L = 1 KΩ. Each diode has a forward bias dynamic resistance rd = 10 Ω. The voltage across half of the secondary winding is 220 sin 314 t. Find values of
   i) peak value of current
   ii) dc or average value of load current
   iii) rms value of load current
   iv) ripple factor
   v) the rectification efficiency. **5**

   b) Turns ratio of transformer used in half wave rectifier is $n_1 : n_2 = 12 : 1$. Primary is connected to power mains 220 V, 50 Hz. Assuming diode resistance in forward bias to be zero, calculate dc voltage across the load. What is PIV of each diode ? **4**

   c) With the help of neat diagram explain the working of half wave voltage doubler. Draw the waveform for output voltage. **6**

   d) With the help of neat diagram and waveforms, explain working of negative clamper. **5**

MODULE – II

3. a) Explain construction and various operating regions for a typical BJT. In which region transistor should be connected if we are using it as an amplifier ? **8**

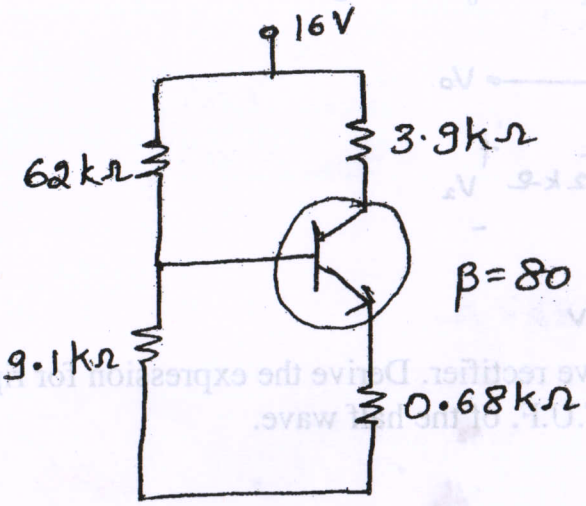
   b) Derive the relation between current gains α and β for a transistor. **3**

   c) Explain limits of operation for transistor. **5**

   d) Determine emitter current I_E for a transistor if $I_B = 40\ \mu A$, $\alpha_{dc} = 0.98$. **4**

4. a) Determine the stability factor $S(I_{10})$ for the voltage divider bias configuration. **6**

   b) Determine I_{BQ}, I_{CQ}, V_{CEQ}, V_C, V_E, V_B for the following network : **6**



c) Explain the working of a transistor as a switch. 5

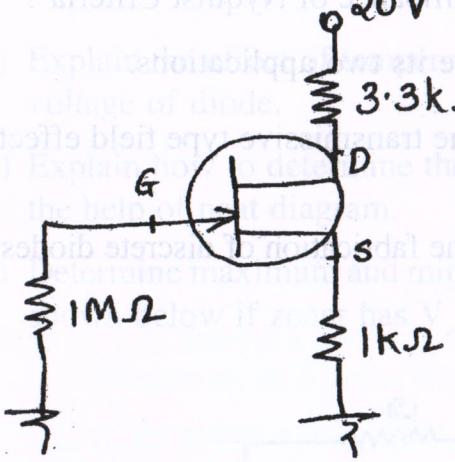
d) Compare the three biasing methods. Which is the best biasing technique ? Justify. 3

MODULE – III

5. a) Explain the construction and characteristics of n-channel JFET. 6

b) With neat diagram and a set of equations, explain the Fixed Bias Configuration of JFET. 7

c) For the network shown below, find V_{GSQ}, I_{DQ}, V_{DS}, V_S, V_G and V_D. 7

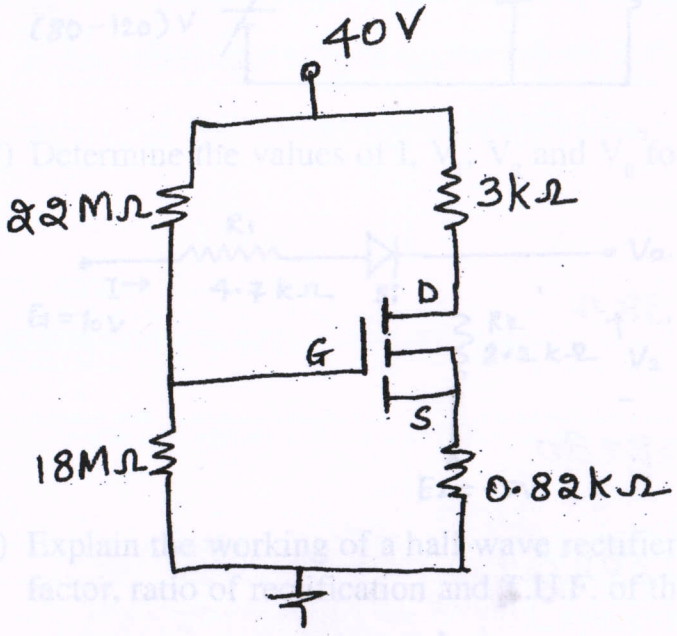


$I_{DSS} = 8$ mA

$V_P = -6$V

6. a) Explain the construction and working of a CMOS. 4

b) 8



$V_{GS\ (th)} = 5$ V

$I_{D\ (ON)} = 3$ mA

$V_{GS\ (ON)} = 10$ V

For the figure shown determine I_{DQ}, V_{GSQ}, V_{DS}.

c) Differentiate between the following :

a) Enhancement and depletion type MOSFET.

b) BJT and JFET. **4**

d) Explain pinch-off in an enhancement-type MOSFET with a neat diagram. **4**

MODULE – IV

7. a) Explain the working of an SCR. Draw the characteristics and define the terms holding current and latching current. **8**

b) Define Nyquist Criterion. What is the significance of Nyquist Criteria ? **4**

c) Explain the working of a photodiode. Give its two applications. **8**

8. a) With the help of a neat diagram, explain the transmissive type field effect LCD. **7**

b) Give the manufacturing steps involved in the fabrication of discrete diodes. **5**

c) With neat sketch, explain IR emitters. **4**

d) Explain gain margin and phase margin. **4**
