F.E. (Semester – II) (Revised in 2007-08) Examination, May/June 2012
BASIC ELECTRONIC ENGINEERING

Duration : 3 Hours | Total Marks : 100

Instructions : 1) *Attempt **five** questions, choosing at least **one** question from **each** Module.*
2) ***Assume** any additional data **if required.***

MODULE – I

1. a) Explain with circuit diagram the details of drawing the load line and finding the apoint of operation on the diode characteristics. 7

   b) Explain the following terms in context with semiconductor theory. 4

      i) Transition capacitance ii) Diffusion capacitance

   c) The turns ratio of a transformer used in a half wave rectifier is $N_1 : N_2 = 12:1$. The primary is connected to the power mains : 220 V, 50 Hz. Assuming the diode resistance in forward bias to be zero, calculate the dc voltage across the load. What is the PIV of the diode ? 4

   d) In a centre tap full wave rectifier, the load resistance $R_L = 1k\Omega$. Each diode has a forward-biased dynamic resistance rd = 10Ω. The voltage across half the secondary winding is 220 sin 314 t. Find : 5

      i) the peak value of current ii) the dc or average value of current

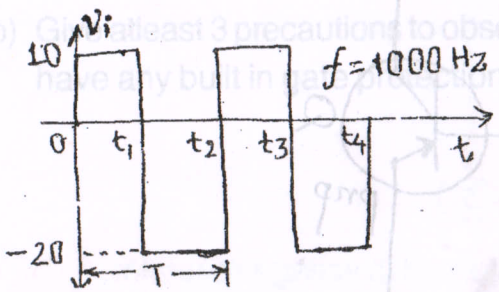
      iii) the rms value of current iv) the ripple factor

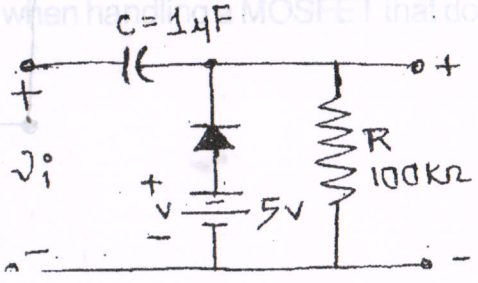
      v) the rectification efficiency.

2. a) Draw the output voltage waveform of a halfwave rectifier and then show the effect on this wave form of connecting a capacitor across the load resistance. 4

   b) Prove that the ripple factor of a half wave rectifier is 1.21 and that of full wave rectifier is 0.482. 9

   c) Determine V_o for the network of fig below. 7





P.T.O.

MODULE – II

3. a) If a transistor used in the CE connection has its collector voltage increased, what will happen to the base current if the base voltage is held constant ? Why ? **5**

   b) Sketch a common base amplifier circuit with an NPN transistor and indicate clearly the polarities of supply voltages. Do the same with a common emitter amplifier with NPN transistor. Can you explain why a CE amplifier may be preferred over CB as far as supply voltages are concerned ? **5**

   c) When the emitter current of a transistor is changed by 1 mA, its collector current changes by 0.995 mA. Calculate **5**

      i) Its common base short circuit current gain α

      ii) Its common emitter short circuit current gain β

   d) Sketch the typical output characteristics curves for a PNP transistor in CB configuration. Label all variables and indicate active, cut-off and saturation region. **5**

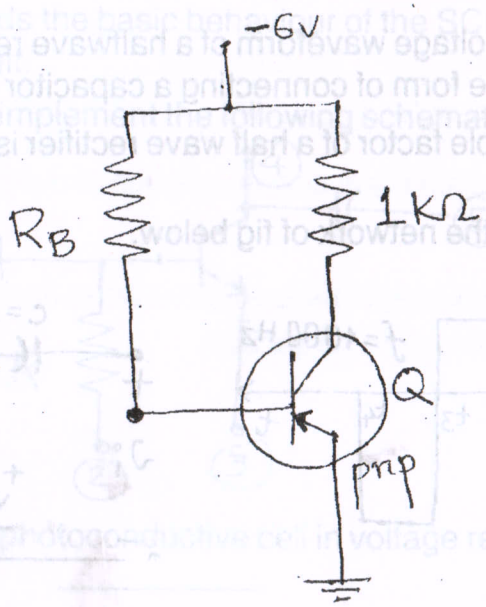
4. a) What is the definition of stability factor 's' ? Why would it seem more reasonable to call this an 'instability factor' ? Which circuit has the highest 's' factor ? **6**

   b) Prove mathematically that the operating point in a potential divider biasing circuit is independent of β. Make relevant assumptions. **7**

   c) In the biasing circuit shown below a supply of 6V and a load resistance of 1 kΩ is used.

      i) Find the value of resistance R_B so that a germanium transistor with $\beta = 20$ and $I_{CBO} = 2\mu A$ draws an IC of 1 mA

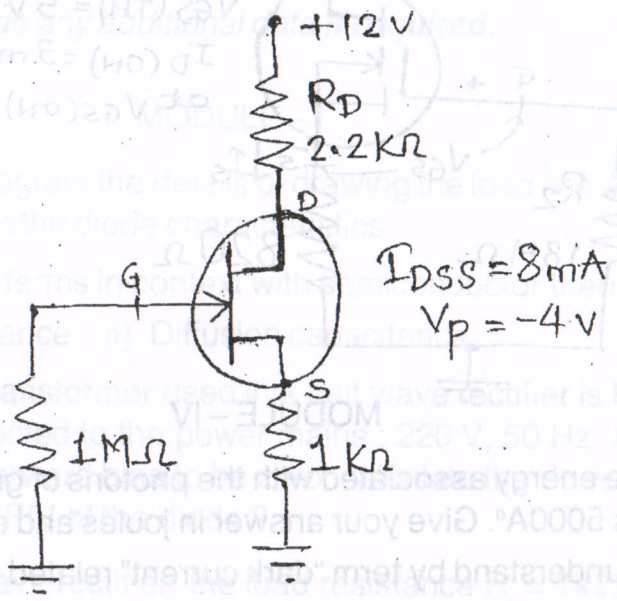
      ii) What I_C is drawn if the transistor parameters change to $\beta = 25$ and $I_{CBO} = 10\ \mu A$ due to rise in temp ?



MODULE – III

5. a) With the help of neat diagram, explain the operation of an n-channel JFET. Show the internal depletion regions and explain their shape. 6

b) For the circuit shown in fig. below. Calculate : 5
V_{GSQ}, I_{DQ}, V_{DS}, V_S & V_D



c) i) What method is used to bias an FET against device and temp. variation ? Explain how this is effective ? 4

ii) What do transfer curves for an FET consists of ?

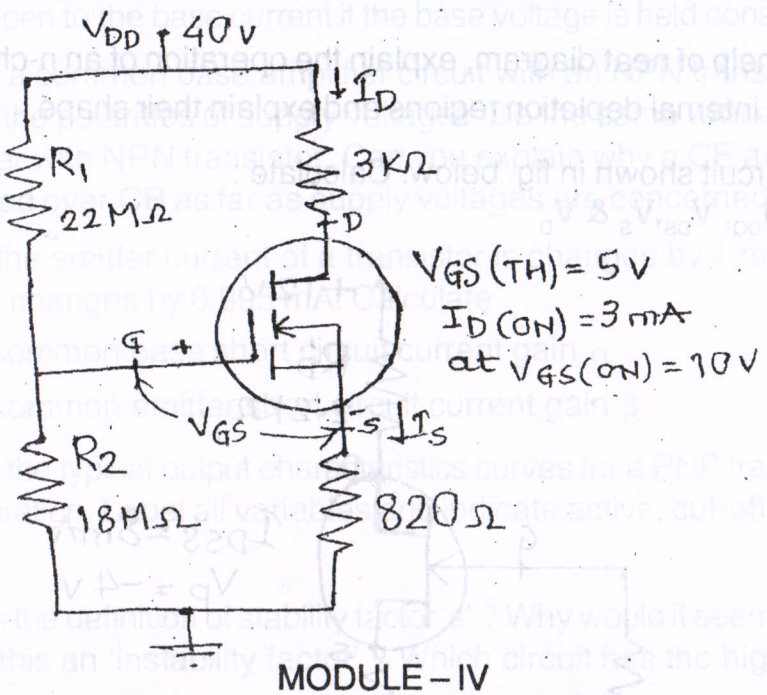
iii) What is a bias line ? What does it imply if, the bias line is not very steep ?

d) Datasheet for a JFET indicate that I_{DSS} = 10 mA and V_{GS}(off) = – 4V. Determine the drain current for V_{GS} = OV, – 1 V & – 4 V. 5

6. a) Draw and explain drain characteristics of n-channel enhancement type MOSFET. 7

b) Give atleast 3 precautions to observe when handling a MOSFET that does not have any built in gate protection. 3

c) For the circuit shown in fig. below, calculate V_G, I_D, V_{GS} & V_{DS}. **10**



MODULE – IV

7. a) Determine the energy associated with the photons of green light, if the wavelength is 5000A°. Give your answer in joules and electron volts. **4**

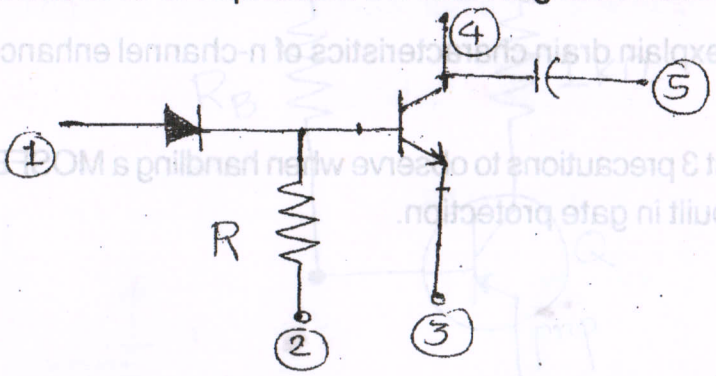
   b) What do you understand by term "dark current" related to photodiode ? **4**

   c) Describe the basic operation of an LCD. Also comment on relative differences in the mode of operation between an LED and LCD display. **7**

   d) If the power rating of a solar cell is determined on a very rough scale by the product V_{OC} I_{SC}, is the greatest rate of increase obtained at lower or higher levels of illumination. Explain your reasoning. **5**

8. a) Describe in your own words the basic behaviour of the SCR using the two transistor equivalent circuit. **8**

   b) Design a monolithic IC to implement the following schematic. **7**



   c) Explain the application of photoconductive cell in voltage regulator. **5**