[Total No. of Questions: 8]

# F.E. (Semester - II) (RC) Examination, Nov. - 2011 BASIC ELECTRONIC ENGINEERING

(Revised in 2007-08)

**Duration: 3 Hours** 

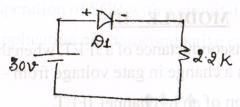
Total Marks: 100

Instructions: 1) Attempt five questions choosing at least one from each Module.

2) Assume any additional data, if required.

#### **MODULE - I**

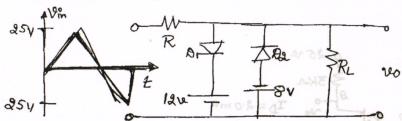
Q1) a) Using the approximate characteristics for a silicon diode, calculate V<sub>D</sub>, I<sub>D</sub> & V<sub>R</sub> for the circuit shown.



b) Explain the following terms in context with a semiconductor diode. [6]

- i) Potential barrier.
- ii) Depletion layer Breakdown.
- c) Explain with circuit diagram the details of drawing the load line & finding the point of operation on the diode characteristics. [8]

22) a) A triangular voltage is applied to the biased clipper circuit. Determine the wave shape of the output voltage for the circuit. [3]



- b) Differentiate between zener breakdown & avalanche breakdown.
- c) Explain how a zenerdiode maintains constant voltage across the load. [6]
- d) Sketch the circuit of a dc restorer. Show input & output waveforms. Briefly explain the operation of the circuit.

  [6]

[5]

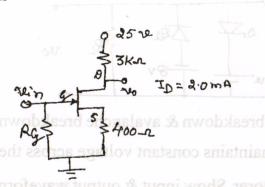
[8]

#### MODULE - II

- Q3) a) What are the factor affecting bias variation. [6]
  - b) Give reason for wide spread use of CE configuration. [6]
  - c) Besides the active region of operation of a transistor, what are the other possible condition of operation of a transistor. Give biasing conditions of each. [8]
- Q4) a) Explain the input and output characteristics of a transistor in CB configuration. [6]
  - b) Draw the circuit symbol for an npn transistor & indicate the reference polarities for the voltages & the reference direction for the three current. [6]
  - c) Draw the circuits of three transistor amplifier configuration using npn transistor & explain how a voltage amplification is achieved in CE configuration. [8]

### **MODULE - III**

- Q5) a) Determine the value of transconductance of a JFET, when the drain current changes from 1 mA to 1.5 mA with a change in gate voltage from -2.125v to -2v. [2]
  - b) Draw the basic construction of an n- channel JFET. [6]
  - c) Define JFET parameter & establish relationship between them. [6]
  - d) Explain with the help of a diagram the basic CMOS operation. [6]
- Q6) a) Explain the voltage divider biasing arrangement for an n channel enhancement MOSFET.
  - b) For the circuit shown. Determine [61
    - i)  $V_{DS}$  and
    - ii)  $V_{GS}$



c) In an N-channel JFET biased by voltage divider method, determine the value of RS to give operating point  $I_D = 4$  mA &  $V_{DS} = 8$  v.

Data provided : 
$$V_{DD} = 25v$$
,  $RG_1 = 1.2 M\Omega RG_2 = 0.6 M\Omega$   
JFET parameters :  $I_{DSS} = 12mA \& V_p = -4v$ .

## **MODULE - IV**

| Q7) | a) | List four application of IR emitter.  | [2] |
|-----|----|---|-----|
|     | b) | Explain the reflective type LCD.  | [6] |
|     | c) | Explain with block diagram feedback concepts.                               | [6] |
|     | d) | Describe the OPAMP operation for double ended output with single ended in   |     |
|     |    |   | [6] |
| Q8) | a) | Give the manufacturing steps involved in the fabrication of discrete diode. | [5] |
|     | b) | Explain how internal synchronization is achieved in CRO.                    | [5] |
|     | c) | Explain the operation of SCR with a circuit diagram.                        | [5] |
|     | d) | Explain the application of photoconductive cell in voltage regulator.       | [5] |
|     |    |   |     |

