SEM 2-5 – (RC 07-08)

F.E. (Semester – II) (Revised in 2007-08) Examination, May/June 2017

BASIC ELECTRONICS ENGINEERING

Duration : 3 Hours

Max. Marks : 100

Instructions : *1) Answer **5** questions choosing atleast **one** from **each** Module.*
*2) Assume data **if** necessary.*

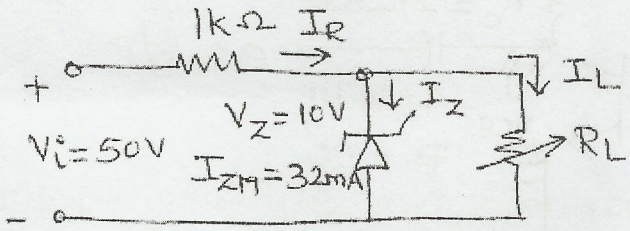
MODULE – I

1. a) Prove that the Ripple factor of a Full Wave Rectifier is 0.482. 4

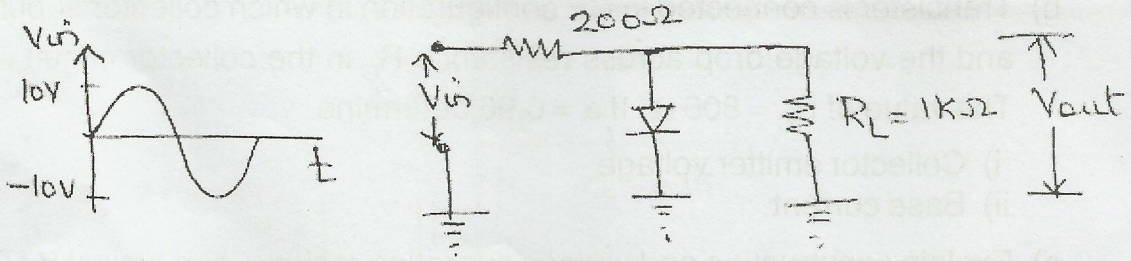
   b) Explain the operation of a half wave Voltage doubler. 5

   c) Explain with circuit diagram the details of drawing loadline and determine the point of operation on the diode characteristics. 5

   d) Determine the range of R_L and I_L that will result in V_{RL} being maintained at 10v. Determine the maximum wattage rating of the diode. 6



2. a) The Positive Shunt Clipper shown in fig. below has the input waveform as indicated. Determine the values of V_{out} for each of the input alternations. 4



   b) Show that the maximum rectification efficiency of a half wave Rectifier is 40.6%. 6

P.T.O.

c) Differentiate between Zener breakdown and Avalanche breakdown. 5

d) Draw V-I characteristics of PN Junction diode and explain piecewise linear equivalent circuit of a diode. 5

MODULE – II

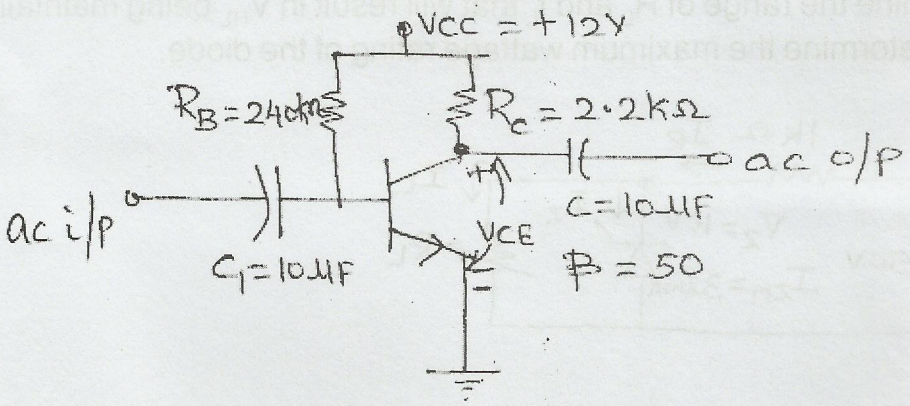
3. a) Explain CE configuration of a NPN transistor. Draw the input and output characteristics. 5

b) Explain how transistor can be used as an amplifier. 5

c) With the help of necessary equations obtain the relation between β and α. 4

d) Determine the following for the fixed bias configuration of fig. 6

i) I_{BQ} and I_{CQ} ii) V_{CEQ} iii) V_B and V_C iv) V_{BC}



4. a) What do you mean by Stabilization of operating point ? Explain the reasons why Stabilization of Q point is necessary ? 5

b) Transistor is connected in CE configuration in which collector supply is 8V and the voltage drop across resistance R_C in the collector circuit is 0.5V. The value of $R_C = 800\,\Omega$. If $\alpha = 0.96$ determine

i) Collector emitter voltage
ii) Base current. 4

c) Explain construction and various operating regions for a typical BJT. 6

d) Compare the Biasing methods. Which is the best biasing technique ? Explain any one biasing technique. 5

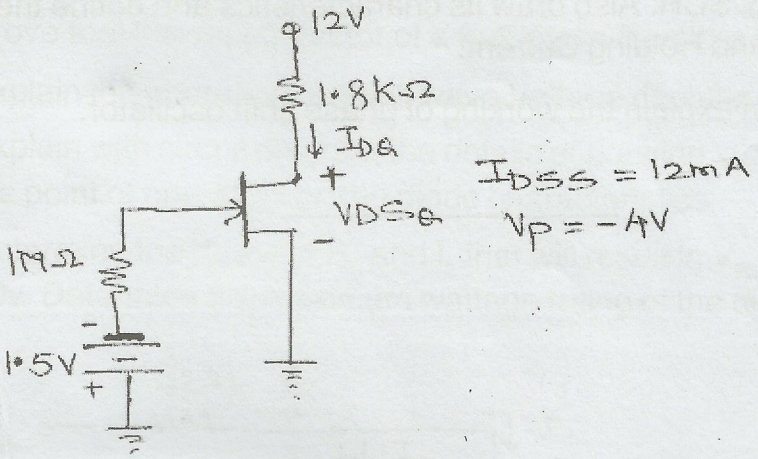
MODULE – III

5. a) With the help of neat diagram, explain the operation of P channel JFET. Also show internal depletion regions and explain their shapes. **8**

b) With the help of neat diagram and set of equations explain self bias configuration of JFET. **7**

c) For fixed bias configuration given below, determine the following : **5**

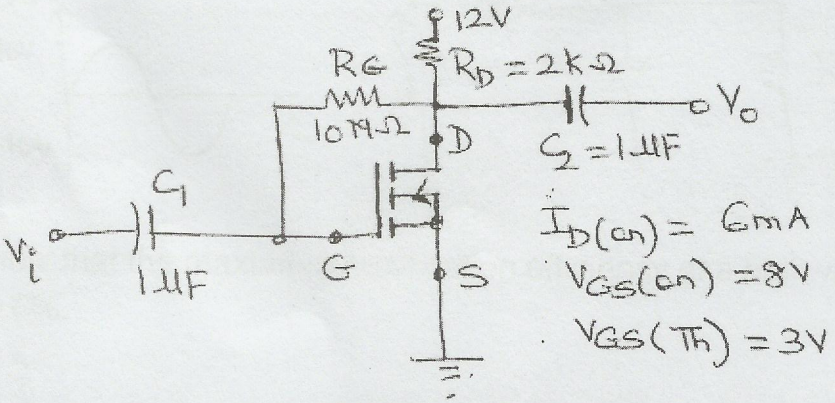
i) V_{GSQ} ii) I_{DQ} iii) V_{DS}



6. a) Explain with a sketch why I_D exceeds beyond I_{DSS} if positive voltage is applied at the gate of n-channel depletion type MOSFET. **6**

b) With the help of neat sketches comment on the Polarity of various voltages and direction of current for n channel and P channel JFET. **6**

c) Determine I_{DQ} V_{GSQ} and V_{DS} for Enhancement type MOSFET given below : **8**



MODULE – IV

7. a) Explain the block diagram of OPAMP. **4**

   b) Give the manufacturing steps involved in Fabrication of discrete diode. **8**

   c) With the help of neat diagram explain the working of transmissive type field effect LCD. **8**

8. a) Explain how internal synchronization is achieved in CRO. **6**

   b) Explain working of SCR. Also draw its characteristics and define the term Latching current and Holding Current. **8**

   c) With neat diagram explain the working of phase shift oscillator. **6**
