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**F.E. Semester II (Revised Course 2016-17)**
**EXAMINATION FEBRUARY 2021**
**Fundamentals of Electronics and Telecommunication Engineering**

**[Duration : Two Hours]** **[Total Marks :60]**

**Instructions:-**
1) Answer THREE FULL QUESTIONS with ONE QUESTION FROM EACH PART.
2) Assume suitable data **only if necessary**.
3) All symbols, notations, and abbreviations have their usual meaning.

## PART A

1. a) With neat diagrams compare insulators, semiconductors and conductors with respect to energy bands in solids. **(6 mks)**

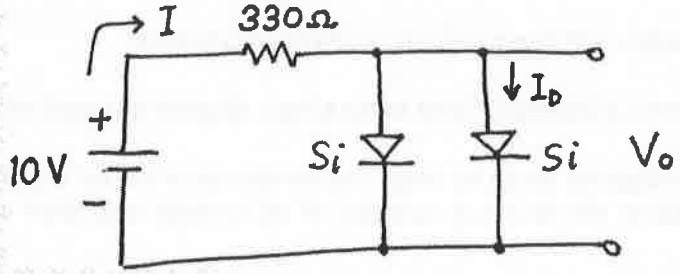
b) Distinguish between Zener and avalanche breakdown mechanisms in a semiconductor diode. **(6 mks)**

c) Define and explain the following terms for a p-n junction diode:

i) Knee voltage, ii) reverse saturation current **(4 mks)**

d) Explain the mechanism which causes an LED to emit light. What factor determines whether visible light is emitted or not? **(4 mks)**

2. a) i) Determine $V_o$, I and $I_D$ for the following circuit.




ii) Determine $V_o$ and I for the following circuit:

**(6 mks)**



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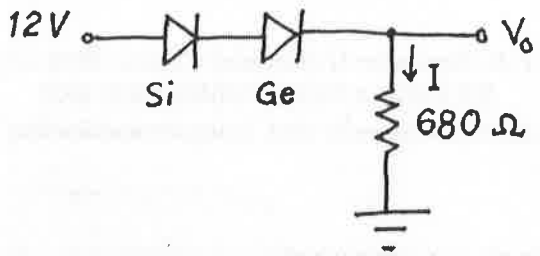


b) Derive the expression for the ripple factor of a full-wave bridge rectifier. Why is a bridge rectifier better than half-wave rectifier? **(6 mks)**

c) i) Derive the expression for $I_{dc}$, $I_{rms}$ and $V_{dc}$ for a half-wave rectifier.

ii) A half-wave rectifier is supplied with $V_m = 20V$ from the transformer secondary, If $R_L = 1k\Omega$, calculate $I_{dc}$ and PIV of each diode. **(8 mks)**

3 a) Derive the relationship between: i) $\alpha$ & $\beta$, ii) $I_{CEO}$ and $I_{CBO}$ for a BJT. **(6 mks)**

b) With the help of a circuit diagram explain the fixed bias circuit for a BJT, and derive the required equations. **(6 mks)**

c) Explain with a neat diagram the working of a n-channel JFET. Draw the transfer characteristics. Show how the transfer curve is obtained. **(8 mks)**

## PART B

4 a) Two square waves of frequencies 100 Hz and 200 Hz are applied as inputs to the logic gates: i) NAND ii) XOR.
Draw the output waves for each case **(4 mks)**

b) Compare positive and negative logic, in digital electronics. **(4 mks)**

c) State and prove De Morgan's laws using a logic diagram and truth tables **(6 mks)**

d) Draw the pin diagram for an op-amp. Explain the operation for a sinusoid input signal applied to the inverting terminal of an op-amp, and draw the output waveform. **(6 mks)**

5. a) What is an LVDT? With neat diagrams explain the internal construction and working principle of an LVDT. List two applications. **(8 mks)**

b) Draw the basic block diagram of a PLC and explain its principle of working. **(6 mks)**

c) With the help of a neat diagram explain the components of a basic communication system. **(6 mks)**



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6. a) Why is a NAND gate called a "universal logic gate"? Using logic diagrams, implement the following logic gates using only NAND gates: i) XOR ii) OR **(5 mks)**

b) Why is modulation needed in communication systems? With the help of a diagram, explain the basic concept of amplitude modulation. **(6 mks)**

c) What is a strain gauge? Define "gauge factor" of a strain gauge and write the expression for it. What is its significance? **(6 mks)**

d) Reduce the following Boolean expression and implement the simplified expression using logic gates: $Y = \bar{A}\bar{B} + A\bar{B}$. Verify using a truth table. **(3 mks)**

## PART C

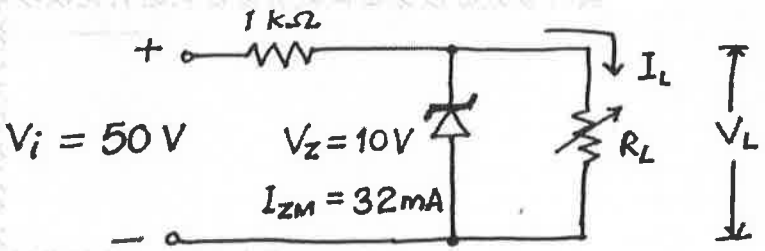
7 a) Draw the block diagram of a microcontroller and list two applications. How is it different from a microprocessor? **(5 mks)**

b) State the associative and distributive laws of Boolean algebra, and prove them using truth tables **(6 mks)**

c) Draw waveforms for the modulating and modulated signals for FM, and define modulation index for the same. **(4 mks)**

d) Give the steps involved in the manufacture of a single sided PCB with the help of a flow diagram. **(5 mks)**

8 a) For the Zener regulator circuit shown below, determine the range of $R_L$ that shall result in the load voltage being maintained at 10 V. **(6 mks)**




b) Simplify the following expressions using laws of Boolean algebra: **(6 mks)**

i) $Y = ABC + B\bar{C}D + \bar{A}BC$

ii) $Y = \bar{A}BC\bar{D} + BC\bar{D} + B\bar{C}\,\bar{D} + B\bar{C}D$

c) Draw the output characteristics for a BJT npn transistor amplifier in common emitter configuration and explain the various regions. **(8 mks)**