

Tutorial - 9

Control Hazard and Branch Predictions

Introduction

- Control hazards

Pipeline hazards are conditions that can occur in a pipelined machine that impede the execution of a subsequent instruction in a particular cycle for a variety of reasons.

Common pipeline hazards:

- a) Data Hazards: RAW hazards, WAR Hazards, WAW hazards.
- b) Control Hazards
- c) Structural Hazards

Question-1

Q. Suppose we have a CPU that has a single branch delay slot. This slot can be filled with a useful instruction 65% of the time. In addition, the branch condition is not known for two cycles beyond the delay slot. If these are predicted properly, there is no penalty. If they are mispredicted, the two intervening instructions must be cancelled. Forward branches are always predicted not taken, while backward branches are always predicted taken. Forward branches make up 75% of all branches, and branches are 20% of all instructions. If 50% of forward branches and 85% of backward branches are taken. What is the new CPI (assuming the original CPI is 1)?

Question-1

Q. Suppose we have a CPU that has a single branch delay slot. This slot can be filled with a useful instruction 65% of the time. In addition, the branch condition is not known for two cycles beyond the delay slot. If these are predicted properly, there is no penalty. If they are mispredicted, the two intervening instructions must be cancelled. Forward branches are always predicted not taken, while backward branches are always predicted taken. Forward branches make up 75% of all branches, and branches are 20% of all instructions. If 50% of forward branches and 85% of backward branches are taken. What is the new CPI (assuming the original CPI is 1)?

Calculate the number of stall cycles.

For 35% of the branch instruction, the delay slot isn't filled.

This adds 0.35 cycles of branch stalls.

50% of forward branches suffer a 2 cycle Penalty.

Since 75% of branches are forward this contributes

$$0.5 \times 0.75 \times 2 \text{ cycles} = 0.75 \text{ cycles}$$

Similarly, 15% of backward branches suffer a 2 cycle penalty, which adds

$$\text{another } 0.15 \times 0.25 \times 2 = 0.075 \text{ cycles.}$$

Therefore total branch penalty is

$$0.35 + 0.75 + 0.075 = 1.175 \text{ cycles}$$

Since branches make up 20% of all instructions,

the penalty to the CPI is $0.20 \times 1.175 = 0.235$ cycles

This makes the new CPI = 1.235

Question-2

Q. Given an application where 20% of the instructions executed are conditional branches and 59% of those are taken. For the MIPS 5-stage pipeline, what speedup will be achieved using a scheme where all branches are predicted as taken over a scheme with no branch prediction (i.e. branches will always incur a 1 cycle penalty)? Ignore all other stalls.

Question-2

Q. Given an application where 20% of the instructions executed are conditional branches and 59% of those are taken. For the MIPS 5-stage pipeline, what speedup will be achieved using a scheme where all branches are predicted as taken over a scheme with no branch prediction (i.e. branches will always incur a 1 cycle penalty)? Ignore all other stalls.

CPI with no branch prediction = $0.8 \times 1 + 0.2 \times 2 = 1.2$

CPI with branch prediction = $0.8 \times 1 + 0.2 \times 0.59 \times 1 + 0.2 \times 0.41 \times 2 = 1.082$

Speed up = $1.2 / 1.082 = 1.109$

Question-3

Q. Consider a 5-stage integer pipeline with forwarding. Assume the branch penalty is 1 cycle (branch condition computed in ID). Now assume we have pipelined the memory system to three stages (rather than 1 stage) for both instruction fetch and data fetch. Branches are resolved at the end of the EX stage. We use a static branch-taken prediction strategy, i.e., if branches are not-taken we incur the branch penalty. Assume conditional branches occur with a frequency of 25%. If branches are taken 35% of the time, what is the increase in CPI due to this prediction strategy?

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The branch penalty is 3 cycles and incurred only when the branch is not taken.

Therefore the increase in CPI = $0.65 * 0.25 * 3$
= 0.4875

Question-4

Q.(a) Consider the correlating predictors for dynamic branch prediction. Compute the number of bits in a 32-entry, (2,2) correlating branch predictor.

(b) Consider a global branch predictor that uses a 2-bit global history and a 2-bit local predictor. If $k=5$, is the number of bits used to represent a branch address, what is the number of bits in the global predictor?

c.) What is the probability that a branch is taken given that 35% of the branches are unconditional branches? Of the conditional branches, 80% branch forward and evenly split between taken and not taken, the rest branch backward and are always taken ?.

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(a) The number of bits in a 32-entry, (2,2) correlating branch predictor = $2^m \times n \times 2^k$. Here, $m = 2$, $n = 2$ and $k = 5$. Therefore the number of bits = $2^2 \times 2 \times 2^5$
= 256

Question-4

Q. (b) Consider a global branch predictor that uses a 2-bit global history and a 2-bit local predictor. If $k = 5$, is the number of bits used to represent a branch address, what is the number of bits in the global predictor?

(b) The given predictor is an (m,n) correlating predictor, also known as global predictor where an m -bit global history and an n -bit local predictor would be used to make the branch predictions. The number of bits in an (m,n) predictor is computed as $2^m * n * \text{num. Of prediction entries}$. Here it is given that $k = 5$ is the number of bits used to represent a branch address. So the number of unique entries would be 2^k

Thus the number of bits in the $(2,2)$ predictor = $2^m * n * \text{num. Of prediction entries}$
 $= 2^m * m * 2^k = 4 * 2 * 32 = 256$

Question-4

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Unconditional branches = 35% of all branches

Conditional branches = 65% of all branches

Thus probability that a branch is taken $p = \text{unconditional branch probability} + \text{conditional branch probability} = 0.35 + 0.65 (0.80 * 0.5 * 1 + 0.20 * 1) = 0.74$

Question-6

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