

Tutorial - 3

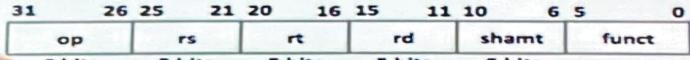
MIPS Instruction-set Architecture(ISA)

Introduction

MIPS instruction-set architecture is based on 32 bit word length. The instruction-set of a MIPS machine consists of three types of instructions.

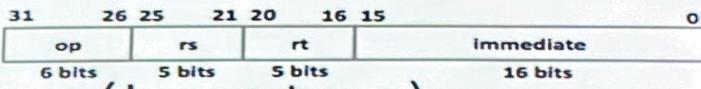
— R-Type: (Register type)

- For register-based instructions (add, sub, etc.)



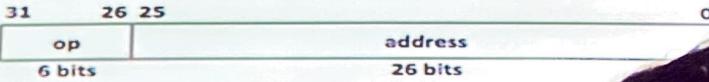
— I-Type: (Immediate type)

- For loads and stores (lw and sw), etc.



— J-Type: (Jump type)

- For the jump (J) instruction



Img ref: <https://media.cheggcdn.com/media/407/40718987-c331-4cda-a6bb-7958085f7b96/phpWJm>

Question - 1

Convert the following program into machine code.

1. 0xFC00000C start:
2. 0xFC000010 loop: addi \$t0,\$t0,-1
3. 0xFC000014 sw \$t0, 4(\$t2)
4. 0xFC000018 bne \$t0, \$t3, loop
5. 0xFC00001C j start

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Solution-1

2. Given :

0xFC000010 addi \$t0,\$t0,-1

2 ans:

immediate value -1 = 0xFFFF (hex rep) (16 bits wide)

0010 00/01 000/0 1000 /1111 1111 1111 1111
8 8 8 -1
Op(6) rs(5) rt(5) immediate(16)

Immediate addressing Mode used.

3 ans:

1010 11/01 010/0 1000 /0000 0000 0000 0100

43 10 8 4

Op(6) rs(5) rt(5) immediate(16)

4(\$t2) Base addressing mode used.

Effective Address (mem) = content of R10 (I2) + sign extended imme value (4)

Solution-1

5. 0xFC00001C j start

target address = last 4 bits of PC : (immediate * 4)

immediate = first 28 bits from target address / 4

= C00000C / 4 (target addr. FC00000C)

= 3000003 = 1100 0000 0000 0000 0000 0000 1100 / 4

or

srl by 2 = 0011 0000 0000 0000 0000 0000 0011

Binary rep of Ins:

0000 10/0011 0000 0000 0000 0000 0000 0011

2 3000003

Op(6) immediate (26)

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Solution-1

4. 0xFC000018 bne \$t0, \$t3, loop

4. sol :

target address = (imme * 4) + address of the following instruction

imme = (target address – address of the following instruction) / 4

$$= (FC000010 - FC00001C) / 4 = - C / 4$$

= -3 1111 1111 1111 1101

hence binary rep of ins

0001 01/01 000/0 1011 /1111 1111 1111 1101

5 8 11 -3

Op(6) rs(5) rt(5) immediate(16)

Addressing mode = PC relative : to branch to loop ,
program counter value would be

pc = current address + sign extended imme value <<2

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Question-2

Explain why an assembler might have problems
directly implementing the branch instruction in
the following code sequence:

Branch: beq \$t1, \$t8, Goto

Goto: mul \$s0, \$s0, \$s0

Show how the assembler might rewrite this code
sequence to solve these problems.

Solution-2

sol :

When using PC-relative addressing which is the case in the above instruction, if the target address is too far away, we won't be able to represent the target address with the 16 bits provided relative to the current PC address.

There are two solutions to the above problem based on the displacement of the target address from the current PC address.

Case 1 : If ' Goto ' refers to a location further than 128 KB from the PC, the solution would be:

Branch: bne \$s0, \$s2, skip

j Goto (imme is 26 bits) and EA = PC (last 4 bits)+ sign extnd imm << 2 (28 bits)

skip: ...

Goto : mul \$s0, \$s0, \$s0

The displacement of larger than 128kb is covered but less than 256 MB.

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Solution-2

Contd...

Sol.

If 'Goto' refers to a location further than 256 MB from the PC, the solution would be:

Branch :bne \$s0, \$s2, skip

```
lui $ra, Goto(upper)
ori $ra, $ra ,Goto(lower)
jr $ra  ( ra register contains target
address(GotoAddress) greater than 28 bits)
```

skip ...

Goto: mul \$s0, \$s0, \$s0

Notes

Comments



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23°C Light rain



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Question-3

Q.

If the instruction set of the MIPS processor is modified, the instruction format must also be changed. For each of the suggested changes, show the size of the bit fields of an I-type format instruction. What is the total number of bits needed for each instruction?

- a) 16 registers
- b) 10 bit immediate constants.
- c) All arithmetic instructions can use base addressing mode with the last argument (Example: add \$a0, \$a2, 0[\$t1]).

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Solution-3

Q. If the instruction set of the MIPS processor is modified, the instruction format must also be changed. For each of the suggested changes, show the size of the bit fields of an I-type format instruction. What is the total number of bits needed for each instruction?

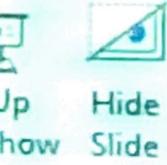
c) All arithmetic instructions can use base addressing mode with the last argument
Example: add \$a0, \$a2, 0[\$t1].

Case 1 : If we assume the immediate value to be strictly an integer constant then there is no change in the I-type instruction format .

Case 2: I-type instruction format

Opcode(6)	Rs(5)	Rt(5)	Rd(5)	Immediate(16)
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Total bits required : 37 bits.



Up
Down
Left
Right

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Question-4

Q4. Convert the following C statements to equivalent MIPS assembly language. Assume that the variables f, g, h are assigned to registers \$s0, \$s1, \$s2 respectively.

Assume that the base address of the array A and B are in registers \$s6 and \$s7 respectively.

- a) $f = g + h + B[4]$
- b) $f = h + A[B[4]]$

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Question-5

Q5. If the instruction set of the MIPS processor is modified, the instruction format must also be changed. For each of the suggested changes, show the size of the bit fields of an R-type format instruction. What is the total number of bits needed for each instruction?

- a) 8 registers.
- b) 10 bit immediate constants
- c) 128 Registers.

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Notes

Comments

