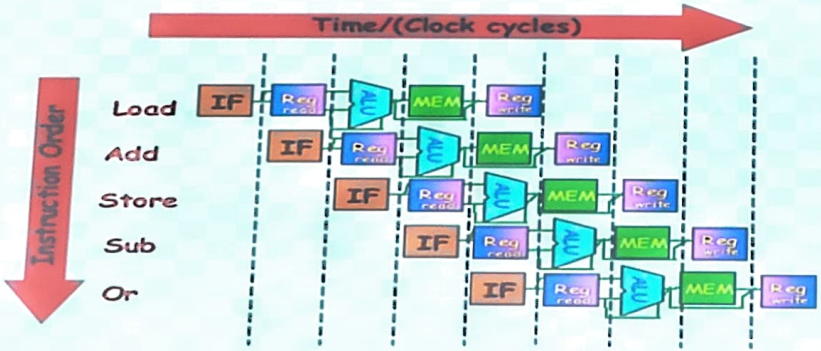
Introduction

- Pipelining



Introduction

- Pipelining

In pipelined architecture hardware of the CPU is split up into several functional units.

Each functional unit performs a dedicated task.

The number of functional units may vary from processor to processor.

Control unit manages all the stages using control signals.

Question-1

Q. If pipelining stages are perfectly balanced ,then the time per instruction on the pipelined processor assuming ideal conditions is equal to ??

b) Pipeline CPI and ideal CPI are related as ??

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Time per instruction on unpipelined machine/Number of pipe stages.

b) Pipeline CPI and ideal CPI are related as ??

Pipeline CPI = Ideal pipeline CPI + structural stalls + Data hazard stalls + control stalls.

Question-2

Q. Consider a pipeline having 5 phases with duration 45, 50, 55,60 and 75 ns. Given latch delay is 5 ns.
Calculate-

Non-pipeline execution time

Sequential time for 500 tasks

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Sol:

a)Non-pipeline execution time for one instruction 45 ns + 50 ns + 55 ns + 60 ns +75 ns
= 285 ns.

b) Non-pipeline time for 500 tasks
= 500 x Time taken for one task
= 500 x 285 ns
= 142500 ns

Question-3

Q.

a) Consider the description given in the following table.

Instruction Class	Instruction fetch	Register read	ALU operation	Data access	Register write	Total time
Load word (lw)	200ps	100ps	200ps	400ps	100ps	1000ps
Store word(sw)	200ps	100ps	200ps	400ps		900ps
R-format(add,sub,and, or ,slt)	200ps	100ps	200ps		100ps	600ps
Branch(beq)	200ps	100ps	200ps			500ps

If the time for a ALU operation can be shortened by 50% compared to the description given in the table.

Will it affect the speedup obtained from pipelining ? If yes , by how much ?otherwise ,why ??

What if the data access operation now takes 25% less time ?

Question-3

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What if the data access operation now takes 25% less time ?

Sol:

a) Shortening the data access operation by 50% will not affect the speedup obtained from pipelining .It would not affect the clock cycle.

b) If the data access operation takes 25% less time ,it still is a bottleneck in the pipeline. The clock cycle needs to be 300ps. Hence speedup would be 400/300 which is 1.33 i.e. 0.33 increase in the speed... Hence the speedup would be 33% more.

Question-4

Q.
A computer architect needs to design the pipeline of a new microprocessor .He has an example workload program with 10^6 instructions. Each instruction takes 100ps to finish.

a)How long does it take to execute this program on a non pipelined processor?

b)Real pipelining is not perfect , since implementing pipelining introduces some overhead per pipeline stage .will this overhead affect instruction latency, instruction throughput ,or both?

Question-4

Q.
A computer architect needs to design the pipeline of a new microprocessor .He has an example workload program with 10^5 instructions. Each instruction takes 100ps to finish.

a)How long does it take to execute this program on a non pipelined processor?

b)Real pipelining is not perfect , since implementing pipelining introduces some overhead per pipeline stage .will this overhead affect instruction latency, instruction throughput ,or both?

Sol

a)It takes 100ps * 10^6 = 100 microseconds to execute on a non pipelined processor (ignoring start and end transients in the pipeline).

b)Pipeline overhead impacts both latency and throughput.

Question-5

Q. A program takes 500ns for execution on a non-pipelined processor .suppose we need to run 100 programs of the same type on a 5-stage processor with a clock period of 20ns .
what is the speed-up ratio of the pipeline?
What is the maximum achievable speed-up?
Assume the instruction cycle takes five clocks.

Question-5

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what is the speed-up ratio of the pipeline?
What is the maximum achievable speed-up?
Assume the instruction cycle take five clocks.

Sol:

Instruction cycle of 5 clock cycles

with 20ns cycle time would take

20 x 5 =100ns for one instruction.
=> no of instructions in the program
= 500ns /100ns =5.
time taken for executing 100 such programs on a non pipelined processor

=5 *100 * 100 (instructions in program * no of program * execution time of one program on a non-pipelined processor)

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Assume the instruction cycle take five clocks.

Sol: contd....

time taken for execution of 100 programs on a pipelined processor

= [no of stages of a pipeline + (total no of instructions -1)] clock cycle time of pipeline .

= [5 + (5*100) -1] *20.

$$\text{Speedup} = \frac{5 * 100 * 100}{[5 + (5*100) - 1] * 20} = \frac{5 * 100 * 100}{504 * 20} = \frac{2500}{504}$$

= 4.96

The maximum achievable speedup is n = no of stages of the pipeline =5

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Question-6

The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.

Calculate the total number of clock cycles required for completing the execution of the 100 instructions ?