
Tutorial - 10

Branch Predictors

Question-1

```
        ADDI R1, R0, 0
LOOP:   MODI R2, R1, 2
0xc44:  BNE  R2, R0, M2    // branch B1
        (do something A)
        ...
M2:     MODI R2, R1, 5
0xc84:  BNE  R2, R0, END    // branch B2
        (do something B)
        ...

END:    ADDI R1, R1, 1
0xcc0:  BNE  R1, 1000000, LOOP // branch LP
```

when the if-condition is met, we do not take the BNE branch.

Branch 1: 1 / 2

Branch2 : 4 / 5

Branch 3(LP): 1:

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Branch2 : 4 / 5

Branch 3(LP): 1:

Question-2

Q. In continuation to the previous question

It is to design a static branch predictor. The static predictor predicts not taken for all forward branches, and taken for all backwards branches. For each branch in the code, what is the accuracy of this static predictor?

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B2: 1 / 5

LP: 1

Question-3

Q. Increasing the size of a branch prediction buffer means that it is less likely that two branches in a program will share the same predictor.

A single predictor predicting a single branch instruction is generally more accurate than is that same predictor serving more than one branch instruction.

(a) List a sequence of branch taken and not taken actions to show a simple example of 1-bit predictor sharing that reduces misprediction rate. (assume loop iterations 4)

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Sol:

Consider two branches, B1 and B2, that are executed alternately. During the execution of the program, B1 and B2 each alternate taken/not taken. If they each had a 1-bit predictor, each would always be mispredicted

	P	B1	P	B2	P	B1	P	B2	P	B1	P	B2	P	B1	P	B2
	NT	T	T	NT	NT	NT	NT	T	T	T	T	NT	NT	NT	NT	T
Correct?		no		no		yes		no		yes		no		yes		No

Because a single predictor is shared, prediction accuracy improves from 0% to 50%.

Question-4

In continuation with the previous question

(b) List a sequence of branch taken and not taken actions that show a simple example of how sharing a 1-bit predictor increases misprediction.(assume loop iterations 4)

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Sol:

Branch 1 is always taken and Branch 2 is always predicted not-taken

Accuracy is 0%

[illegible]