Tutorial - 8

Pipeline Hazards

Introduction

- Pipeline hazards

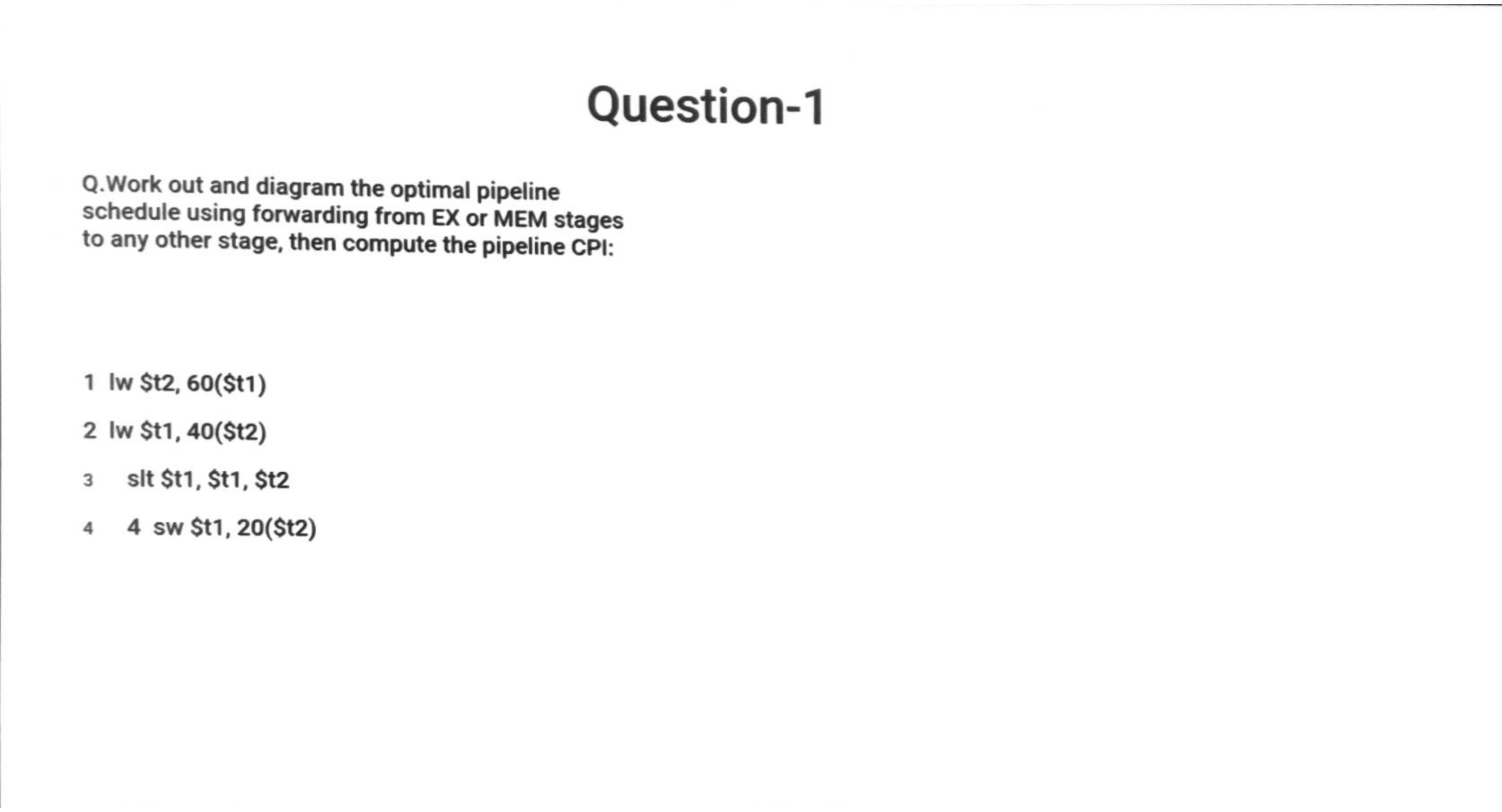
Pipeline hazards are conditions that can occur in a pipelined machine that impede the execution of a subsequent instruction in a particular cycle for a variety of reasons.

Common pipeline hazards:

a) Data Hazards: RAW hazards, WAR Hazards,WAW hazards.

b) Control Hazards

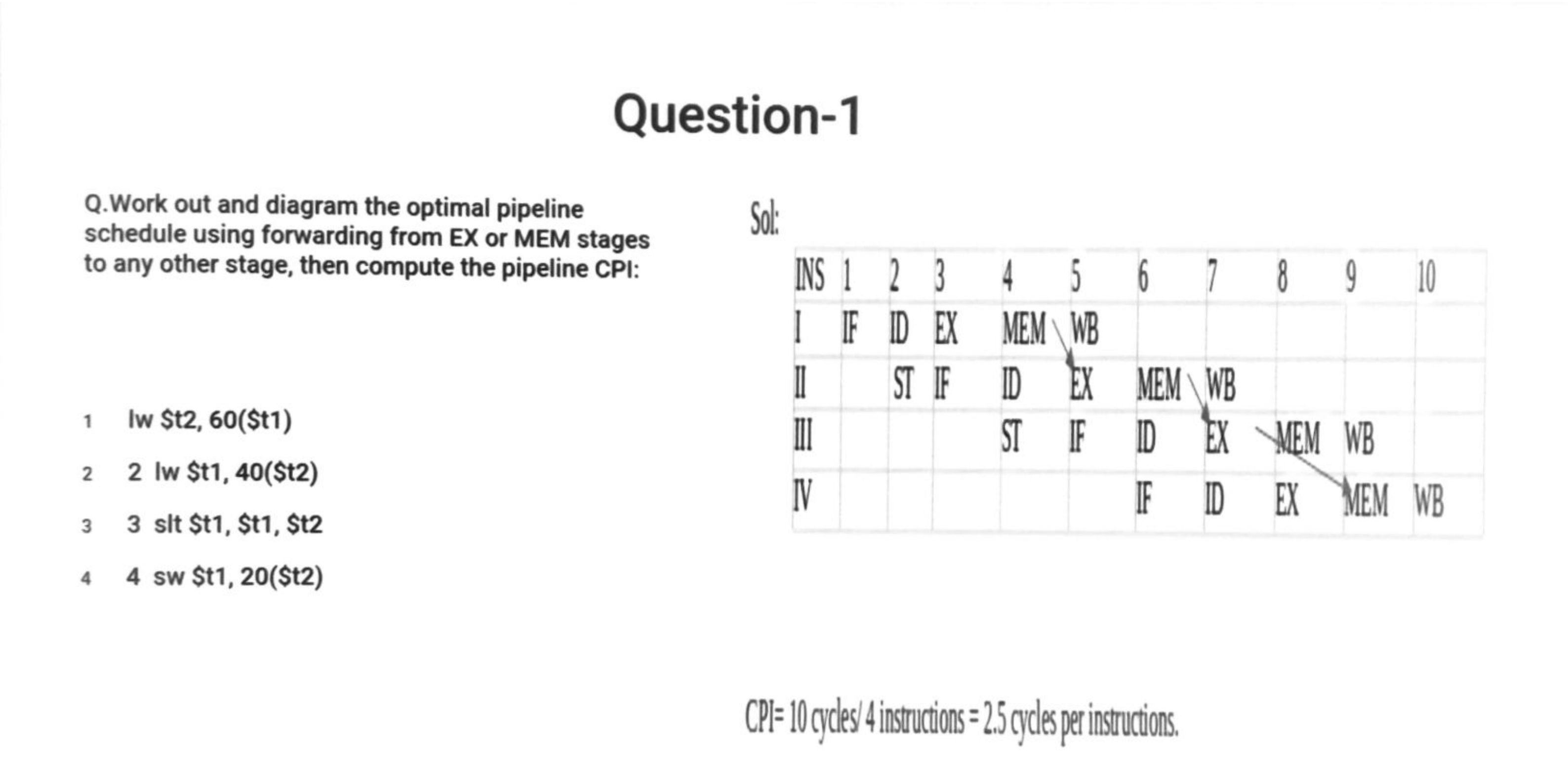
c) Structural Hazrads



Question-1

Q.Work out and diagram the optimal pipeline schedule using forwarding from EX or MEM stages to any other stage, then compute the pipeline CPI:

```
1 lw $t2, 60($t1)
2 lw $t1, 40($t2)
  slt $t1, $t1, $t2
  4 sw $t1, 20($t2)
```



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```

Sol:

INS	1	2	3	4	5	6	7	8	9	10
I	IF	ID	EX	MEM	WB					
II		ST	IF	ID	EX	MEM	WB			
III				ST	IF	ID	EX	MEM	WB	
IV						IF	ID	EX	MEM	WB

CPI= 10 cycles/ 4 instructions = 2.5 cycles per instructions.

Question-2

Q.Sequence of instructions:

1. lw $s2, 0($s1)
2. lw $s1, 40($s6)
3. sub $s6, $s1, $s2
4. add $s6, $s2, $s2
5. or $s3, $s6, $zero
6. sw $s6, 50($s1)

Mention the data dependencies??

Question-2

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2. lw $s1, 40($s6)
3. sub $s6, $s1, $s2
4. add $s6, $s2, $s2
5. or $s3, $s6, $zero
6. sw $s6, 50($s1)

Mention the data dependencies??

sol:

3 depends on 1 ($s2)

3 depends on 2 ($s1)

4 depends on 1 ($s2)

5 depends on 4 ($s6)

6 depends on 2 ($s1)

6 depends on 4 ($s6)

Question-3

Q.Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3 and I4 in stages S1, S2, S3 and S4 is shown below-

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop and how many are the stall cycles ?

for(i=1 to 2) { I1; I2; I3; I4; }

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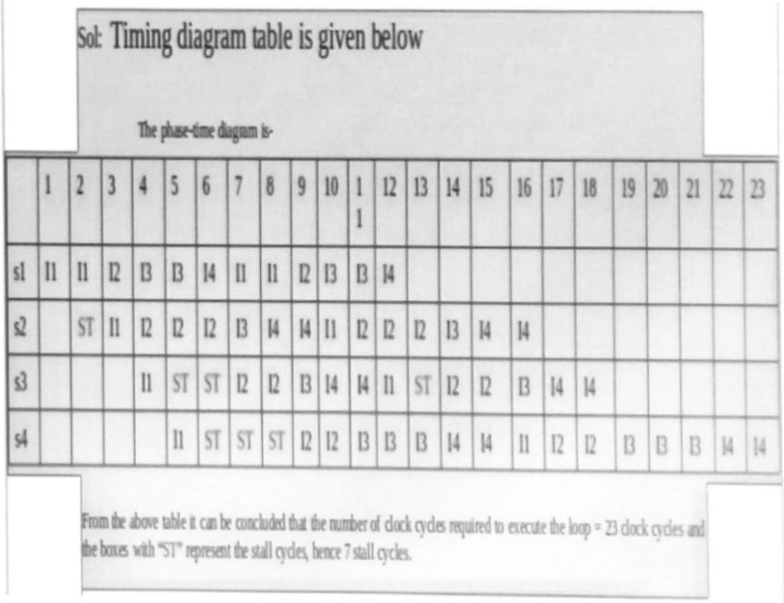
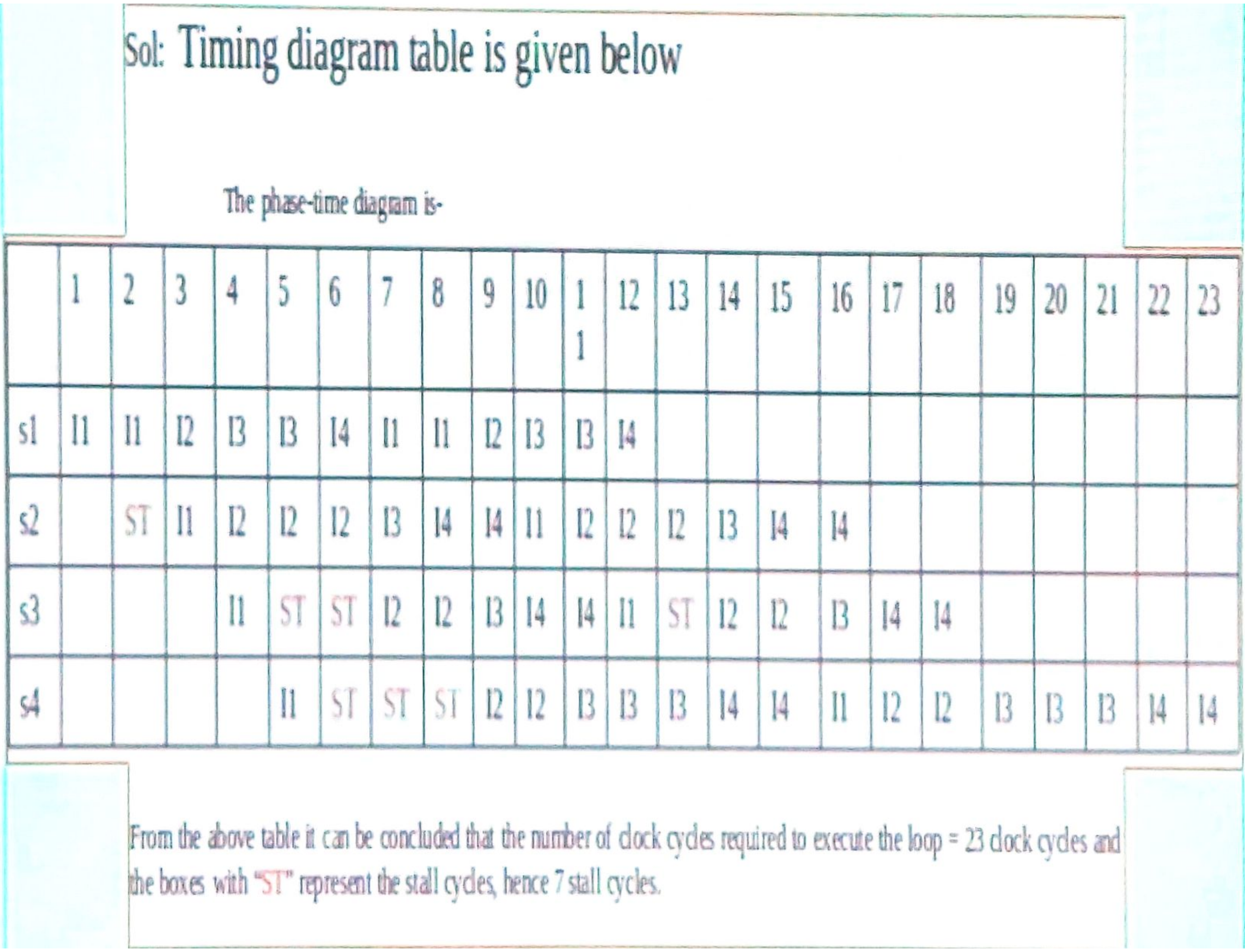


Sol: Timing diagram table is given below

The phase-time diagram is-

	1	2	3	4	5	6	7	8	9	10	1 1	12	13	14	15	16	17	18	19	20	21	22	23
s1	I1	I1	I2	I3	I3	I4	I1	I1	I2	I3	I3	I4											
s2		ST	I1	I2	I2	I2	I3	I4	I4	I1	I2	I2	I2	I3	I4	I4							
s3				I1	ST	ST	I2	I2	I3	I4	I4	I1	ST	I2	I2	I3	I4	I4					
s4					I1	ST	ST	ST	I2	I2	I3	I3	I3	I4	I4	I1	I2	I2	I3	I3	I3	I4	I4

From the above table it can be concluded that the number of clock cycles required to execute the loop = 23 clock cycles and the boxes with "ST" represent the stall cycles, hence 7 stall cycles.



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The phase-time diagram is-

	1	2	3	4	5	6	7	8	9	10	1 1	12	13	14	15	16	17	18	19	20	21	22	23
s1	I1	I1	I2	I3	I3	I4	I1	I1	I2	I3	I3	I4											
s2		ST	I1	I2	I2	I2	I3	I4	I4	I1	I2	I2	I2	I3	I4	I4							
s3				I1	ST	ST	I2	I2	I3	I4	I4	I1	ST	I2	I2	I3	I4	I4					
s4					I1	ST	ST	ST	I2	I2	I3	I3	I3	I4	I4	I1	I2	I2	I3	I3	I3	I4	I4

From the above table it can be concluded that the number of clock cycles required to execute the loop = 23 clock cycles and the boxes with "ST" represent the stall cycles, hence 7 stall cycles.

Question-4

Q. We have a RISC processor with register-register arithmetic instructions that have the format R1 = R2 op R3. The pipeline for these instructions runs with a 100 MHz clock with the following stages: instruction fetch = 2 clocks, instruction decode = 1 clock, fetch operands = 1 clock, execute = 2 clocks, and store result = 1 clock.

a)At what rate (in MIPS) can we execute register-register instructions that have no data dependencies with other instructions?

b)At what rate can we execute the instructions when every instruction depends on the results of the previous instruction?

Question-4

Q. We have a RISC processor with register-register arithmetic instructions that have the format R1 fl R2 op R3. The pipeline for these instructions runs with a 100 MHz clock with the following stages: instruction fetch = 2 clocks, instruction decode = 1 clock, fetch operands = 1 clock, execute = 2 clocks, and store result = 1 clock.

a)At what rate (in MIPS) can we execute register-register instructions that have no data dependencies with other instructions?

Sol: a) No dependencies rate = 1 inst/2 cycles at 100 MHz clock = 50 MIPS.

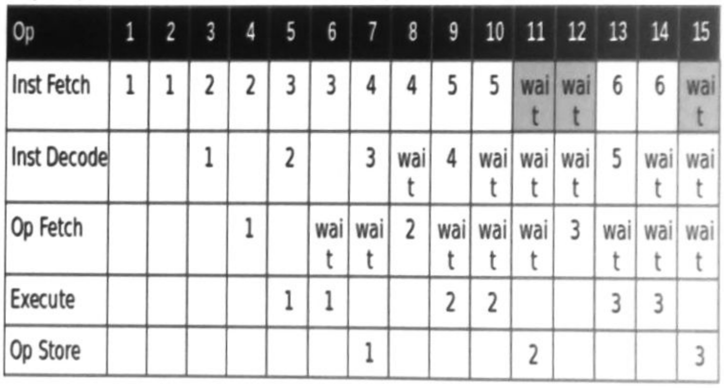
Op	1	2	3	4	5	6	7	8	9	10	11	12
Inst Fetch	1	1	2	2	3	3	4	4	5	5	6	6
Inst Decode			1		2		3		4		5	
Op Fetch				1		2		3		4		5
Execute					1	1	2	2	3	3	4	4
Op Store							1		2		3	

Question-4

Q. We have a RISC processor with register-register arithmetic instructions that have the format R1 fl R2 op R3. The pipeline for these instructions runs with a 100 MHz clock with the following stages: instruction fetch = 2 clocks, instruction decode = 1 clock, fetch operands = 1 clock, execute = 2 clocks, and store result = 1 clock.

b)At what rate can we execute the instructions when every instruction depends on the results of the previous instruction?

b) Dependencies rate = 1 inst/4 cycles = 25 MIPS.



Op	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Inst Fetch	1	1	2	2	3	3	4	4	5	5	wait	wait	6	6	wait
Inst Decode			1		2		3	wait	4	wait	wait	wait	5	wait	wait
Op Fetch				1		wait	wait	2	wait	wait	wait	3	wait	wait	wait
Execute					1	1			2	2			3	3	
Op Store							1				2				3

Question-5

Q.An instruction requires four stages to execute: stage 1 (instruction fetch) requires 30 ns, stage 2 (instruction decode) = 9 ns, stage 3 (instruction execute) = 20 ns and stage 4 (store results) = 10 ns. We want to set this up as a pipelined operation. How many stages should we have and at what rate should we clock the pipeline?

Question-5

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Sol:

We have 4 natural stages given and assuming that each stage is not further subdivided. A 4 stage pipeline is designed. Now, the clock rate for the pipeline going by the convention would be equal to the latency of the slowest stage i.e 30ns. Therefore, the pipeline will fetch a new instruction every 30ns with a pipeline latency for each instruuction being 30*4 =120ns.

The optimized choice would be 10ns with 3 clocks for stage1, 1 clock for stage2, 2 clocks for stage3, 1 clock for stage4 totalling to 7 clocks latency for each instruction ie 70ns instead of 120ns.

Question-6

Q.For a pipelined CPU with a single ALU, consider the following :

A: The j+ 1st instruction uses the result of jth instruction as an operand

B: Conditional Jump Instruction

C: jth and j +1st instructions require ALU at the same time which one of the above causes a hazard ?