Ivame		interrace	Slave Segment	Master Base Address	-	tange	Master High Address
∨ 🛱 Network 0							
Fused_c	core_0						
∨ III /Fuse	d_core_0/M00_AXI (32 address bits : 4G)						
¹ ‡ /dd	r4_0/C0_DDR4_MEMORY_MAP	C0_DDR4	CO_DDR4_ADDRE	0x8000_0000	0 2	2G	• 0xFFFF_FFFF
# /MB_FU_0	0						
∨ III /MB_FI	U_0/M00_AXI (32 address bits : 4G)						
¹ ‡ /dd	r4_0/C0_DDR4_MEMORY_MAP	C0_DDR4	CO_DDR4_ADDRE	0x8000_0000	0 2	2G	• 0xFFFF_FFFF
√	aze_0						
∨ 🔡 /micro	blaze_0/Data (32 address bits : 4G)						
1 1 /axi	_uartlite_0/S_AXI	S_AXI	Reg	0x4060_0000	0 6	54k	▼ 0x4060_FFFF
¹≇ /dd	r4_0/C0_DDR4_MEMORY_MAP	C0_DDR4	CO_DDR4_ADDRE	0x8000_0000	0 2	2G	• 0xFFFF_FFFF
¹ ‡ /mio	croblaze_0_local_memory/dlmb_bram_if_cntlr/S	LSLMB	Mem	ΘxΘ	0 1	.6k	▼ 0x3FFF
∨ III /microblaze_0/instruction (32 address bits : 4G)							
¹\$ /dd	r4_0/C0_DDR4_MEMORY_MAP	C0_DDR4	CO_DDR4_ADDRE	0x8000_0000	0 2	2G	• 0xFFFF_FFFF
¹ ‡ /mio	croblaze_0_local_memory/ilmb_bram_if_cntlr/SL	SLMB	Mem	0x0	0 1	6k	▼ 0x3FFF