1. Fetch

# Instruction Set Architecture

|  |  |
| --- | --- |
| One Operand | Opcode |
| NOP | 00000 |
| SETC | 00001 |
| CLRC | 00010 |
| NOT | 00011 |
| INC | 00100 |
| DEC | 00101 |
| OUT | 00110 |
| IN | 00111 |

|  |  |
| --- | --- |
| Two Operand | Opcode |
| MOV | 01000 |
| ADD | 01001 |
| SUB | 01010 |
| AND | 01011 |
| OR | 01100 |
| SHL | 01101 |
| SHR | 01110 |
| MOV | 01000 |

|  |  |
| --- | --- |
| Memory Operations Instructions | Opcode |
| PUSH | 10000 |
| POP | 10001 |
| LDM | 10010 |
| LDD | 10011 |
| STD | 10100 |

|  |  |
| --- | --- |
| Branch and Change of Control Operations | Opcode |
| JZ | 11000 |
| JN | 11001 |
| JC | 11010 |
| JMP | 11011 |
| CALL | 11100 |
| RET | 11101 |
| RTI | 11110 |

# IR Content for ONE OPERAND Instructions

1. Opcode[3] | SRCexist[1] | DSTexist[1] | XXXX | DST[3]

# IR Content for TWO OPERAND instructions:

01 | Opcode[3] | SRCexist[1] | DSTexist[1] | X | SRC[3] | DST[3]

SHL,SHR:  
01 | Opcode[3] | SRCexist[1] | DSTexist[1] | imm | DST[3]

# IR Content for MEMORY instructions:

1. Opcode[3] | SRCexist[1] | DSTexist[1] | X | SRC[3] | DST[3]

# IR Content for BRANCHING and CONTROL instructions:

11 | Opcode[3] | SRCexist[1] | DSTexist[1] | XXXX | DST[3]

1. Decode

# Generated Signals:

## Signal S:

A signal to detect if the two instructions can be executed together, or an instruction needs two memory words and the second part of it hasn’t been fetched yet (LDM).

S = ‘1’ if   
(dst1 = dst2) && (dst1, dst2 exist) && (inst2!= {IN, POP,LDD}) OR  
(dst1 = src2) && (src2, dst1 exist) OR  
(inst2 = LDM) OR  
(inst1 && inst2 use memory ) OR  
(inst1 = (oneOp || twoOp) && not(NOP,OUT,MOV) )&& (inst2 = branch)

## Signal WB1, WB2:

WB1 = dst1 && (inst1 != STD)  
WB2 = dst2 && (ints2 != STD)

## Signal W/R Memory:

W = (inst1 or inst2 = {PUSH, STD,CALL })  
R = (inst1 or inst2 = {POP, LLD, RETURN })

## First Operand

|  |  |
| --- | --- |
| Instruction | ALU |
| NOP | F=0 |
| SETC | C <= 1 |
| CLRC | C <= 0 |
| NOT | F = NOT B |
| INC | F = INC B |
| DEC | F = DEC B |
| OUT | F = 0 |
| IN | F=0 |

## Two Operands

|  |  |
| --- | --- |
| Instruction | ALU |
| MOV | F = 0 |
| ADD | F = A + B |
| SUB | F = B – A |
| AND | F = A and B |
| OR | F= A OR B |
| SHL | F = SHL B |
| SHR | F = SHR B |

## Memory

|  |  |
| --- | --- |
| Instruction | ALU |
| STD | F = 0 |
| Others | F=0 |

## Branch

|  |  |
| --- | --- |
| Instruction | ALU |
| JZ , JN , JC , CALL , JUMP | F = B |
| Others | F=0 |

1. Execute

# Generated Signals:

## Bubble:

A signal to indicate load-use.

B = ‘1’ if:  
(ID/IE.R1) && (ID/IE.dst1 = ( (IF/ID.dst1 && IF/ID.dst1 exist) ||   
(IF/ID.dst2 && IF/ID.dst2 exist ) || ( IF/ID.src1 && IF/ID.src1 exist ) ||  
 (IF/ID.src2 && IF/ID.src2 exist ) ) ) OR  
(ID/IE.R2) && (ID/IE.dst2 = ( (IF/ID.dst1 && IF/ID.dst1 exist) ||   
(IF/ID.dst2 && IF/ID.dst2 exist ) || ( IF/ID.src1 && IF/ID.src1 exist ) ||  
 (IF/ID.src2 && IF/ID.src2 exist ) ) ).

## Jump:

Jmp1 = ‘1’ if  
(C = ‘1’ && inst1= JC) || (N=’1’ && inst1 = JN) || (Z=’1’ && inst1 = JZ) || (.inst1 = JMP) || (inst1 = CALL)

Jmp2 = ‘1’ if  
(C = ‘1’ && inst2= JC) || (N=’1’ && inst2 = JN) || (Z=’1’ && inst2 = JZ) || (inst2 = JMP) || (inst2 = CALL)

## Memory Forward:

MF = A1 || B1 || C1 || D1 || A2 || B2 || C2 || D2

A1 = (IM/WB.R1) && (IM/WB.dst1 = (ID/IE.dst1 && ID/IE.dst1 exist))  
B1 = (IM/WB.R1) && (IM/WB.dst1 = (ID/IE.dst2 && ID/IE.dst2 exist ))  
C1 = (IM/WB.R1) && (IM/WB.dst1 = ( ID/IE.src1 && ID/IE.src1 exist ))  
D1 = (IM/WB.R1) && (IM/WB.dst1 = (ID/IE.src2 && ID/IE.src2 exist ))

A2 = (IM/WB.R2) && (IM/WB.dst2 = (ID/IE.dst1 && ID/IE.dst1 exist))  
B2 = (IM/WB.R2) && (IM/WB.dst2 = (ID/IE.dst2 && ID/IE.dst2 exist ))  
C2 = (IM/WB.R2) && (IM/WB.dst2 = ( ID/IE.src1 && ID/IE.src1 exist ))  
D2 = (IM/WB.R2) && (IM/WB.dst2 = (ID/IE.src2 && ID/IE.src2 exist ))

## ALU Forward:

AluF = E1 || F1 || G1 || H1 || E2 || F2 || G2 || H2

E1 = (IE/IM.Ex1) && (IE/IM.dst1 = (ID/IE.dst1 && ID/IE.dst1 exist))  
F1 = (IE/IM.Ex1) && (IE/IM.dst1 = (ID/IE.dst2 && ID/IE.dst2 exist ))  
G1 = (IE/IM.Ex1) && (IE/IM.dst1 = ( ID/IE.src1 && ID/IE.src1 exist ))  
H1 = (IE/IM.Ex1) && (IE/IM.dst1 = (ID/IE.src2 && ID/IE.src2 exist ))

E2 = (IE/IM.Ex2) && (IE/IM.dst2 = (ID/IE.dst1 && ID/IE.dst1 exist))  
F2 = (IE/IM.Ex2) && (IE/IM.dst2 = (ID/IE.dst2 && ID/IE.dst2 exist ))  
G2 = (IE/IM.Ex2) && (IE/IM.dst2 = ( ID/IE.src1 && ID/IE.src1 exist ))  
H2 = (IE/IM.EX2) && (IE/IM.dst2 = (ID/IE.src2 && ID/IE.src2 exist ))