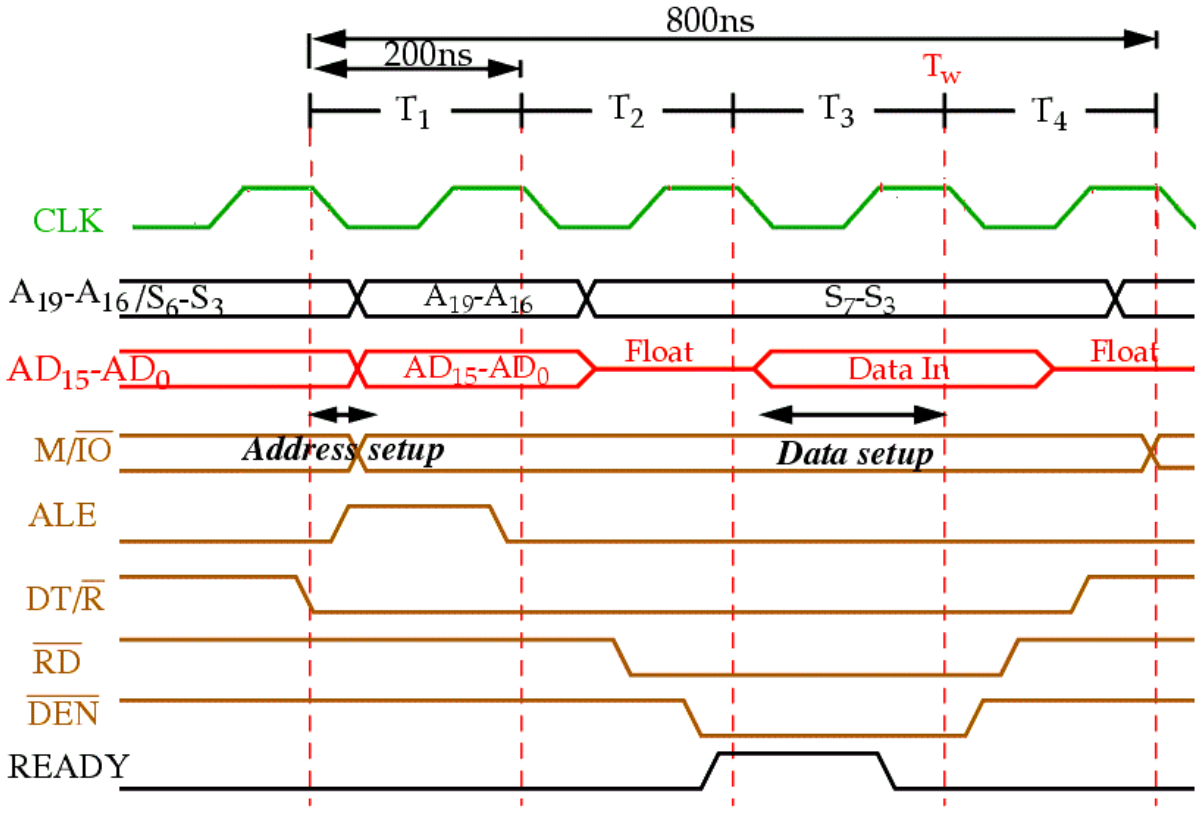
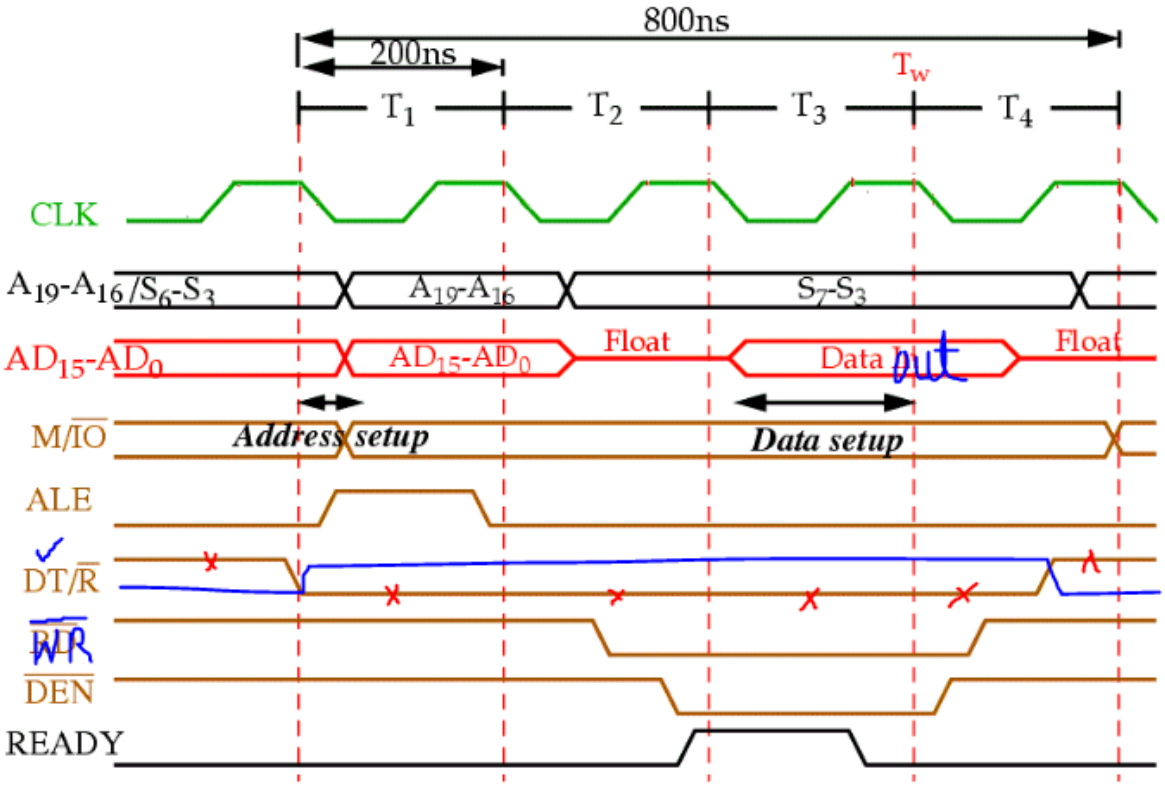
Read Cycle Timing Diagram:



T1	T2	T3	Tw (optional)	T4
AD15–AD0: 1st 16 bit address [high/low] **A19–A16**: Last 4 bit address [high/low] **ALE**: Goes HIGH → Latch the address **M/$\overline{IO}$**: Identifies where to read data memory or IO from the 20 bit address **DT/ $\overline{R}$ goes LOW**	**$\overline{RD}$ goes LOW** → To read from memory **DEN goes LOW** → **Data Enable**; allows the system to use the data bus. .	The memory places the **actual data** onto the data bus (**AD15–AD0**). This is shown as **"Data In"** in the diagram. Processor reads this data during T3.	If memory/IO is **slow**, the **READY signal stays LOW**, and a **wait state** is added. This gives memory more time to place the data on the bus. When READY goes HIGH → 8086 continues reading.	$\overline{RD}$ goes HIGH (read done) DEN goes HIGH (disable data bus) DT/ $\overline{R}$ goes HIGH (bus direction neutral) Data lines **float** again, meaning they are released. Cycle ends, CPU now **has the data**, and moves to the next instruction.

→ tells bus transceivers this is a **read** operation. Bus is now set up to **receive** data				

Write Cycle Timing Diagram:



T1	T2	T3	Tw (optional)	T4
AD15–AD0: 1st 16 bit address [high/low] **A19–A16**: Last 4 bit address [high/low] **ALE**: Goes HIGH → Latch the	**Data (to be written) is placed on AD15–AD0** by the CPU. **DT/ R̄** = HIGH (data is going out from CPU). $\overline{DEN}$ = **LOW** (data	**WR̄** remains low Data lines hold valid data. Memory or IO receives it	Same as in read: if **READY = LOW**, CPU **waits**. Useful for slow memory or I/O devices.	**WR̄ goes HIGH** → end of write. $\overline{DEN}$ = **HIGH** → release the data bus. **DT/ R̄** = LOW → reset direction. **Data lines float** or reset

address **M**/$\overline{IO}$: Identifies where to write data memory or IO from the 20 bit address	bus is enabled). **W**$\overline{R}$ = **LOW** → To signal - Start Writing			for next operation.