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a) ionic movements rely in the device preformance on the available defects and their mobilities. http://ma.ecsdl.org/content/MA2018-01/32/1952.short

# 1. Memristive device, ion-migration devices, and their application in non-conventional computing

## 1.1 memristive devices and its types

Here, memristive device is defined as the devices with non-volatile programmable resistance or transfer characteristics. In a memristive device, information is represented with the internal resistance state which is stably retained within its retention time, showing a long-term memory effect. For example, binary bit 0 or 1 is represented in the high-resistance state (HRS) and low-resistance state (LRS) of a non-volatile programmable resistive switch. A numerical value is represented in term of a conductance level. A memristive device is programmed with voltage and current, and stored information is read out by probing current or voltage following Ohmic law.

An intensively discussed concept "memristor" is a kind of passive two-end continuously tunable resistor devices. In the definition made by Chua, memristor is a hypothetical basic element, whose resistance is not a constant or a value depending on instant inputs, but on the integral of passed current, i.e. the historical charge flux passed through it[1,2]. In 2008 the concept of memristor is firstly linked to real world devices[3,4]. In these research, 50-nm-thick $TiO_2$ is sandwiched between two Pt layers, constructing a 2-end resistive device. $O^{2-}$ anions migrate under applied voltage, resulting in the non-volatile resistance change of device.

Alongside 2-end memristors, memristive device can also be built in 3-end configurations, similar to FETs[5,6]. In this configuration, memristive materials are usually adopted as a conductive channel connected with 2 electrodes as the source and drain contacts, with a third gate electrode separated by an insulation (e- blocking) layer. Channel conductance are controlled by gate voltage applied. Different from FETs, the conductance change in channel is non-volatile, showing the memory effect.

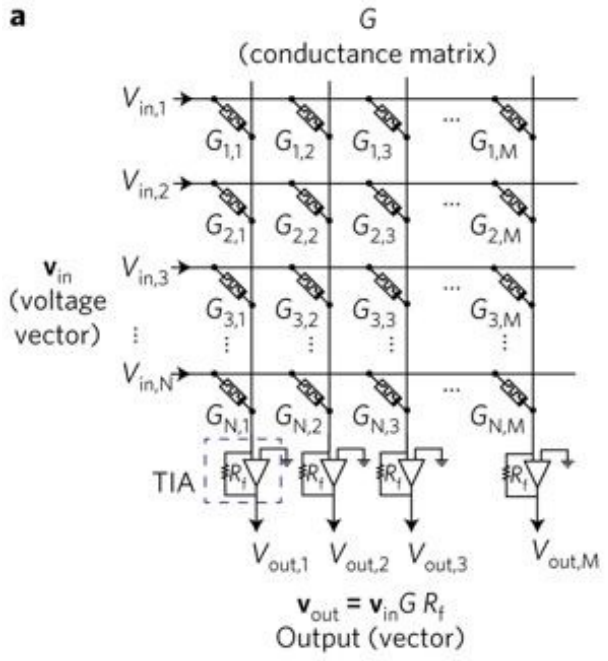
Though starts with transition metal oxides, the concept of memristive devices has expanded to various material systems, based on different conductive modulation mechanisms. These materials types are discussed in relevant reviews[7-20]. Commonly studied material categories and mechanisms are: O-vacancies-mediated conduction in O-deficient oxides[14-16], metal conductive bridge in dielectrics[17,18], crystal/amorphous phase change in phase change materials (PCM)[19], floating-gate FETs, traps-mediated transporting and barrier, domain movement in ferroelectric materials, carrier regulations in conductive polymers[20], etc. Their common feature is the ability to provide non-volatile resistance changes, which is determined by the history of current passing

through or gate voltage applied. A memristor has non-linear I-V characteristic, programming is only valid when voltage exceed the threshold. Therefore for a 2-end memristive device, read operations can be done with a current smaller than the threshold current.

### 1.2 memristive devices in non-conventional computing

Conventional computer architecture is deeply attached to the von Neumann architecture, which contains a memory unit containing instructions and data, a processing unit for performing arithmetic and logical operations, and a control unit for interpreting instructions. In von Neumann architecture, the central processing unit (CPU) and memory unit are separated, and the program memory and data memory share the same system bus. This leads to a limitation of data transfer rate between the CPU and memory, i.e. the von Neumann bottleneck. Besides, the transferring causes a loss in energy efficiency. Therefore, to circumvent the limitation brought by von Neumann bottle neck, non-conventional computation concepts have been raised. Among them what memristive devices are to be involved in are parallel computing and neuronal computing.

An exact example of how memristors perform parallel computing is performing vector productions with memristor crossbar array[21]. With continuously controllable resistivity, memristive devices provide an expression of numeric values in the form of resistance value. In such an application, input vector is represented in paralleled voltage inputs, and a multiplication result can be represented by a current equals to voltage multiple memristor conductance, based on Ohmic relationship. And the current sums up at the node following Kirchoff's current law, resembling the adding up of each element in the vector inner production. In a memristive device, the inner product of two vectors can be represent by voltage inputs applying on an equal-length 1D memristor array, and the sum of the results from each memristor. Similarly, a 2-d memristor crossbar array can represent the product of one vector and a matrix, with each element of matrix stored in the form of memristor conductance.



Schematic of the VMM operation. Multiplication is performed via Ohm's law, as the product of the voltage applied to a row and the conductance of a cross point cell yields a current injected into the column, while the currents on each column are summed according to Kirchhoff's current law. The total current from each column is converted to a voltage by a trans-impedance amplifier (TIA), which also provides a virtual ground for the column wires[21]

In this demonstration, a 128x64 array is built with each memristor combining with a transistor as selectors ("1T1R" structure). The devices are of high uniformity, and can be programmed to nearly arbitrary resistance values. Image compression and convolutional image filtering are performed with the memristor array as vector multiplexer. This implement shows the potential of computation based on memristive hardware, and especially the potential in Internet of Things (IoT) edge computing due to the ultra-low energy consumption.

Another non-conventional computing concept is neuronal computing based on artificial neural networks (ANNs). ANN is a computing system inspired by the way the bio nervous system operates. In a biology neural system, neurons are the processing units, and are interconnected through synapses. One neuron receives potentiation or inhibition signals from preceding neurons through synapses, and passes the computation results to the following neurons in terms of spikes. During a learning process, according to the learning rules in bio systems, the connection between two neurons are strengthened or weakened, and the network's responses to input stimulus are modified.

Similarly, in an ANN, artificial neurons are the computation nodes connected to each other in a hierarchical form, and each connection is assigned a weight *w*. During a learning process, the weights between neurons in different layers are adjusted according to learning rules. Each neuron (except in input or output layers) accepts several output values from the preceding layer through the connections, integrates and propagates the integration to neurons in the next layer. Among these steps, the acceptance of inputs is represented by the propagation function, having the form of:

$$p_j(t) = \sum_i o_i(t) w_{ij}$$

In which $p$ is the input passing to neuron $j$, and $o_i$ indicates the output from each neuron in the preceding layer, $w$ is the weight between neuron $i$ and $j$. And the output of a neuron is defined by the activation function, usually in the form of a sigmoid function such as:

$f(x) = \frac{1}{1+e^{-x}}$ and $f(x) = \tanh x = \frac{e^{x} - e^{-x}}{e^{x}+e^{-x}}$, etc.

ANN has made significant progresses in artificial intelligence applications, such as image analyzing, natural language processing, speech recognition, etc. ANN related works are commonly accelerated on GPUs and FPGAs[22]. To further fulfill the high requirements of calculation in AI tasks, ASICs are also designed for ANN acceleration[23].

From the way the ANN operates we can find: the weight is the representation of the interrelation between neurons, and the weight multiplication and the integration is basically the vector-matrix multiplication, which has been illustrated to be able to perform on memristive arrays. This is fundamentally why ANNs can be directly realized at the hardware level with memristive devices act as the weight matrix. In this configuration the memory (weight) and processing units (neurons) are integrated together. Also the energy efficiency of the inferencing is greatly improved. Another favorable factor is that ANN has inherent tolerance to device variation. The device-to-device and cycle-to-cycle variations, which are the significant drawbacks of memristive devices, are less intense when the training result (weight values) converges.

Like software ANNs, this hardware ANN is trained by updating the weight values (resistances) according to back-propagation method. Therefore the weight updating typically relies on external electronics. An example of memristor-based HNN training is given in Ref.[24]. In this demonstration, the training task is a 3x3 pixels pattern classification, performing on a one-layer network. The inputs are nine input positive or negative voltages indicates whether white or black is the pixel, and one bias voltage as the 10th input. The *i* th output target value $f_i^{(g)}(n)$ =+0.85V or -0.85V indicating the right or wrong, for the *n* th input pattern. For one neuron, the integration of inputs is $I_i = \sum_{j=1}^{10} W_{ij} V_j$, where I is current, W is conductance, and Vj indicates the j th input signal in voltage, and the activation function is $f_i = \tanh(\beta I_i)$. Delta function is calculated by $\delta_i(n) = \left[f_i^{(g)}(n) - f_i(n)\right] \left.\frac{df}{dI}\right|_{I=I_i(n)}$ and weight change is given by $\Delta W_{ij} = \eta \, \mathrm{sgn} \sum_{n=1}^{N} \Delta_{ij}(n)$ $\Delta_{ij}(n) = \delta_i(n) V_j(n)$ where η is the learning rate. Negative/positive programming pulses with identical amplitude is applied on memristor according to the signature of ΔWij. As training epoch number increases, the number of misclassified patterns decreases, showing the effect of training.

On the other hand, also inspired by biology neural systems, spiking neural networks (SNNs) are illustrated. The difference between SNN and common ANN is the way of encoding information. Conventional ANNs use real numbers to represent values and correlations. In every calculation, values and correlations are constants which are irrelevant to time or temporal sequence. In a hardware ANN, the information are encoded in voltages or conductance levels, therefore is described as “level-based” encoding. On the contrary, the emerging concept SNN is based on discreet spikes, rather than static values in ANN. In SNNs, information is encoded in the dimension of time, such as spike intervals, spike frequency. SNN more closely resembles bio neural systems than ANN. Like bio systems use spikes to convert signal, SNN neurons do not provide outputs constantly, but only fire when the integration of inputs reaches the threshold, similar to the membrane potential reaching firing threshold in bio systems, and the output result is transmitted to the next neuron layer in terms of a spike train. The event-driven feature gives SNN extraordinary energy efficiency[25,26], and internal consistency with hardware neuron networks. A famous example of SNNs is the IBM TrueNorth[27]. Based on SNN, the neuromorphic

computation can be performed with an extreme energy efficiency. As for the realization in memristive HNN, the spike trains are represented by voltage pulses, weights are represented by conductance, and the function of neuron can be described with a leaky integrate-fire elements.

SNN is appealing to hardware neural networks because of the potential of realizing on-line and non-supervised training. In this training protocol, the weight is updated according to input and output pulses temporal relations, following the learning rules like Hebbian learning, which is introduced in the next section. This training protocol is promising to avoid the limitation induced by off-line back-propagation training, in which the weight update have to be performed with peripheral efforts. Therefore SNN is consider an implement to fully utilize the potential of hardware neural networks.

### 1.3 Concepts in neuromorphic computing: STP, LDP; un-supervised learning, Hebbian learning and STDP

Synaptic plasticity is the ability of synapses to strengthen or weaken its connection activity. According to the difference between strengthening or weakening, and the effect duration time scale, there are 4 forms of plasticity: short-term potentiation (STP), short-term depression (STD), long-term potentiation (LTP) and long-term depression (LTD). Paired pulse facilitation (PPF) and paired pulse depression (PPD) are typical short-term plasticity behaviors. In the HNN implementations, the synaptic activity is the response of post-synaptic current to the pre-synaptic stimuli, usually pulse voltages. In a 2-end structure the synaptic activity is the relation between current and applied voltage, while in a 3-end structure the pre-synaptic stimuli is usually applied on the gate, and post-synapse current is the channel current under a read Vds. Due to the complex and rich physics properties in memristive devices, various synaptic plasticity behaviors are observed in memristive devices, similar to the four forms of plasticity in biology neural systems. For example, STP and LTP, and the transition between STP and LTP are found in conductive bridge devices[28]. In 3-end structure with ion migration in electrolyte layers, STP is found shortly after each programming pulse, and shows a overall LTP[29]. PPD and PPF are found to co-exist in Ag:SiOxNy devices, and the transition is induced by different pulse intervals[30].

Spike-timing-dependent plasticity (STDP) is a learning rule that attracts intense attention in SNN training. It extracts the temporal correlation of events as numeric values. Simplistically, STDP is “fire together, wire together”. Specifically, in two correlated neurons A and B, if B fires shortly after A fires in time, the correlation from A to B is strengthened[31]. In bio systems, neurons learning rules is described by Hebbian learning rules. As defined by Hebb, if the neuron A repeatedly or persistently takes part in firing the neuron B, the efficiency of A firing B is increased. STDP simplifies the causal relationship to temporal relationship: if A takes part in firing B, the firing of B is shortly delayed from A, but not advanced. Therefore in STDP learning, pre-synaptic spikes preceding the post spikes leads to LTP of the synapse, while pre spikes following post spikes lead to LTD.[32] Besides the learning feature mentioned, there are also anti-Hebbian learning rules, and symmetric Hebbian learning rules, as shown in FIG. X. The weight change and timing relationship (B fires after $\Delta t$ from A fires) are shown in the figure.

STDP attracts attention because of its easily implement on SNN hardware, more importantly it allows an unsupervised learning fashion, in which a HNN can adjust the weights according to constantly incoming inputs. This allows a hardware implement handle continuous data inputs, and fully able the potential of HNNs. For example, in an IoT system, edge devices obtain the spatio-temporal data from environment. The spatial and temporal distribution of input signals covers abundant information. A STDP HNN can find the correlation and perform basic data processing with an extreme low energy consumption, enhancing the computing and data efficiency of the whole IoT system.

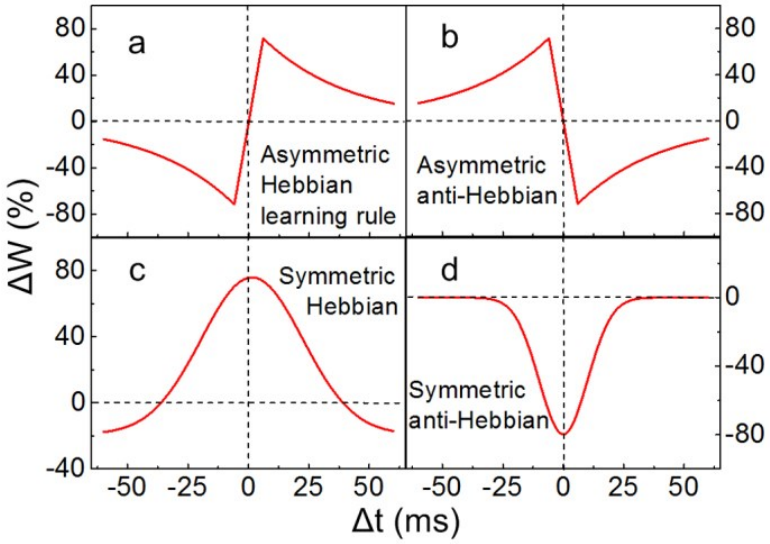



FIG. STDP learning rules. (a) Asymmetric Hebbian learning rule. (b) Asymmetric anti-Hebbian learning rule. (c) Symmetric Hebbian learning rule. (d) Symmetric anti-Hebbian learning rule.[33]

# 2. **Synaptic Memory Materials**

## 2.1 memristive devices

In this article, we will discuss the memristive materials and devices based on ions migration. This type of memristive devices utilize the movement of atoms, are the behavior is closely related to atoms migration, distribution, and defects, therefore sharing a similarity in device characteristic and modeling. This device type has been intensely studied and have many successful demonstrations. Based on the types of ions, the materials can be categorized into 3 types: 1) anions in compound semiconductors/insulators (typically oxygen anion, nitrogen anions are also reported in some researches); 2) heavy metal cations (e.g. Ag+ in AgS2 matrix); 3) small cations such as Li+ and H+. According to different types of ions, the design and characteristics of devices are also different.

## 2.2. Metal-oxides-based nonvolatile

Defects conduction drives the functionality of oxide-based nonvolatile memristive devices. The characteristic of oxides-based memristive devices is that the conductance is mediated by donor-type O-vacancies ($V_O$) and therefore local oxidize state (valence change). $V_O$ concentrates and disperses under the synergistic effects of electric field and temperature. The region where the $V_O$s concentrate has lower oxidize state and higher carrier density, and are the conductive structures in a device. The geometric and composition change alter the conductance of devices.

A typical 2-end oxides-based memristor has a top electrode (TE) /oxides/bottom electrode (BE) sandwiched structure. Here the electrode could be metal, conductive diffusion barrier like TiN[34], or conductive oxides like FTO[35,36] STO[37]. The oxide layer is be one uniform O-deficient oxides[38], or bilayer structure consisting of an O-deficient layer base layer and a thinner layer with higher oxidation state thus higher resistance[39,40]. Mostly in bilayer structures, the base layer serves as an O-vacancy reservoir, and the high resistance layer works as the resistance modulating layer. Bilayer structures are beneficial to device uniformity and energy consumption[24,40].

Numerous oxides have been investigated for resistance flexibility. Research on the non-volatile resistance flexibility of metal-oxides-based devices starts from bipolar resistive switches, aiming at the realization of resistive random access memories (ReRAM). Early demonstrations on ReRAMs include SrZrO3[41], SrTiO3[42], then NiO[43-47], TiO2[48,49], Nb2O5[50], and HfO2[51], Ta2O5[40]. These demonstrations focus on the stability, uniformity and retention of two high and low-resistance states.

With the increasing attention to neuronal computing, the multilevel or continuous conductance modulating devices came into sight. In the first demonstration of oxides memristor from HP lab in 2008[52], TiO2/TiO2-x bilayer structure are fabricated by ALD with metal Pt working as TE/BE. Recent TiOx-based demonstrations include [53]. As a CMOS-compatible high-k material, HfO2 also attracts intense interests in memristive devices, due to great scalability (less than 10 nm), fast switching speed (on the order of ns), satisfactory switching endurance (greater than $10^{10}$ cycles), and reliable data retention[54]39,40[21,55]. TaOx is another extensively studied memristive oxide, multi-level resistance are achieved on TaOx[39,56]. CeOx is another widely used oxide material[57,58]. Perovskite materials (e.g. SrTiO3, PrCaMnO3, LaSrTiO3) are also demonstrated intensively in memristors[59-67], and in many reports interfacial-type resistance switching is observed. Superconductor perovskite materials[68] (e.g. ReNiO3, YBaCuO, LaSrMnO3) are also demonstrated as memristors due to high migration rate and large conductivity change ratio, and in these materials the resistive switching is a bulk process other than filamentary[68]. Switching of filamentary and interfacial geometrics are observed in ZnO[69]. Cross-interface O-migration is observed in $V_2O_5$/ITO[35]. The criteria for material selection mainly depend on the O migration feasibility at room temperature.

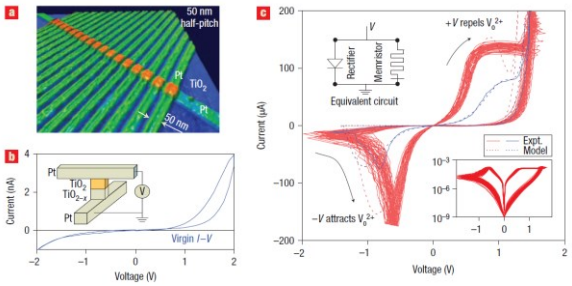
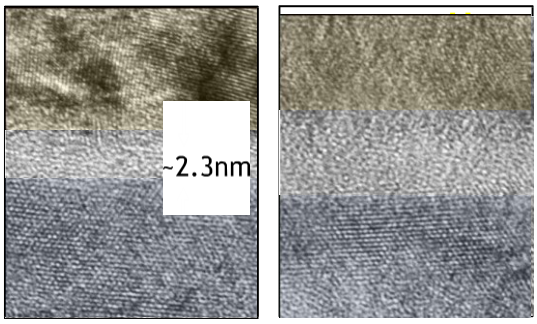



Fig. X. (a) AFM image of the structure of Pt/TiO2/Pt devices. (b) The TiO2 layer has two sections: a near-stoichiometric TiO2 layer and an O-deficient TiO2-x layer. The curve shows the initial state before the initiation. (c) The experimental result of the switching between the ON and OFF states[52].

In most cases the mechanism of resistance change is attributed to the formation of low-valence conductive filaments, as observed in in-situ TEM[49,70,71], scanning TEM electron energy loss spectroscopy [37,72]. These conductive filaments are described to shunt the metal/oxide Schottky barrier by tunneling effect[38,52] or bridge through the insulating layer. Here the insulating layer could be the whole oxide layer[49,73] or a specified high-resistance layer, such as Ta2O5 in Ta2O5/TaO2-x structure[40,70,74]. In common n-type wide-bandgap oxides like TiO2, Ta2O5, O-vacancies are considered as n-type doping, providing additional electrons and increasing the semiconductor conductivity. Besides general semiconductors, strongly correlated metal oxides that have higher sensitivity to oxidation state change, such as WO3[75], are also demonstrated for memristive devices. Compared to general band semiconductors, these oxides have complex electron structures and are more susceptible to defects and change in stoichiometry.

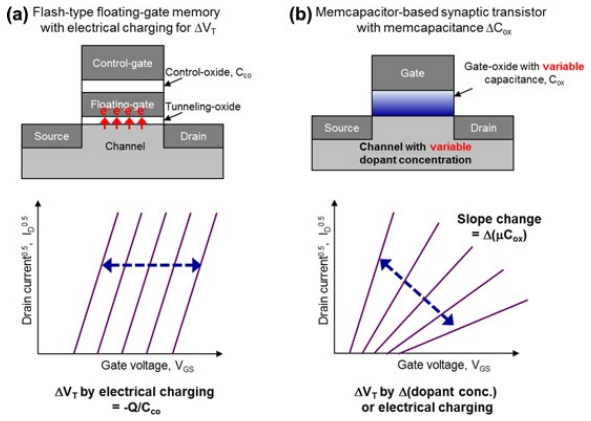
Besides filamentary switching, devices functioned interfacial-type change are also demonstrated. In an interfacial type switching, Vos are believed to accumulate at the switching material/electrode interface, or migrate across interfaces. This induces a modulation in the height of interfacial barrier[76-78], or redox reaction and formation of a third layer at the interface[61,63,64]. For example, Figure shows a cross sectional image of an interfacial type device. As a result of the O migration from PCMO to Mo/PCMO interface, the thickness high-resistance MoOx layer increases, altering the device resistance to high-resistance state. This interfacial type switching attracts interests because it avoids abrupt resistance change and randomness of filament formation, allows more resistance levels and usually gives a more continuous behavior[76]. Unlike filamentary switching, this change occurs with a 2D region adjacent the electrode, other than a channel penetrating the switching layer. Therefore the conductance of interfacial-type devices are closely related to electrode area, which is a signature of interfacial-type devices[79]. This feature provides a way to reduce energy consumption by scaling down. The conversion of these two types are determined by device structure and dimension, and O migration rate of oxides(?).




**(a) Cross-sectional TEM image of a Mo/PCMO device in the low resistance state (LRS). (b) TEM image of a Mo/PCMO device in the high resistance state (HRS). The different thickness of the oxide layer is considered to be the main cause of the change in conductance**

Other O-vacancy-mediated mechanism are raised. In some research the change in conductivity is attributed to bulk defects migration[68,75]. Also mentioned are because of the influence on trap-mediated transport instead of conductive region formation[36,80]. And for devices using oxides electrodes such as FTO, another possible mechanism is pointed out that $O^{2-}$ could migrate across the electrode interfaces, affecting the interface Schottky barrier[35]. As suggested, in these configurations the resistance change is induced by interfacial or bulky change, therefore may have further potential in continuous resistance modulation.

O migration in the gate oxide of FET changes the permittivity of material and the gate capacitance of device. Therefore the FET transfer characteristics is altered accordingly. Based on this idea a synaptic FET is demonstrated with a Pt/HfOx/IGZO stack structure. If oxygen ions migrated from IGZO to HfOx when +V was applied, both the permittivity of HfOx and $C_{ox}$ would be increased, resulting in the change of channel current[81].




Schematic illustrations comparing the transfer characteristics in (a) conventional floating-gate memory and (b) the synaptic transistor in this study.[81]

Though mostly the conductive region formation is attribute to O2- migration, recent researches prove that metal cations also migrate under external field in a short range, and participate in the formation of conductive filaments in oxides[82-86], especially when O2- migration and redox are suppressed. In these researches, metal atoms are observed to form conductive filaments, when the amount, generation, or mobility of oxygen vacancies are confined. E.g. Ta filaments are observed in TaOx when Ta electrode is passivated by amorphous carbon[82] or graphene[86]; in ref[83], Ti

filaments appear when Vo is reduced by oxidation annealing. This mechanism is attribute to the reduction of metal cations, similar to the mechanism of conductive bridge devices. This mechanism leads to a sharper (less continuous) conductance change than O-migration. In addition, since metal exists as atoms in oxides, the metal filaments is less stable and tend to be re-oxidized to cations. Therefore conductance formed by this mechanism decays as time passes.

(Switching review: [87])

## 2.3. Metal cation migration

This kind of devices is based on the migration of diffusible metal atoms dissipated in a dielectric matrix, where metal ions have high migration rate, while anions migration are low (?). Such as Ag, Cu[88,89] in sulphieds[28,90], silicon oxides[91], silicon[92], nitride[93], nitroxides[30], 2D materials[94], or polymer[95,96] and bio-materials[97]. Similarly there is report on In metal in h-BN[98], Ta is also observed to form Ta metal filaments in TaOx under specific condition[86]. Ni or Pt are also observed to be able to transport and form conducting inclusions, but more difficult than Ag and Cu[99]. In the resistance transition process, metal cations are reduced to simple substance, and form a conductive bridge through the dielectric matrix, therefore the metal cation based devices are called conductive bridge (CB) devices. A typical CB-memristor has an asymmetry structure: a dielectric layer is sandwiched between one active electrode (e.g. Ag, Cu) working as the anode, and one inert electrode (e.g. Pt, W) as the cathode. In most cases the migrating cation and the reactive anode are of the same element, but not necessarily. Such as Al used as the anode to drive the migration and reduction of Cu cation[100]. Different from oxygen-migration-mediated devices, in CB devices, conduction is not mediated by carriers introduced by defects. The conductance comes from the conductivity of metal, and the conducting part has significant conductivity compared to non-conductive matrix.

A closer look at nanoscopic scale change during resistance switching gives a more detailed picture of mechanism of metal bridge forming. Observed in in-situ TEM, metal inclusions inside dielectrics can have various morphology and kinetics. The conductive form can be clusters and filaments inside the dielectrics, or dendrites/cone grown on cathode[95], depending on the migration rate and redox rate of metal cations[91,99]. Specifically, cations having low mobility tend to be reduced inside the dielectric matrix, leaving nano-particles and filaments inside the dielectric layer, such as Cu in SiO2[101]; while cations with high mobility tend to reach the inert cathode and be reduced near the cathode, such as Ag in AgS2[102]. The redox rate determines the dimension of conductive bridge. High redox rate tend to result in large clusters and cones, while low redox rate tend to result in nano particles and thin dendrites[99]. Besides, the phase change of dielectric matrix under external fields also contributes to the formation of conductive bridge. E.g. A phase change of Ag2S from the acanthite to argentite plays a role in the formation of Ag filaments[102].

Worth noting that metal conductive filaments are relatively less stable compared to oxygen migration devices, and exhibit a self-dissipation under some conditions. The first factor is that the reductive metal filaments are formed in the oxidative matrix, and tend to be spontaneously oxidized to cations. Also, the conductive filaments are tiny secondary phases with large relative surface area and high surface energy, therefore tend to self-dissipate over time based on the Ostwald ripening process[30] or Gibbs–Thomson effect[103]. Therefore, short-term behaviors, such as short-term memory (STM)[28], paired-pulses facilitation (PPF)/ paired-pulses depression (PPD) subject to different spike interval[30], are often observed in metal cation based memristive systems. The time scale of self-dissipation could go down to 250 ns[103]. Therefore the CB devices can also be used as high-speed threshold switch or selector, which allows the realization of STDP with overlapped pulses. An example is connecting a self-dissipate CB device (SiOxNy:Ag-based) in series with a non-volatile drift memristor (TaOx-based). Due to the voltage distribution in the serial circuit, most of the voltage drops on the CB diffusive devices when the first spike comes. The first spike turns the diffusive memristor to the self-dissipating ON (low-resistance) state, regardless of the plus or minus of the first spike; and at the second spike, voltage is applied on the TaOx device, and the direction of spike determines the resistance change of the drift memristor. Because of the self-dissipation of Ag based diffuse device, there is a window time following the first spike, when it's in low resistance state and spike voltage works on the drift TaOx device. Therefore in this configuration, Hebian and anti-Hebian learning rules (STDP) can be implemented.

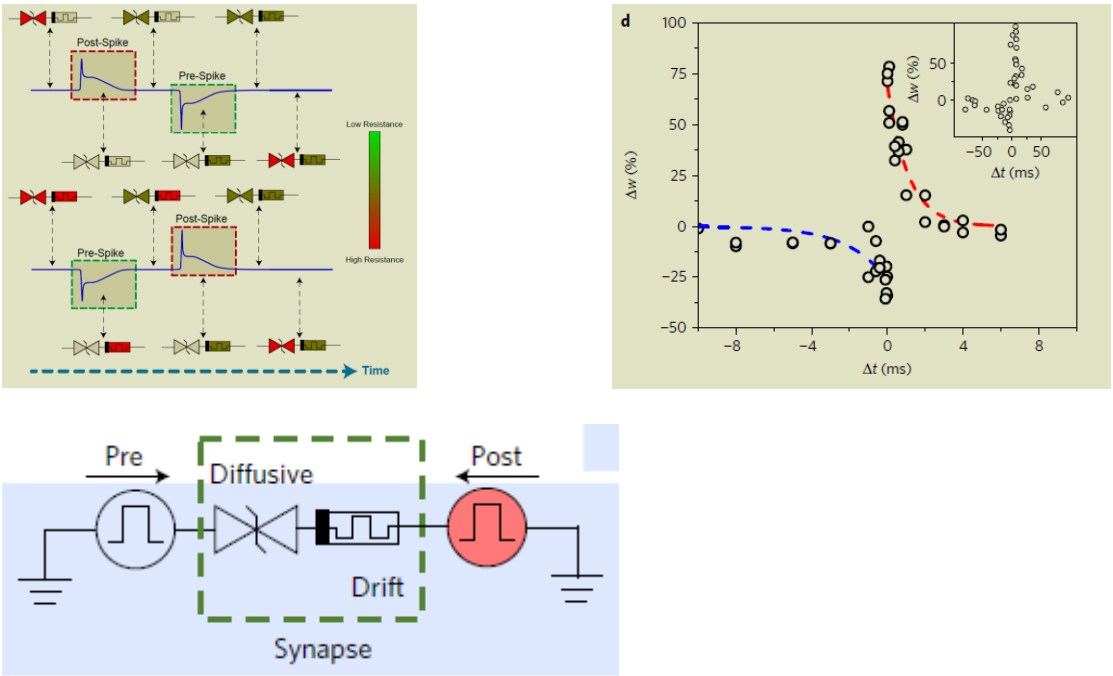
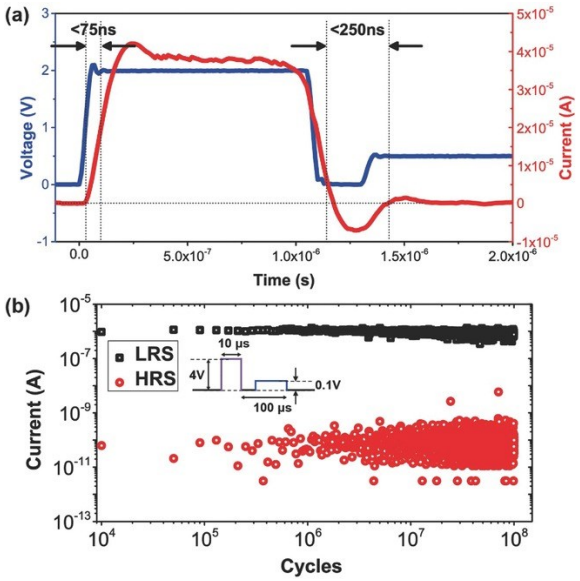



Fig.X. a) Illustration of states evolution in a STDP protocol. The pre-spike turns diffusive mersister to the ON state, and the second spike determines the change of resistance of drift memristor. Due to the self-dissipation of the conducting filaments in diffusive memristo, the time-interval determines the weight change coefficiency. B) STDP demonstrated with a Pt/HfOx/TiN drift memristor.[30]

Self-dissipation is related to the dimension of conductive filaments. The formation and dissipation of filaments are basically the nucleation and dissolution of a secondary phase. Therefore there is a critical dimension, beyond which the secondary phase tends to exist stably. Since the dimension of CBs is determined by applied current or voltage and the current and voltage history, the transition between short-term behavior and long-term behavior is controllable by applied pulses. When strong input stimuli are applied, or sub-threshold pulses are given with high frequency that the relax time isn't enough for the self-dissipation, the CBs build up and exist in a stable state. This is a representation of learning process in bio neuron systems[104,105]: unstable short-term conduction turns into a stable long-term conduction, like the rehearsal turns short-term-memory to long-term-memory in a learning process. The short-term memory to long-term memory transition can be used to realize spike-rate-dependent learning, where forgetting is involved, and high-frequency inputs result in a long-term memory effect[28].




Switching speed and endurance performance of the bidirectional Pd/Ag/HfOx/Ag/Pd selectors.[103]

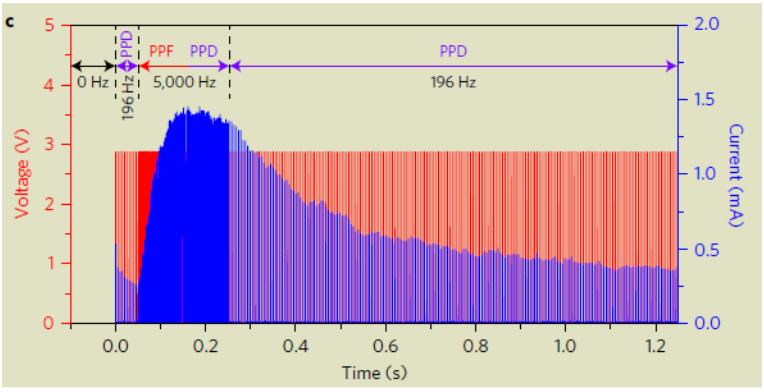
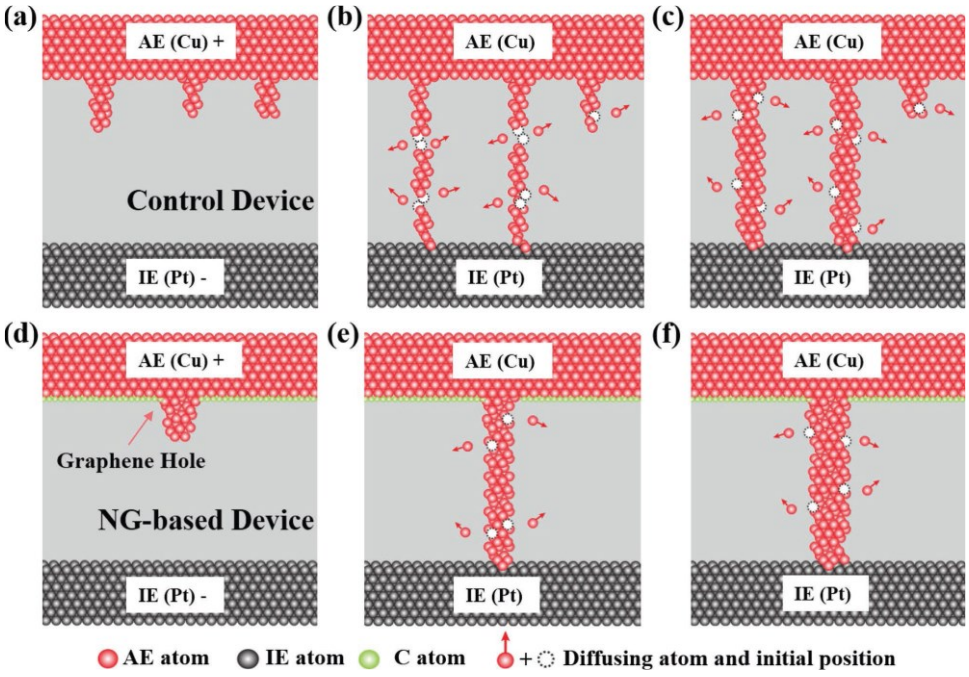



Fig. X. Experimental demonstration of PPD following PPF in the diffusive SiO*x*N*y*:Ag memristor. Device current (blue) response to a train of voltage pulses (2.8V, 100 us) of the same amplitude but different frequencies. The device begins with PPD (depression)

following low-frequency (196 Hz) stimulation and experiences an increase in current (facilitation) once the stimulation frequency is raised (5,000 Hz).[30]

Compared to other memristive devices, CB-memristors usually have higher on-off ratio but discontinuous transition behavior[30]. This jump in resistance indicates the connecting of two electrodes with the filament. In some cases analog resistance change behavior is observed, such as in 30um*30um Cu-SiO2 devices, where the conductive change is ~1 order and continuous[106]. The abrupt resistance change can also be modified by introducing current limitation and diffusion barrier layer. In [107], an r-GO layer is stacked between inert FTO electrode and dielectric layer. The diffusion resistance to Ag atoms of r-GO blocks Ag+ from forming dendrites from FTO surface, and the high out-of-plane resistance of r-GO limits the current level. In this device a smaller on-off ratio but an analog resistance change is realized.

Beside the discontinuous transition, CB-based devices have randomness in switching due to the stochastic nature of conductive filaments geometry. In the SET process, metal cations are injected from reactive electrode to dielectric layer, the amount is more abundant than needed for conductive filaments, and cannot fully be electroplated back to the anode. The excessive cations accumulate in the dielectric layer, and degrade the durability of device. Also, the growth and dissipation of conductive bridge are of high-randomness inherently. This hampers CB devices from high operation repeatability (temporal uniformity) and reproducibility (less variation from device to device). Defect controlling is an approach to reduce the device randomness. In one recent approach, graphene with nanopores are used as a blocking layer between active electrode and resistance switching layer, where metal atoms are only allow penetrating through from nanopores, to spatially confine the injection of metal atoms. The localized atom injection regulates the spatial distribution of conductive filaments. And the device uniformity, endurance and high-resist state endurance are improved[88].



Spatial confinement of metal injection achieved by nano-hole graphene.

Another example of defect spatially controlling is utilizing penetrative dislocation as the atoms migration channel, to confine the geometry of conductive filaments. In this research, Ag is used as the active electrode, epitaxial SiGe is used as the high-resistance matrix, and widened dislocations in SiGe layer are the diffusion channel of Ag atoms. Due to the low solubility of Ag in Si, Ag conductive filaments are confined in the widened dislocations. This device maintains a high on-off ratio, and shows highly analog performance, good linearity, and very low temporal (repeatability) and spatial (device to device) variation[108]. Besides barrier layer and penetrating dislocations, quantum dots such as GO QD[109] inside the dielectric layer can also work as guiding defects and enhance the uniformity and reduce switching energy. Nanoparticles fabricated by ion implementation also show influences on metal clusters formation and device behavior[110].

{
Diffusive memristors exhibit a threshold-switching characteristic.

In these kind of materials, reversible generation and elimination of the conductive secondary can be externally controlled, forming and deforming the conductive filaments embedded in a insulating or less conductive matrix. Notable examples included: GeSbTe (conductive in its crystal state and semi-conductive in its amorphous state), Silver sulfide Ag2S (a Ag+ ion conductor in which Ag+ can migrate and reduce to Ag metal filaments).
}

## 2.4 H+ & Li+ migration devices

In oxide-based or metal-cation-based devices, the conductance originates from the conductive filaments in insulating matrix. For devices utilizing H+ and Li+, due to the lower migration barrier and high migration rate, the conductance change usually originates from the material bulk conductivity change induced by H+/Li+ intercalations, and the accompanied electrochemical redox reactions. Materials exhibiting resistivity change in this electrochemical reaction can be adopted as the resistance switching material in Li+/H+ devices. When negative voltage applied, the host material absorbs H+ or Li+ inserting into it, and meanwhile be reduced. Conversely, when positive voltages applied, the resistance switching material is oxidized and cations are extracted. Unlike in CB devices where metal cations are reduced to metal substances and form metallic conductive channel, in H+/Li+ devices, inserted cations such as Li+ are not reduced to metal, since the reduce potential of alkaline metal is considerably low. Instead, the change in matrix material induced by Li+/H+ intercalation or redox reactions gives the resistance programmability.

Li/H+ devices can be built in 2-end structure or 3-ends structure. In 2-end structures[111-116], a resistance switching material is sandwiched between metal blocking electrodes or active electrodes. More H+/Li+ -based devices are designed as 3-end structures, similar to FETs: a H+/Li+ host material works as the device channel, with source/drain contacts at each ends, and a counter electrode working as the gate, with an ionic-conductive (electronically-insulating) layer exists between the gate and the channel. When a positive gate voltage is applied, positive ions transport through ion-conductive layer, and insert into the channel material, reducing the channel

material. Conversely, when negative gate voltage is applied the channel is oxidized and positive ions are extracted. A typical example of this kind of device is Li+-based synaptic transistor with $LiCoO_2$ channel[117]. $Li_xCoO_2$ exhibits insulator-metal transition as x decreases from 1 to 0.8, yielding a resistivity change of 6 orders of magnitude[118]. When Li+ is extracted from the channel, its conductance increases accordingly. The Li+ extraction is controlled by applied gate pulses, and channel conductance is measured by applying a constant weak reading current.

Similarly, materials with Li+ capacity and high diffusion rate are demonstrated as the resistance switching materials in Li devices. These materials can be TMO electrode materials such as $LiCoO_2$[114,117], $LiNbO_3$[111,112,116], lithium lanthanum titanate (LLTO)[115], $Li_{4+3x}Ti_5O_{12}$; 2D materials like MoO3, transition metal dichalcogenide such as MoS2, $WSe_2$[29], and transition metal phosphorus trichalcogenides in $MPX_3$ form, such as $NiPS_3$, $FePS_3$[29]. The ion-conduction layer can be solid electrolyte such as LiPON[117], LLZO, PEO-based gel electrolyte[29], or liquid electrolyte. Non-conventional dielectrics are also used such as oxidized ultrathin $SiO_2$[114]. The counter electrode (gate electrode) can be symmetric (same as the channel) or non-symmetric electrode material such as Si[114,117], inert electrode like Au are also used in some researches.

Proton-based devices have similar operation principles. A typical 3-end device consists of resistance switching channel, ionic conduction layer, and gate. Common proton conductors can be Nafion[119,120], and ionic liquid[121], or aqueous electrolytes[122]. As experimentally demonstrated, the resistance switching material can be PEDOT:PSS[119,122,123], SiO2,[124] layered material MoO3[121]. H+ devices have similar mechanisms with Li+ devices, however since H+ have smaller size than Li+, H+ devices have faster speed and lower switching energy compared to Li+ devices.

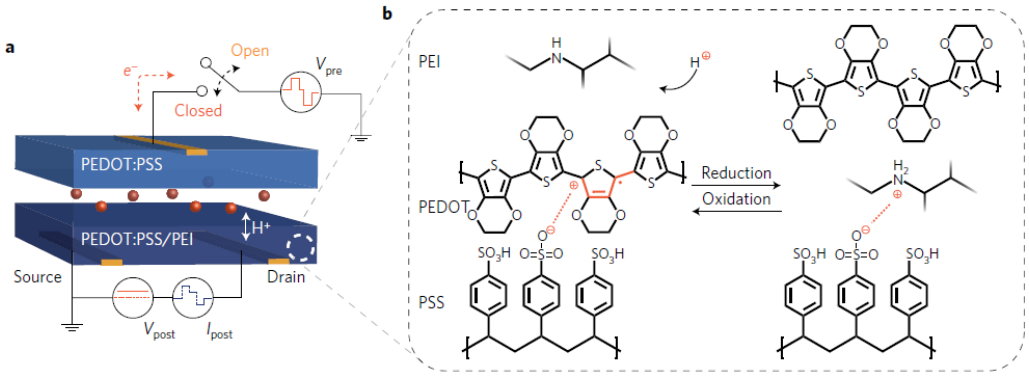
The switching of SiNx:H devices also relies on H migration[125-127]. In CVD SiNx there are inherently H atoms which compensates the dangling bonds on Si. When the Si-H bonds break and H migrates under electric field, the released dangling bonds become trap centers and allow electrons move through by trap to trap tunneling[126]. In SiNx devices the migration includes the two steps of breaking of Si-H bond and H migration, and the conductive region has the shape of filaments. SiNx is a commonly used material in CMOS processing, and the devices are built in 2-end configuration.

Conductivity of the oxides is provided by O-vacancies and related donor doping. And for CB devices is from conductivity of metal substances. However the high-conductivity states in H+/Li+ devices have various origins. Some are explained as ions intercalation induced band-gap change, some are explained with the electron state change induced by reduction. A commonly used organic resistance switching material is conductive polymer PEDOT:PSS, in which the PEDOT is positively charged, and compensated by negatively charged PSS. The mobility of positive holes generates the conductivity of PEDOT:PSS. Therefore, when the positive charge of PEDOT is reduced or partially reduced, the conductance of PEDOT:PSS changes accordingly.

Therefore, known from the mechanism, H+/Li+ devices utilize the migration of small ions, and the resistance change in electrochemical redox of the channel material. Therefore, H+/Li+ devices have following features compared to filamentary oxide-based and metal cation-based devices: 1)

H+/Li+ devices usually have more analog switching behavior inherently than CB devices. Because Li/H have higher migration rates and more spatially uniform distribution. And the resistance transition is not dependent on filaments geometry, but on a constant change in chemical composition and oxidize state. 2) Because of the feasibility of small ions migration, H+/Li+ has higher migration rates under room temperature, and lower migration energy barrier than O2- or Cu, Ag cations. Therefore the devices have lower theoretical energy consumption. However in a 3-end structure the energy consumed in EDBL capacitance charging needs to be considered. Also the easy diffusion limits the theoretical retention in 2-end structures. Recently a retention time of >80 min @100C is configured in LiNbO3 two-end structure[116]. 3) 3-end Li/H devices have intrinsic non-volatility. The electrolyte layer between gate and channel is electrically insulating. And the channel electrochemical reactions are prohibited if external circuit is kept open. Worth noting that this non-volatility may degrade and conductance may drift if undesired reaction happens, such as the reaction with moistures and air.

A research on H+ migration device illustrates these favorable features[119]. In this research, one layer of PEDOT:PSS works as the gate electrode (pre-synapse structure compared to biology system); Nafion is selected as proton conductor (electrolyte). A PEDOT:PSS/poly(ethylenimine) (PEI) layer works as the resistance switching channel (post-synaptic structure). In the pristine state, partially oxidized conductive PEDOT is stabilized by negatively charged PSS, and shows high conductivity. When a positive voltage is applied to the gate, protons migrate from Nafion layer to the channel, together with electron flux from external circuits. In this process, PEI is protonized and positively charged, compensating negatively charge PSS. And PEDOT is reduced by injected electrons, therefore the conductivity drops. This device shows almost continuous and linear adjustability of the channel conductance according to current-controlled gate pulses (i.e. charge/discharge amount). 500 stable conductance states are obtained in the device operating range. When gating voltage is removed, Nafion layer prevents any electron flux, therefore the device shows long retention time, showing a 0.04% standard deviation in conductance measured over 25 h.



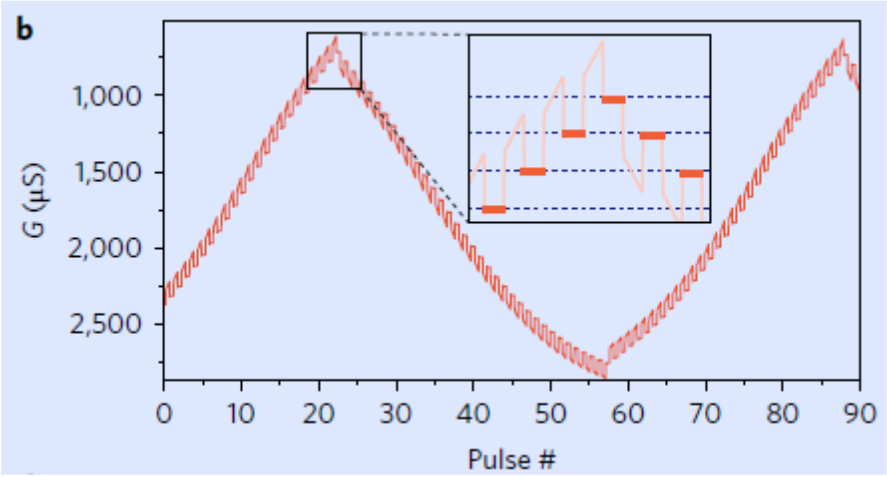
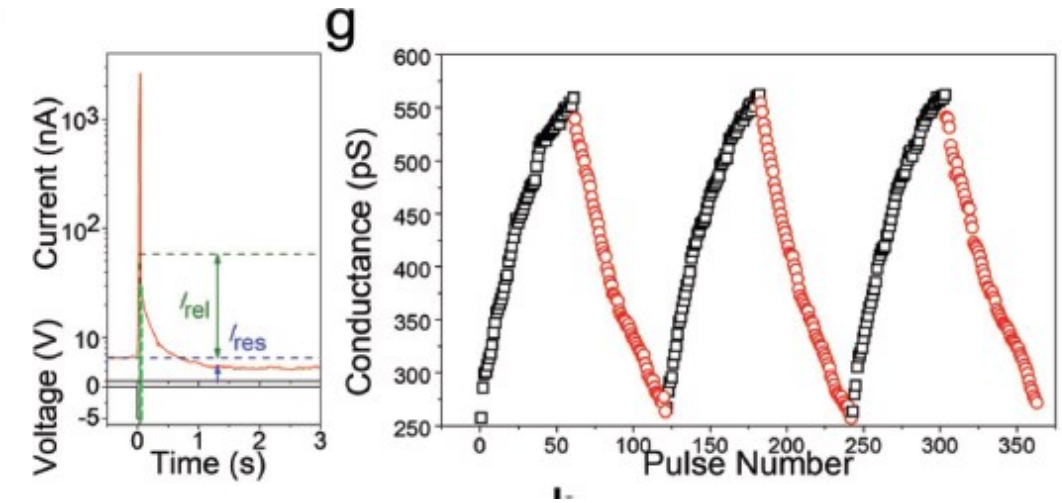



Fig.X (a) The device configuration, (b) When protons are driven into post-synaptic layer, the PEI is protonated, and some PSS- is compensated by the protonated PEI. This causes the reduction of PEDOT and decrease of conductance[119]; (c) Long-term potentiation and depression under current control..

The limitation of Li+/H+ -based devices are the sensitivity to humidity and oxygen, and therefore the lack of compatibility with CMOS processing. Li ions are easily combined with humidity and oxygen synthesizing Li2O and LiOH. Some of the resistance switching and electrolyte materials are solubale in water and degrades in air. H2O molecules also infect the protons reactions in ionic liquid. In fact some demonstrates utilizes the moisture as a proton source. As shown in [121], RH% determines the gating efficiency and channel current.

Another of cons is the slow response time of programming. The programming process of Li/H+ devices is based on the electrode reactions on the channel surface, therefore the programming speed is limited by the stabilizing time of ion-conducting layer, which is determined by diffusion time of ions. Also, surface-absorbed cations on the switching material will diffuse backward shortly after the end of programming pulse. Therefore, a H+/Li+ device will show short-term effects and long-term effect concurrently. Fig. X gives a typical example of short-term and long-term behavior. Shortly after the programming pulse, Ids increases because of the electrolyte diffusion layer (?) and surface absorb cations. After the short-term current deceased, the non-volatile conductance decrease is revealed[29]. In addition, the setup of EDBL also consumes energy, since $E = ½ CU^2$, larger device capacitance means more energy consumption. An approach to increase the programming speed and reduce non-ideal effects of Li/H devices is down-scaling and putting a threshold selector device (such as SiOx:Ag CB) in series with the gate[123].




f) Ids response in WSe2 based synaptic transistors when a negative gate pulse (−5 V, 50 ms) was applied to the device that has been set to a potentiated state with an initial current of ≈5 nA (Vds = 0.5 V), showing overall long-term depression. g) Long-term potentiation and depression of the WSe2 based synaptic transistors using 60 potentiation (1.2 V, 100 ms) and depression (−0.4 V, 100 ms) gate pulses with an interval of 3 s, showing excellent linearity, symmetry, and reproducibility.[29]

Some 3-end devices are based on anion (e.g. O2-, Br-) migration, but are more similar to the H, Li 3-end devices introduced here. These devices have a high migration rate liquid or polymer electrolyte layer, and rely on electrochemical electrode reactions. Ions migrate across the interface with the aid of EBDL, inducing bulky resistance change in the channel. Deeper similarities are they face similar difficulties with CMOS process compatibility, and have strong short-term behavior, and good potential in analog performance. Examples of O2- migration are: SrCoOx in aqueous electrolyte[5], VO2 in ionic liquid (1-hexyl-3-methylimidazolium bis(trifluoromethylsulfonyl)-imide (HMIM-TFSI) )[128] . These materials are sensitive in O composition change. With O vacancies accumulate in the channel oxide, defects-induced conductivity changes accordingly.

## 2.5 Discussion

In above sessions, 3 kinds of ion migration memristive devices are introduced: O-migration, heavy metal migration, and Li/H migration. In these devices, ions migration and redistribution play a key role in the functionality. Therefore the characteristic and performance of these devices are determined by some common essential factors.

### Migration rate

Migration rate is determined by the (?). and depends on both the elements and migration matrix lattice. H+ has the least diameter, and the least energy barrier, and therefore shows faster reaction speed and more significant efficiency (ref?). Similar phenomenon is observed in halogen-polymer

device: Cl-, Br-, I- have different radius and devices have different response to programming spikes[129].

Migration rate also determines the geometry of high-conductance channels. In conditions having more feasible ions migration, the conductive region tend to migrate through a long-range forming structures related to device structures, other than localized filaments or clusters. An extreme example is Ag in liquid electrolyte forms dendrite crystals on cathode. And interfacial type (non-filamentary) transition are often reported in perovskite oxides. Worth noting that the migration range is compared with device dimensions. If the dimension is scaled down to the migration length or filaments size, non-filamentary transition can be observed with the same migration characteristics.

In addition to programming speed and efficiency, migration barrier (?) also determines the retention of resistive states. Therefore there is a trade-off between the programming voltage and rentention, which is referred to as "voltage-time dilemma"[130]. Take TiOx and HfOx as example. TiO2 have a very high relative permittivity of 50~80[131], much higher than commonly used high-k material HfOx (k~25), but suffers from high O-migration rate and following device deterioration when used as gate insulator of FETs[132] ([133]phd thesis http://www.iue.tuwien.ac.at/phd/windbacher/node13.html). When applied in resistive switches, TiOx-based devices[134] have lower switching voltage and energy consumption, while shorter retention time than HfOx-based devices[135]. Another example is shown in Ref[136]. In this work TaO/HfOx and TaO/AlOx stacks are built as RRAM device. AlOx has lower migration than HfOx. Both the set voltage and reset voltage range of a TaO/$AlO_x$ are higher than the voltage range of a TaO/$AlO_x$ device. And AlOx devices show better low-resistance-state retention than HfOx devices.

Migration is closely related to defects, where atom diffusion and migration is significantly facilitated. For example, diffusion energy at grain boundary is significantly lower than lattice diffusion, and migration rate through grain boundary is much higher. If the switching layer of an ion migration device contains defects like grain boundaries, the characteristic of device will be determined by defects, not the properties of materials. Therefore, in a migration device, material defects must be carefully considered, two avoid variations induced by randomly distributed defects. And defect designing is an effective approach to reducing the device variation.

Ability of conductivity change of switching materials

The function of ion-migration device is achieved by the change in conductivity of the switch material. The resistance switching material must exhibit notable conductive change during the ions migration. Donor excessive carriers in common oxides, metal substances in CB devices, electron states change in strong correlated oxides, and Li-intercalation or protonation in Li/H devices. Ion migration is accompanied with local redox reactions and valence change. The inducer of conductivity change can be understood as the change in valence.

The resistance switching material and ion migration matrix are not necessarily one. For example,

in a N:TiN/PCMO 2-end structure, PCMO is where O2- has high migration, and the resistance switching is achieved with the formation and dissipation of TiON layer at the TiN/PCMO interface[64]. Also in 3-end structures ion-migration material and resistance switching layer are separated. Ion exchange across the interface is achieved from electrochemical reactions.

Device structure: 2-end or 3-end

Ion migration devices can be constructed with 2-end or 3-end configurations. 2-end structures can be integrated in the form of cross-bar array, therefore possessing better scale down capability. In fact, the scalability of ReRAM is one of the major advantages over FETs based registers. In 2-end structures, the migration and diffusion coexists along the device structure toward opposite directions, therefore there is a trade-off between the retention and switching energy. In 3-end structures the writing and reading use different current paths retention is unrelated to switching energy. Therefore, oxides and CB devices are usually fabricated in 2-end structure, and small cation devices are more often in 3-end structures. 3-end devices usually have better analog performance since the resistance switching is based on bulk change instead of filamentary conducting. Since the ion-migration material and the resistance-switching material are separated in a 3-end structure, there is more freedom in material selection, even liquid and gel materials can be used. Due to the formation of EDBL, 3-end devices have significant short-term behavior and lower programming speed. These features can be improved by reducing device footprint.

In summary, when selecting the materials and designing an ion-migration device, the above factors need to be considered comprehensively. Migration rate and conductivity change are the major concerns of material selection. The material selection influences the device structures. And the material characteristics and device configuration determine the behavior of a device.

# 3. Improvement: repeatability, device-device variation, analog performance (quantity of states and linearity)

## 3.1 Repeatability (temporal uniformity), reproducibility (device-device spatial uniformity), and energy consumption

A major obstacle to the practical use of ReRAMs and other memristive devices is the poor uniformity[24,137]. Here the uniformity includes repeatability, which indicates the variation between each cycle on the same device, and reproducibility, which indicates the parameter variation

between device and device. For a resistive switch, the variations exist in the SET and RESET voltage, and resistance of HRS and LRS. For a multi-level memristive device, this variations are also presented in the conductance -- programming pulses profile, from each cycle to cycle and device to device.

Numerous efforts have been made to improve the uniformity. Based on a filamentary picture, the variations origin from the stochasticity of filaments formation, growth, and annihilation. In non-filamentary type switching this can be understood as the change in the geometry of conductive regions. Therefore to minimize the variation of ion-migration device, it is essential to control the conductive region spatially. The distribution and movement of conductive region are representations of ions distribution, generation, migration, and diffusion. Therefore, efforts to improve the uniformity can be understood as the confinement of these behaviors of ions.

During the electric forming process, the dielectric material breaks down and filaments are formed. Similarly the SET process includes the re-formation and growth of filaments. In these process there exists large electrical stress and strong current overshoot, which increase the device variation. In some extreme condition devices may be processed to stuck-ON of stuck-OFF state, cause device yield loss and degradation of inference application accuracy. Therefore, lower forming and operating voltage is beneficial to reducing the forming variation[138]. The stoichiometry of switching layer is adjusted to lower oxide state to reduce the required voltage[24].

A thin active metal layer at the oxide/electrode interface as the oxygen scavenging layer can facilitate the generation of O-vacancies. The scavenging layer benefits the uniformity in two ways. First, the scavenging layer are oxidized during operation or fabrication, and oxygen vaccancies are generated in the oxide near the interface. The abundancy of Vos lower the energy and field required for the generation of conductive filaments, and reduces the device resistance, thus the forming voltage is also reduced. Second, the oxidization of scavenging layer is an interfacial reaction[139]. Vos are formed at the whole area scavenging layer, thus the formation and distribution are less dependent on existing filaments, residuals and defects[140]. Also, oxidized ultra-thin scavenging layer becomes an interfacial oxide layer, therefore have the function of an oxide capping layer. Such as in [141], an ultrathin (1–2 nm) Ti layer is deposited on TaOx base layer. The Ti layer is then oxidized to TiOx and adjacent TaOx is reduced by Ti and generates a thin O-deficient layer, providing the switching function. The TiOx layer acts as a resistor in SET process, and provides O in the RESET process, and the uniformity and endurance are improved.

Similar to scavenging layer, an active electrode has similar redox reaction, and different active electrodes have positive or negative effect to the uniformity, and device duration. Kim et.al. compared different active electrode materials on Ta2O5 switching devices, and found the influence of electrode depends on the Vo formation energy[142]. Among the electrodes, Ta and W showed a positive influence on the device duration and Ti and Hf show a negative influence inducing RESET failure. The device uniformity with Ta and W electrodes are also studied. A recent research points out that the penetration of scavenging metal into the oxide layer is a cause of the performance degradation[143]. In this research an ALD 2-nm TiN bufferlayer is inserted between Ti and HfOx, and device uniformity is significantly improved compared to devices

without TiN barrier.

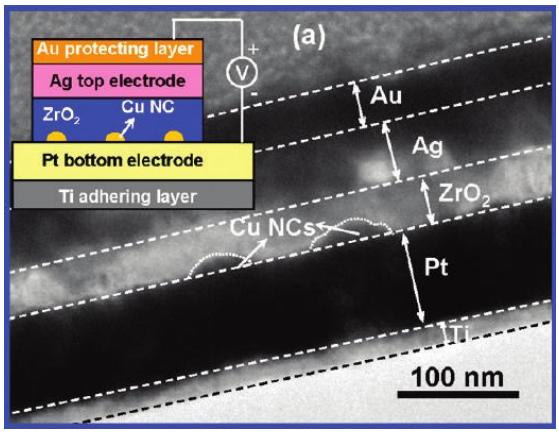
Bilayer structure can effectively enhance the uniformity and duration of memristive device. One approach is using an ultra-thin high-resistance layer as the switching layer, instead of the operation in the whole dielectric layer. A typical example is Ta2O5/TaOx structure. In Ref. [40] , an ultra-thin Ta2O5 layer is formed by O2 plasma oxidization of TaOx layer. The TaOx serves as an oxygen reservoir, and the conductive filaments are confined within the Ta2O5 layerIn a recent research, Cu CB-based devices are built in both Cu/TaOx/Ta2O5-x/Pt structures. In this structure both Cu filament and Vo filaments exist, and two filaments grow oppositely. In this structure, cycle-to-cycle variation coefficiency (sigma/miu) reduced from 60.92% to 2.77% and device-to-device reduced from 82.73% to 4.85% compared to Cu/Ta2O5-x/Pt structure[144]. Worth noting this combined structure has a low switching voltage at 0.4V but long retention.

A barrier layer without conductive region formation capability is also reported to increase the uniformity[145,146]. Banerjee et.al. studied the influence of Al2O3 thickness in a TiN/TiOx/Al2O3/IrOx structure. 8-nm Al2O3 layer breaks down and acts as the switching layer, and the conducting behavior follows a trap-assisted-tunneling mechanism. While a 2-nm thick Al2O3 acts as a tunneling barrier, and the conducting follows F-N tunneling model. The device with 2-nm thick Al2O3 shows improvement in the uniformity, illustrating the role of a tunneling barrier layer. In addition, due to the tunneling conduction mechanism, devices with a ultra-thin barrier show a high IV nonlinearity, which can replace the function of selectors in a crossbar array[147].

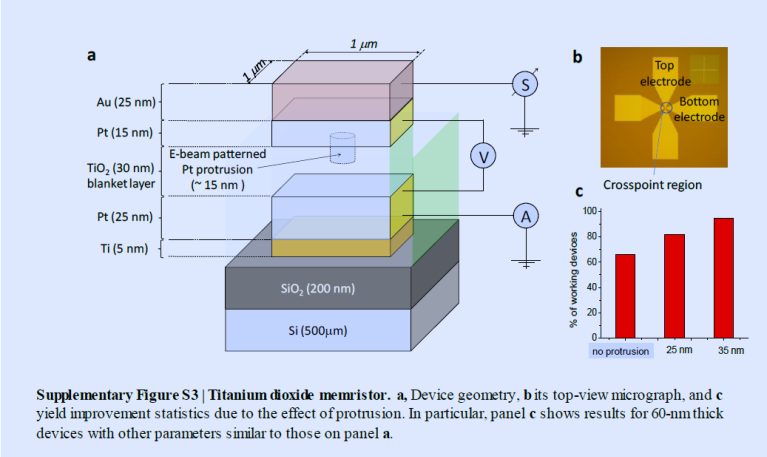
The formation of conductive region is driven by electric field and temperature. In a filamentary switching application, stochastic filament growth further influence the distribution of field and temperature, and increase the randomness in both SET and RESET process. Therefore to reduce the device variations through device design, structures that can define the distribution of field/temperature are used. These structures are used to concentrate the field distribution, and suppress the stochasticity of resistance switching.

Based on this idea, some modification to electrodes are demonstrated. In Ref. [148], nano-indented top electrode are used in both Ag/SiO2/Pt and W/Ta2O5/Pt stacks, to concentrate the electric field distribution inside the switching layer. Conductive filaments tend to form only at the electrode tip, where the field is strongest. The nano-indented cells possess a better cell-to-cell uniformity compared with the conventional cells. The concentration of field also provide benefits like lower operating voltage, larger ON/OFF ratio, faster speed and sharper transition.

Similarly, in [149], Cu nanoparticles are placed on the Pt electrode in a Ag/ZrO2/Pt structure. Cu nanoparticles also concentrate the field and acts as a nucleation of Ag. And the stability and uniformity are improved. And in [150], a protrusion is fabricated on the Pt top electrode into TiO2 switching layer. And the uniformity and device yield are improved. In another research[151], Ag (active electrode) protrusion is fabricated by etching the SiO2 matrix covered with Cr nanoscale mesh mask before Ag deposition. As shown in figure, operation voltage uniformity and resistance uniformity are significantly improved.

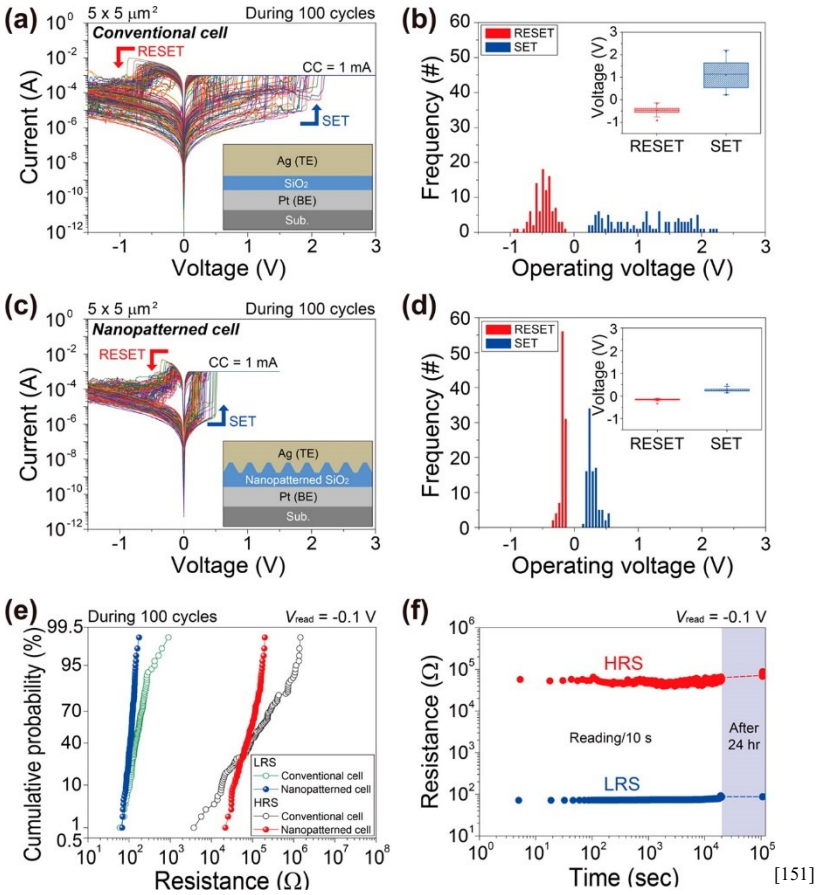



**Cross-section TEM image for the Ag/ZrO2/Cu NC/Pt memory device.**[149]




**Supplementary Figure S3 | Titanium dioxide memristor. a,** Device geometry, **b** its top-view micrograph, and **c** yield improvement statistics due to the effect of protrusion. In particular, panel **c** shows results for 60-nm thick devices with other parameters similar to those on panel **a**.

[150]



[151]

Similarly the field can be concentrated by implementing quantum dots or nanoparticles inside the switching layer. In Ref. [152], Ru nanoparticles are imbedded in TiOx switching matrix by ALD. And both the device yield and uniformity are improved. Also the power consumption is reduced since the field is concentrated. In Ref. [153], Ag nanoparticles are implemented between Al2O3 and ZnO switching layer by spin-coating. In a recent research Pt nanoparticles are imbedded in TiO2-x layer using sputtering[154][][]. In Ref. [155] Pt and Ta particles are implemented in TiOx for compration, and uniformity, ON/OFF ratio are improved. Interestingly a large capacitance change are observed in these two device, and the author suggests that the band alignment between metal NPs and semiconductor matrix should be considered in these applications. In a recent research, CoPtx nano particles are embedded in AlOx and HfOx switching layer[156], to improve the uniformity by concentrating the field.

The functions of ionic devices are realized by ion migration. The geometry of conductive region is also depended on migration, which is highly facilitated by defects, including point defects, dislocations and interfaces. Therefore another idea is to regulate the spatial behavior of conductive regions by designing the defects. Artificially induced defects guide the migration of ions and avoid the randomness of natural defects.

As mentioned in Sec.2, superior uniformity is achieved in Ag/ZrHfO2 with GO QDs[109], Ag/SiGe with threading dislocations[108]. In Ref.[157] a structure with threading interfaces are designed. STO (or BaSrTiO, BTO) is co-deposited with Sm2O3. With a diffusion and phase separation, a

self-assembled nano-scafford structure forms in the deposition, with discrete Sm2O3 columns distributed in STO matrix, and vertically running through the thin film. In this way the oxygen generation and migration and preferred being in the vertically threading interfaces, and the devices exhibit multi resistance states and good repeatability.

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Reliability depends on the material inherent characteristics. Lian et.al. analyzed the voltage and current of the RESET point of a Ta/TaOx/Pt device, and suggested that the distribution of voltage and current follow Weibull distribution, and the variability of device can be describe with Weibull slope and bigger Weibull slope indicates smaller variability.

Low-migration rate cap layer can partially preserve the filaments in the RESET process. Low resistance filaments are stuck in the cap layer, and facilitate the filament formation in the next cycle.
}

## 3.2 Analog performance

In software artificial neuronal networks, the correlation intensity (weight) between neurons are high accuracy floating-point numbers. However in memristive devices, the accuracy of a weight representation is limited by the allowed resistance states of the material, and this accuracy is not comparable to the accuracies in software ANNs. Researches suggest that 6-bits (64 distinct levels) are enough to perform inference tasks with applicable accuracy[21,77,158], and higher inference accuracy is supported by more available resistance states. The SET process in a filamentary-type memristor is basically a positive feedback process, in which the growth of filament further facilitate the ion generation, migration and heat generation in the front of filament tips, on the other hand the RESET process is more in a gradual manner. Therefore in early demonstrations only the RESET process is taken advantage for neuromorphic computing[54,159], and now researches are perusing multistate in both potentiating and depression, for implementing a bi-directional updating in one device.

Another critical analog performance is the programming linearity[77]. In off-line training applications, the synaptic weights (resistance of memristors) can be programmed by read-and-write feedback control, and the resistance can be programmed to any expected level. However to implement memristors in online training applications and take full advantage of the potentials of hardware neuronal networks, the resistance updating should be performed with high accuracy without reading and feedback steps. Therefore, a reliable mapping between programming pulses, conductance, and weight is required. This requires the linearity and symmetry in potentiation and depression programming profiles, i.e. linear conductance increase or decrease with pulse numbers. Another expected performance is weight update rate being irrelevant to the current resistance state. In other words the resistance can be programmed back and forth arbitrarily, with a fixed updating rate only relevant to pulse amplitude and duration. However in a potentiate/depress cycle of ion migration devices, a universal trend is that starting several pulses

give the most significant resistance change, while during following programming pulses the resistance updating shows a saturation behavior, which means the weight update rate decreases as the pulse number increases in one programming period. The asymmetry and nonlinearity of updating profile damage the integrity of the mapping between programming and weight, and limits the training accuracy.

The improvement in resistance continuity and programming linearity can be achieved by various ways. One of the solutions is representing a synaptic weight using multiple devices[160]. In this article we will discuss the methods to improve the analog performance without increasing device amount. The dominant factor is materials and device selection. Non-filamentary type resistance switching is considered an approach to avoid abrupt resistance jump, minimize stochasticity and increase the quantity of resistance levels. Proposed non-filamentary type switching are such as interfacial switching in oxides, as discussed in sec 2, and some bulk change found in oxides or low-migration barrier H+, Li+ devices. In a SET process of filamentary-type devices, since filaments are significantly more conductive than insulating matrix, both field and temperature are enhanced at the tip of filaments. Without current compliance, the SET operation is more of a positive-feedback process. In interfacial transition this is less significant since the concentration of field and heat is avoided. In addition, in an interface-type device the resistance is modulated by the thickness of barrier or interfacial layer, which is a continuously changing physical quantity. Therefore the interfacial type devices naturally have better analog switching potentials than filamentary ones. Compared to filamentary-type switching, resistance update of non-filament devices are also less susceptible to the randomness of defects distribution and filaments geometry, and minimize the influence of filaments residuals (meta-plasticity as referred to[161]), therefore having less fluctuation and errors in synapse updating[78].

In filamentary and interfacial 2-end devices, the conductive/barrier region expands and contracts along the current of field. At different device states resistance spatial distributions in device is different at different device states. Therefore the response to programming voltage/current depends on the current state of device, as a result the symmetry and linearity are limited. In an electrochemical 3-end device, conductive region is not along the programming path, and theoretically has a more uniform field and migration distribution, since electrolyte is essentially insulating. In addition in a 3-end device resistance programming can be operated in the form of bulky change. The combination of the above factors constitutes the cause of nearly ideal analog performance achieved in 3-end electrochemical devices[29,119,123].

(concurrent inhibitory and excitatory synaptic plasticity, low synaptic conductance with minimal fluctuation, and ultralow energy consumption comparable to that of a biological synapse (<10 fJ/spike))

Analog switching can be achieved and improved by controlling programming current. In filamentary switching, final state of filament growth is highly dependent on current compliance.

Analog performances can be enhanced with improved programming schemes. A straight forward approach is to program with incremental pulse amplitude. Since memristor devices have a

programming update rate decreasing with pulse dumber, an incremental scheme, in which pulses voltage (or duration) increases with pulse number. A quasi-linear programming profile can be achieve by this method[125,162]. Figure shows a compare between identical pulses and incremental pulses applied on a SiNx/AlOy device. From Figure (a) it can be observed, potentiation and depression pulses have different weight update efficiency. And if programmed with identical -5V pulses, the first pulse induces 2/3 of the full conductivity change. And as shown in (b), incremental programming pulses with a uniform voltage increment step yields a higher linearity and better accuracy in relevant classification application.

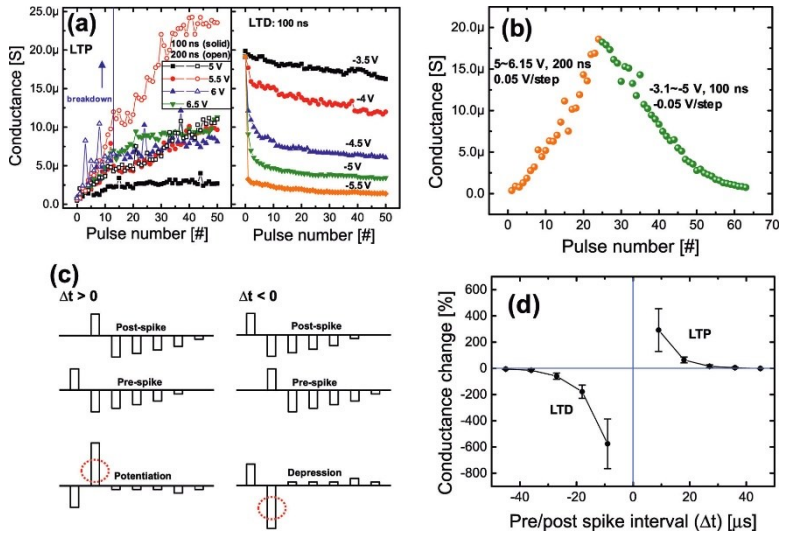
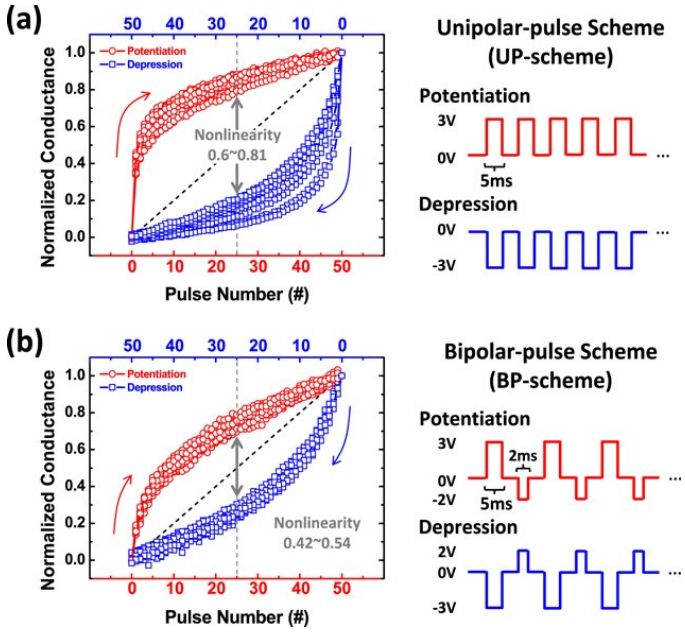



Figure. Conductance modulation of Ni/SiNx/AlOy/TiN memristor in (a) an identical pulse response and (b) a pulse amplitude incremental response.[125]

However, in an incremental programming scheme, each programming pulse needs to be determined from the current state of device. Therefore using incremental pulses requires an additional reading step, also peripheral circuit design or complex programming algorithms are required, which greatly increases the difficulty of applications. Another modification made in programming scheme is bipolar pulses. Since during the starting several pulses in each cycle, the device updating is more sensitive to programming pulse, by applying a weak opposite pulse after each programming pulse, the update rate of the starting pulses in each cycle is compensated, and linearity is therefore improved. Figure gives an example of bipolar-pulse programming. By applying an opposite 2V, 2ms opposite pulse after each 3V 5ms programming pulse, the jump in resistance update of first several pulses in suppressed, showing improved linearity. This program scheme is non-dependent on current state, and pulse pairs are identical through the programming cycle.




(a) The conventional UP-scheme and (b) the proposed BP-scheme. The *P*-pulse and *D*-pulse waveforms are also illustrated. The conductance was read using a −1.5 V/1 ms read pulse, and the values are normalized to the total plasticity from 0 to 1.

Besides materials selection and programming schemes, several device level modifications are demonstrated:

The first approach is adding a capping barrier layer on one side of the switching layer. This capping layer is usually an inert oxide thinner than the switching layer, such as Al oxide, Si oxides, and a-Si layers as well. As an example in Reference, 1.5 nm Al2O3 layer is added to TiO2-x device, and the devices shows good uniformity and stable multi-level resistance switching[146]. In Ref.[163], a 4.5 – 9 nm a-Si layer is used as barrier and rectifying layer. Multilevel resistance switching is observed with a very low operating current.

The role of the capping layer was explained differently in studies. In Ref[164], an AlOx layer is added to HfOx 2-end device to improve the programming linearity. The improvement in analog performance is attributed to the confinement of filament geometry. In AlOx, O mobility is lower than that of HfOx, and the dissolution of filaments in the AlOx layer is limited during the reset process. Therefore the dissolve of filament is more of a change in the filaments width within the HfOx layer, than the breaking and reconnecting of filaments. This change is more gradual and gives the analog switching behavior.

Another function of capping layer is raising the device operation temperature, thus enhancing the analog performance. O2- migration is a synergy between electric field and temperature. At higher temperature, O-vacancies distribute more uniformly, and filaments tend to exist in the form of multi weak filaments other than single strong conducting channel, therefore behave a gradual resistance change[165]. Figure gives an illustration of the effect of temperature. High device temperature induces graduate resistance change. In this research, a low-thermal-conductivity and high-electrical-conductivity oxide (TaOx) is placed between one TiN electrode and HfOx

resistance-switching layer. The transition from abrupt to analog behavior is attributed to the filament geometry change induced by thermal effect.

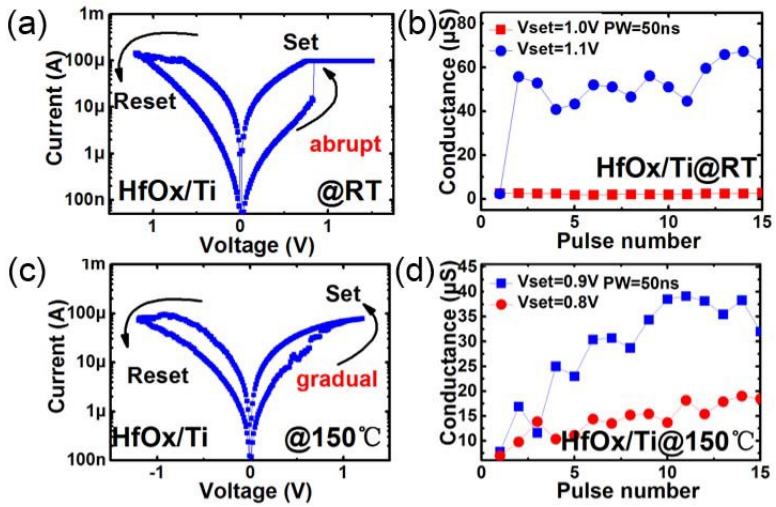
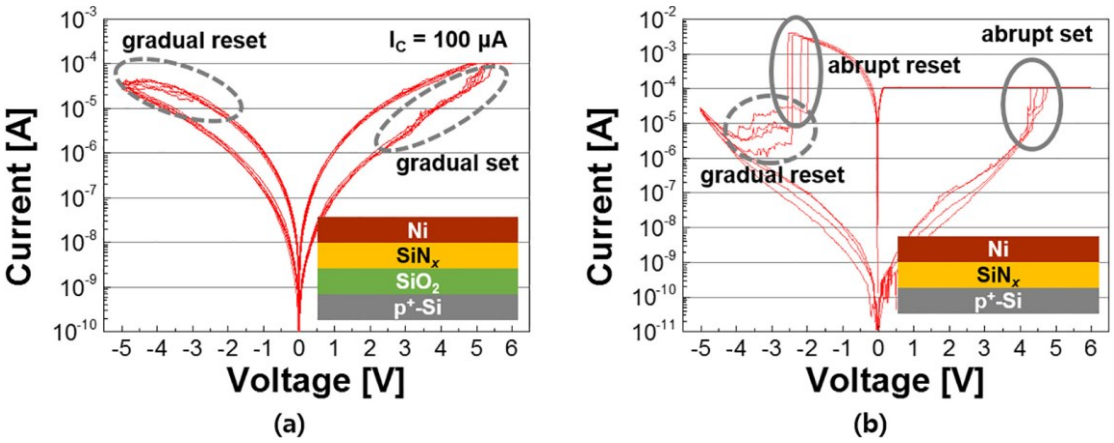



Figure. (a) Typical DC-IV of HfOx/Ti RRAM at room temperature (RT). (b) Conductance of HfOx/Ti RRAM changes with identical pulses at RT. (c) Typical DC-IV of HfOx/Ti RRAMat 150°C Abrupt SET changes to analog SET at high temperature. (d) Conductance of HfOx/Ti RRAM changes with identical SET pulses at 150°C. Analog switching is obtained. [165]

Another explanation is the capping layer acts as a current-limiting layer, limiting programming current and preventing from current overshoot. AlOx[125] and SiOx[127] capping layers are used in SiNx devices to act as tunnel barriers, and suppress the current overshoot during programming. Figure shows the function of the SiOx layer in SiNx device: SiO2 layer (2.5nm) is added in the SiNx (5 nm) device. Device with SiOx shows gradual set and gradual reset; while the device without SiOx shows abrupt change and a gradual reset after the abrupt set. In research[166], an a-Si/TiOx device is built where a-Si acts as the tunneling barrier, and the scavenging layer generating O vacancies. A graduate conductance change is found.

Similar applications are applied in oxide devices. In research[167], a 60 nm-TaOx capping layer is applied on HfOx and HfAlOx devices to improve the analog performance. The function of this capping layer is explained as an in-built current compliance layer and oxygen reservoir.




DC characteristics (a) of Ni/SiNx (5 nm)/SiO2 (2.5 nm)/p+-Si structured cell showing both gradual set (from LRS to HRS) and gradual reset (from HRS to LRS) operation and (b) of Ni/SiNx (5 nm)/p+-Si structured cell showing abrupt set and reset operation. Interestingly, even for Ni/SiNx (5 nm)/p+-Si structured cell, additional gradual reset operation (in the range below 100 lA) occur after abrupt reset operation (in the range over 1 mA).[127]

A capping layer has the function of internal resistive current-limiting, similarly, an external serial resistance can increase the analog linearity. The resistance of the external resistor is comparable to the memristive device, and acts as a voltage divider. When memris device is in its low-resistance state, most of the programming voltage falls on the current-limiting resistor. Therefore the abrupt changes at the start of each programming cycle are corrected, and the device is given a more symmetric programming characteristic between potentiation and depression. Figure gives a compare of programming profile of devices with or without a resistor (memristor conductance 1-6 nS, resistor 2 nS). Asymmetric programing response is corrected to a symmetric profile, and in the following recognition applications the accuracy increases from 30% to 96%[64].

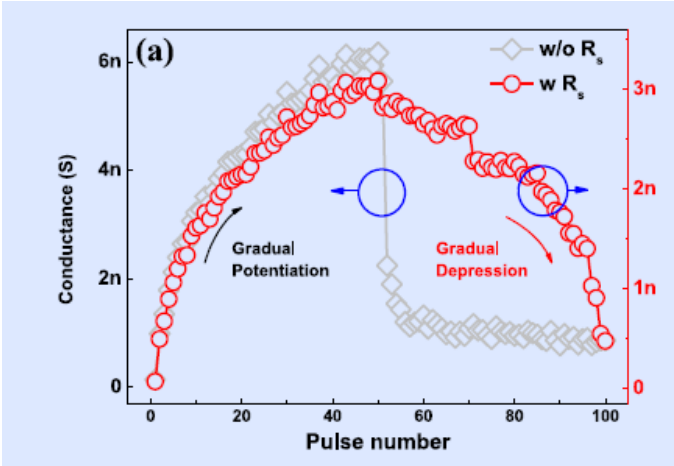
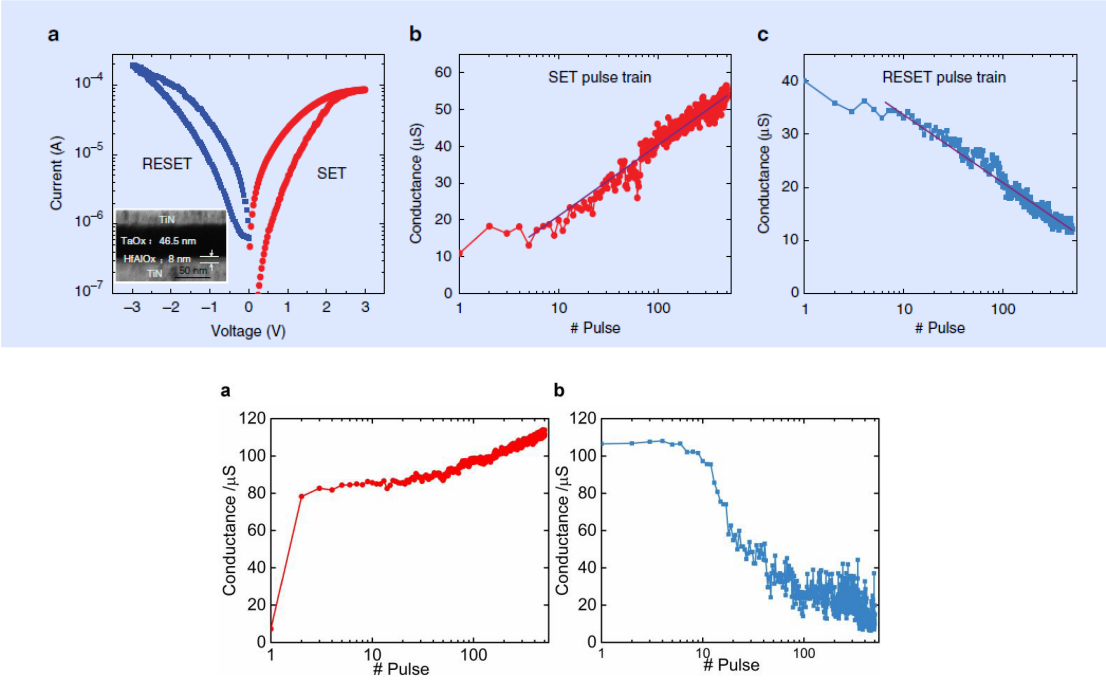



Figure . (*a*) Significantly improved conductance change of the PCMO-synapse. On the basis of the modulated Vpcmo (w Rs), the PCMO-synapse exhibited more symmetric conductance changes between the potentiation and depression than that of without Rs case (w/o Rs)[64]

Another improvement done by Yao et.al. [167] is the introducing of a laminate switching material structure. In this research single layer HfOx is replaced by a Hf/Al oxide mixed laminate layer, which is prepared by ALD, with periodically repeating alternating HfO2 and Al2O3 reaction

cycles. The thickness of each cycle is ~1A and Hf/Al ratio is preferred to be 3:1, and the thickness of the laminate layer is ~8 nm. As shown in Figure. HfAlOx laminate layer as resistance switching layer exhibits significantly improved linearity.




(a) Typical I–V curve of a single 1T1R cell for a quasi-DC sweep, the gate voltage is 1.8 and 8 V during SET and RESET process, respectively. Inset is a transmission electron microscope (TEM) image of the RRAM device. (b) An example of the typical continuous conductance tuning performance under an identical pulse train condition during SET process, along with the fitting curve. Vwl¼2.4V, Vbl¼2.0V (50 ns), Vsl¼0V. (c) Tuning performance during RESET operation, along with the fitting curve. Vwl¼8V, Vbl¼0V, Vsl¼2.3V (50 ns). D-e: non-linear tuning performance of TiN/TaOx/HfO2/TiN stack. (**a**) Continuous conductance tuning performance under an identical pulse train condition during SET process. *V*wl = 3.5 V, *V*bl = 1.6 V / 50 ns, *V*sl = 0 V. (**b**) Continuous conductance tuning performance during RESET operation. *V*wl = 5 V, *V*bl = 0 V, *V*sl = 1.6 V / 50 ns. [167]

In approaches mentioned above, device-level improvements are all realized by introducing a 2-D functional layer at the interface, based on conventional 2-end memristor structure. Another idea is governing the atoms motion by designed defects. In the research of Ag conductive bridge in epitaxy SiGe[108], Ag atoms are confined inside the threading dislocations. A 3-D random growth of filaments is restricted to a highly defined 1-D manner. The devices exhibit good analog performance: the conductance can be programmed to 100 distinct states in a quasi-linear way, and quantity of supported resistance levels can be up to 240. Kim et.al. found that doping Si in Ta2O5-x can facilitate the formation and transport of oxygen, and the devices are easily programmed to intermediate resistance states. Misha et.al. found introducing N doping to TaOx switching layer can improve the switching uniformity and analog performance, due to the confinement of filaments induced by N atoms[168].

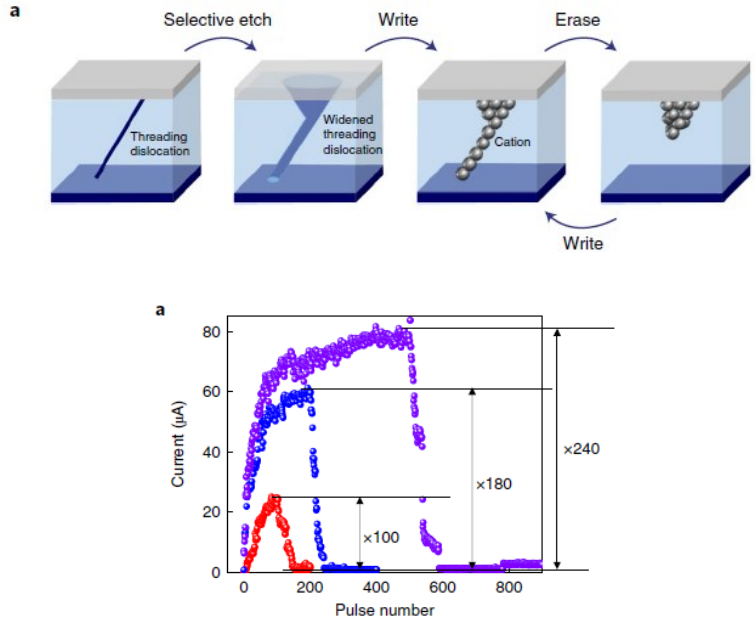



Figure. (a) A conceptual schematic of the epiRAM during switching (b) Potentiation and depression of epiRAM by set/reset training pulses showing the analog on/off conductance ratio. The pulse train consists of consecutive set pulses (5 V, 5 μ s) followed by consecutive reset pulses (− 3 V, 5 μ s). The pulse trains include 100/200/500 set pulses and 100/200/500 reset pulses, respectively. The current was measured at a 2 V read pulse after each set/reset pulse.[108]

Besides the switching and capping layer, the electrodes also play an important role in the switching behavior. Electrodes can be divided as active electrode, which can be oxidized and participate in the redox reaction in switching layer, or inert electrode such as Pt electrode. In oxides switching devices, a thin layer of metal is often used as layer to facilitate the formation of Vo, and reduce the SET/RESET voltage. Similarly, an active electrode in ion-migration device also participate in the formation of O vacancies. To illustrate the effect of active electrode, Li et.al. make a comparison between Al and Pt electrode with the same TaOy/Ta2O5-x/AlOx stack as switching layer[169]. With tungsten back electrode, Al and Pt are deposited as top electrode. Due to the generation of Vo near the Al electrode interface, the switching mechanism changes from filaments in TaOx layer to barrier modulation at the AlOx/Al interface. While the device with Pt top electrode shows an abrupt filamentary-type switching. In another research, an a-Si layer in TiN/Si/TaOx/TiN is reported to induce the interfacial-type transition[79]. In this report, the device conduction is governed by barrier at the TaOx/Si interface. a-Si participates in the formation of Vos and a Vo-rich layer at the interface, which reduces the barrier and device resistance. In RESET process Vos migrates inside Si layer (O released from Si), relaxing the Vo-rich layer and device resistance increases.

Cap layer with low migration rate is

Analog resistance switching and an on-off ratio larger than 10^5 are observed in Pt/CeO2/Pt structure[57]. The mechanism is not fully clear.

# Modeling

Lian et.al. stasticaly analysed the distribution of RESET voltage and current of a Ta/TaOx/Pt device. The finding is RESET voltage is independent on ON-state resistance, which indicates the RESET of this device is in accordance with thermal-activated dissolution model.
Between the ON and OFF states of oxides resistive switch lies the continuous resistance change region. Generally there are two ways to multilevel resistance or further continuous resistance: one is by controlling current compliance or stop voltage[55,170], the other is programming with series of pulses, and get a continuous relation between pulse number and device conductance[]. Based on filaments-induced resistance modulation, quantitative models are raised to describe the behavior of resistance change under programming pulses. Attempts on modeling the resistance change in this region have discovered the rich and complex dynamics of resistance modulating. This nature builds up modelling difficulty, and increases the device variability[171]. In sum, the model can be based on following features:

1) On the basis of filament-mitigated resistance modulating, the device conductance is determined by the geometrics and conductivity of filaments. A filaments can be described using two parameters: defects (mostly O-vacancy) concentration and filament shape. In the modeling process, these two parameters can be interpreted by the 2-D distribution of Vos on the device cross-section.

2) The forming and depletion of filaments are considered to be originated from defects migration. Therefore 3 effects should be taken to consideration: drift, diffusion, and thermophoresis effect. Accordingly, 3 driving forces should be included in the modeling: local electric field, Vo concentration and gradient, local temperature and gradient[172].

   Since the drift of Vo is migration under electric field, the migration rate is associated with diffusion rate, following Einstein relation [38]u=q/kT*D, where u is the migration rate, and D is the diffusion rate, exponentially related to temperature as D = D0*e(-G/kT), where G is the diffusion activation energy. Drift rate and diffusion rate can also interpreted in hopping mechanism. Where

   $D = 1/2 \cdot a^2 \cdot f \cdot \exp(-E_a / kT)$ Diffusivity of $V_o$ [$cm^2 s^{-1}$]
   $v = a \cdot f \cdot \exp(-E_a / kT) \cdot \sinh(qaE / kT)$ Drift velocity of $V_o$ [cm/s]
   $S = -E_a / kT^2$ Soret diffusion coefficient [1/K]

   Influenced by device configuration and programming pulses parameters, the competition between electrical and thermal effects may result in different device behaviors.

3) To capture the filament deformation, the filament growth can be divided to 2 steps: in the

first step, external field is applied on filaments, leading to a temperature rise and defect migration along the direction of filaments, and diffusion along the Vo gratitude. In second step, when external pulse is stopped, temperature exponentially declines. Drift is stopped while diffusion is continuing. The existence of continuing diffusion have influence on shape of filaments. Similarly the depletion of filaments can also divided into 2 steps.

4) Recovery and depletion of conductive filaments driven by programming pulses are asymmetric. Conductive filaments have different conductivity from the insulating matrix. This results in unevenly distributed electric field and temperature profile. In the insulating gaps defects are under stronger field and have a higher migration rate than in conductive filaments. (As suggested in ref [172], the recovery is dominated by electrical drift while the depletion is more relied on thermal effects.) In addition, in filaments recovery drift and diffusion are on the same direction while in the depletion are opposite.[172] Therefore the recovery and depletion show different plasticity to programming pulses: the forming of filaments in insulating gaps will be faster than the depletion. Less pulses are required in the filament recovery. This phenomenon is observed in different devices[38,161].

5) Programming behavior of oxides memristors are intrinsically time-dependent. During a program pulse the device especially insulating gaps near the filament tips are heated up. Temperature decays in exponential way. Depend on device configuration, this decay time could go up to 500 ns[173], which is relatively long in a MHz circuit. When following programming pulse arrive before the heat is fully dissipated, a further elevated temperature will influence the drift and diffusion rates. Here we define the variance of conductance $\Delta G/G$ under a specific programming pulse as the plasticity of devices. The interval of pulses determines device plasticity as well as pulse amplitude and duration. Shorter interval gives higher plasticity, which is similar to the STDP manner. To depict this timing-depend behavior, researchers introduce temperature as the second variable besides conductance[173]. The temperature profile is determined by timing characteristics of programming pulses, and have a straight relation to the plasticity. By governing pulse interval, intrinsic STDP or spike-rate-dependent plasticity (SRDP) can be achieved in memristors.

6) Besides timing parameters, the programming behavior of device is subject to the programming history as well. Different programming history results in different filament shapes and geometric distribution. Due to the historical continuity of filaments geometrics, the plasticity is also dependent on filaments forming condition and operation history [161].

   In Ref.[161], this is mainly attributed to the variety of filament shape. In this article, TaOx-based memristors are preprogramed to a same conductance value using different programming pulse voltage, and then stimulated by pulses of the same amplitude and length. Researches finds that a larger conductance change occurs when the device is preprogrammed using larger pulse amplitude. This is explained as that filaments grown under higher pulse amplitude have less diameter i.e. higher anisotropy, since ion migration rate is exponentially depend on pulse amplitude. When presenting the same

conductance, thinner filaments are longer than thicker ones and result in stronger local electric field when stimulating pulses are applied, therefore having higher plasticity.

## Summary

This article reviewed recent publications on memristive materials and device prototypes. Concepts such memristivity, neuromorphic computing are introduced. Ion-migration-based memristive materials and applications are categorized according to different migration ions. Based on the different ions, devices possess different inherent characteristics, and different issues are to be addressed in the device design. This provides a new perspective on memeristive materials selection and device design. Finally, a short discussion of diffusion modeling is presented, which provides insight into the points need to be considered in ion-migration-based memristive devices.

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